NXP Semiconductors
Application Note

Document Number: AN5426
Rev 0, 03/2017

Hardware Design Guidelines for S32K1xx Microcontrollers

Contents

1 Introduction

The S32K series further extends the highly scalable portfolio of ARM® Cortex® MCUs in the automotive industry. It builds on the legacy of the KEA series, whilst introducing higher memory options alongside a richer peripheral set extending capability into a variety of automotive applications.

With a 2.70–5.5 V supply and focus on automotive environment robustness, the S32K series devices are well suited to a wide range of applications in electrical harsh environments. These devices are optimized for cost-sensitive applications offering low pin-count options.

The S32K series offers a broad range of memory, peripherals, and package options. They share common peripherals and pin counts allowing developers to migrate easily within the MCU family or among the MCU families to take advantage of more memory or feature integration. This scalability allows developers to standardize on the S32K series for their end product platforms, maximizing hardware and software reuse and reducing timeto-market.

Following are the general features of the S32K series MCUs:

- 32-bit ARM Cortex-M4 core with IEEE-754 compliant FPU, executing up to 112 MHz
- Scalable memory footprints up to 2 MB flash and up to 256 KB SRAM
- Precision mixed-signal capability with on chip analog comparators and multiple 12-bit ADCs
- Powerful timers for a broad range of applications including motor control, lighting control and body applications
- Serial communication interfaces such as LPUART, LPSPI, LPI2C, FlexCAN, CAN-FD, FlexIO and so on.
- SHE specification compliant security module
- Single power supply (2.70–5.5 V) with full functional flash program/erase/read operations
- Functional safety compliance with ISO26262, with internal watchdog, voltage monitors, clock monitors, memory protection and ECC
- Ambient operation temperature range: –40 °C to 125°C
- Software enablement: S32 Software Development Kit (SDK), S32 Design Studio (S32DS)

2 S32K family comparison

Please refer to the latest version of the Reference Manual for details.

3 Power supplies

The power and ground pins are described in subsequent sections.

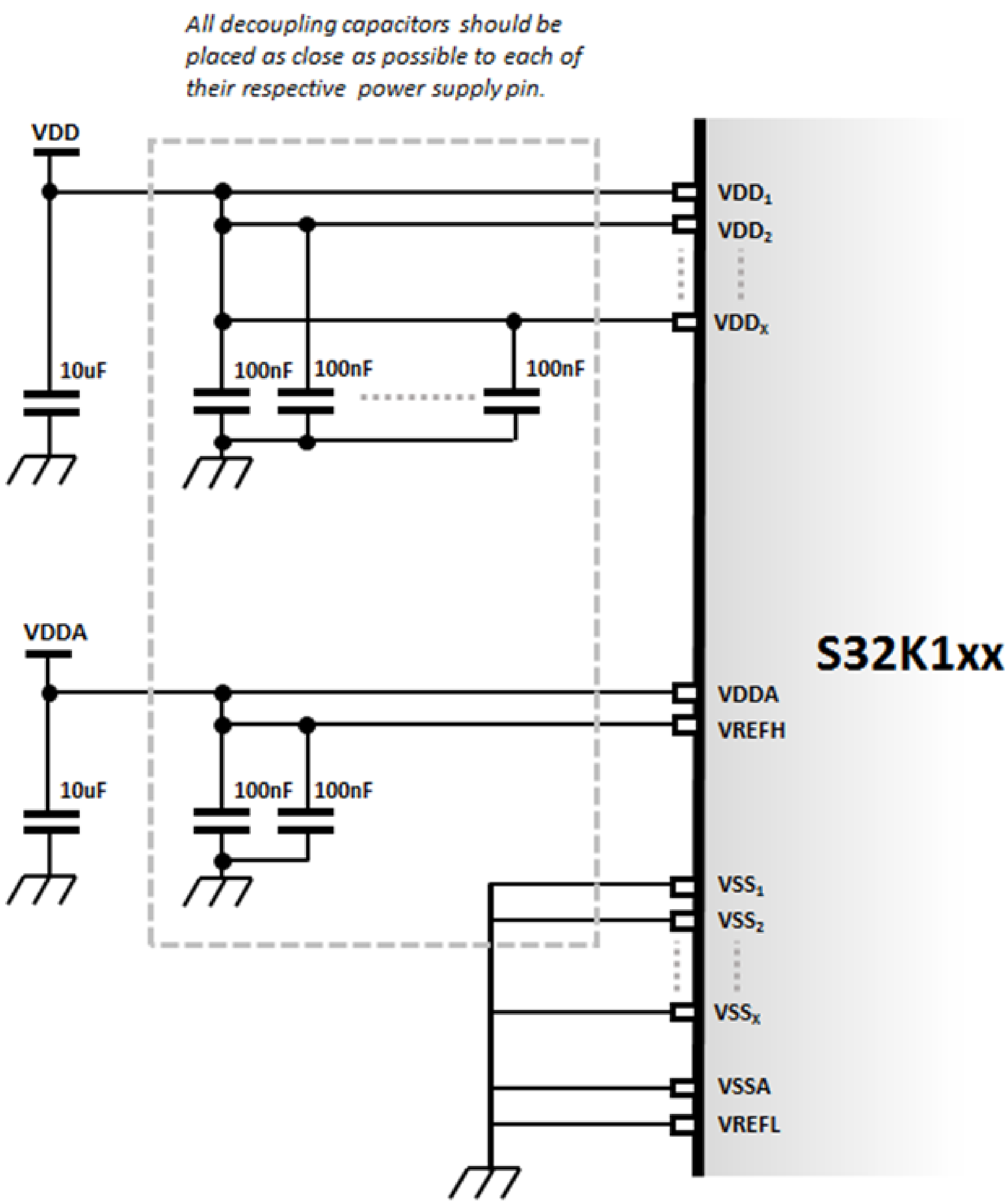


Figure 1. Power supply pins

Table 1. Power domains and decoupling capacitors

Power Domain	Description	Voltage	Bulk/Bypass Capacitor for group	Decoupling Capacitor per pin	Characteristics
VDDX	Supply voltage	5 V/3.3 V	10uF	0.1uF	X7R Ceramic
VDDA	Analog supply voltage		10uF	0.1uF	X7R Ceramic
VREFH	ADC reference voltage high			0.1uF	X7R Ceramic
VSS	Ground	GND	VSS, VSSA and VREFL must be shorted to GND at package level.		
VSSA	Analog Ground				
VREFL	ADC reference voltage low				

3.1 Bulk and decoupling capacitors

The bulk capacitor acts as a local power supply to the power pin, near the decoupling capacitors. Minimize the trace length between the bulk capacitor and the decoupling capacitors.

Decoupling capacitors make the current loop between supply, MCU, and ground reference as short as possible for high frequency transients and noise. Therefore, all decoupling capacitors should be placed as close as possible to each of their respective power supply pin; the ground side of the decoupling capacitor should have a via to the pad which goes directly down to the ground plane. The capacitor should not route to the power plane through a long trace.

4 Clock circuitry

The S32K1xx has the following clock sources:

- Fast internal reference clock (FIRC): 48–60 MHz.
- Slow internal reference clock (SIRC): 8 MHz.
- PLL: External oscillator as input source.
- External square wave input clock: up to 60 MHz.
- External oscillator clock (OSC): 4–40 MHz.

FIRC, SIRC are internal and does not have to be considered from the hardware design perspective. The external oscillator works with a range from 4–40 MHz. It provides an output clock that can be provided to the PLL or used as clock source for some peripherals. When using the external oscillator as input source for the PLL, the frequency range of the external oscillator should be 4–40 MHz.

4.1 EXTAL and XTAL pins

These pins provide the interface for a crystal to control the internal clock generator circuitry. EXTAL is the input to the crystal oscillator amplifier. XTAL is the output of the crystal oscillator amplifier. The pierce oscillator provides a robust, low-noise and low-power external clock source. It is designed for optimal start-up margin with typical crystal oscillators. S32K1xx supports crystals or resonators from 4 MHz to 40 MHz. The Input Capacitance of the EXTAL, XTAL pins is 7 pF.

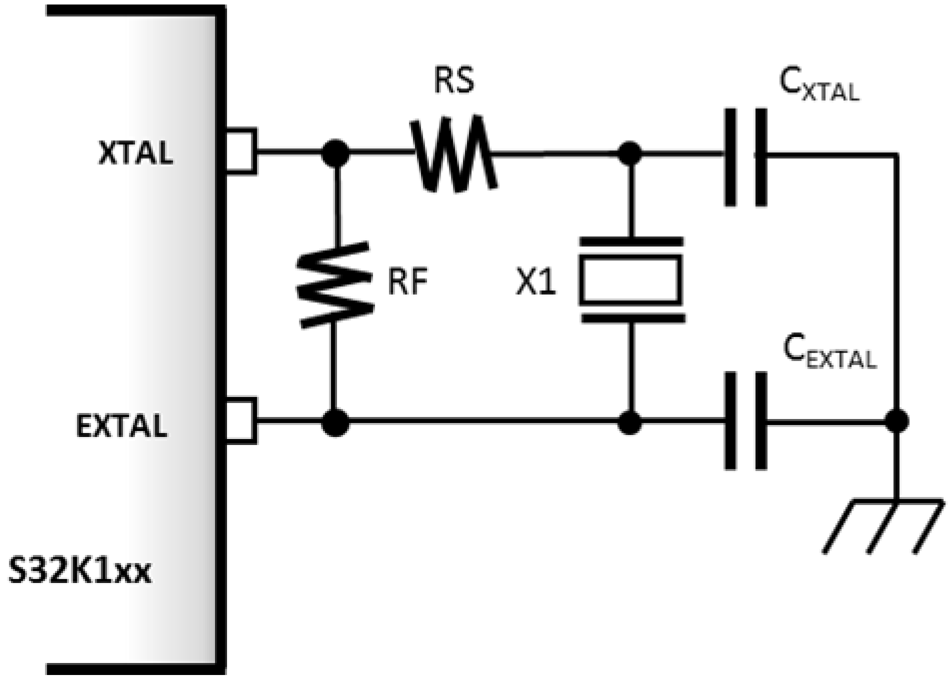


Figure 2. Reference oscillator circuit

Table 2. Components of the oscillator circuit

Symbol	Description
RS	Bias Resistor
RF	Feedback Resistor • When Low-gain is selected, internal RF will be selected, and external RF is not required. • When High-gain is selected, external RF(1M Ohm) need to be connected for proper operation of crystal. For external resistor, up to 5% tolerance is allowed.
X1	Quartz Crystal / Ceramic Resonator
CXTAL	Stabilizing Capacitor
CEXTAL	Stabilizing Capacitor

The load capacitors are dependent on the specifications of the crystal and on the board capacitance. It is recommended to have the crystal manufacturer evaluate the crystal on the PCB.

4.2 Suggestions for the PCB layout of oscillator circuit

The crystal oscillator is an analog circuit and must be designed carefully and according to the analog-board layout rules:

- External feedback resistor [Rf] is not needed because it’s already integrated.

- It is recommended to send the PCB to the crystal manufacturer to determine the negative oscillation margin as well as the optimum regarding CXTAL and CEXTAL capacitors. The data sheet includes recommendations for the tank capacitors CXTAL and CEXTAL. These values together with the expected PCB, pin, etc. stray capacity values should be used as a starting point.
- Signal traces between the XTAL/EXTAL pins, the crystal and the external capacitors must be as short as possible, without using any via. This minimizes parasitic capacitance and sensitivity to crosstalk and EMI. The capacitance of the signal traces must be considered when dimensioning the load capacitors.
- Guard the crystal traces with ground traces (guard ring). This ground guard ring must be clean ground. This means that no current from and to other devices should be flowing through the guard ring. This guard ring should be connected to VSS x of the S32K1xx with a short trace. Never connect the ground guard ring to any other ground signal on the board. Also avoid implementing ground loops.
- The main oscillation loop current is flowing between the crystal and the load capacitors. This signal path (crystal to CEXTAL to CXTAL to crystal) should be kept as short as possible and should have a symmetric layout. Hence, both capacitor's ground connections should always be as close together as possible.
- The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

The following figure 3, shows the recommended placement and routing for the oscillator layout.

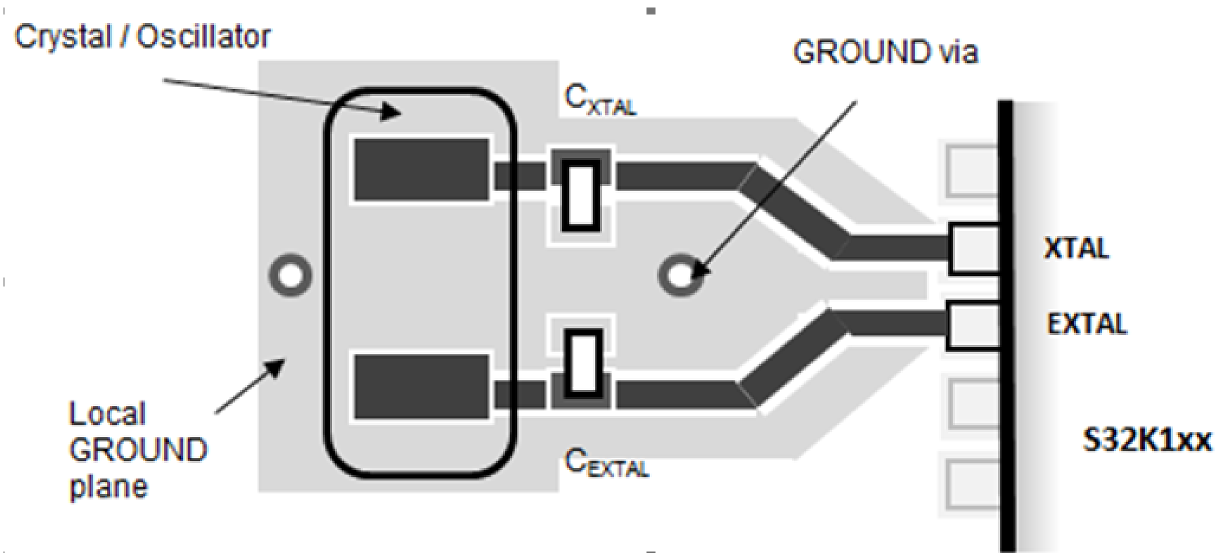


Figure 3. Suggested crystal oscillator layout

5 Debug and programing interface

A number of commonly used debug connectors are shown here. Most of the ARM development tools uses one of these pin out's. When developing your ARM circuit board, it is recommended to use a standard debug signal arrangement to make connection to debugger easier.

The SWD/SWV pins are overlaid on top of the JTAG pins as follows:

Table 3. JTAG signal description

JTAG Mode	SWD Mode	Signal	Required pull-up / pull-down (if not implemented internally by MCU)
TCK	SWCLK	Clock into the core	Use 10–100 K Ohm pull-down resistor to GND
TDI	-	JTAG Test Data Input	Use 10–100 K Ohm pull-up resistor to VCC
TDO	SWV	JTAG Test Data Output / SWV trace data output (SWO)	Use 10–100 K Ohm pull-up resistor to VCC
TMS	SWDIO	JTAG Test Mode Select / SWD data in/out	Use 10–100 K Ohm pull-up resistor to VCC
GND	GND	-	-

Usually, MCUs do not include pull-up or pull-down resistors on JTAG/SWD pins. Resistors should be added externally onto the board as detailed above. You may use resistors between 10–100 K for these signals. This will prevent the signals from floating when they are not connected to anything.

5.1 Debug connector pinouts

5.1.1 20-pin Cortex Debug D ETM connector

Some newer ARM microcontroller board use a 0.05” 20-pin header (Samtec FTSH-110) for both debug and trace. (The signals greyed out are not available on the Cortex-M3 or Cortex-M4.) The 20-pin Cortex Debug D ETM connector support both JTAG and Serial Wire debug protocols. When the Serial debug protocol is used, the TDO signal can be used for Serial Wire Viewer output for trace capture. The connector also provides a 4-bit wide trace port for capturing of trace that require a higher trace bandwidth (example, when ETM trace is enabled).

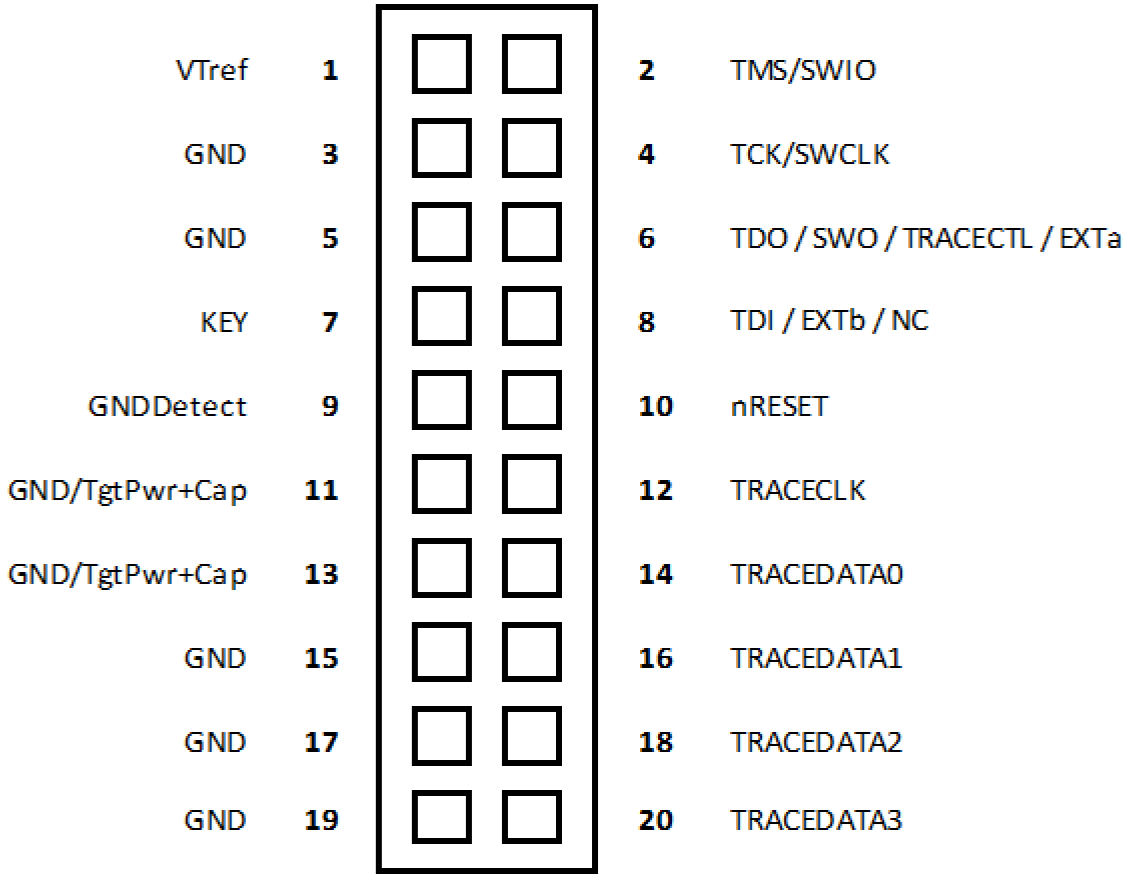


Figure 4. 20-pin Cortex Debug D ETM connector pin layout

5.1.2 10-pin Cortex Debug connector

For device without ETM, you can use an even smaller 0.05” 10-pin connector (Samtec FTSH-105) for debug. Similar to the 20-pin Cortex Debug D ETM connector, both JTAG and Serial-Wire debug protocols are supported in the 10-pin version.

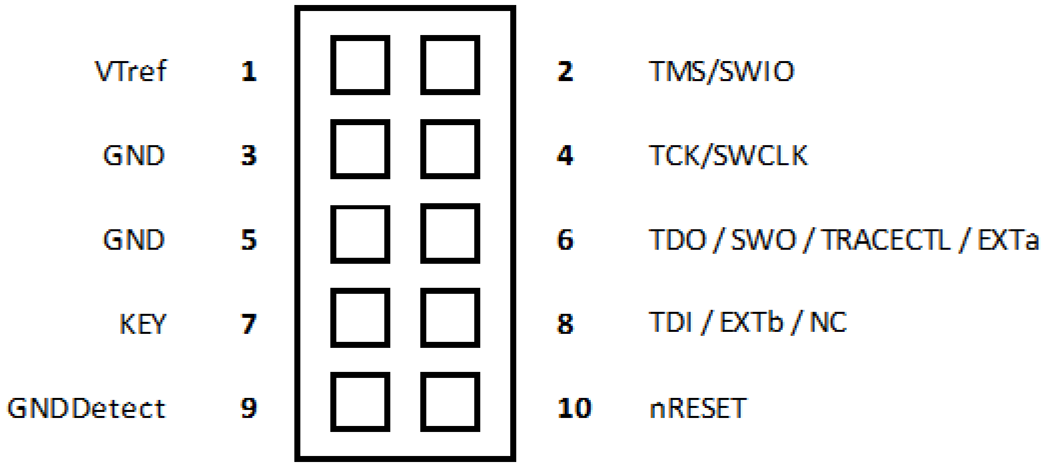


Figure 5. 10-pin Cortex Debug connector pin layout

5.1.3 Legacy 20-pin IDC connector

A common debug connector used in ARM development boards is the 20-pin IDC connector. The 20-pin IDC connector arrange support JTAG debug, Serial Wire debug (SWIO and SWCLK), Serial Wire Output (SWO). The nICEDETECT pin allows the target system to detect if a debugger is connected. When no debugger is attached, this pin is pulled high. A debugger connection connects this pin to ground. This is used in some development boards that support multiple JTAG con- figurations. The nSRST connection is optional; debugger can reset a Cortex-M system via the System Control Block (SCB) so this connection is often omitted from the top level of microcontroller designs.

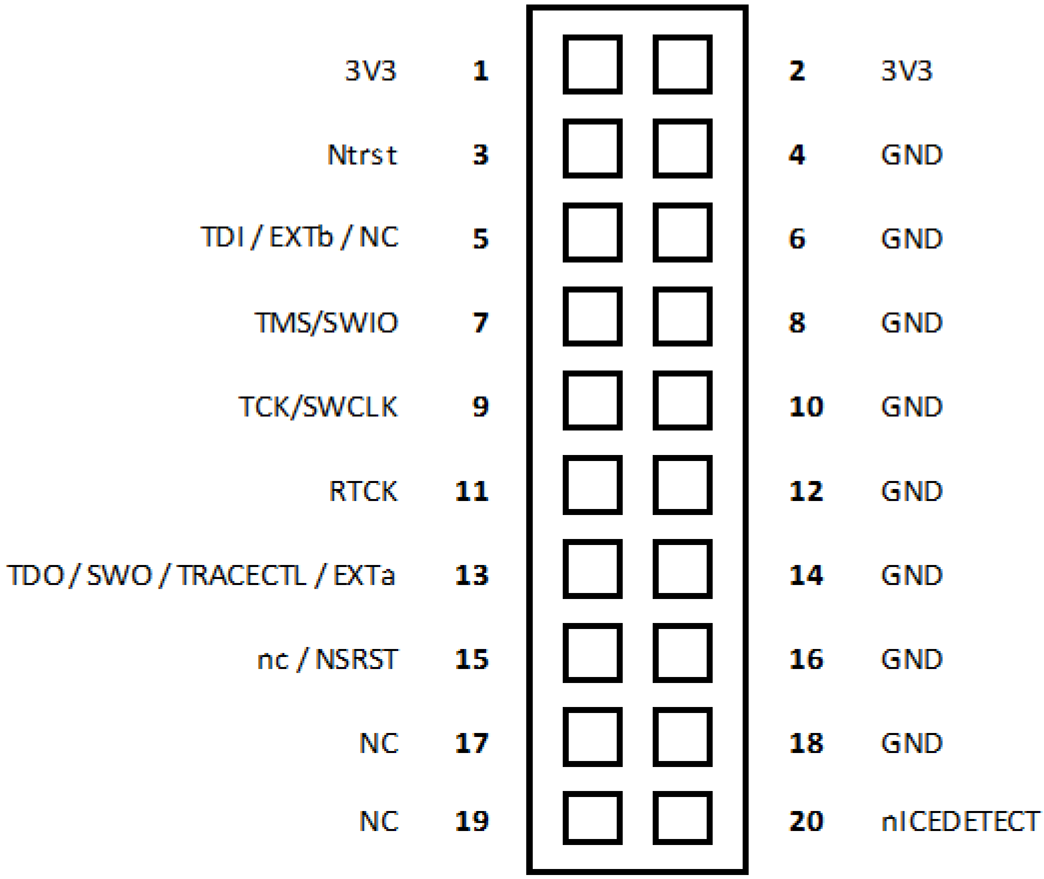


Figure 6. 20-pin IDC connector

5.1.4 38-pin Mictor connector

In some ARM system designs, Mictor connector is used when trace port is required (example, for instruction trace with ETM). It can also be used for JTAG/SWD connection. The 20-pin IDC connector can be connected in parallel with the Mictor connector (only one is use at a time).

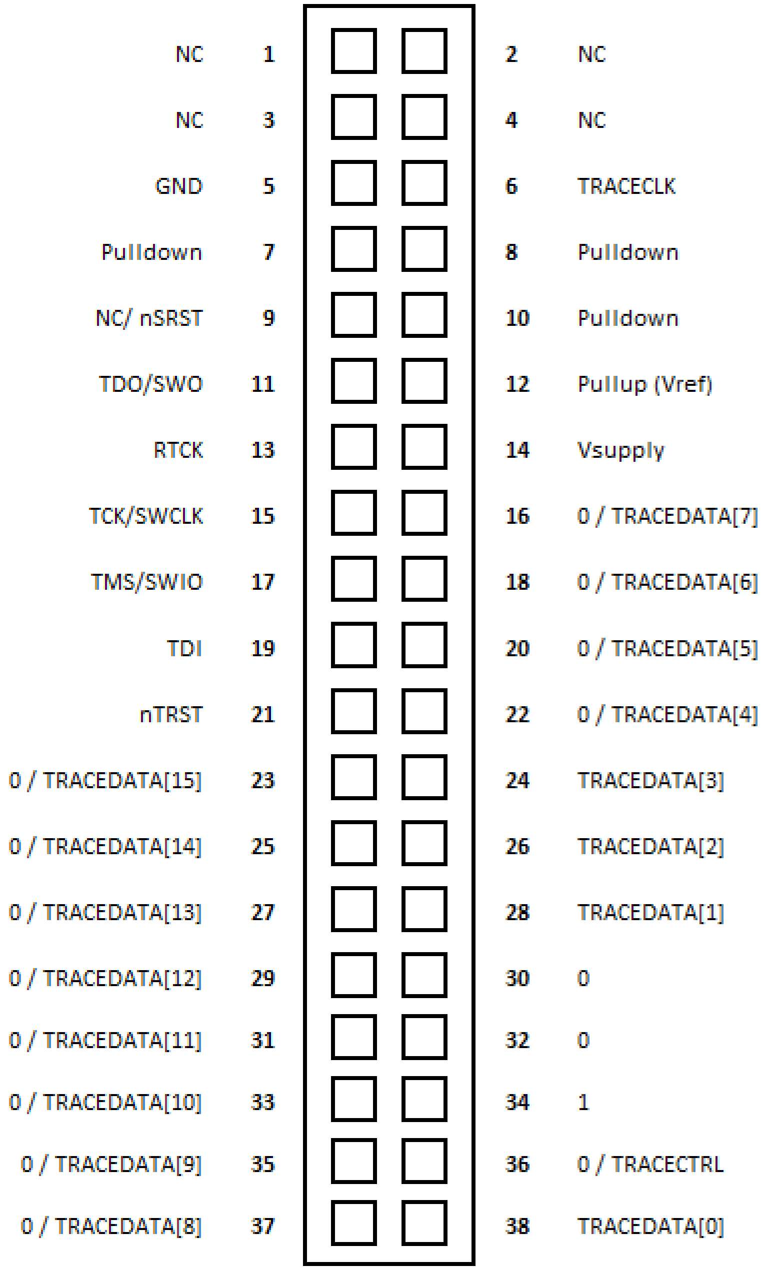


Figure 7. 38-pin Mictor connector

Typically a Cortex-M3 or Cortex-M4 microcontroller only has 4-bit of trace data signals, so most of the trace data pins on the Mictor connectors are not used. The Mictor connector is used mostly in other ARM Cortex processors (CortexA8/A9, Cortex-R4) or in some multiprocessor systems the trace system might require a wider trace port. In such cases, some of the other unused pins on the connector will also be used. For a typical Cortex-M3 or Cortex-M4 system, the Cortex Debug D ETM connector is recommended.

5.2 RESET system

Resetting the MCU provides a way to start processing from a known set of initial conditions. System reset begins with the on-chip regulator in full regulation and system clocking generation from an internal reference.

5.2.1 External pin RESET

For all reset sources, the RESET_B pin is driven low by the MCU for at least 128 bus clock cycles and until flash memory initialization has completed.

After flash memory initialization has completed, the RESET_B pin is released and the internal chip reset desserts. Keeping the RESET_B pin asserted externally delays the negation of the internal chip reset.

On this device, RESET is a dedicated pin. This pin is open drain and has an internal pull/up device. Asserting RESET wakes the device from any mode. During a pin reset, the RCM's SRS[PIN] bit is set. Hence, application software can detect an external pin RESET by reading this register.

In case RESET_PIN_CFG within Flash Option Register (FTFC_FOPT) is cleared, RESET_B pin is disabled following a POR and cannot be enabled as reset function. When this option is selected, there could be a short period of contention during a POR ramp where the device drives the pin low prior to establishing the setting of this option and releasing the reset function on the pin. When the RESET pin is disabled and configured as a GPIO output, it operates as a pseudo open drain output.

This bit is preserved through system resets and low-power modes. When RESET_B pin function is disabled, it cannot be used as a source for low-power mode wake-up.

NOTE

When the reset pin has been disabled and security has been enabled by means of the FSEC register, a mass erase can be performed only by setting both the Mass Erase and System Reset Request fields in the MDM-AP register.

In prototype designs, it is common to add a push-button to manually force a reset. In this case, the designer could choose to add a debounce capacitor to this button. In the event of an internal reset event, the MCU forces the RESET pin low and up again so that other circuits connected to this pin reset as well. This reset pulse must last less than 24 µs. The debounce capacitance on the reset line must ensure that this timing constraint is met. Capacitors smaller than 330 pF are recommended.

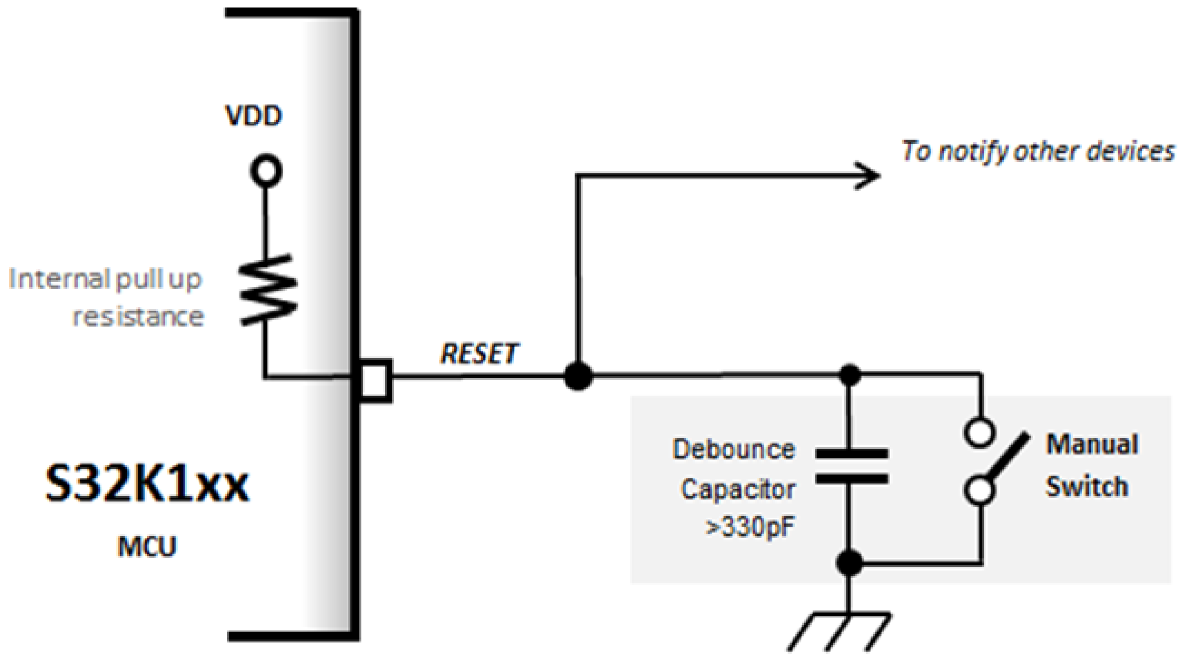


Figure 8. RESET circuit

6 Communication modules

6.1 LIN interface for LPUART module

The Local Interconnect Network (LIN) is a serial communication protocol, designed to support automotive networks. As the lowest level of a hierarchical network, LIN enables cost-effective communication with sensors and actuators when all the features of CAN are not required.

Features of the LPUART module supports and include:

- LIN master and slave operation
- Full-duplex, standard non-return-to-zero (NRZ) format
- Programmable baud rates (13-bit modulo divider) with configurable oversampling ratio from 4x to 32x
- Transmit and receive baud rate can operate asynchronous to the bus clock:
  - Baud rate can be configured independently of the bus clock frequency
  - Supports operation in Stop modes
- Interrupt, DMA or polled operation:
  - Transmit data register empty and transmission complete
  - Receive data register full
  - Receive overrun, parity error, framing error, and noise error
  - Idle receiver detect

- Active edge on receive pin
- Break detect supporting LIN
- Receive data match
- Hardware parity generation and checking
- Programmable 7-bit, 8-bit, 9-bit or 10-bit character length
- Programmable 1-bit or 2-bit stop bits
- Three receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
  - Receive data match
- Automatic address matching to reduce ISR overhead:
  - Address mark matching
  - Idle line address matching
  - Address match start, address match end
- Optional 13-bit break character generation / 11-bit break character detection
- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64 or 128 idle characters
- Selectable transmitter output and receiver input polarity
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse width
- Independent FIFO structure for transmit and receive
  - Separate configurable watermark for receive and transmit requests

Option for receiver to assert request after a configurable number of idle characters if receive FIFO is not empty.

Table 4. LPUART signal description

Signal	Description	I/O
TXD	Transmit data. This pin is normally an output, but is an input (tristated) in single wire mode whenever the transmitter is disabled or transmit direction is configured for receive data.	I/O
RXD	Receive data.	I
CTS_B	Clear to send.	I
RTS_B	Request to send.	O

The LIN bus topology utilizes a single master and multiple nodes, as shown below. Connecting application modules to the vehicle network makes them accessible for diagnostics and service.

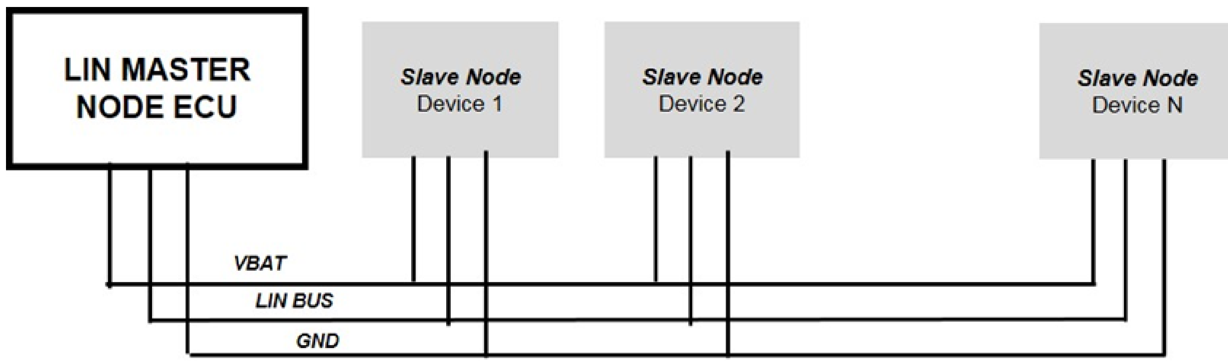


Figure 9. LIN bus topology

The LIN transmitter is a low-side MOSFET with current limitation and overcurrent transmitter shutdown. A selectable internal pull-up resistor with a serial diode structure is integrated, so no external pull-up components are required for the application in a slave node. To be used as a master node, an external resistor of 1 kΩ in series with a diode must be placed in parallel between VBAT [Battery Voltage] and the LIN Bus line. The fall time from recessive to dominant and the rise time from dominant to recessive is selectable and controlled to guarantee communication quality and reduce EMC emissions.

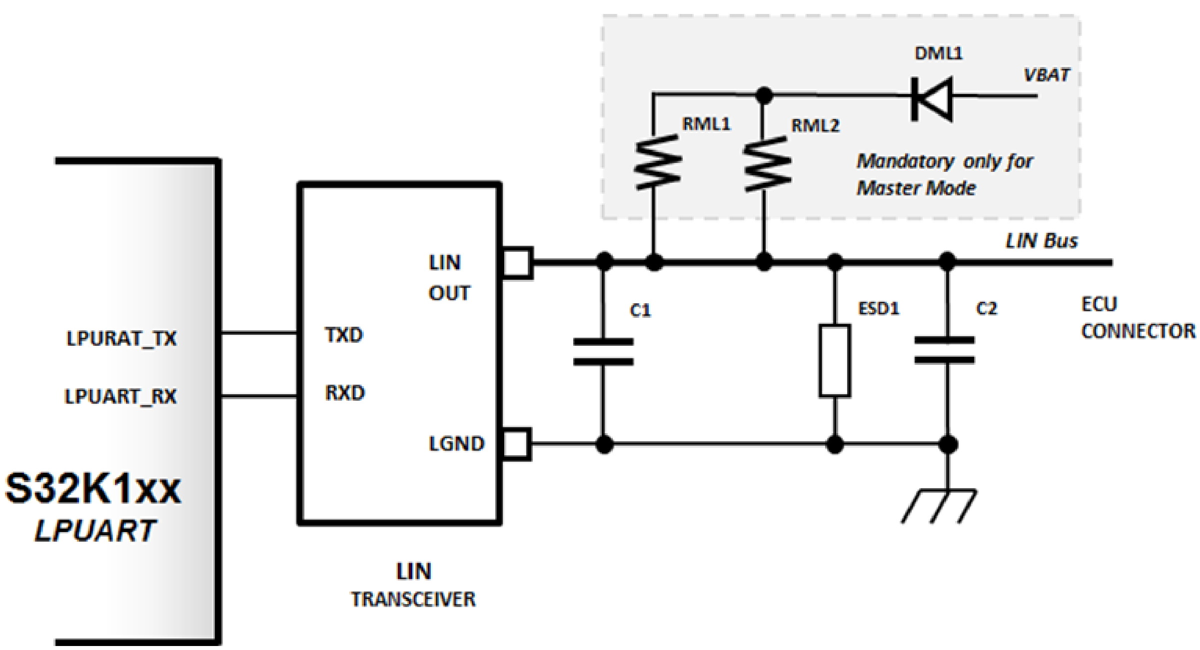


Figure 10. Circuit diagram for LIN interface

6.2 LIN components data

Table 5. LIN components

Reference	Part	Mounting	Remark
DMLIN	Diode	Mandatory only for master ECU	Reverse Polarity protection from LIN to VSUP.
RML1 and RML2	Resistor: 2 kΩ Power Loss: 250 mW Tolerance: 1% Package Size: 1206 Requirement: Min Power rating of the complete master termination has to be ≥ 500 mW	Mandatory only for Master ECU	For Master ECU If more than 2 resistors are used in parallel, the values have to be chosen in a way that the overall resistance RM of 1 kΩ and the minimum power loss of the complete master termination has to be fulfilled. For Slave ECU RMLIN1 and RMLIN2 are not needed on the PCB layout
C1	Capacitor: Slave ECU: typically 220 pF Master ECU: from 560 pF up to approximately ten times that value in the slave node [CSLAVE], so that the total line capacitance is less dependent on the number of slave nodes. Tolerance: 10% Package Size: 0805 Voltage: ≥50 V	Mandatory	The value of the master node has to be chosen in a way that the LIN specification is fulfilled.
C2	Capacitor: Package Size: 0805	Optional	Mounting of the optional part only allowed if there is an explicit written permission of the respective OEM available. Place close to the connector.

Table continues on the next page...

Table 5. LIN components (continued)

Reference	Part	Mounting	Remark
ESD1	ESD Protection Package Size: 0603-0805	Optional	Layout pad for an additional ESD protection part. Mounting of the optional part only allowed if there is an explicit written permission of the respective OEM available. Place close to the connector.

6.3 CAN interface for FlexCAN module

The physical layer characteristics for CAN are specified in ISO-11898-2. This standard specifies the use of cable comprising parallel wires with an impedance of nominally 120 Ω (95 Ω as minimum and 140 Ω as maximum). The use of shielded twisted pair cables is generally necessary for electromagnetic compatibility (EMC) reasons, although ISO-11898-2 also allows for unshielded cable. A maximum line length of 40 meters is specified for CAN at a data rate of 1 Mb. However, at lower data rates, potentially much longer lines are possible. ISO-11898-2 specifies a line topology, with individual nodes connected using short stubs.

Though not exclusively intended for automotive applications, CAN protocol is designed to meet the specific requirements of a vehicle serial data bus: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness, and required bandwidth.

Each CAN station is connected physically to the CAN bus lines through a transceiver device. The transceiver is capable of driving the large current needed for the CAN bus and has current protection against defective CAN or defective stations. A typical CAN system with an S32K1xx microcontroller is shown in Figure 11. CAN system on page 16

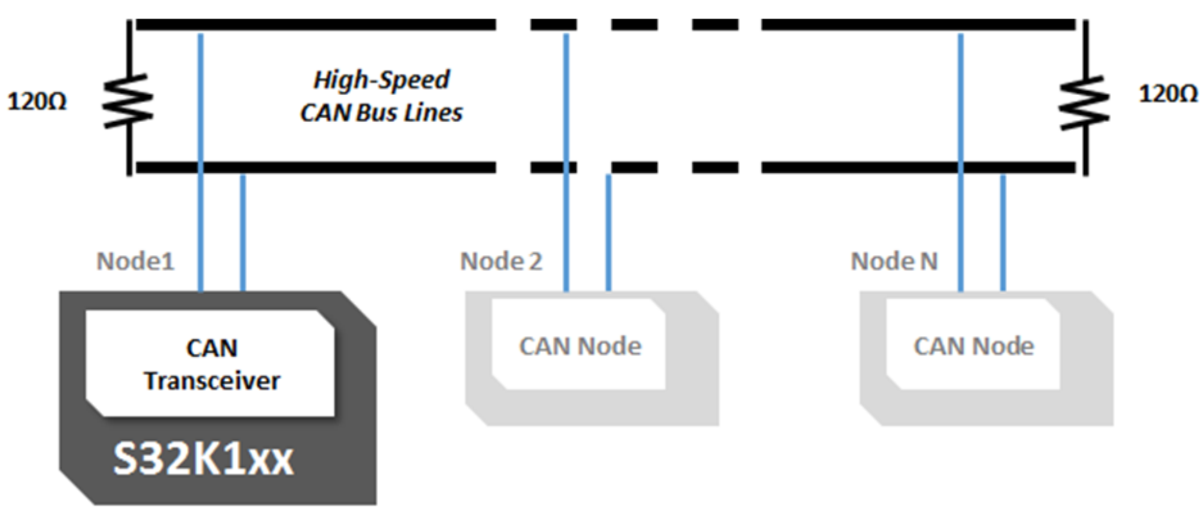


Figure 11. CAN system

The FlexCAN module is a full implementation of the CAN protocol specification, the CAN with Flexible Data rate (CAN FD) protocol and the CAN 2.0 version B protocol, which supports both standard and extended message frames and long payloads up to 64 bytes transferred at faster rates up to 8 Mbps. The message buffers are stored in an embedded RAM dedicated to the FlexCAN module. See the chip configuration details in the Reference Manual for the number of message buffers configured in the chip.

Like most others CAN physical transceivers, the CANH, CANL and SPLIT pins are available for the designer to terminate bus depending on the application. The Figure 12. CAN physical transceiver circuit on page 17 and Figure 13. CAN physical transceiver circuit with common mode choke on page 17 show examples of the CAN node terminations.

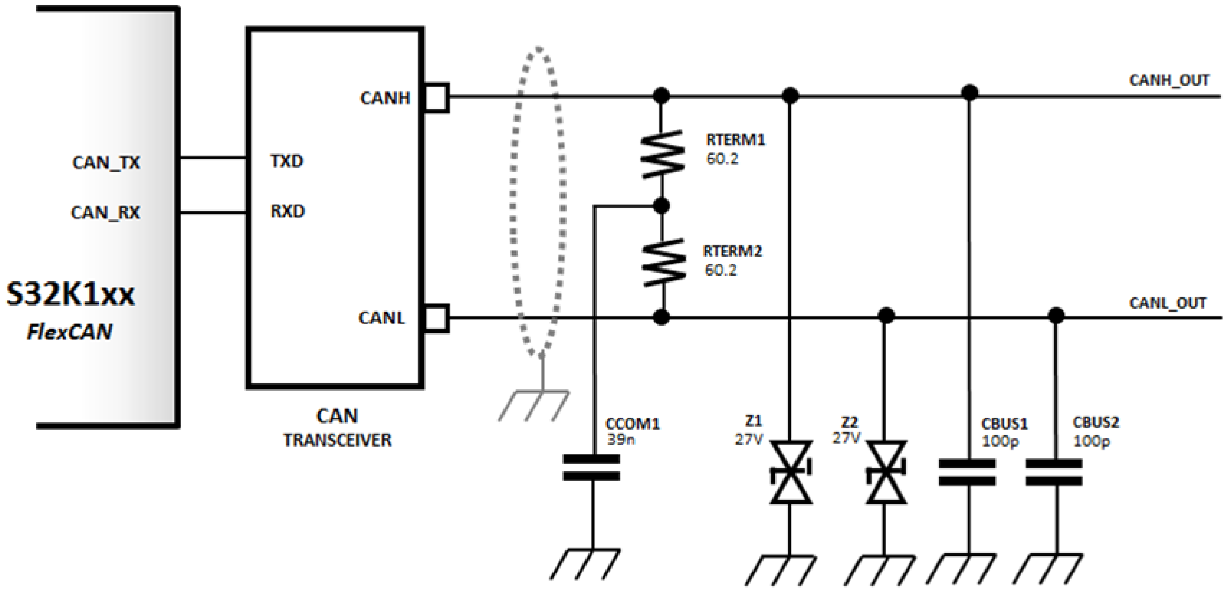


Figure 12. CAN physical transceiver circuit

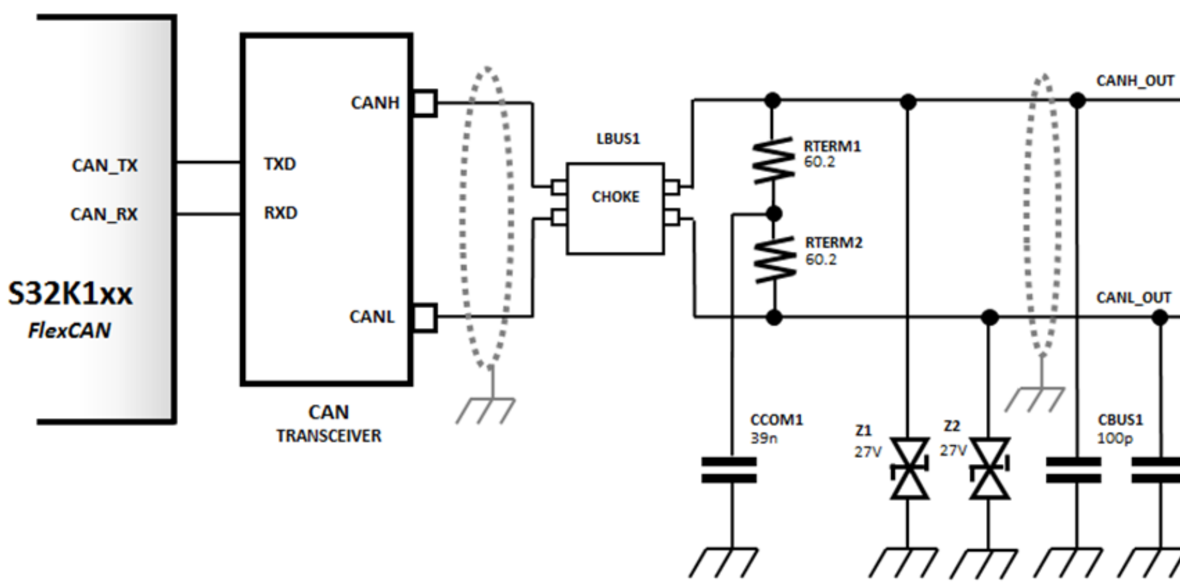
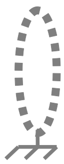


Figure 13. CAN physical transceiver circuit with common mode choke

6.4 CAN components data

Table 6. CAN components

Reference	Description
	Denotes a guard track next to a high/medium speed track. Guard tracks are connected such that each end of the track is connected to ground. A guard track should be connected to the ground plane at least every 500 mils. Spacing from any protected conductor and the guard track must not exceed 20 mils.
CBUS1 and CBUS2	The Capacitors CBUS1 and CBUS2 are not specifically required. They may be added for EMC reasons, in which case the maximum capacitance from either bus wire to ground must not exceed 300 pF total. If zener stacks are also needed, the parasitic capacitance of the zener stacks must also be included in the total capacitance budget.
Z1 and Z2	The zener stacks Z1 and Z2 could be required to satisfy Automotive EMC requirements (ESD in particular). These devices should be placed close to the connector.
RTERM1, **RTERM2 and CCOM1**	Depending on the position of the node within the CAN network it might need a specific termination. RTERM1, RTERM2 and CCOM1 must be that they assist in having an overall cable impedance. On a bus implementation of a CAN network only the two nodes on the two ends of the bus have terminator resistors. The nodes not placed on the end of the CAN bus do not have termination. A thorough analysis is required to maintain this requirement of the CAN networks. The SPLIT pin on the transceiver is optional and the designer might choose not to use it. This pin helps stabilize the recessive state of the CAN bus and can be enabled or disabled by software when required.
LBUS1–Common mode choke	A common mode choke on the CANH and CANL lines can help reduce coupled electromagnetic interference and needed to satisfy Automotive EMC requirements. This choke, together with transient suppressors on the transceiver pins can greatly reduce coupled electromagnetic noise, and high-frequency transients. LBUS1 is not specifically required.

6.4.1 CAN termination

In a transmission line, there are two current paths, one to carry the currents from the driver to the receiver and another to provide the return path back to the driver. In the CAN transmission lines is more complex because there are two signals that are sharing a common termination as well as a ground return path. For reliable CAN communications, it is essential that the reflections in the transmission line be kept as small as possible. This can only be done by proper cable termination. Figure 14. d CAN Bus - parallel termination on page 19 and Figure 15. CAN Bus – parallel transmission with common-mode filtering on page 19 demonstrates two CAN termination schemes.

Reflections happen very quickly during and just after signal transitions. On a long line, the reflections are more likely to continue long enough to cause the receiver to misread logic levels. On short lines, the reflections occur much sooner and have no effect on the received logic levels.

6.4.1.1 Parallel termination

In CAN applications, both ends of the bus must be terminated because any node on the bus may transmit/receive data. Each end of the link has a termination resistor equal to the characteristic impedance of the cable, although the recommended value for the termination resistors is nominally 120 Ω (100 Ω as minimum and 130 Ω as maximum).

There should be no more than two terminating resistors in the network, regardless of how many nodes are connected, because additional terminations place extra load on the drivers. ISO-11898-2 recommends not integrating a terminating resistor into a node, but rather attaching standalone termination resistors at the furthest ends of the bus. This is to avoid a loss of a termination resistor if a node containing that resistor is disconnected. The concept also applies to avoiding the connection of more than two termination resistors to the bus, or locating termination resistors at other points in the bus rather than at the two ends.

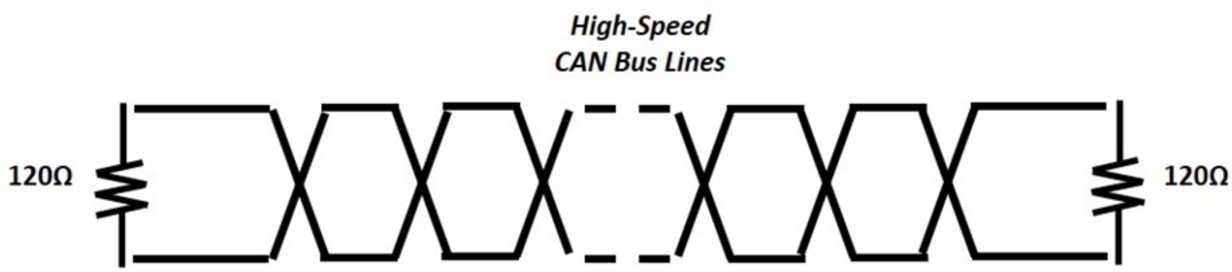


Figure 14. d CAN Bus - parallel termination

6.4.1.2 Parallel termination with common-mode filtering

To further enhance signal quality, split the terminating resistors at each end in two and place a filter capacitor, CSPLIT, between the two resistors. This filters unwanted high frequency noise from the bus lines and reduces common-mode emissions.

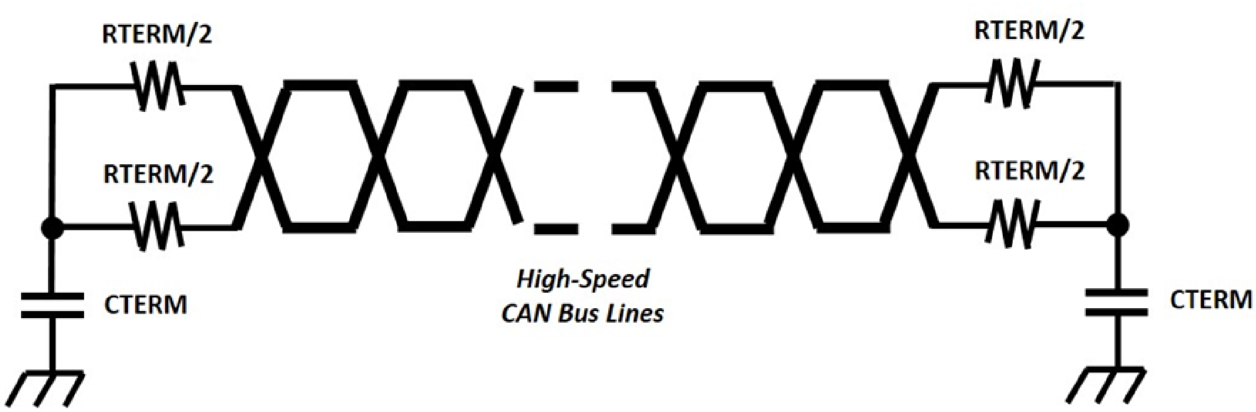


Figure 15. CAN Bus – parallel transmission with common-mode filtering

6.5 Inter-Integrated Circuit IIC

The Inter-Intergrated Circuit (IIC) bus is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange between devices. Being a two-wire device, the IIC bus minimizes the need for large numbers of connections between devices, and eliminates the need for an address decoder. This bus is suitable for applications requiring occasional communications over a short distance between a number of devices. It also provides flexibility, allowing additional devices to be connected to the bus for further expansion and system development. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull-up resistor (see Figure 16. Connection of I2C-bus devices to the I2C-bus on page 20. When the bus is free, both lines are high. The output stages of devices connected to the bus must have an open-drain or open collector in order to perform the wired-AND function. The interface is designed to operate up to 100 kbps with maximum bus loading and timing. The device is capable of operating at higher baud rates, up to a maximum of clock/20, with reduced bus loading. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400 pF.

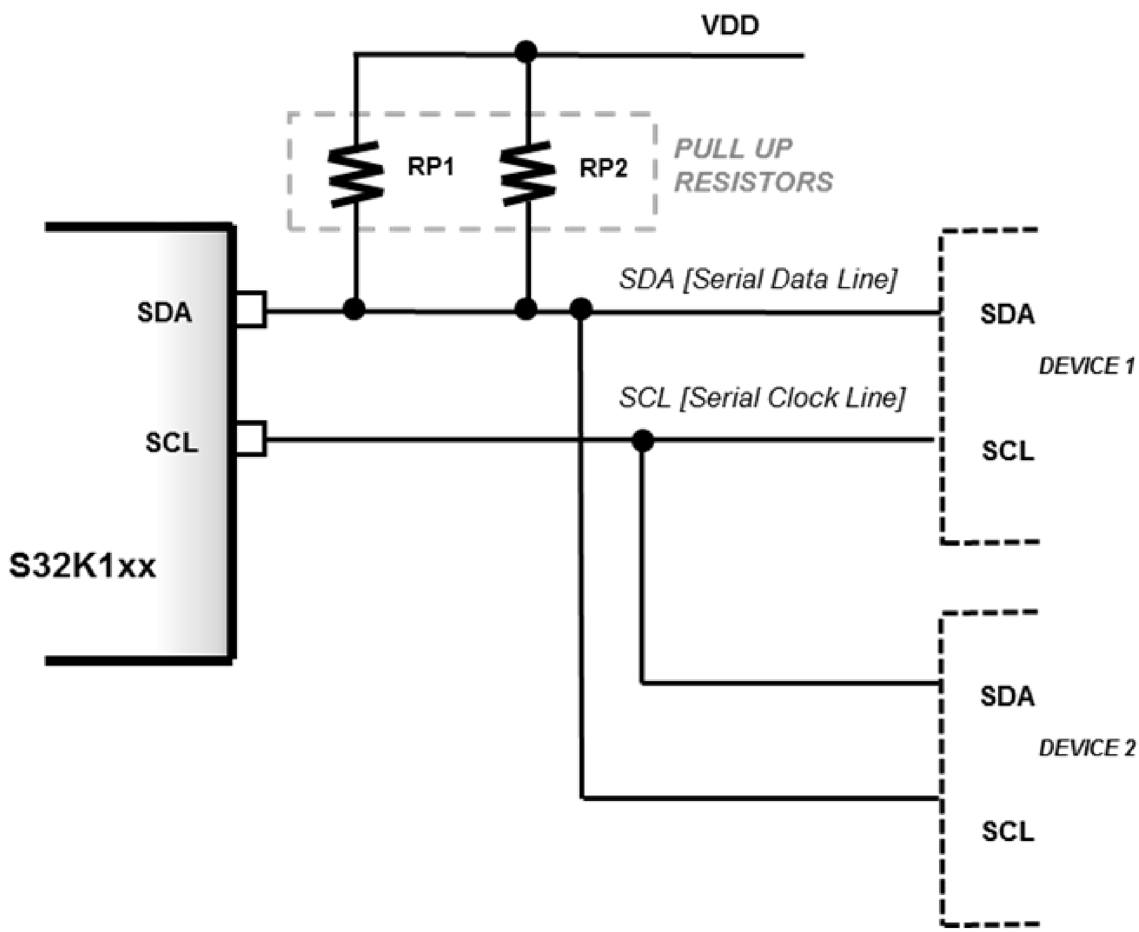


Figure 16. Connection of I2C-bus devices to the I2C-bus

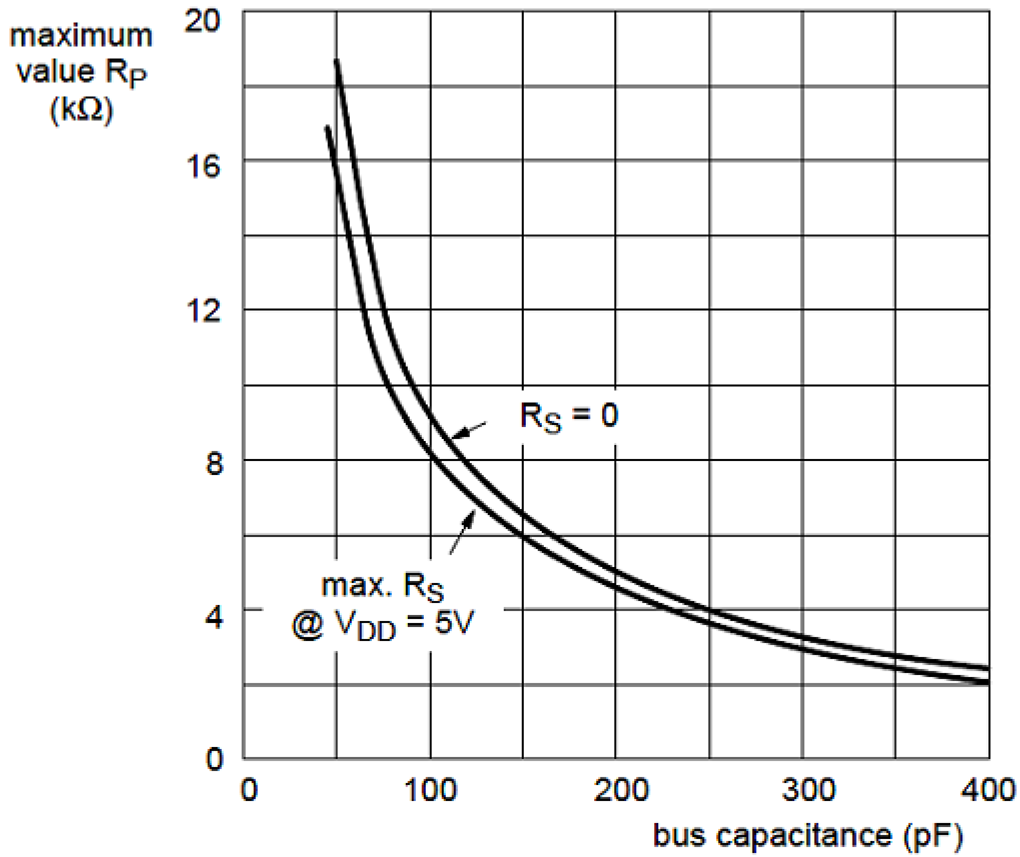


Figure 17. Maximum value of RP as a function of bus capacitance for a standard-mode I2C-bus

7 Unused pins

Unused digital pins can be left floating. To reduce power consumption, it is recommended that these unused digital pins are configured as inputs and have the internal pull resistor enabled. This will decrease current consumption and susceptibility to external electromagnetic noise. ADC unused pins should be grounded to reduce leakage currents. The EXTAL and XTAL pins default reset condition is to have pull-downs enabled. These pins should be connected to ground if not used.

8 General board layout guidelines

8.1 Traces recommendations

A right angle in a trace can cause more radiation. The capacitance increases in the region of the corner and the characteristic impedance changes. This impedance change causes reflections. Avoid right-angle bends in a trace and try to route them with at least two 45° corners. To minimize any impedance change, the best routing would be a round bend, as shown in Figure 18. Poor and correct way of bending traces in right angles on page 22.

Figure 18. Poor and correct way of bending traces in right angles

To minimize crosstalk, not only between two signals on one layer but also between adjacent layers, route them 90° to each other.

Complex boards need to use vias while routing; you have to be careful when using them. These add additional capacitance and inductance, and reflections occur due to the change in the characteristic impedance. Vias also increase the trace length. While using differential signals, use vias in both traces or compensate the delay in the other trace.

8.2 Grounding

Grounding techniques apply to both multi-layer and single-layer PCBs. The objective of grounding techniques is to minimize the ground impedance and thus to reduce the potential of the ground loop from circuit back to the supply.

- Route high-speed signals above a solid and unbroken ground plane.
- Do not split the ground plane into separate planes for analog, digital, and power pins. A single and continuous ground plane is recommended.
- There should be no floating metal/shape of any kind near any area close to the microcontroller pins. Fill copper in the unused area of signal planes and connect these coppers to the ground plane through vias.

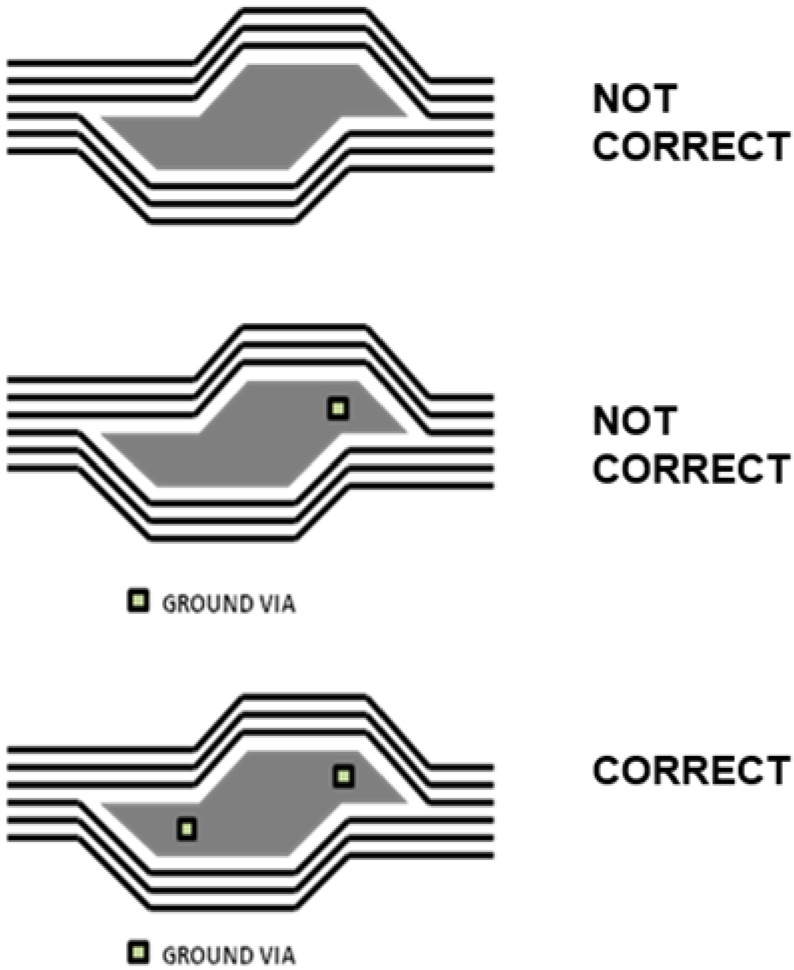
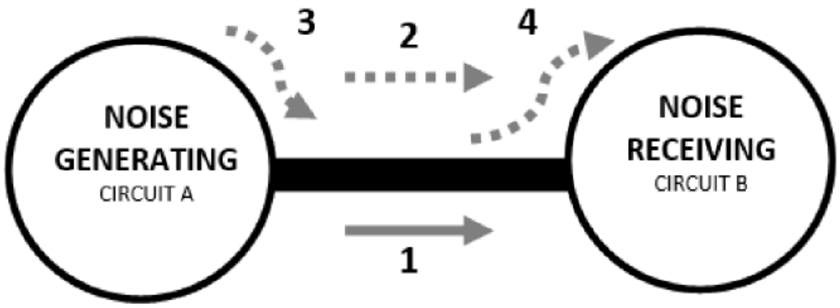


Figure 19. Eliminating floating metal/shape

8.3 EMI/EMC and ESD considerations for layout

These considerations are important for all system and board designs. Though the theory behind this is well explained, each board and system experiences this in its own way. There are many PCB and component related variables involved.

This application note does not go into the electromagnetic theory or explain the whys of different techniques used to combat the effects, but it considers the effects and solutions most recommended as applied to CMOS circuits. EMI is radio frequency energy that interferes with the operation of an electronic device. This radio frequency energy can be produced by the device itself or by other devices nearby. Studying EMC for your system allows testing the ability of your system to operate successfully counteracting the effects of unplanned electromagnetic disturbances coming from the devices and systems around it. The electromagnetic noise or disturbances travels via two media: Conduction and Radiation.



	Propagation path
1	Conductor
2	Air
3	Air to Conductor
4	Conductor to Air

Figure 20. Electromagnetic noise propagation

The design considerations narrow down to:

- The radiated & conducted EMI from your board should be lower than the allowed levels by the standards you are following.
- The ability of your board to operate successfully counteracting the radiated & conducted electromagnetic energy (EMC) from other systems around it.

The EMI sources for a system consists of several components such as PCB, connectors, cables and so on. The PCB plays a major role in radiating the high frequency noise. At higher frequencies and fast-switching currents and voltages, the PCB traces become effective antennas radiating electromagnetic energy; e.g., a large loop of signal and corresponding ground. The five main sources of radiation are: digital signals propagating on traces, current return loop areas, inadequate power supply filtering or decoupling, transmission line effects, and lack of power and ground planes. Fast switching clocks, external buses and PWM signals are used as control outputs and in switching power supplies. The power supply is another major contributor to EMI. RF signals can propagate from one section of the board to another building up EMI. Switching power supplies radiate the energy which can fail the EMI test. This is a huge subject and there are many books, articles and white papers detailing the theory behind it and the design criteria to combat its effects.

Every board or system is different as far as EMI/EMC and ESD issues are concerned, requiring its own solution.

However, the common guidelines to reduce an unwanted generation of electromagnetic energy are as shown below:

- Ensure that the power supply is rated for the application and optimized with decoupling capacitors.
- Provide adequate filter capacitors on the power supply source. The bulk/bypass and decoupling capacitors should have low equivalent series inductance (ESL).
- Create ground planes if there are spaces available on the routing layers. Connect these ground areas to the ground plane with vias.
- Keep the current loops as small as possible. Add as many decoupling capacitors as possible. Always apply current return rules to reduce loop areas.
- Keep high-speed signals away from other signals and especially away from input and output ports or connectors.

9 References

- Crystal Oscillator Troubleshooting Guide - NXP Semiconductors
- AN2049 Some Characteristics and Design Notes for Crystal Feedback ...
- AN10853 ESD and EMC sensitivity of IC - NXP Semiconductors
- AN2321: Designing for Board Level Electromagnetic Compatibility - NXP Semiconductors
- AN10897 A guide to designing for ESD and EMC

10 Revision history

Table 7. Sample revision history

Revision number	Date	Substantive changes
0	03/2017	Initial release

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