

# MCIMX6UL-BB

# Schematics DevBoard

## Table of Content

Page 1	Cover
Page 2	Block Diagram
Page 3	PWR TREE
Page 4	LCD
Page 5	HDMI
Page 6	USB
Page 7	CAN
Page 8	Sensor
Page 9	Codec
Page 10	Ethernet x1
Page 11	Ethernet x2
Page 12	SD/BT
Page 13	Camera
Page 14	DBG/JTAG
Page 15	SYS PWR
Page 16	SODIMM BB
Page 17	NOTE
Page 18	IOMUX
Page 19	
Page 20	
Page 21	
Page 22	
Page 23	
Page 24	
Page 25	
Page 26	
Page 26	
Page 27	
Page 28	

## Revision History

Rev. Code	Date	By	Description
A	2015-02-28	Javen	1 Revision A released
B	2015-07-07	Javen	1 DNP R1023 DNP R1435, R1404, Add R1436 DNP R1517, Install R1520 Change Camera J1801 connector Change JTAG J1902 footprint Change SODIMM J2101 footprint Change R2101 from PU to PD Change J1901 PIN sequence
C	2015-07-14	Javen	1 Add R919-R946, L903-L905 DNP R1436, Install R1404, R1435 Change HP_MIC1N to LINPUT1 Add BT_DISABLE, ECSPi4_SS0, ECSPi4_MOSI, ECSPi4_SCLK for BT Add R2107-R2116 to reduce the VSNVS power consumption due to the TAMPER reason Add L903-L930 as FCC/CE backup  Change Camera J1801 connector direction on layout Add C905  Change J1701 from TOP contact to BOT contact for BT
C1	2016-05-05	Javen	1 DNP J1801, J1001 due to cost reason
C2	18-Oct-2016	Marek B.	Updated to be NCL compliance. - parts: J901, J1701, J1802, J2101 - Title blocks

1. Unless Otherwise Specified:

- All resistors are in ohms, 10%, 1/8 Watt, 0603
- All capacitors are in uF, 20%, 50V, 0603
- All voltages are DC
- All polarized capacitors are aluminum electrolytic


2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:

- \_B Denotes - Active-Low Signal
- <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

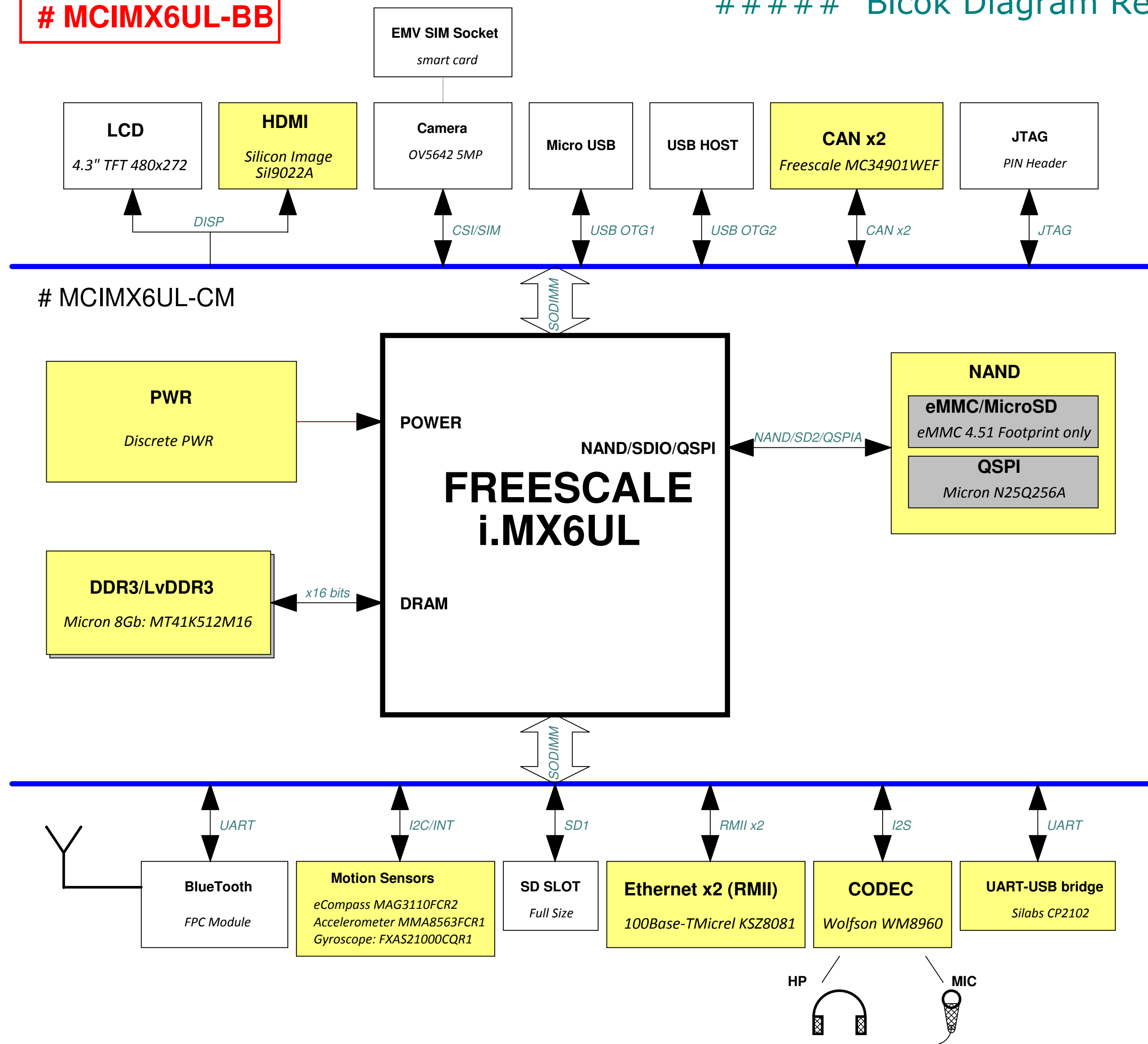
		<b>Microcontroller Solutions Group</b> 6501 William Cannon Drive West Austin, TX 78735-8598	
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.			
ICAP Classification: CP: IUC: X PUBL:			
Designer: <Designer>	Drawing Title: <b>MCIMX6UL-BB</b>		
Drawn by: <DrawnBy>	Page Title: <b>Title and Rev History</b>		
Approved: <Approver>	Size C	Document Number SCH-28616 PDF: SPF-28616	Rev C2
Date: Tuesday, October 18, 2016 Sheet 1 of 18			

# i.MX6UL EVK Block Diagram

##### Blcok Diagram Rev 1.0 #####

# MCIMX6UL-BB

MPN: MCIMX6UL-BB Agile No: 28616  
MPN: MCIMX6UL-CM Agile No: 28617

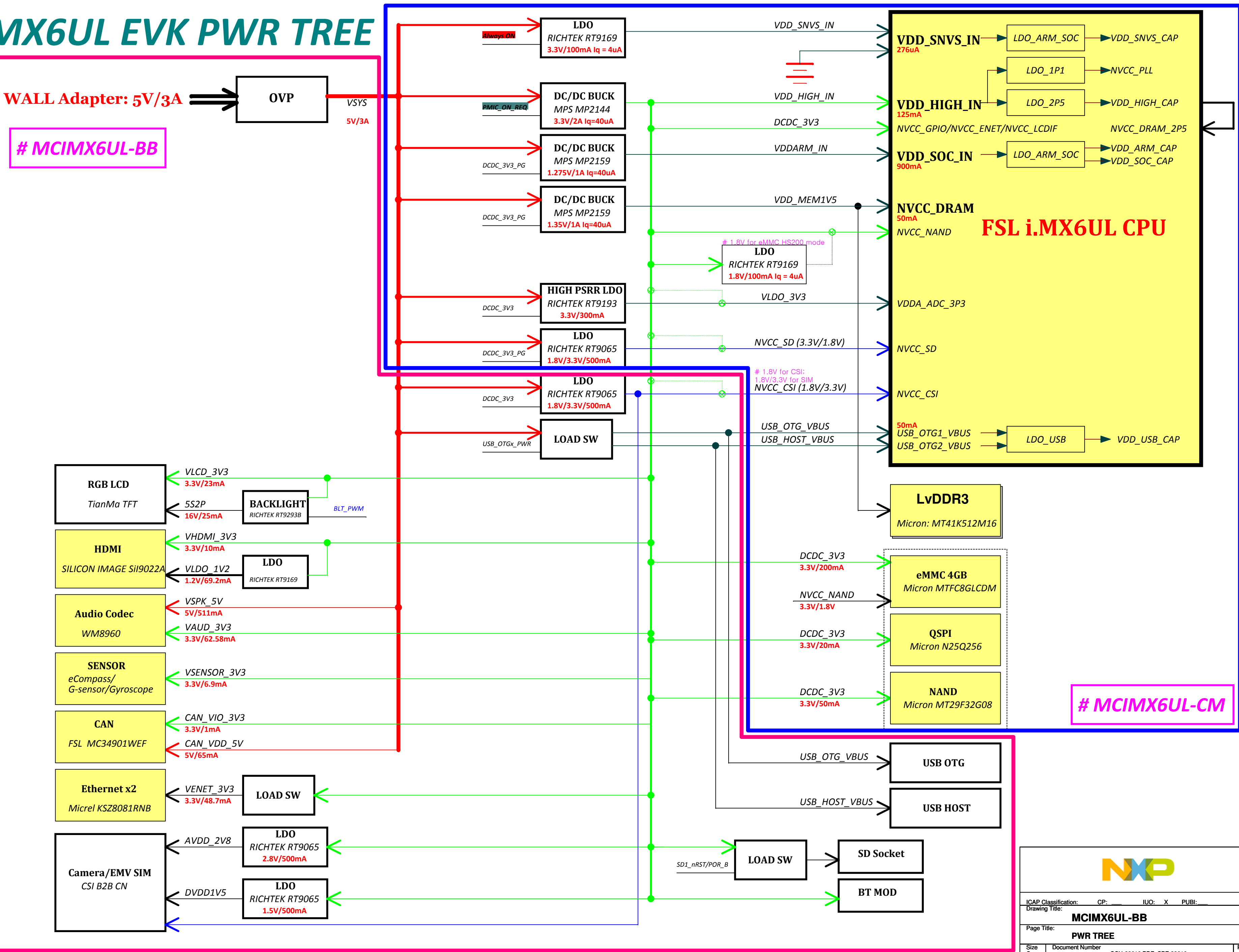


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Drawing Title:	<b>MCIMX6UL-BB</b>		
Page Title:	<b>Block Diagram</b>		
Size C	Document Number	SCH-28616 PDF: SPF-28616	Rev C2
Date:	Wednesday, October 12, 2016	Sheet 2	of 18

# i.MX6UL EVK PWR TREE

WALL Adapter: 5V/3A

# MCIMX6UL-BB



# MCIMX6UL-CM

**NXP**

ICAP Classification: CP: IVO: X PUBI:

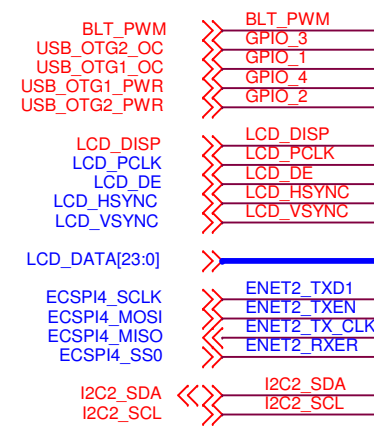
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Page Title: **PWR TREE**

Size C Document Number SCH-28616 PDF: SPF-28616 Rev C2

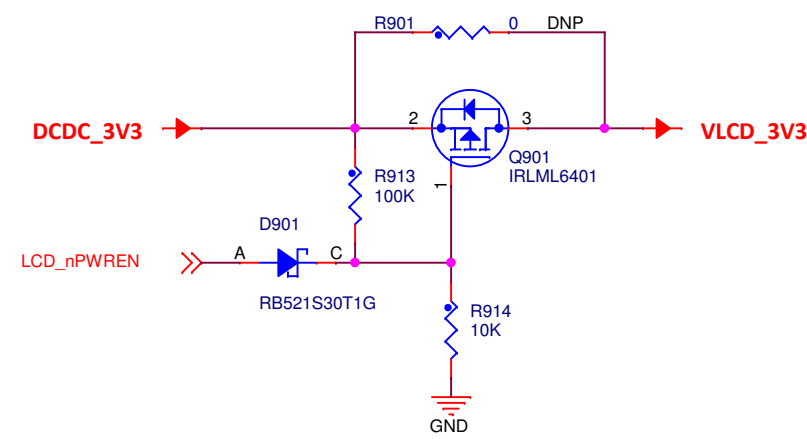
Date: Wednesday, October 12, 2016 Sheet 3 of 18

## LCD IF

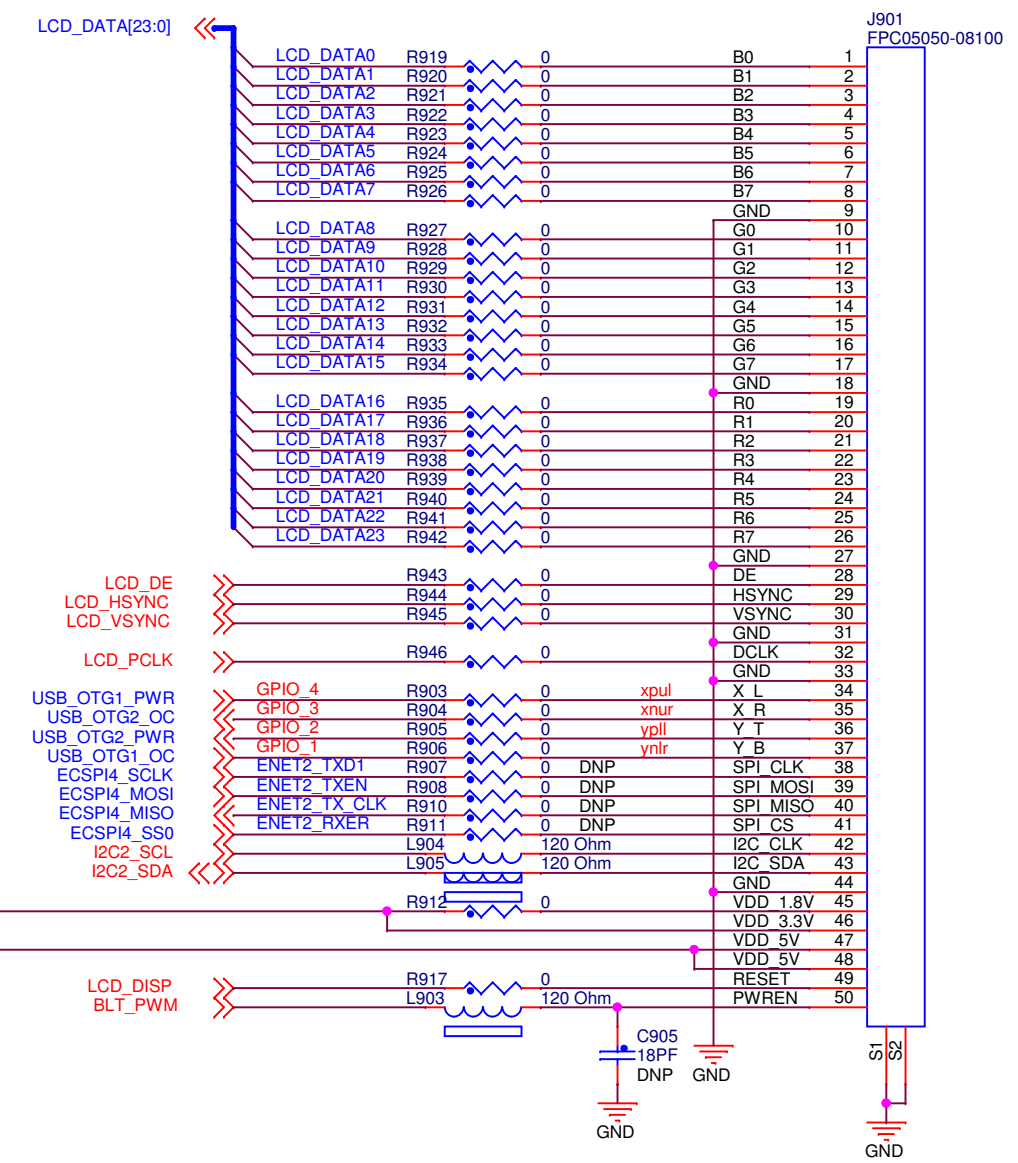


## PWR

# LCD Standby Mode PWR: 50uW



## LCD CN

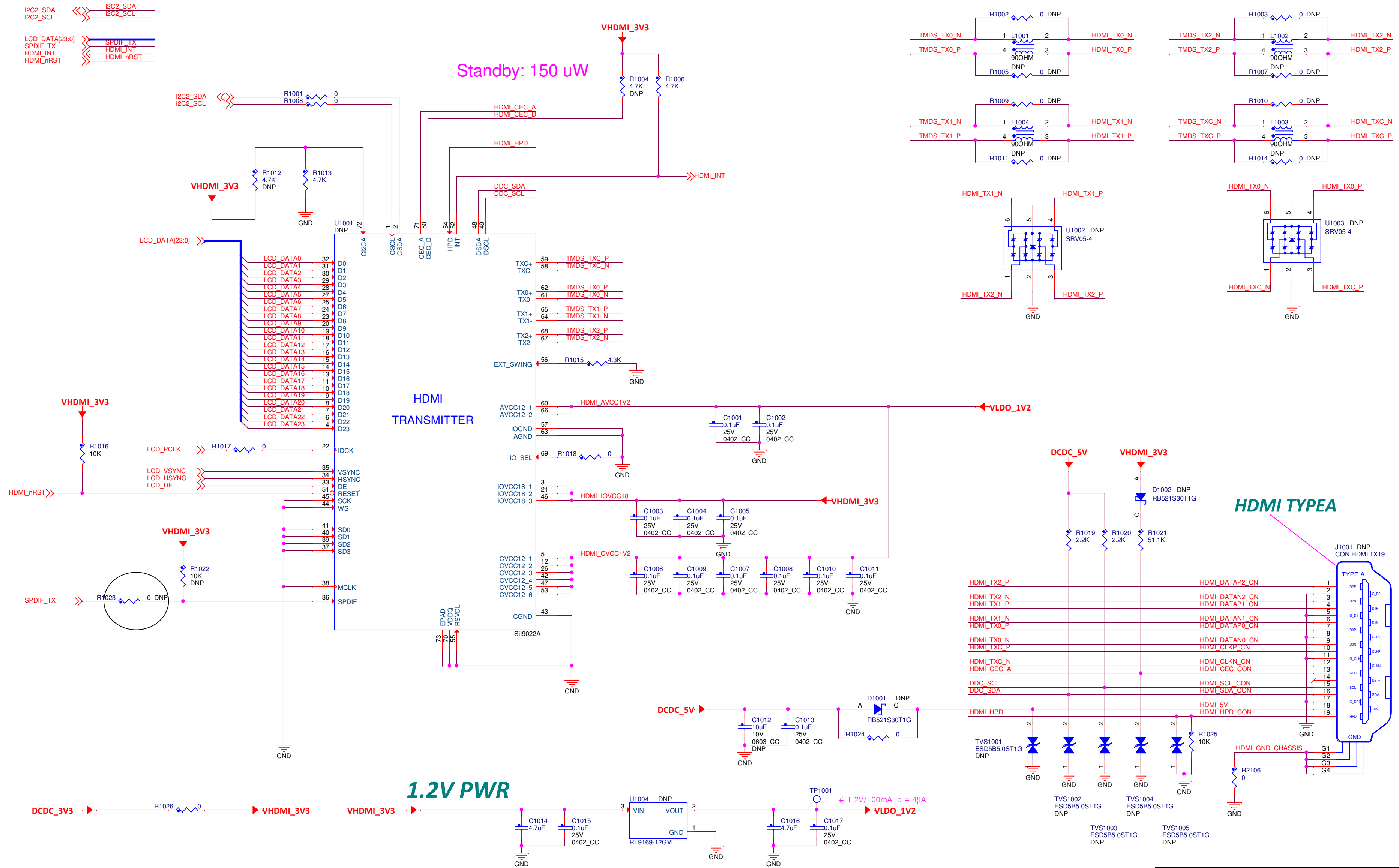


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Drawing Title:			
<b>MCIMX6UL-BB</b>			
Page Title:			
<b>LCD</b>			
Size	Document Number	SCH-28616 PDF: SPF-28616	Rev
C			C2
Date:	Tuesday, October 18, 2016		Sheet 4 of 18

# HDMI Transmitter

# EMI/ESD

#Res Overlap with EMI Choke



Standby: 150 uW

1.2V PWR

HDMI TYPEA

Internal Function	CI2CA = LOW	CI2CA = HIGH
Transmitter Programming Interface (TPI) device address	0x72	0x76
CEC Programming Interface (CPI) device address	0xC0	0xC4
Si9020-compatible internal registers: first device address	0x72	0x76
Si9020-compatible internal registers: second device address	0x7A	0x7E

**NXP**

ICAP Classification: CP: IUC: X PUBI: \_\_\_\_\_  
 Drawing Title: **MCIMX6UL-BB**  
 Page Title: **HDMI**  
 Size C Document Number SCH-28616 PDF: SPF-28616 Rev C2  
 Date: Wednesday, October 12, 2016 Sheet 5 of 18



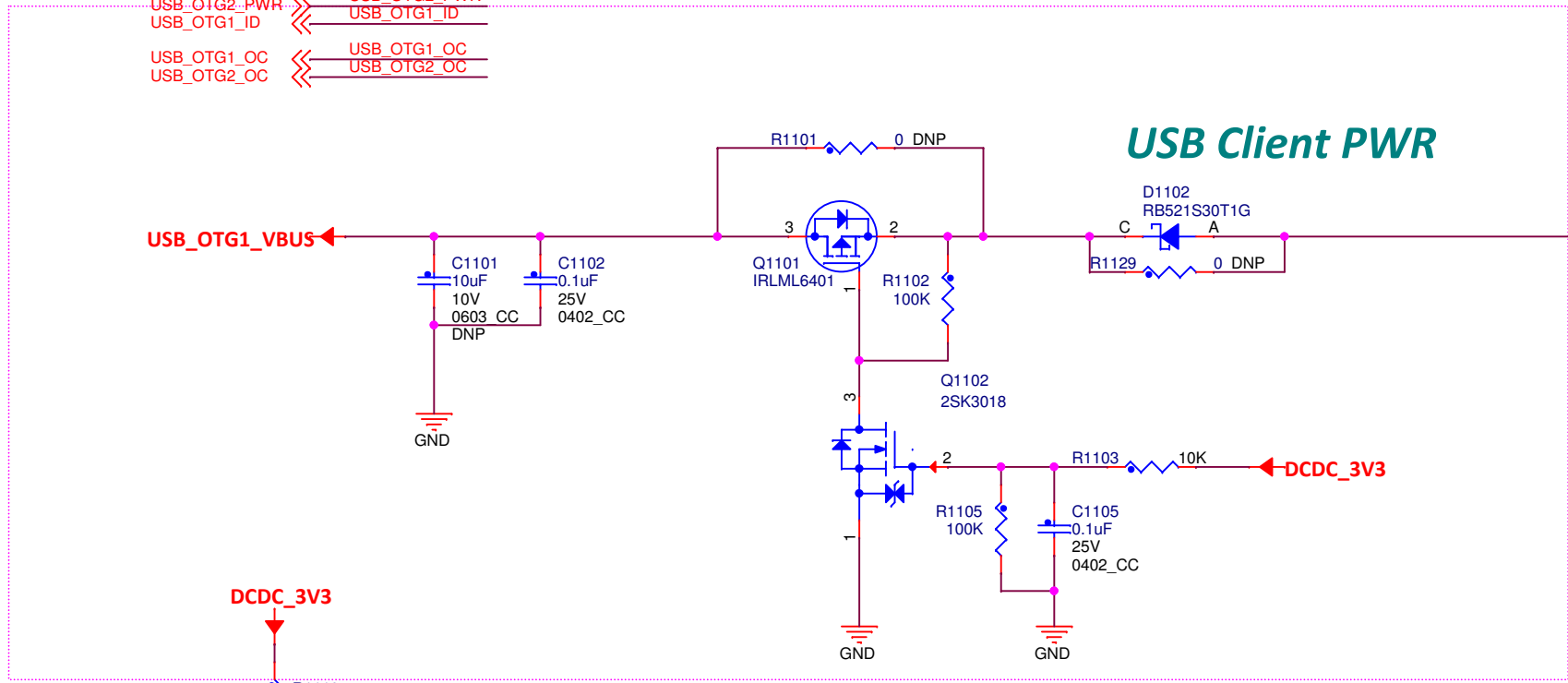
# USB HOST/OTG

USB\_OTG1\_DN <<> USB\_OTG1\_DN  
 USB\_OTG1\_DP <<> USB\_OTG1\_DP  
 USB\_OTG2\_DN <<> USB\_OTG2\_DN  
 USB\_OTG2\_DP <<> USB\_OTG2\_DP

USB\_OTG1\_PWR <<> USB\_OTG1\_PWR  
 USB\_OTG2\_PWR <<> USB\_OTG2\_PWR  
 USB\_OTG1\_ID <<> USB\_OTG1\_ID

USB\_OTG1\_OC <<> USB\_OTG1\_OC  
 USB\_OTG2\_OC <<> USB\_OTG2\_OC

## USB Client PWR



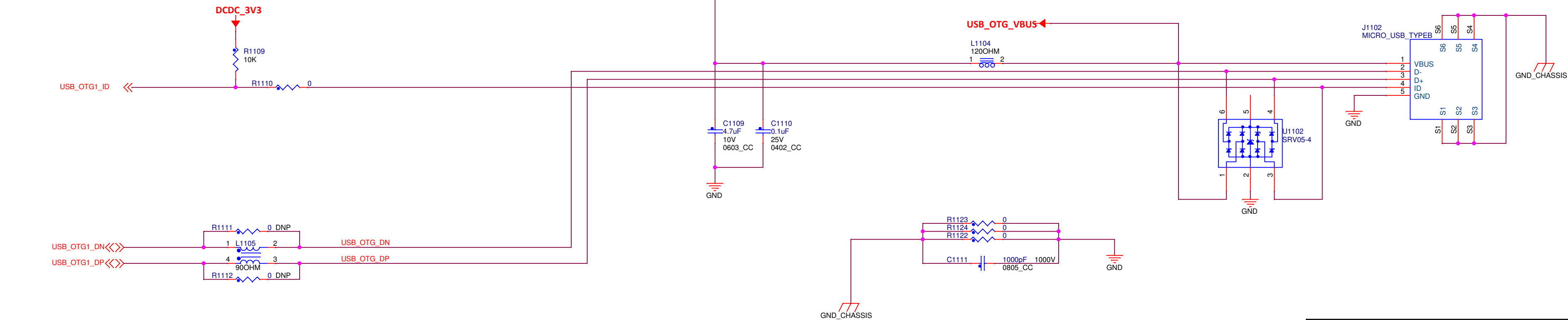
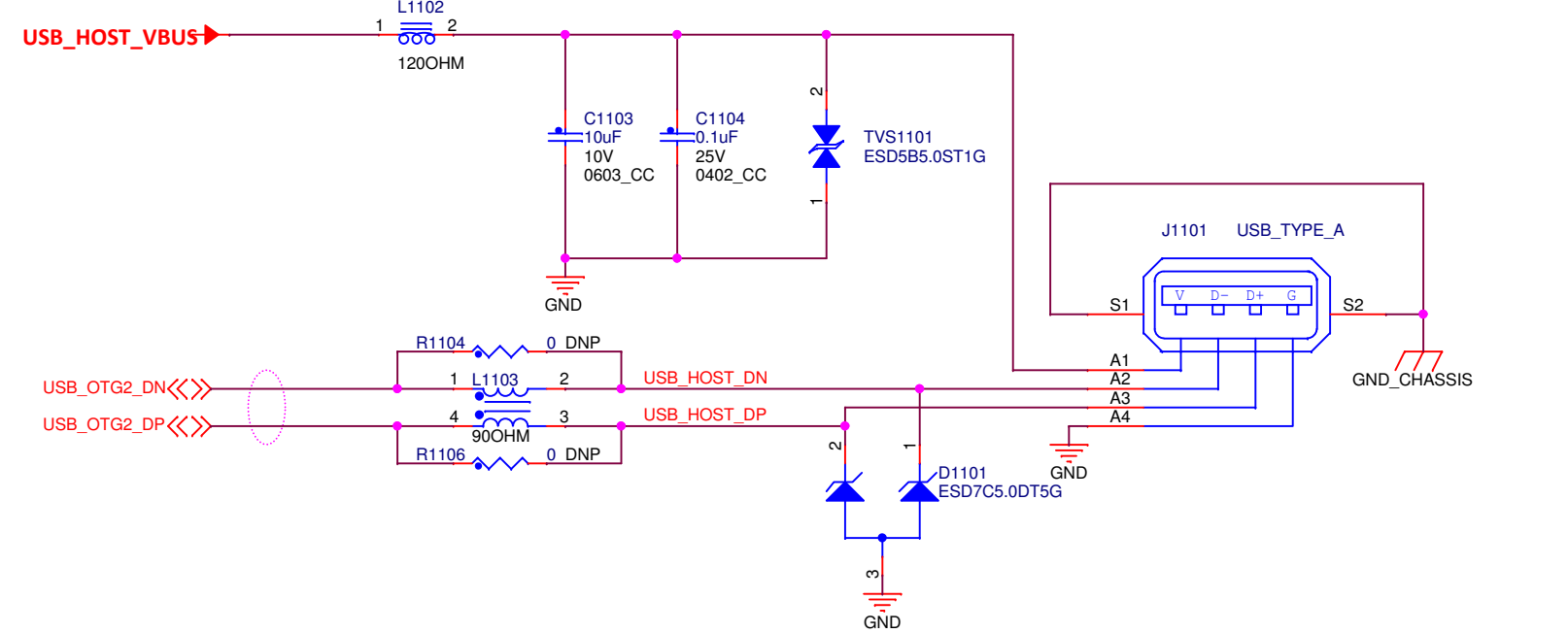
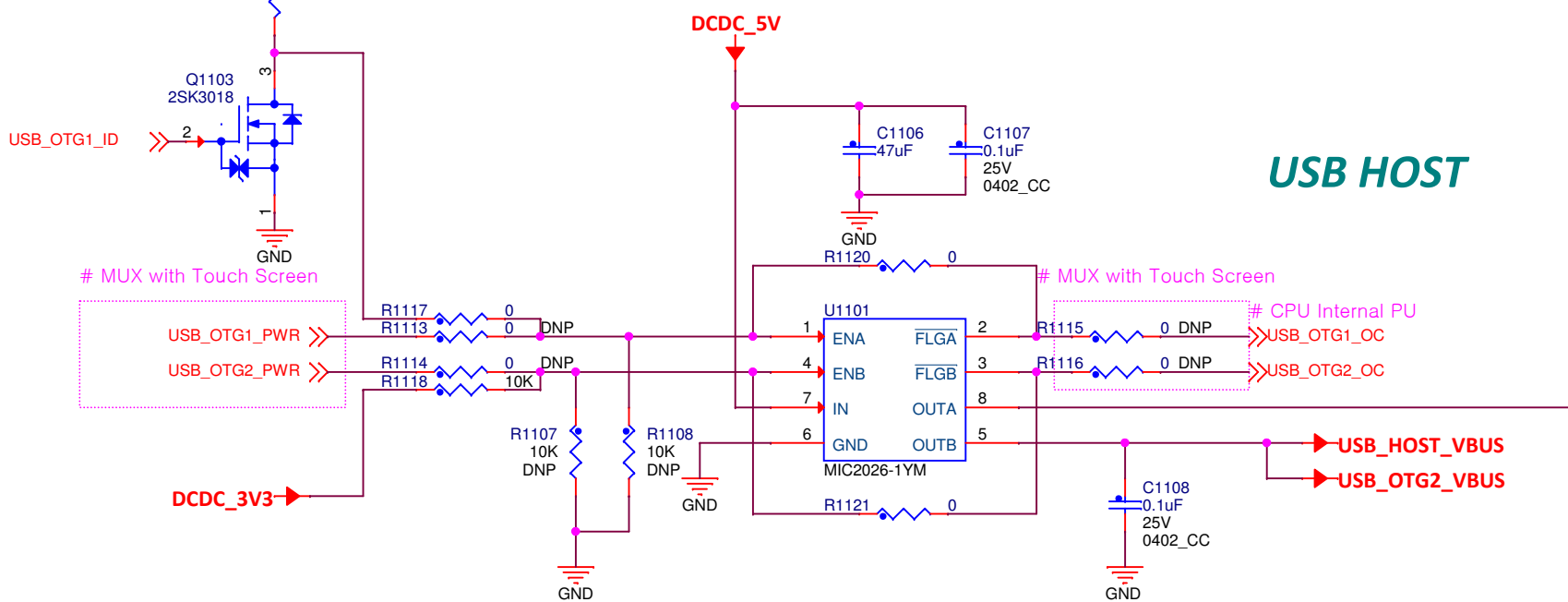
Need to use MIC5225 for ceramic output cap.

Max output current from MIC5225 is 150mA

$$V_o = 1.24V \times (1 + R_a/R_b)$$

This block is reserved for USB OTG certification test.

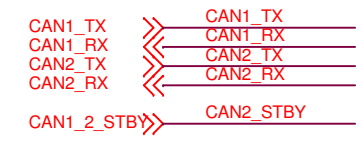
## USB HOST



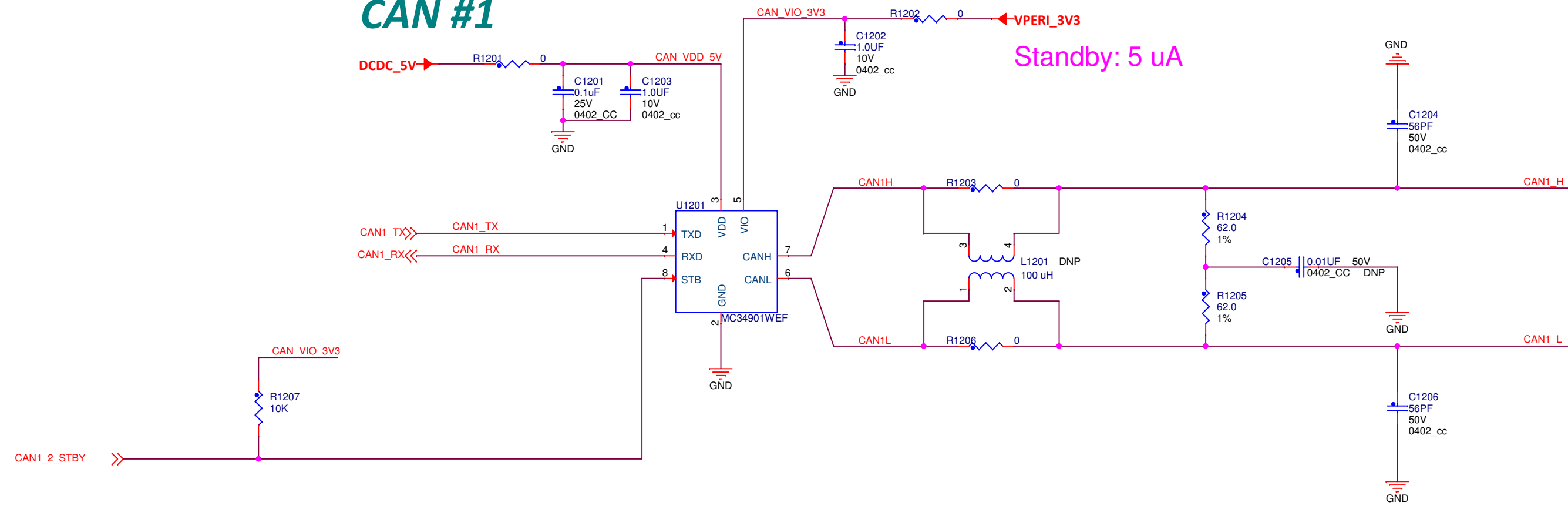
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Page Title:					
<b>USB</b>					
Size	Document Number	SCH-28616 PDF: SPF-28616			Rev
C					C2
Date: Wednesday, October 19, 2016					
				Sheet	6 of 18

# High Speed CAN Transceiver

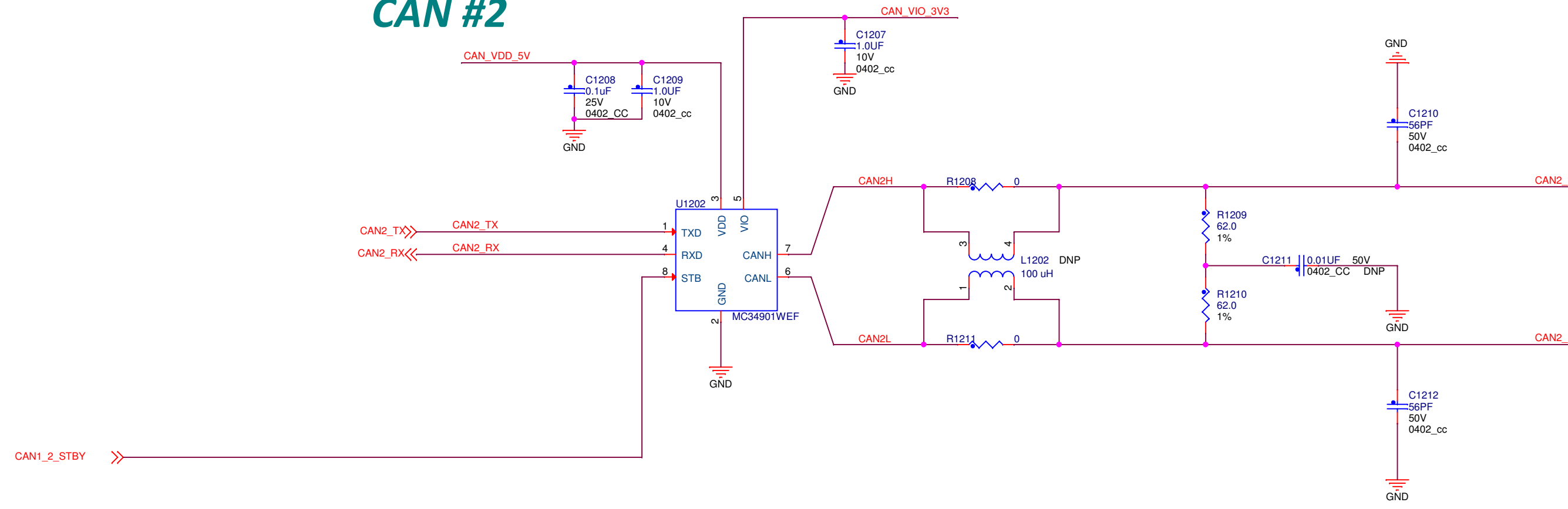
# FSL High Speed CAN Transceiver



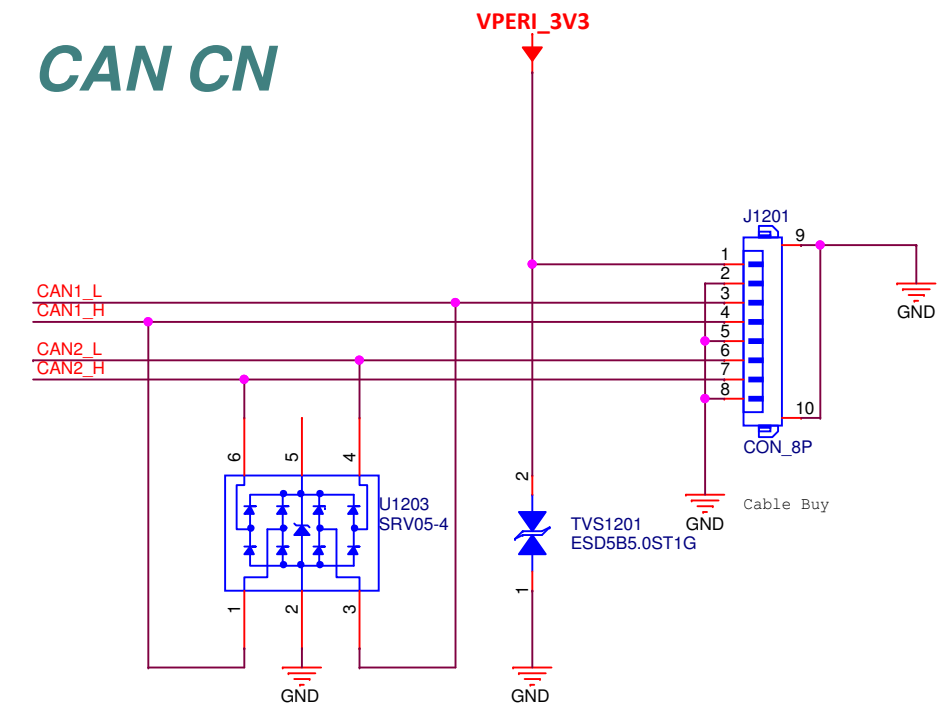
## CAN #1



## CAN #2



## CAN CN



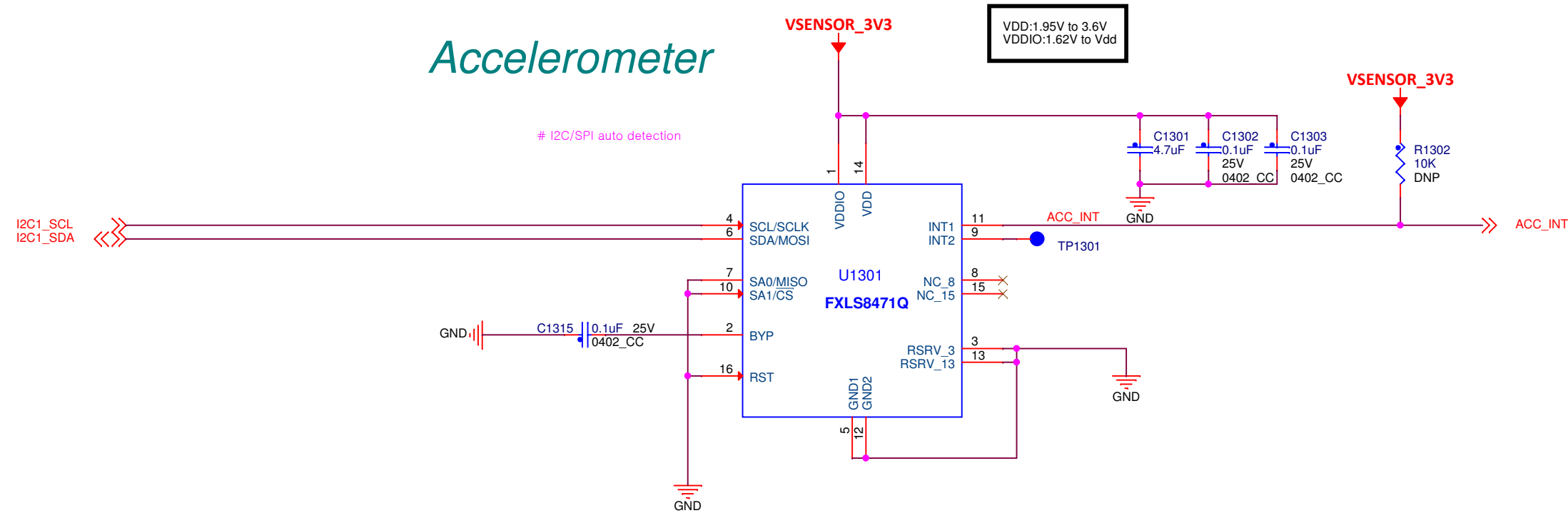
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Drawing Title: <b>MCIMX6UL-BB</b>	
Page Title: <b>CAN</b>	
Size C	Document Number SCH-28616 PDF: SPF-28616
Date: Wednesday, October 12, 2016	Sheet 7 of 18

# Motion Sensor 9-axis

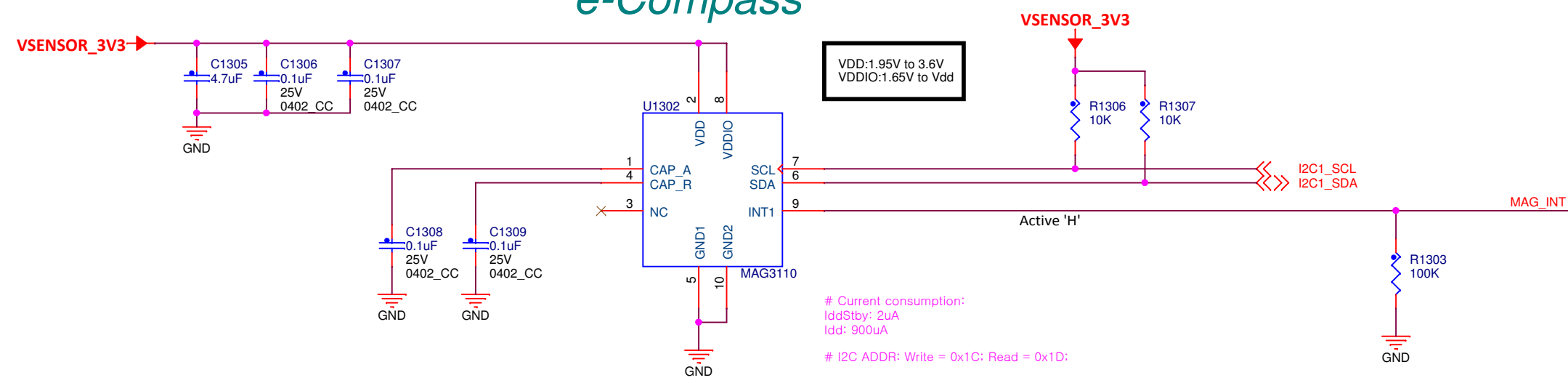
I2C1\_SDA  
I2C1\_SCL  
ACC\_INT

VPERI\_3V3 → R1301 → VSENSOR\_3V3

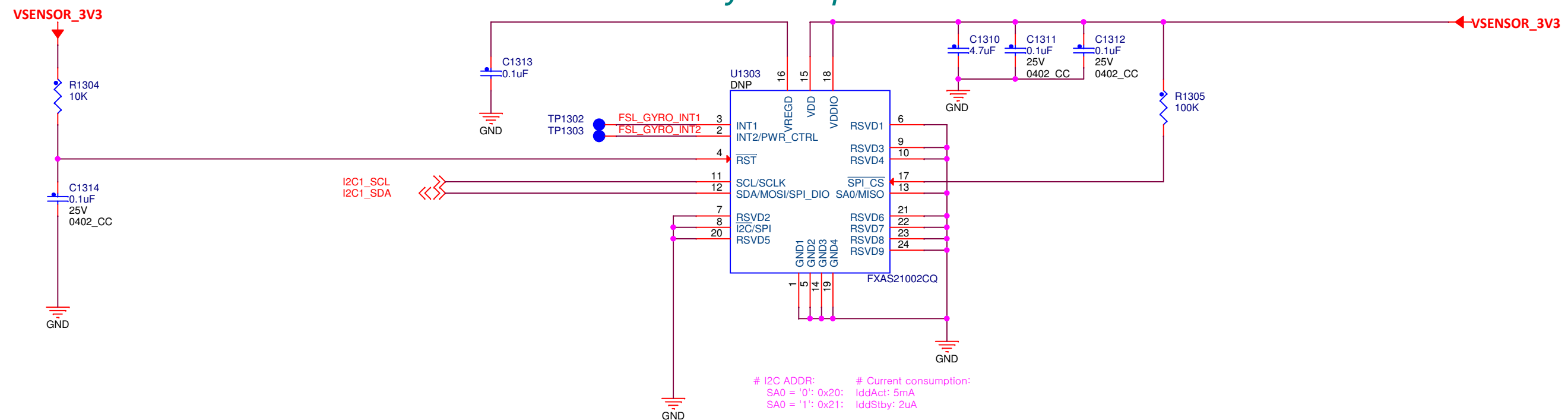
## Accelerometer



## e-Compass



## Gyroscope

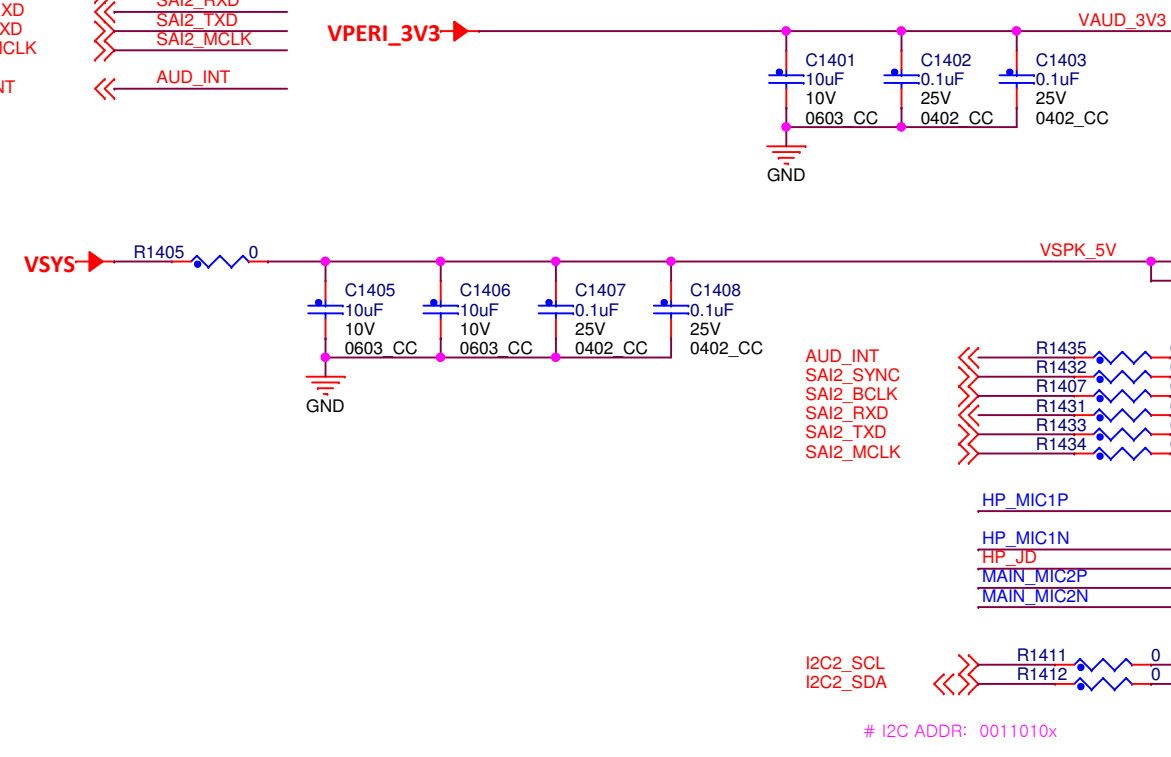


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Drawing Title: <b>MCIMX6UL-BB</b>			
Page Title: <b>Sensor</b>			
Size C	Document Number	SCH-28616 PDF: SPF-28616	Rev C2
Date:	Wednesday, October 12, 2016	Sheet 8	of 18

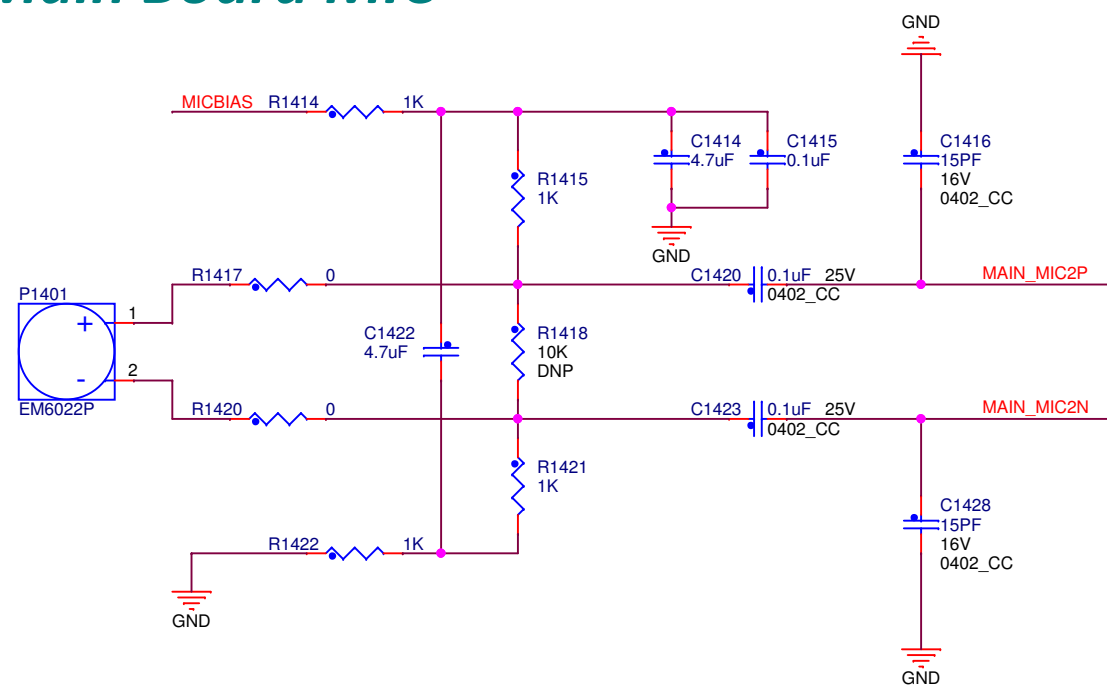


# Audio Codec

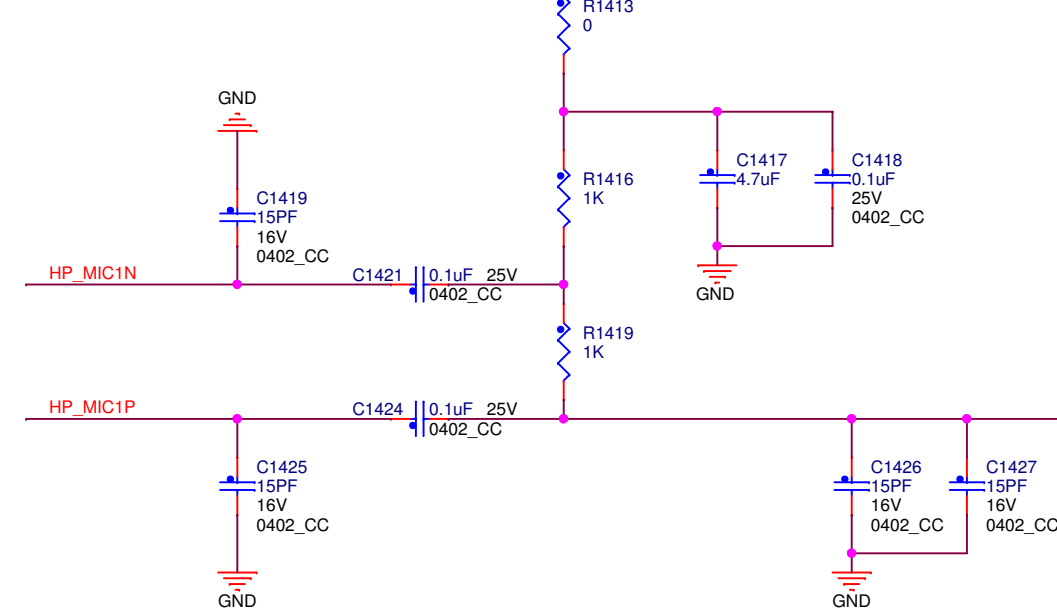
I2C2\_SDA <<> I2C2\_SDA  
 I2C2\_SCL <<> I2C2\_SCL  
 SAI2\_SYNC <<> SAI2\_SYNC  
 SAI2\_BCLK <<> SAI2\_BCLK  
 SAI2\_RXD <<> SAI2\_RXD  
 SAI2\_TXD <<> SAI2\_TXD  
 SAI2\_MCLK <<> SAI2\_MCLK  
 AUD\_INT <<> AUD\_INT



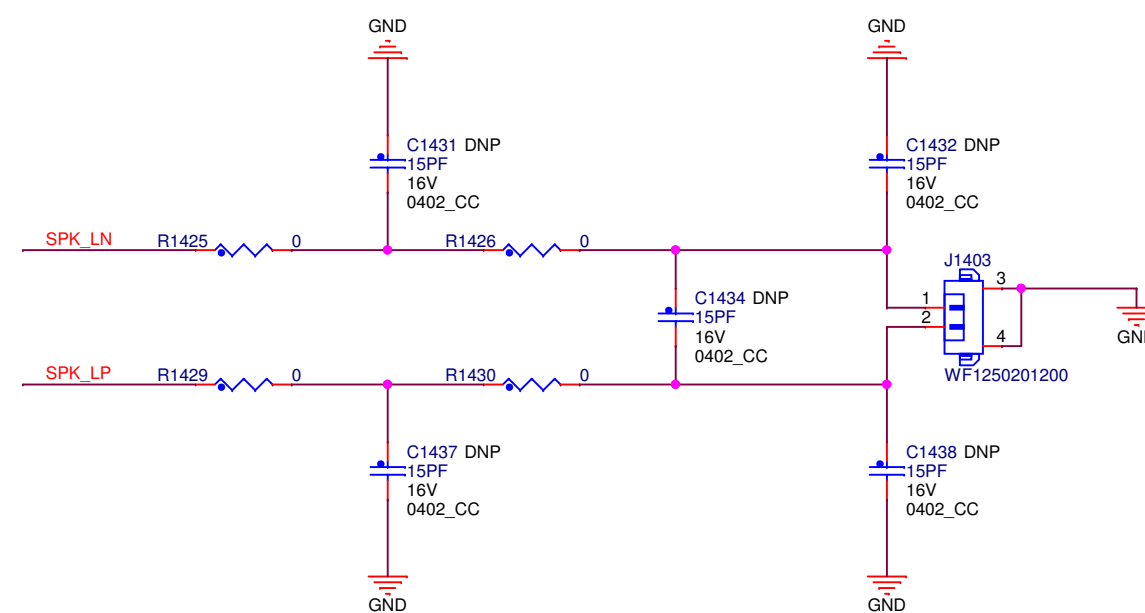
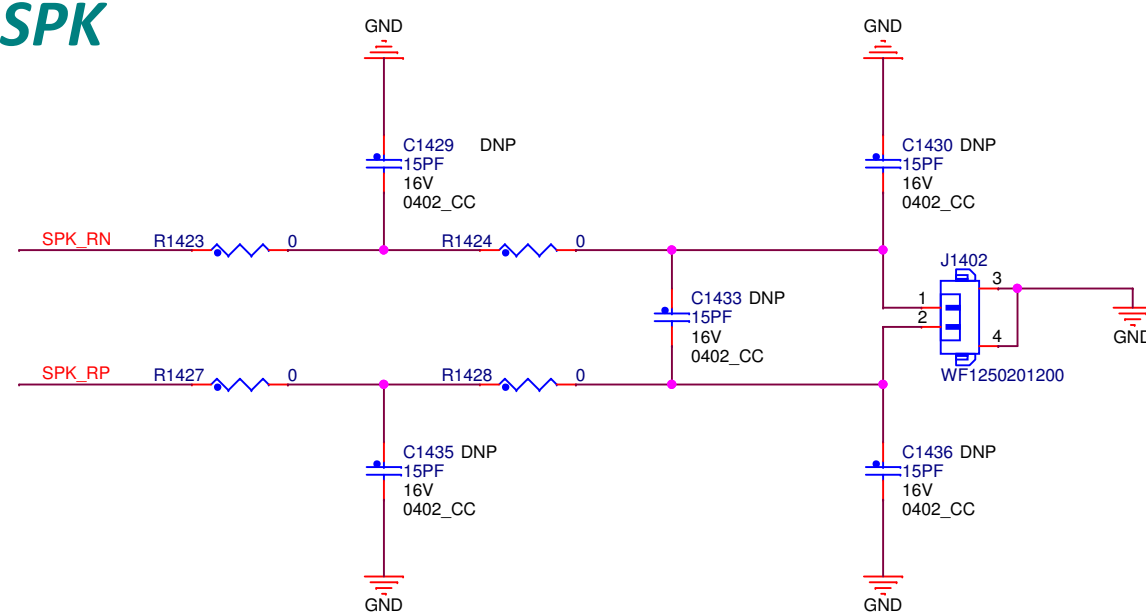
# Main Board MIC



# HP MIC



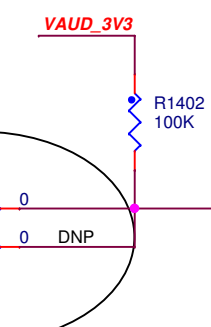
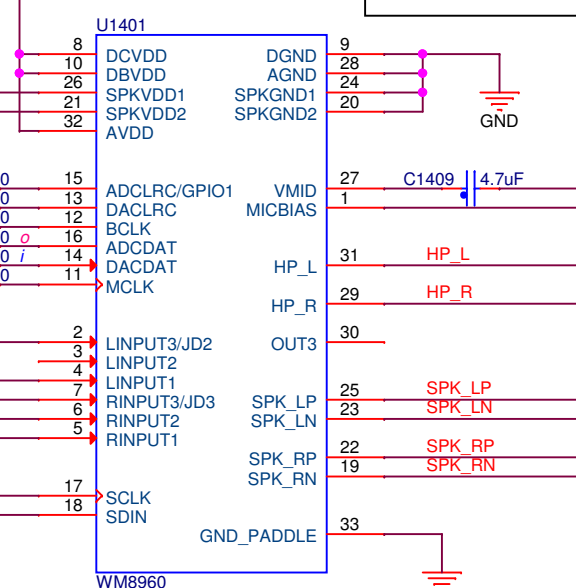
# SPK



# Codec

OFF, SLEEP MODE

DCVDD 1.71V - 3.6V  
 DBVDD 1.71V - 3.6V  
 AVDD 2.70V - 3.6V  
 SPKVDD 2.70V - 5.5V



# HP JACK

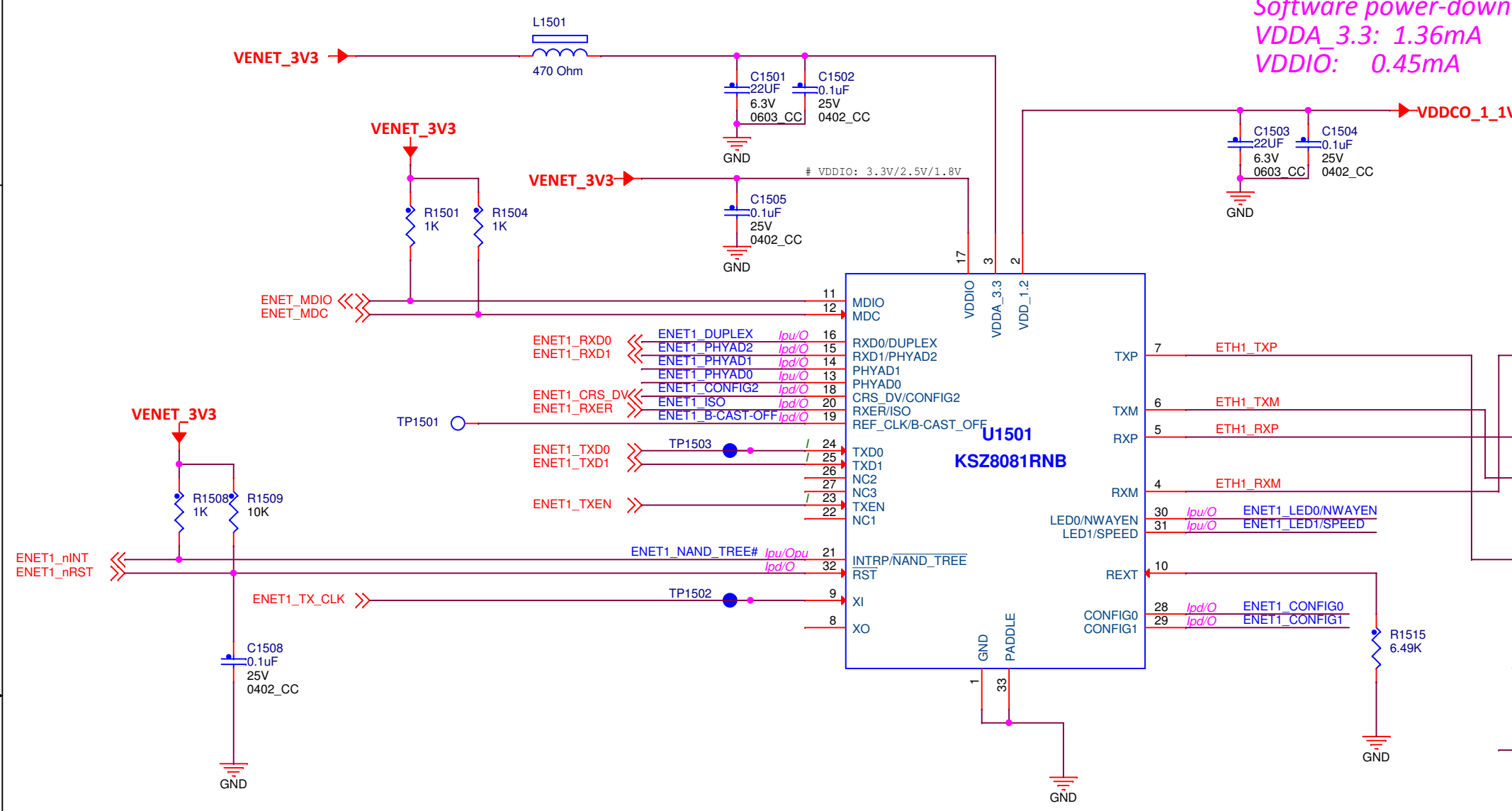
# HP\_DET:  
 LOW : REMOVE  
 HIGH : PLUG



ICAP Classification:	CP:	IUO: X	PUBI:
Drawing Title: <b>MCIMX6UL-BB</b>			
Page Title: <b>Codec</b>			
Size C	Document Number	SCH-28616 PDF: SPF-28616	Rev C2
Date:	Wednesday, October 12, 2016	Sheet 9	of 18

# 100M ETHERNET RMII PHY x1

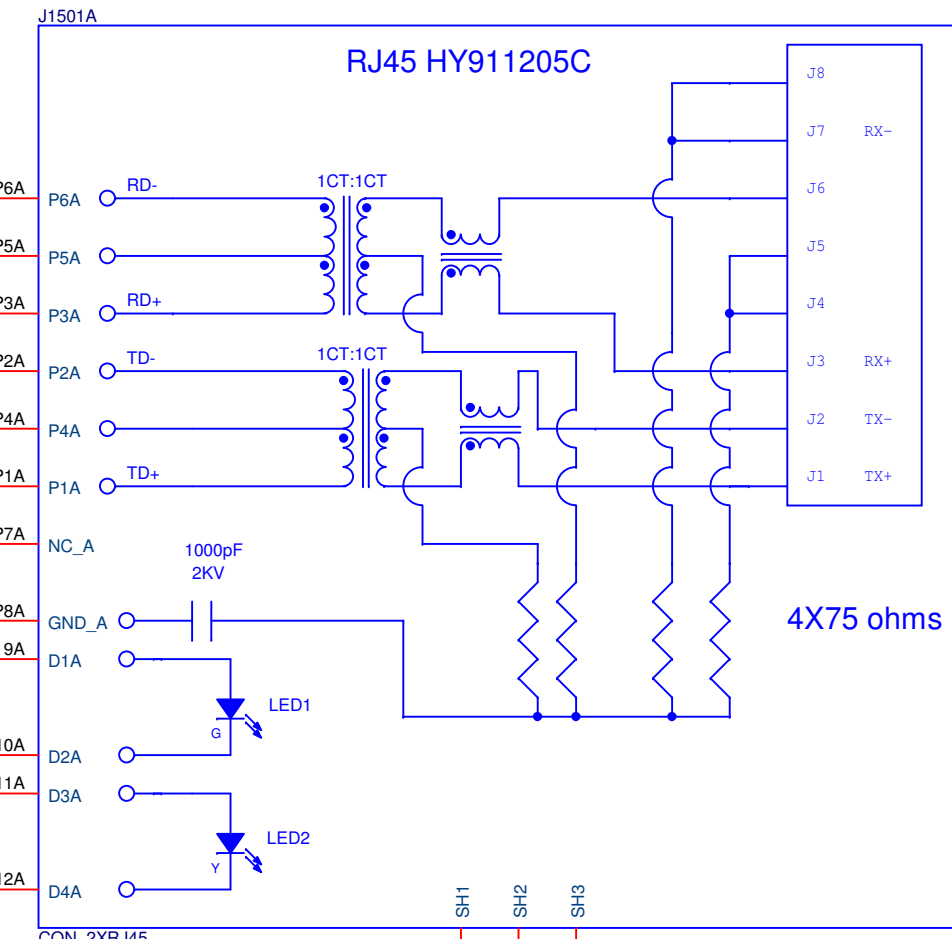
ENET\_MDIO <<> ENET\_MDIO  
 ENET\_MDC <<> ENET\_MDC  
 ENET1\_TXD0 <<> ENET1\_TXD0  
 ENET1\_TXD1 <<> ENET1\_TXD1  
 ENET1\_TXEN <<> ENET1\_TXEN  
 ENET1\_TX\_CLK <<> ENET1\_TX\_CLK  
 ENET1\_RXD0 <<> ENET1\_RXD0  
 ENET1\_RXD1 <<> ENET1\_RXD1  
 ENET1\_RXER <<> ENET1\_RXER  
 ENET1\_CRSDV <<> ENET1\_CRSDV  
 ENET1\_nINT <<> ENET1\_nINT  
 ENET1\_nRST <<> ENET1\_nRST



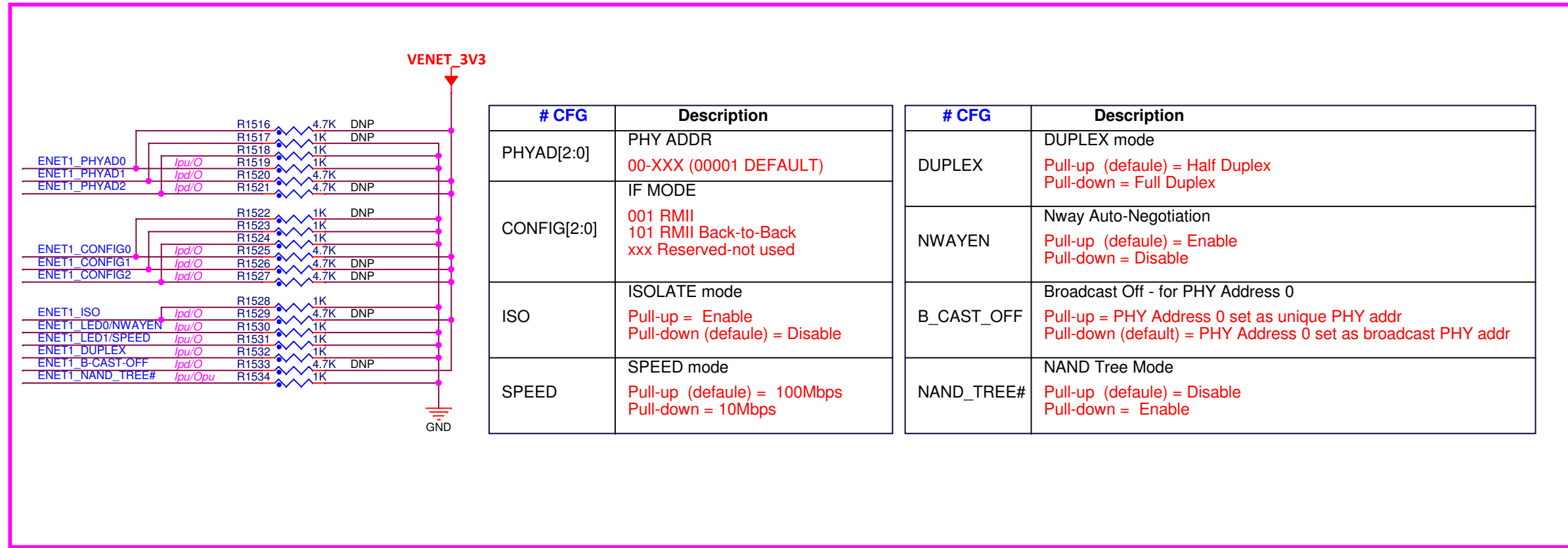
Software power-down mode:  
 VDDA\_3.3: 1.36mA  
 VDDIO: 0.45mA

## PHY PWR

VPERI\_3V3 → VENET\_3V3

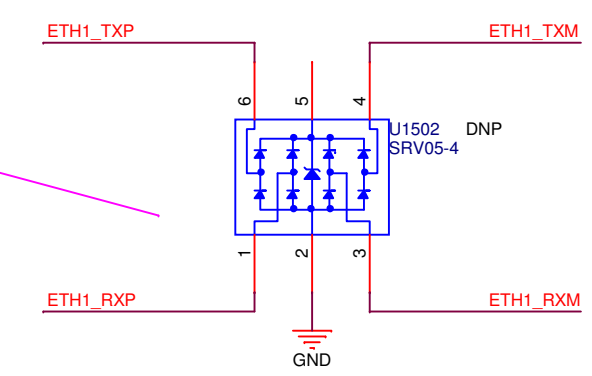


## RMII CFG



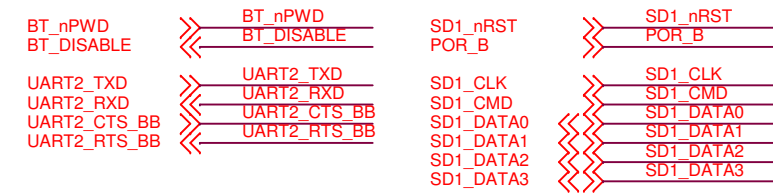
## ESD PROTECTION

# 2rd LEVEL ESD





# BLUETOOTH / SD FULL SOCKET

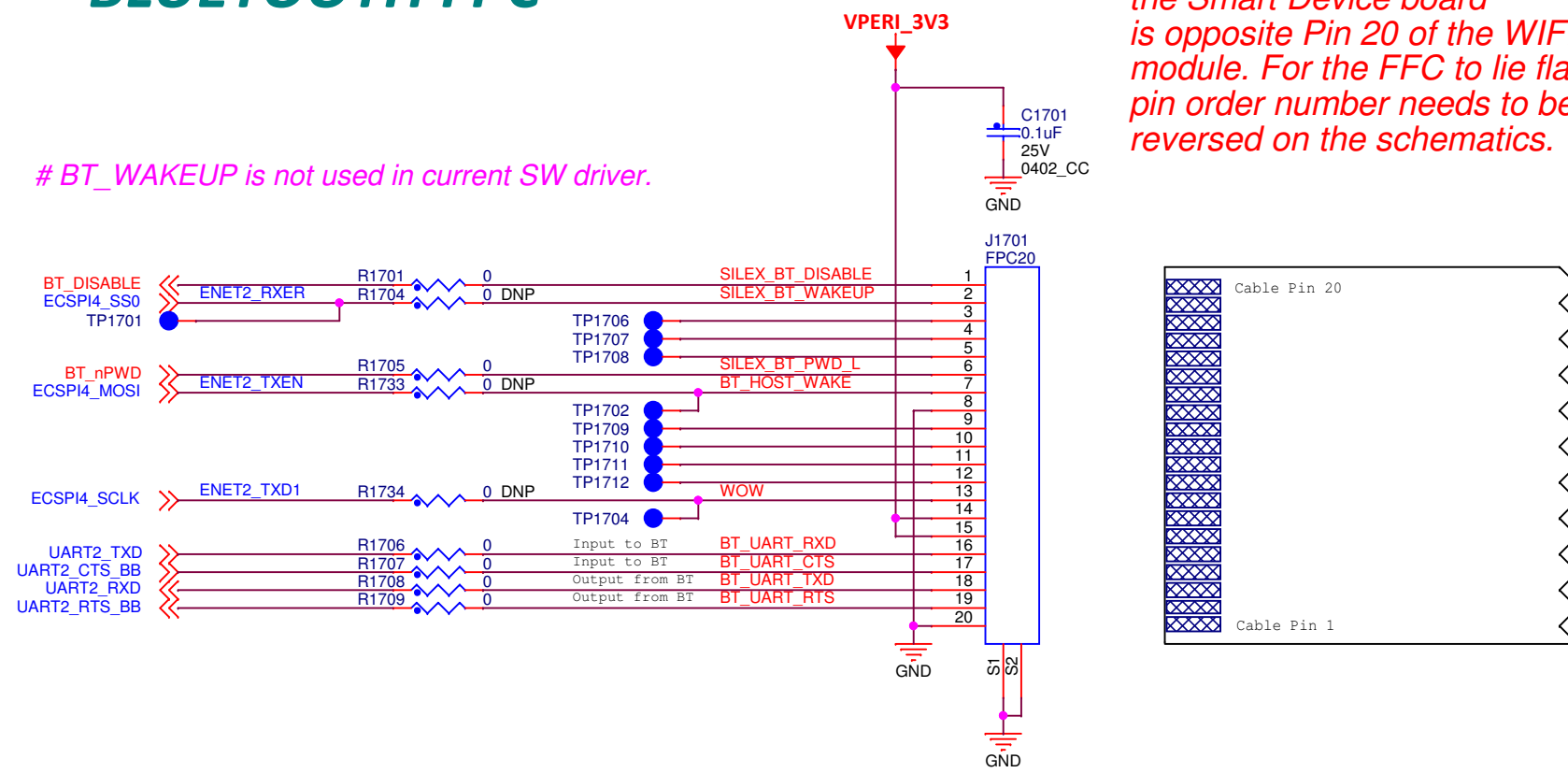


**NOTE:**  
The AUX SDIO CARD SOCKET and the BLUETOOTH CABLE CONNECTOR have been designed and tested specifically for use with the WIFI/BT combo card SX-SDCAN-2830BT Developed and sold by Silex Technology. The developer may need to consult the datasheet of other WIFI solutions for compatibility with this card socket.

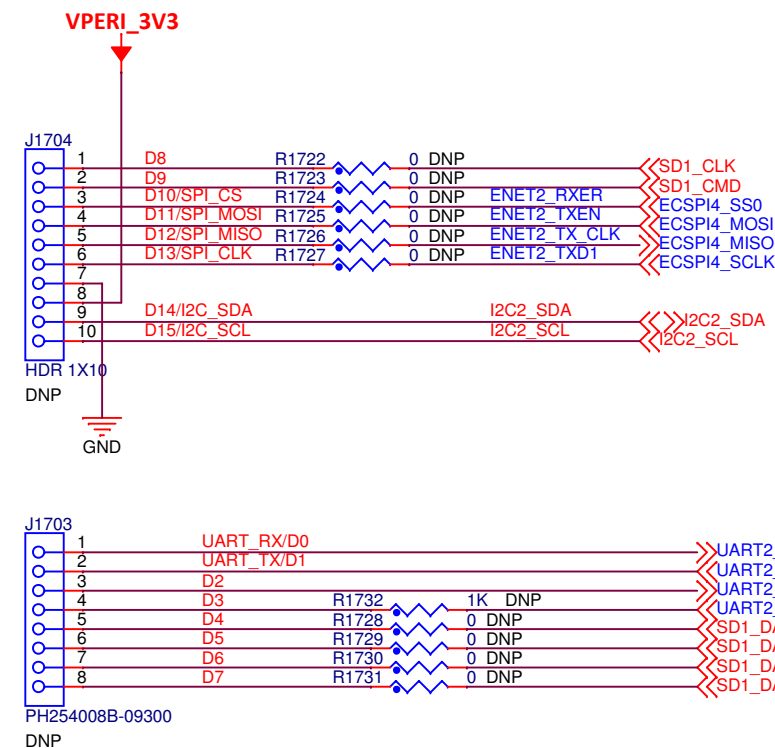
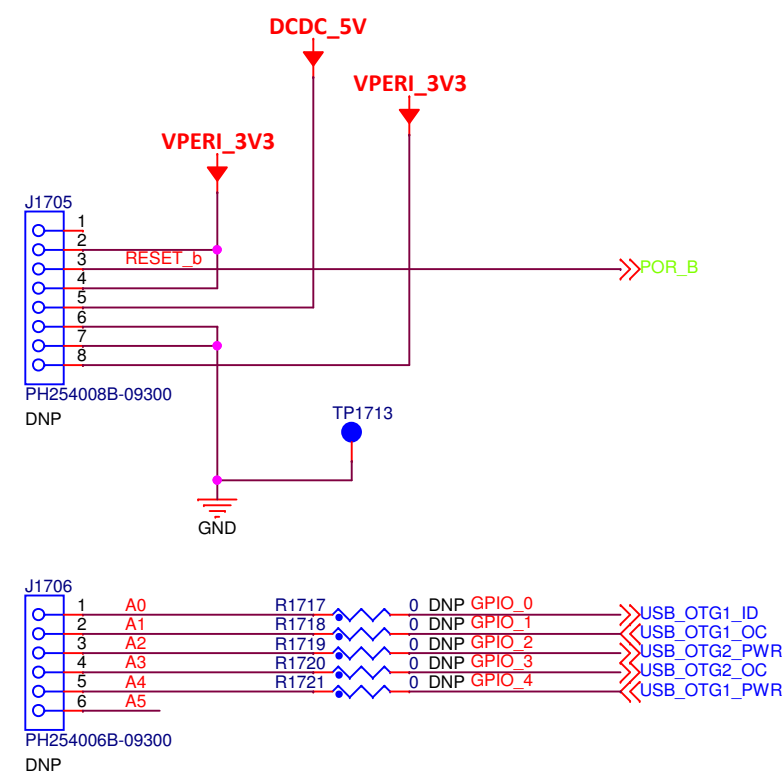
**NOTE:**  
Pin 1 of the cable connector on the Smart Device board is opposite Pin 20 of the WIFI/BT module. For the FFC to lie flat, the pin order number needs to be reversed on the schematics.

## BLUETOOTH FPC

# BT\_WAKEUP is not used in current SW driver.

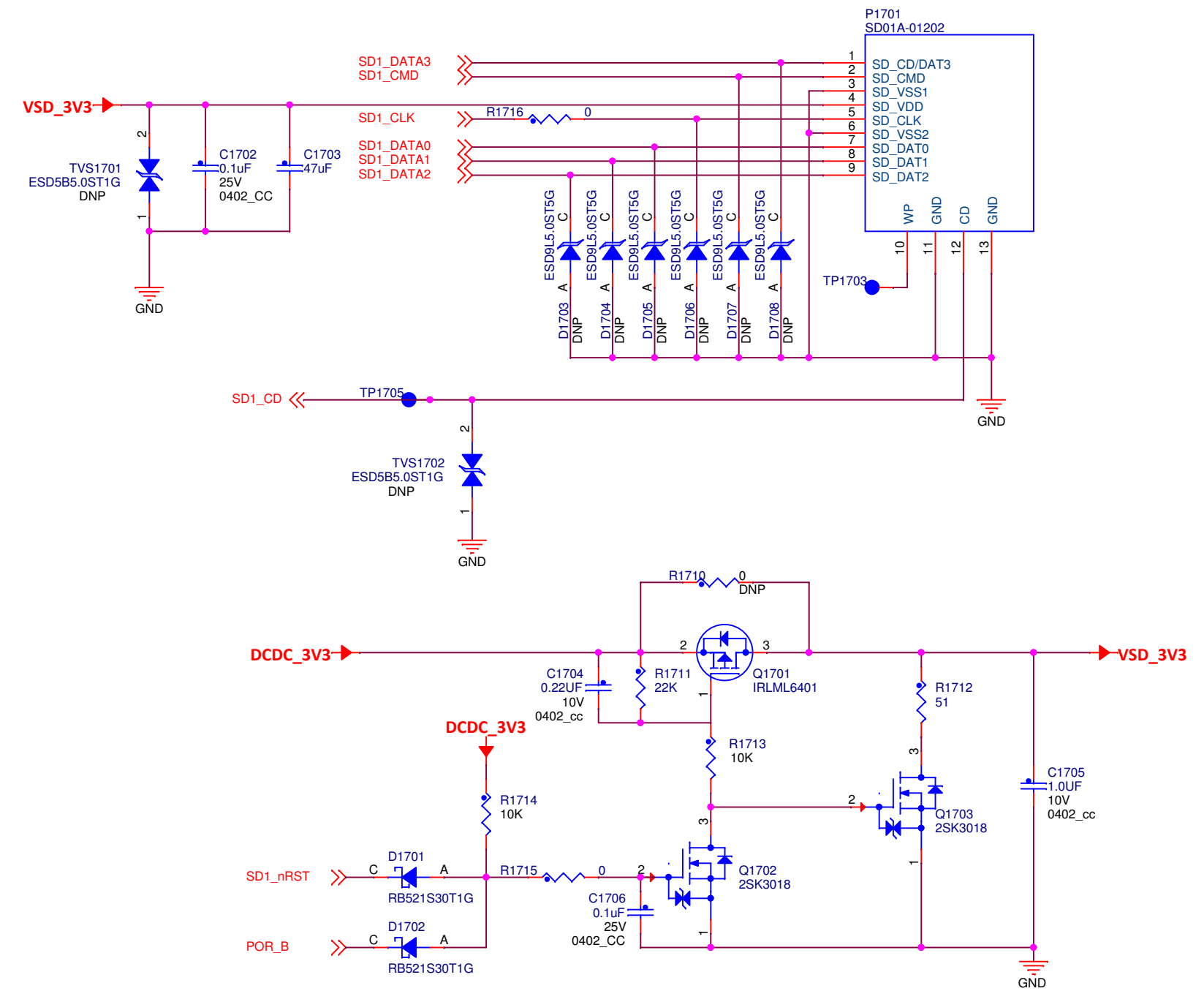


## ARDUINO\_HEADERS



## SD SLOT

# for WiFi and SD Accessories



ICAP Classification:	CP:	IUO:	X	PUBI:
Drawing Title: <b>MCIMX6UL-BB</b>				
Page Title: <b>BT/SD</b>				
Size C	Document Number	SCH-28616 PDF: SPF-28616	Rev C2	
Date:	Tuesday, October 18, 2016	Sheet	12	of 18

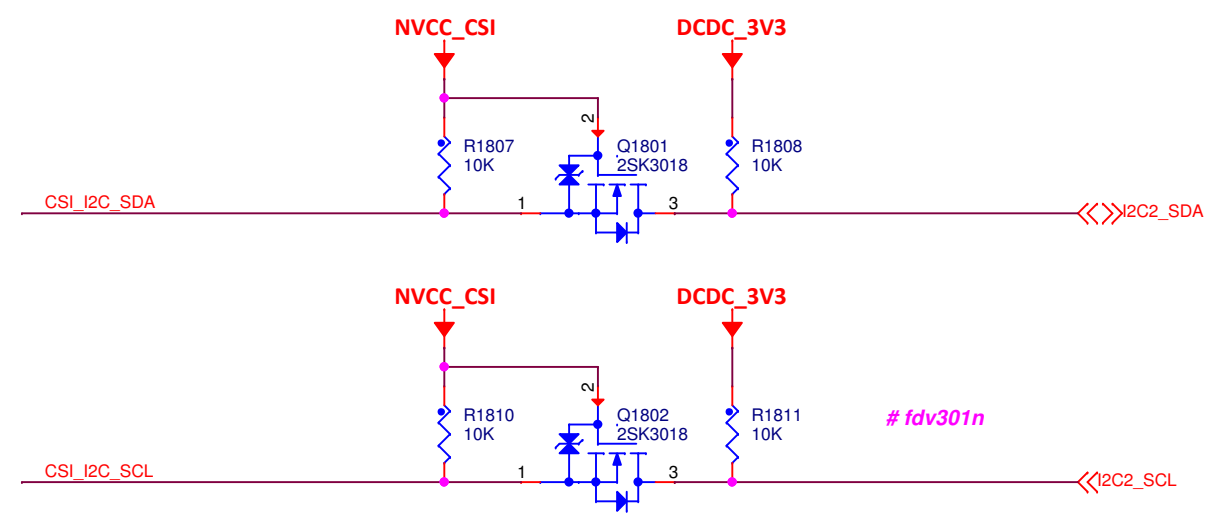
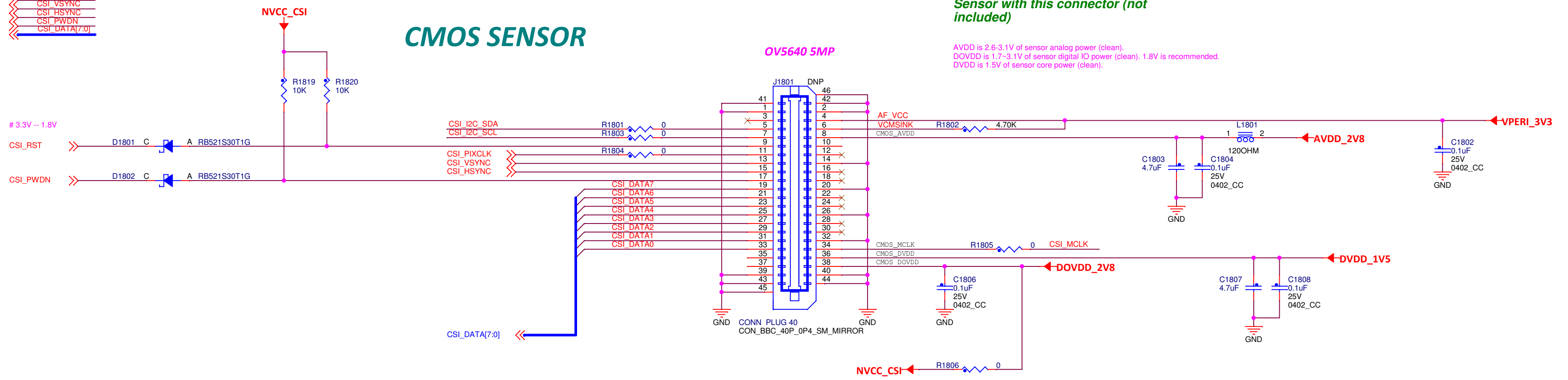
# Camera / SIM

- I2C2\_SDA
- I2C2\_SCL
- CSI\_RST
- CSI\_MCLK
- CSI\_PIXCLK
- CSI\_VSYNC
- CSI\_HSYNC
- CSI\_PWDN
- CSI\_DATA[7:0]

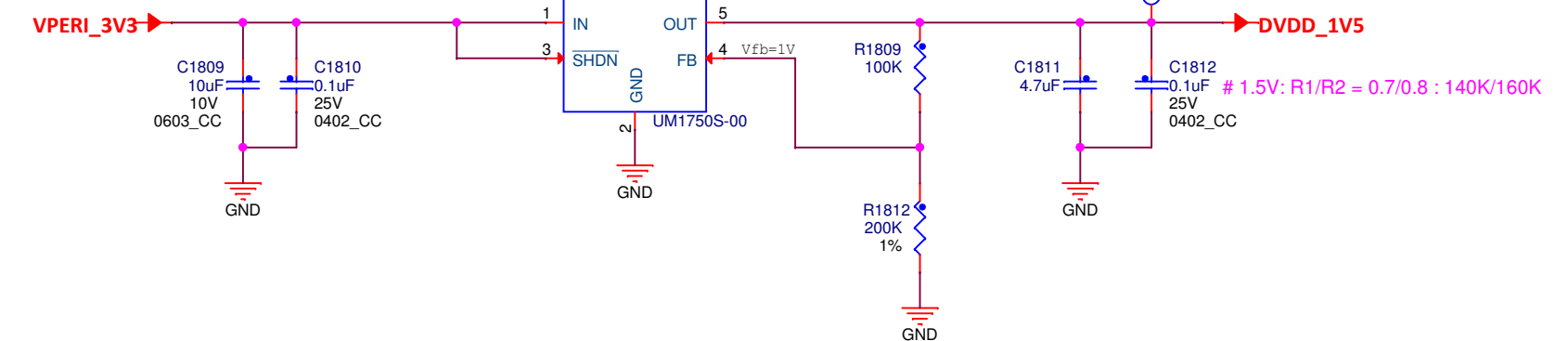
## CMOS SENSOR

Use Omnivision OV5640/5642 5M Pixel Sensor with this connector (not included)

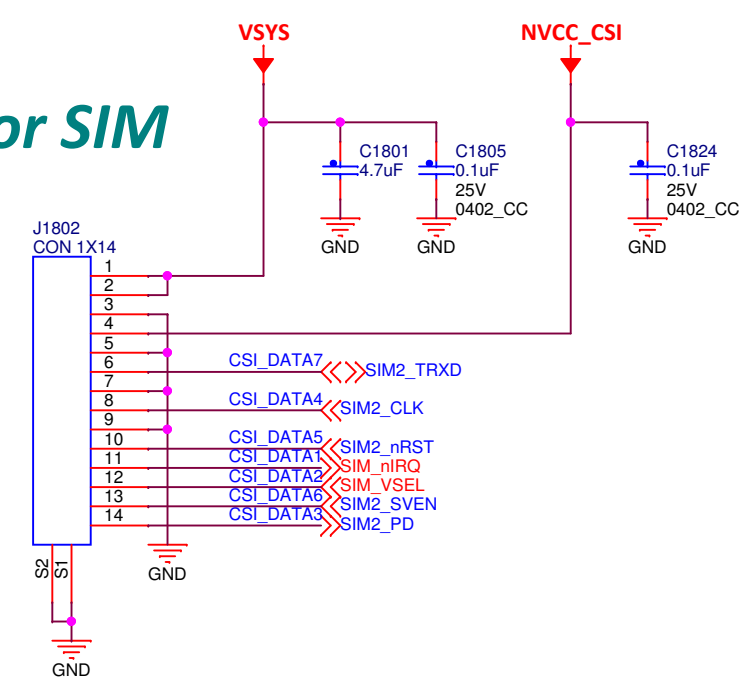
AVDD is 2.6-3.1V of sensor analog power (clean).  
 DOVDD is 1.7-3.1V of sensor digital IO power (clean). 1.8V is recommended.  
 DVDD is 1.5V of sensor core power (clean).



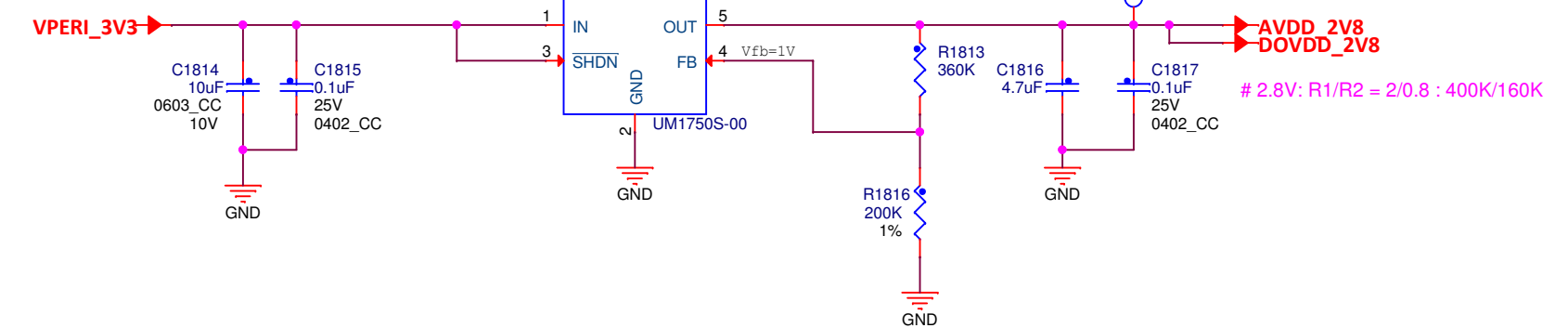
## 1.5V PWR



## RSV for SIM



## 2.8V PWR



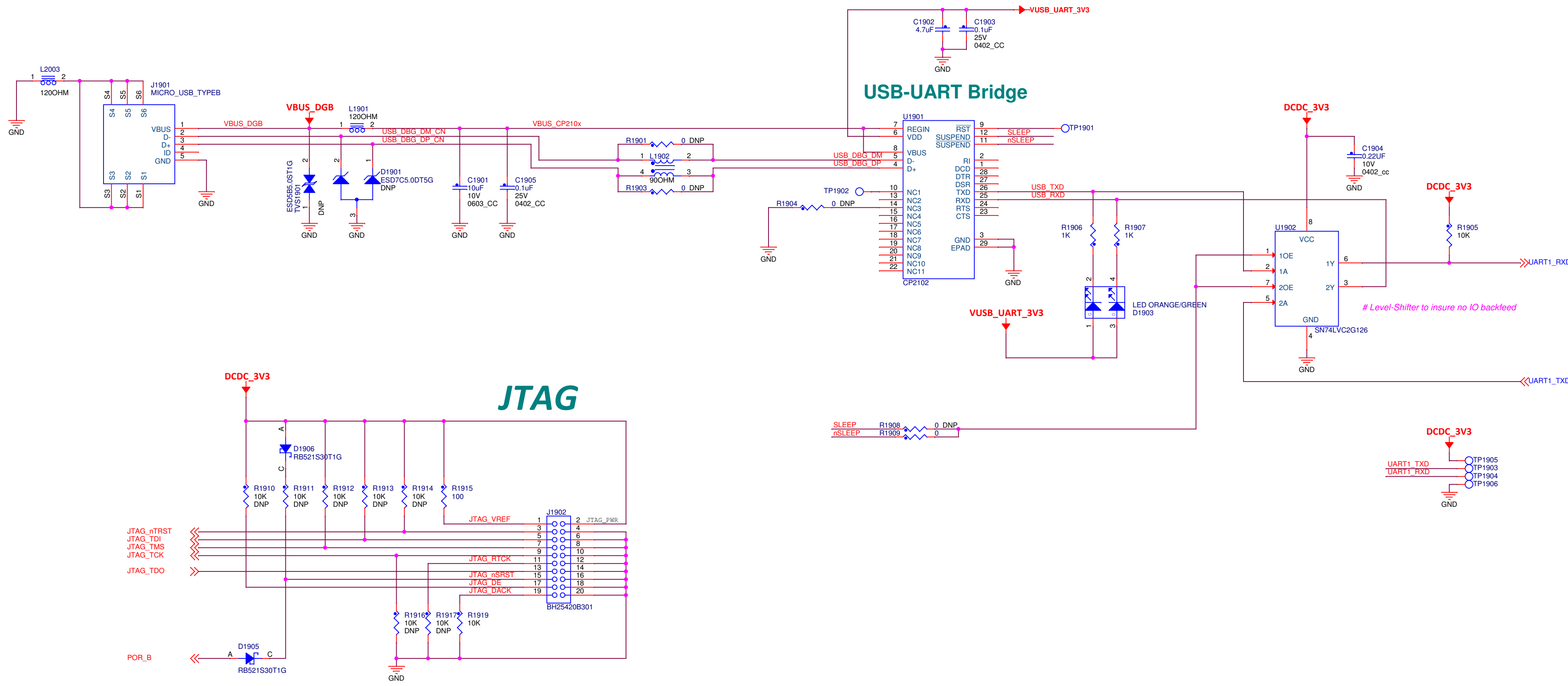
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Drawing Title: <b>MCIMX6UL-BB</b>	
Page Title: <b>CAMERA/EMV SIM</b>	
Size C	Document Number SCH-28616 PDF: SPF-28616
Date: Tuesday, October 18, 2016	Rev C2



# UART-USB DBG / JTAG

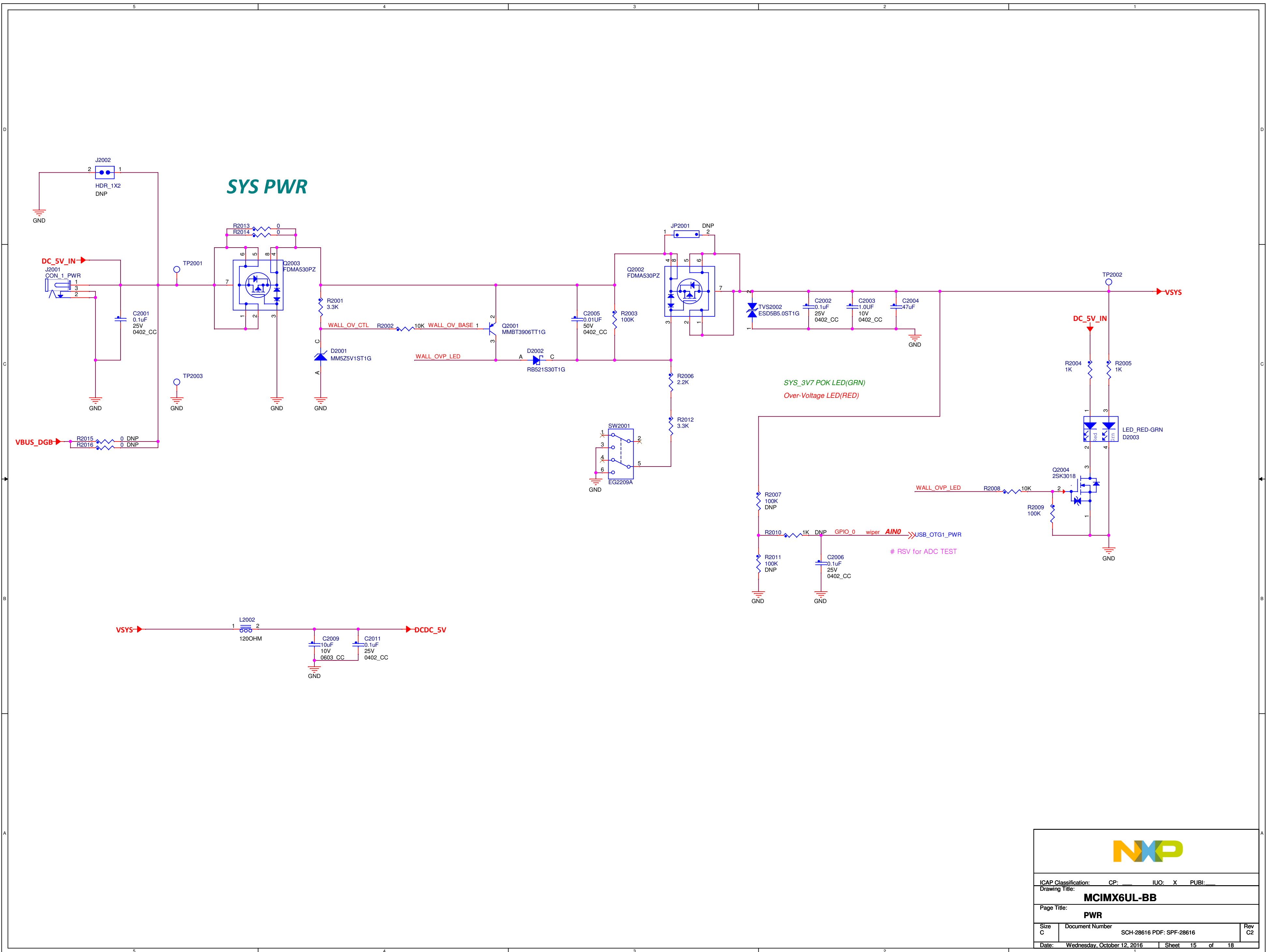
JTAG\_nTRST <<< JTAG\_nTRST  
 JTAG\_TDO <<< JTAG\_TDO  
 JTAG\_TDI <<< JTAG\_TDI  
 JTAG\_TMS <<< JTAG\_TMS  
 JTAG\_TCK <<< JTAG\_TCK  
 POR\_B <<< POR\_B

UART1\_RXD <<< UART1\_RXD  
 UART1\_TXD <<< UART1\_TXD



ICAP Classification:	CP:	IUO: X	PUBI:
Drawing Title: <b>MCIMX6UL-BB</b>			
Page Title: <b>DEBUG/JTAG</b>			
Size C	Document Number	SCH-28616 PDF: SPF-28616	Rev C2
Date:	Wednesday, October 19, 2016	Sheet 14	of 18



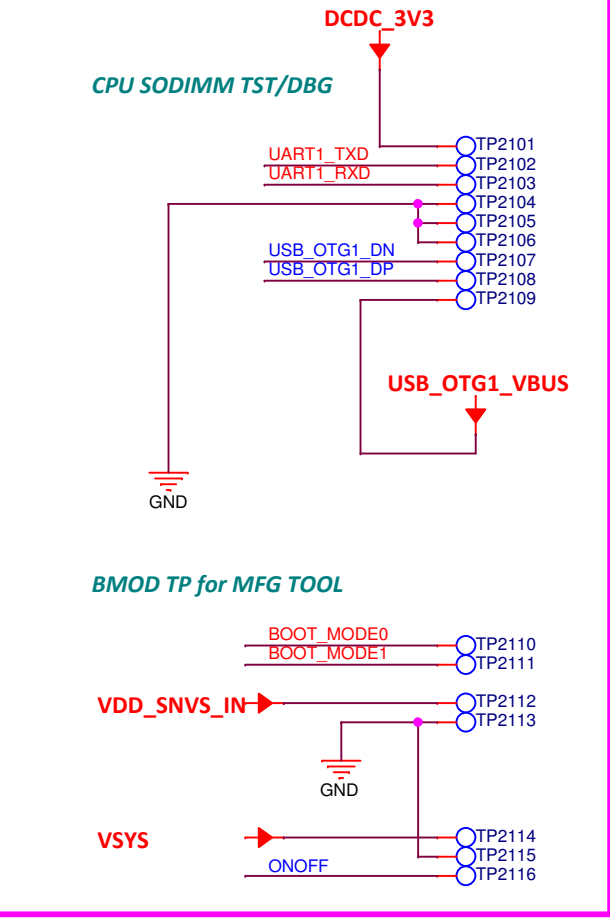


**SYS PWR**

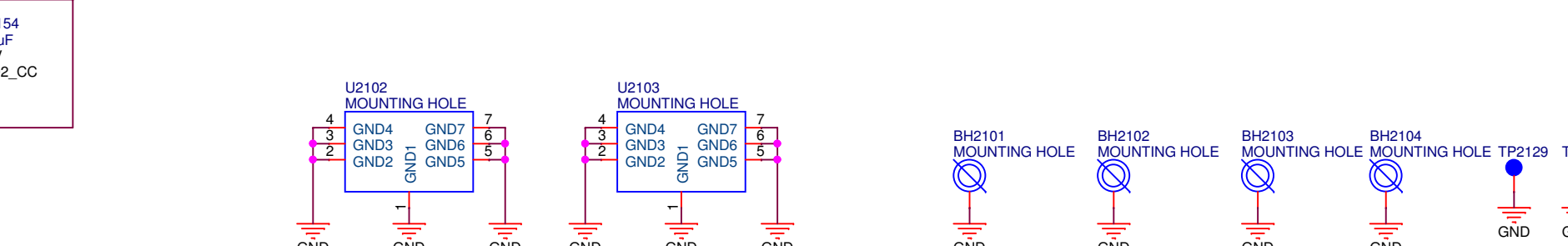
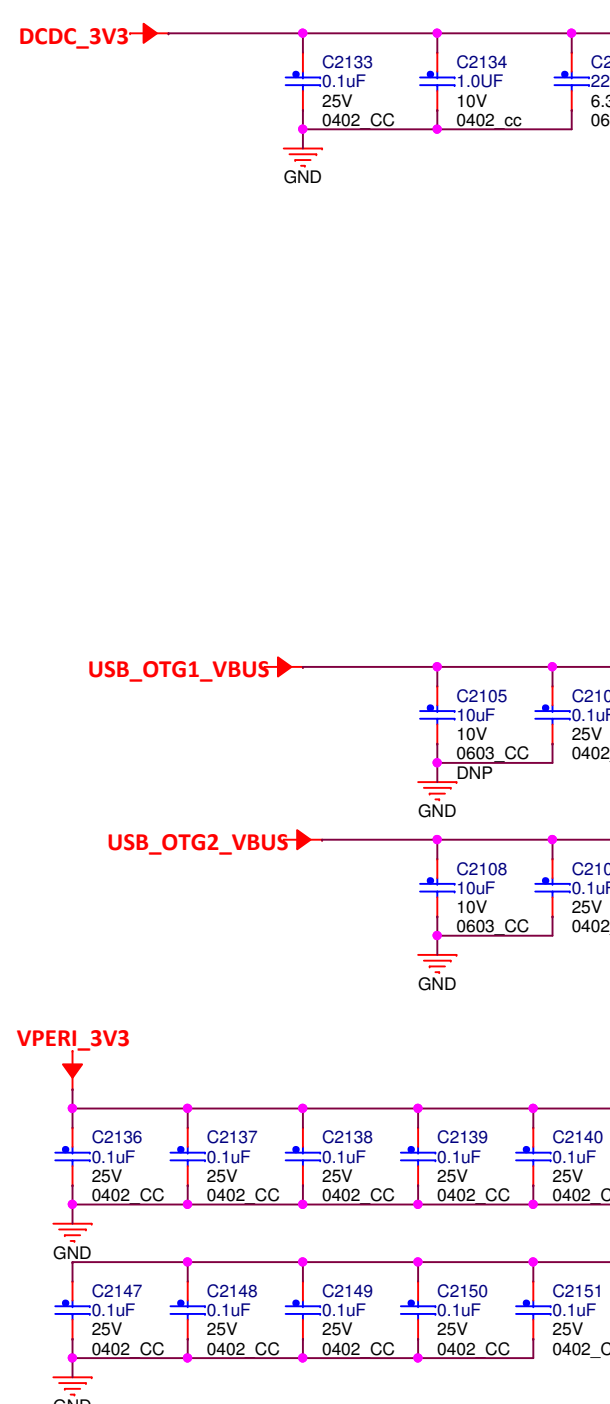
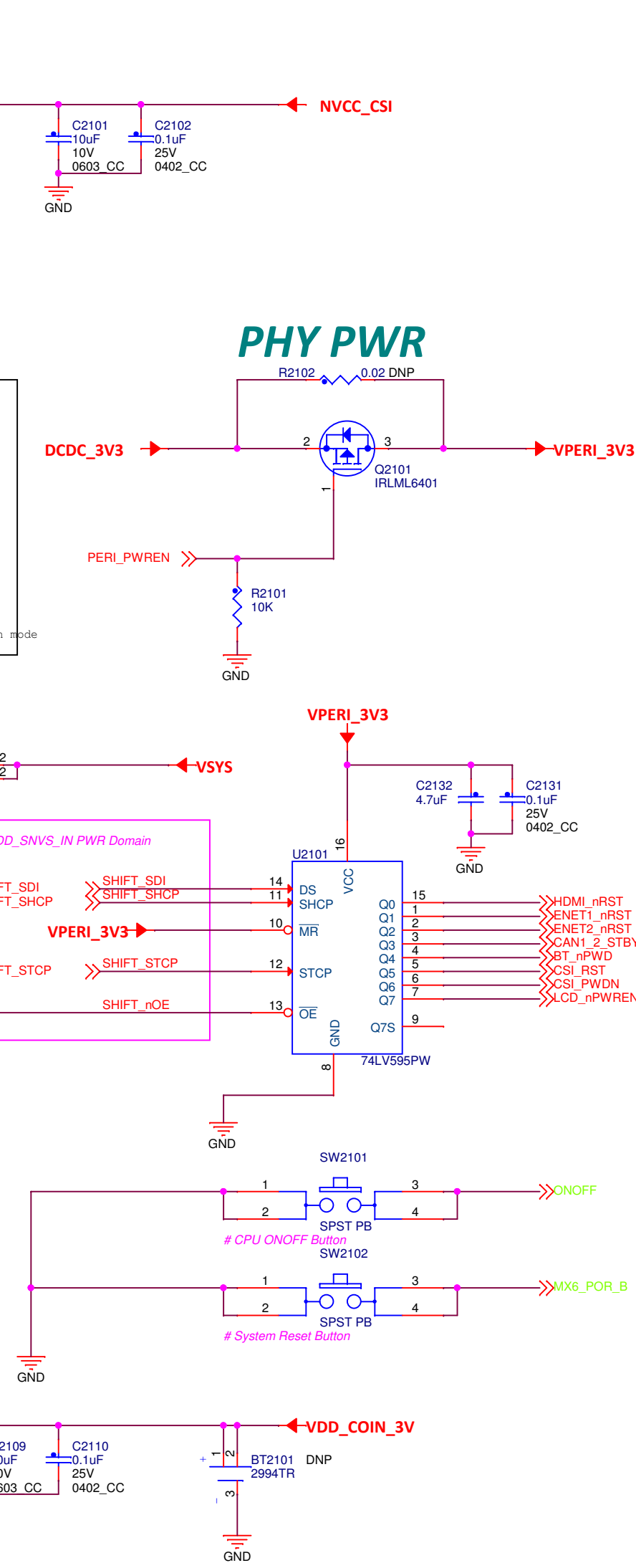
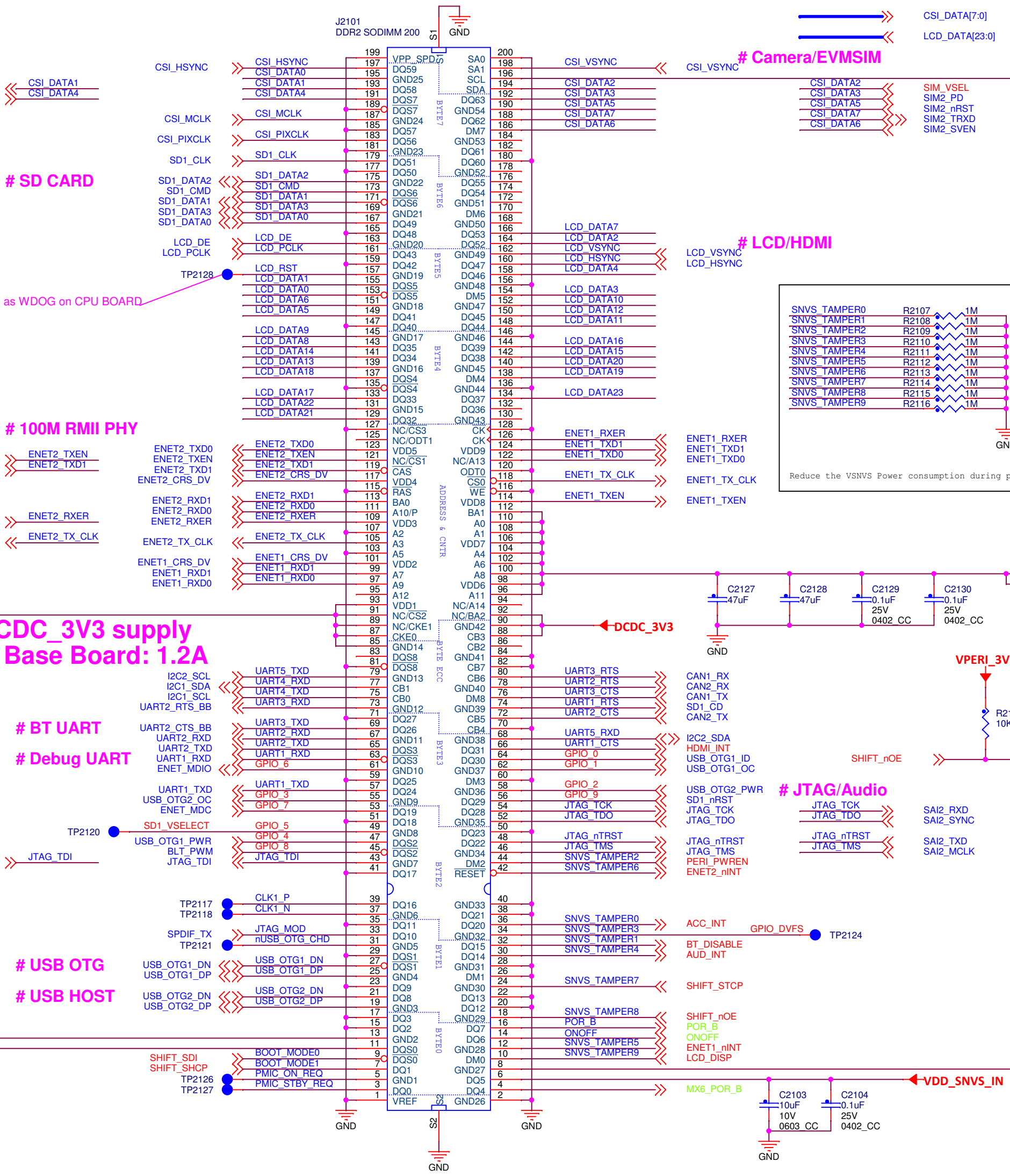
SYS\_3V7 POK LED(GRN)  
Over-Voltage LED(RED)

ICAP Classification:	CP:	IUO: X	PUBI:
Drawing Title: <b>MCIMX6UL-BB</b>			
Page Title: <b>PWR</b>			
Size C	Document Number	SCH-28616 PDF: SPF-28616	Rev C2
Date:	Wednesday, October 12, 2016	Sheet 15	of 18

### TP for SODIMM MFG



# SODIMM 200



**NXP**

ICAP Classification: CP: I UO: X PUBI:  
 Drawing Title: **MCIMX6UL-BB**  
 Page Title: **BASE-SODIMM200**  
 Size C Document Number SCH-28616 PDF: SPF-28616 Rev C2  
 Date: Tuesday, October 18, 2016 Sheet 16 of 18

**NOTE:** EMV SIM will be placed on the daughter board

All pins using ~reset as harden :

PAD	Default State	Simulation Value
UART3_TX_DATA	Output Buffer(LOW) during reset --> Output keeper + Input enable after reset done	0 in real silicon
LCD_DATA00~LCD_DATA23	100K pull down + input enable during reset --> Output keeper + Input enable after reset done ( this is boot option, we don't need change)	0 in real silicon

PAD	Default State	Signal Path	PAD Simulation Value
UART3_TX_DATA	Output Buffer(LOW) during reset --> Output keeper + Input enable after reset done	sjc.ipt_jta_active --> PAD	0 in real silicon
		(note : sjc.ipt_jta_active also connected to snvs_hp.sec_vio_in_1. This is security related, we don't plan to change it.)	ALT7

All pins using ~src.en\_system\_clk as harden :

PAD	Default State	Simulation Value
GPIO1_IO03	100K pull down + input enable during reset --> Output keeper + Input enable after reset done	0 in real silicon

PAD	Default State	Signal Path	PAD Simulation Value
GPIO1_IO03	100K pull down + input enable during reset --> Output keeper + Input enable after reset done	PAD --> ccmsrcmix.src_tester_ack	0 in real silicon
		This is the requirement of TE test	ALT7

All pins using snvs\_hp.snvs\_sec\_vio\_in\_5\_en as harden :

PAD	Default State	Simulation Value
CSI_PIXCLK	Output keeper + Input enable (snvs_sec_vio_in_5_en is 1'b0 in normal state, so harden is not triggerd in normal state). snvs_sec_vio_in_5_en is controlled by SNVS register. It can be disable or enable.	X (0 or 1 in real silicon )



