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Design of Phase Shifted Full-Bridge Converter with Current Doubler Rectifier

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1 Introduction

While the front-end stage of an AC/DC rectifier achieves power factor correction and regulates the bus voltage to a dc value (~390V), the dc-dc stage must step down the bus voltage and provide a galvanically isolated and tightly regulated dc output (eg. 12V, 24V, 48V). This document is intended to discuss the topology and operation of the dc-dc stage for medium to high power applications (>400W), and provide detailed design equations with examples.

A wide range of isolated topologies are available for the dc-dc stage, but the choice depends primarily on power level, complexity and cost. Ideally it is desired to select the topology with the least cost and complexity, nevertheless, one that can handle the power level with reliable and acceptable performance.

Figure 1.1 shows a chart for topology selection, it must be noted that topologies in this chart are not necessarily limited to the indicated power ranges, the intention of the chart is only to illustrate topologies power handling and their common application, relatively.

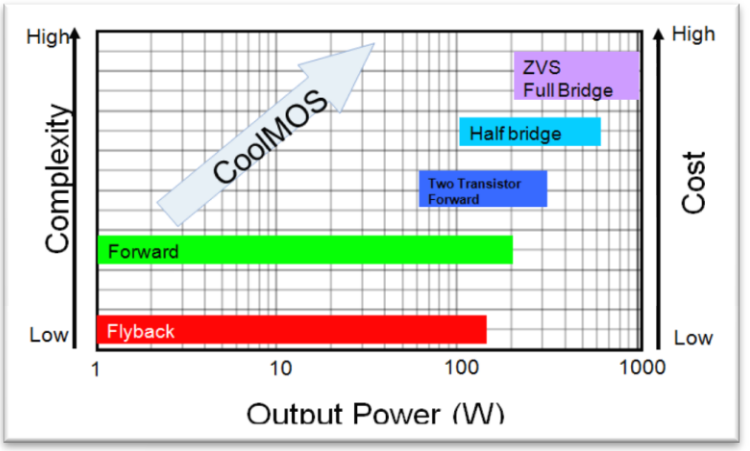

Figure 1.1

2 Full-Bridge Converter with Current Doubler Rectifier

According to specifications in Table 1 and the chart above, 600W could be realized with either a half-bridge or full-bridge. 600W falls in the high end of the half-bridge power handling range, while a full-bridge can handle that power with less stress and better performance. A full-bridge has half the rms current compared to a half-bridge, also, it can be implemented with phase shift control which provides Zero Voltage Switching (ZVS) for primary side switches.

Since the output is 12V and 50A, current double rectifier with synchronous rectification (Figure 2.1) is the most suitable for such high current application, as it splits the output current between two filter inductors, which reduces conduction losses, improves thermal distribution, and allows for lower profile, in addition to the ripple cancellation effect on the output capacitance.

Table 1 Specifications

Input voltage	390 V
Output voltage	12 V
Maximum power	600 W
Switching frequency	200 kHz
Inductor current ripple	20%
Output capacitor voltage ripple	12 mV_{p-p}

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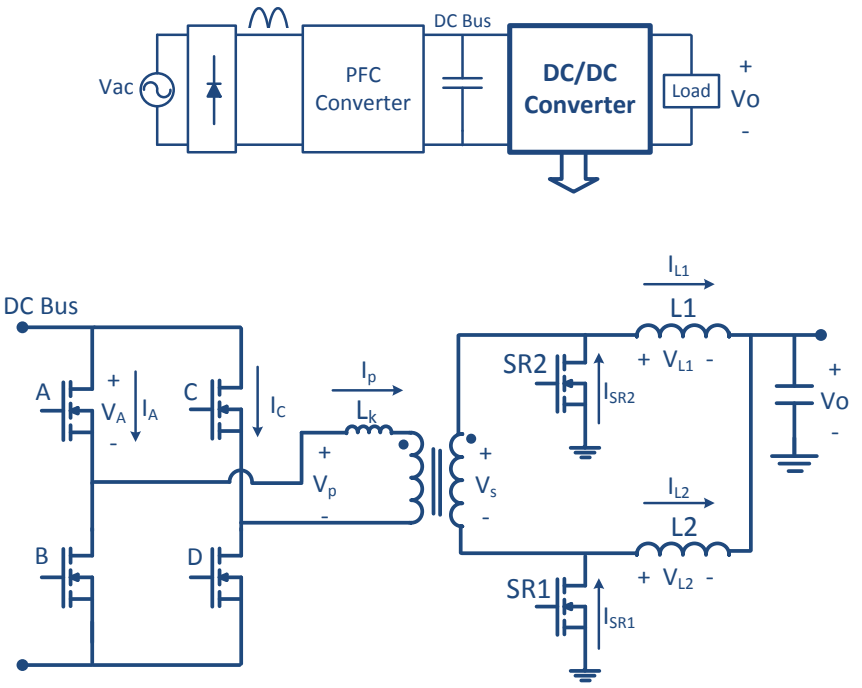

Figure 2.1

3 Modes of Operation

Figure 3.1 shows the equivalent circuit of each mode and key waveforms, switches A and B are switched complimentary with 50% duty cycle minus a short dead time, switches C and D are also switched complimentary with 50% duty cycle minus a short dead time, phase shift control between the two switches pairs A,B and C,D is used for output voltage regulation.

Mode 1: (t_0-t_1)

Duty Cycle Loss Mode

At $t=t_0$, switch A is turned on with ZVS (as a consequence of Mode 10 below), transformer secondary voltage V_s will remain zero and both secondary side rectifiers SR1 and SR2 will remain conducting current eventhough that SR2 is gated off, both inductors L_1 and L_2 are discharging, secondary voltage V_s remain zero until the primary current I_p reverses its direction and rise to reach the reflected output inductor current $I_{L1}*N_s/N_p$ at $t=t_1$. I_p rises with a slope as the input voltage V_{in} charges the leakage inductor L_k, and SR2 current slopes down to reach zero at $t=t_1$. No power is delivered to the output in this mode.

Mode 2: (t_1-t_2)

Power Delivery Mode

At $t=t_1$, the transformer secondary voltage V_s is equal to $V_{in}*N_s/N_p$, the output inductor L_1 is charging, the output inductor L_2 is discharging, SR1 carries both inductors current. The effective phase shift Ph_{eff} starts in this mode. The primary winding current I_p is equal to the reflected output inductor current $I_{L1}*N_s/N_p$.

Mode 3: (t_2-t_3)

Switch C ZVS Mode

At $t=t_2$, switch D is turned off, the primary current I_p charges the capacitance of switch D and discharges the capacitance of switch C. when switch C is discharged to zero, its body diode conducts to achieve zero voltage switching condition, the transformer secondary voltage V_s becomes zero and both SR's carry current.

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Mode 4: (t_3-t_4)

Freewheeling Mode

At $t=t_3$, switch C is turned on with ZVS, current I_p freewheels through switches A and C, the transformer secondary voltage V_s is zero, inductor L_1 discharges by the output voltage through SR2, and inductor L_2 discharges through SR1.

Mode 5: (t_4-t_5)

Switch B ZVS Mode

At $t=t_4$, switch A is turned off, the primary current charges the capacitance of switch A and discharges the capacitance of switch B. when switch B is discharged to zero, its body diode conducts to achieve zero voltage switching condition, the transformer secondary voltage V_s remains zero and both SR's keeps conducting.

Mode 6: (t_5-t_6)

Duty Cycle Loss Mode

At $t=t_5$, switch B is turned on with ZVS, transformer secondary voltage V_s will remain zero and both secondary side rectifiers SR1 and SR2 will remain conducting current eventhough that SR1 is gated off, Bothe inductors L_1 and L_2 are discharging. secondary voltage V_s remain zero until the current I_p reverses its direction and rise (in the negative direction) to reach the reflected output inductor current $I_{L2}*N_s/N_p$ at $t=t_6$. I_p changes with a slope as the input voltage V_{in} discharges the leakage inductor L_k, and SR1 current slopes down to reach zero at $t=t_6$. No power is delivered to the output in this mode.

Mode 7: (t_6-t_7)

Power Delivery Mode

At $t=t_6$, the transformer secondary voltage V_s is equal to $V_{in}*N_s/N_p$, the output inductor L_2 is charging, the output inductor L_1 is discharging, SR2 carries both inductors current. The effective phase shift *Pheff* starts again in this mode. The primary current I_p (in the negative direction) is equal to the reflected output inductor current $I_{L2}*N_s/N_p$.

Mode 8: (t_7-t_8)

Switch D ZVS Mode

At $t=t_7$, switch C is turned off, the primary current I_p charges the capacitance of switch C and discharges the capacitance of switch D. when switch D is discharged to zero, its body diode conducts to achieve zero voltage switching condition, the transformer secondary voltage V_s becomes zero and both SR's carry current.

Mode 9: (t_8-t_9)

Freewheeling Mode

At $t=t_8$, switch D is turned on with ZVS, current I_p freewheels through switches B and D, the transformer secondary voltage V_s is zero, inductor L_1 discharges by the output voltage through SR2, and inductor L_2 discharges through SR1.

Mode 10: (t_9-t_{10})

Switch A ZVS Mode

At $t=t_9$, switch B is turned off, the primary current I_p charges the capacitance of switch B and discharges the capacitance of switch A. when switch A is discharged to zero, its body diode conducts to achieve zero voltage switching condition, the transformer secondary voltage V_s remains zero and both SR's keeps carrying current.

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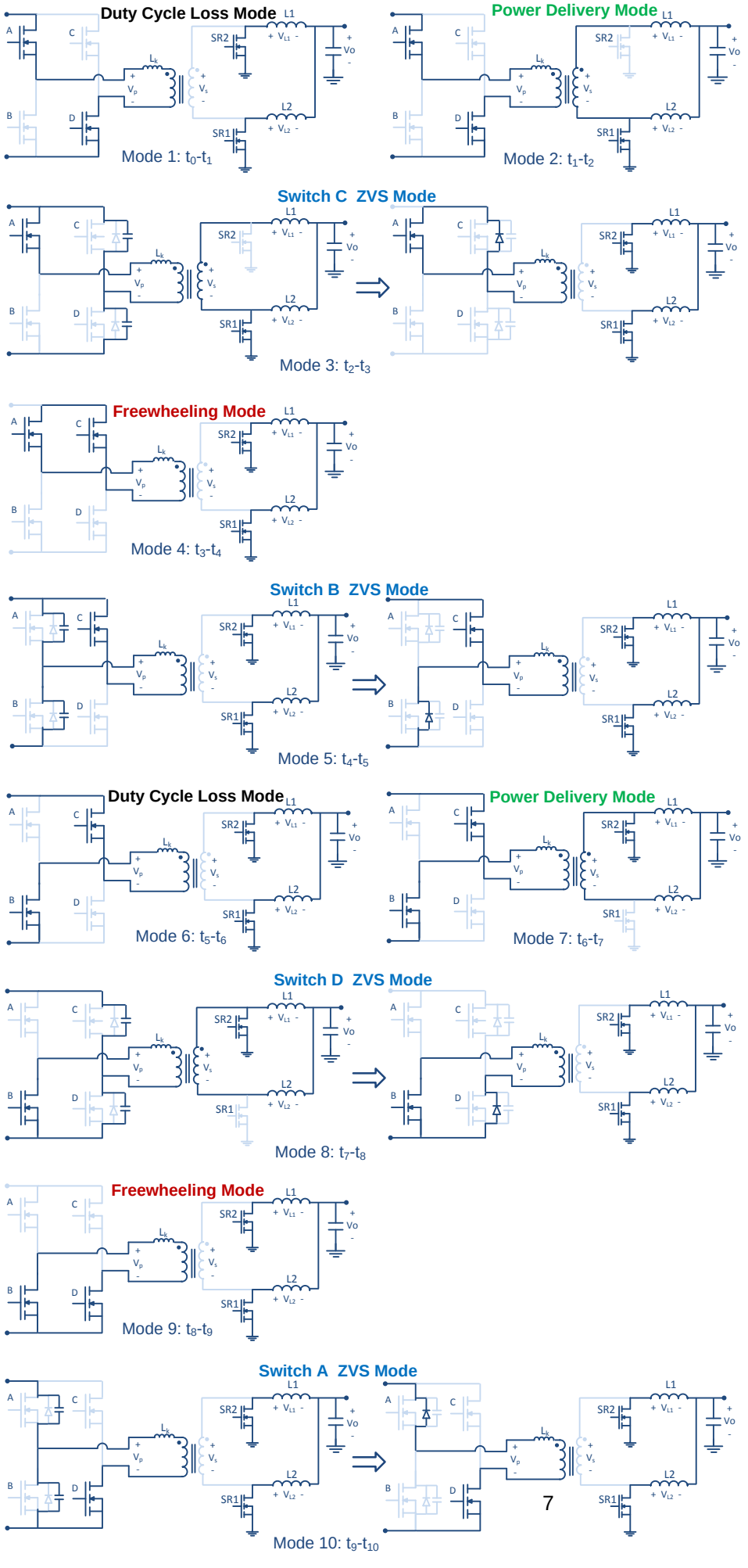

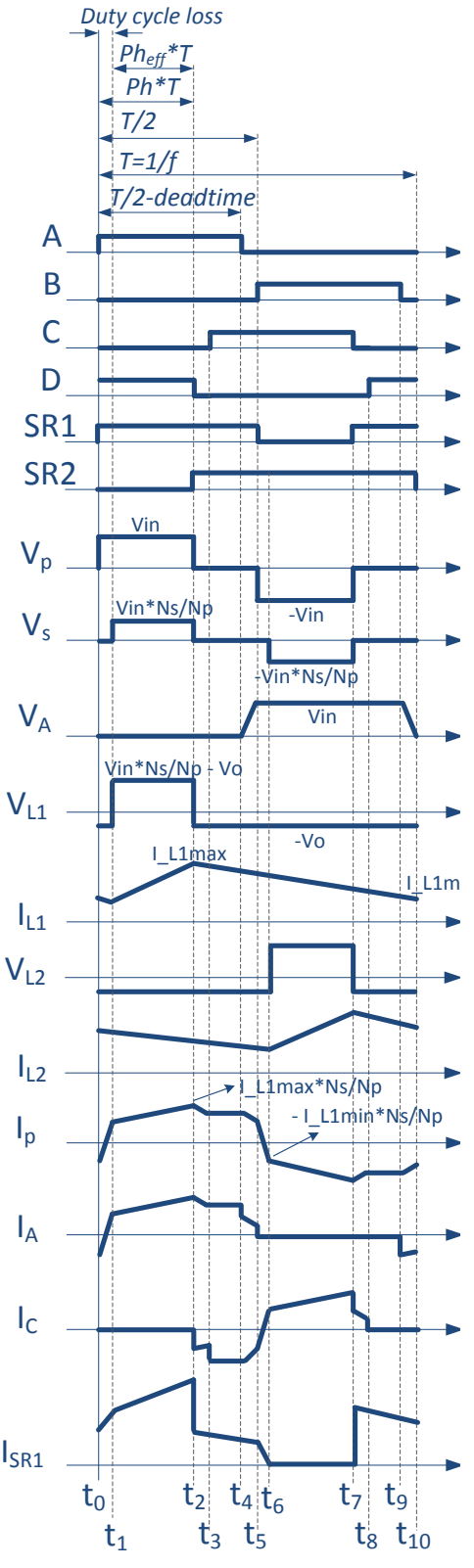

Figure 3.1

Design of Phase Shifted Full-Bridge Converter with Current Doubler Rectifier

4 Energy and Deadtime Conditions for Acheiving ZVS

Although Figure 3.1 shows ZVS turn on for all primary side switches, ZVS may be lost partially or completely due to lack of energy or insufficient deadtime.

During no load and light load conditions, ZVS may be lost if the inductive energy available in the circuit is not sufficient to charge and discharge the output capacitance of the two FETs in the same bridge leg in addition to the transformer capacitance.

The Energy condition for achieving ZVS is:

$$Inductive\ Energy\ E_L \geq Capacitive\ Energy\ E_C$$

The total capacitive energy in the switching leg and transformer is:

$$E_C = 0.5 \cdot (2 \cdot C_{\mathrm{oss(er)}} + C_{\mathrm{XFMR}}) \cdot {V_{in}}^2$$

Where C_{XFMR} is the transformer capacitance, and $C_{\mathrm{oss(er)}}$ is the MOSFET's equivalent energy related output capacitance as list in the datasheet, below is an example from the IPW65R310CFD datasheet to show the $C_{\mathrm{oss(er)}}$ parameter and its definition.

Effective output capacitance, energy related[1)]	$C_{o(er)}$		44		pF	V_{GS} = 0V, V_{DS} = 0 ... 400V

[1)] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

The inductive energy available for ZVS for switches C and D is higher than that for switches A and B. For that reason, switches C and D have a wider ZVS range compared to switches A and B.

In regards to ZVS for both switches C and D, it can be seen in the equivalent circuits of modes 3 and 8 (Figure 3.1) that leakage inductor, magnetizing inductor and reflected inductor all contribute to the ZVS available energy, therefore, the total inductive energy available for ZVS for switches C and D is:

$$E_L = 0.5 \cdot L_M \cdot {I_{M,pk}}^2 + 0.5 \cdot L_1 \cdot \left(\frac{N_p}{N_s}\right)^2 \cdot \left(I_{L1,max} \cdot \frac{N_s}{N_p}\right)^2 + 0.5 \cdot L_k \cdot \left(I_{M,pk} + I_{L1,max} \cdot \frac{N_s}{N_p}\right)^2$$

Where L_M is the magnetizing inductor and $I_{M,pk}$ is its peak current.

However, in regards to ZVS for both switches A and B, it can be seen in the equivalent circuits of modes 5 and 10 (Figure 3.1) that the transformer is clamped to zero voltage, and both output inductors currents freewheels in the SRs, hence the leakage inductor is the only inductive energy source available for ZVS, therefore, the total inductive energy available for ZVS for both switches A and B is:

$$E_L = 0.5 \cdot L_k \cdot \left(I_{M,pk} + I_{L1,min} \cdot \frac{N_s}{N_p}\right)^2$$

Since the magnetizing energy is not a function of the load current, the designer could slightly gap the transformer core, in order to tune the magnetizing energy such that ZVS range of is extended at light loads conditions. Another design practice used to extend the ZVS range is to add an external leakage inductor in series with the transformer primary, which adds to the leakage energy.

Besides having sufficient energy for achieving ZVS, the deadtime must also be enough to make the voltage transition, which is dependent on the resonant circuit parameters. Figure 4.1 shows a simple illustration of the ZVS transition during deadtime, it is seent that the voltage (Vds) transitions to zero in a resonant manner with a resonant frequency equal to f_r, therefore the V_{ds} requires at least one forth of the resonant period ($T_r/4$) to complete the transition. Deadtime below $T_r/4$ will cause switching at a non-zero voltage (partial ZVS), on the other hand, deadtime higher than $T_r/4$ will cause extra body diode conduction losses, furthermore, might cause losing ZVS if the resonant circuit is highly damped (or lossy).

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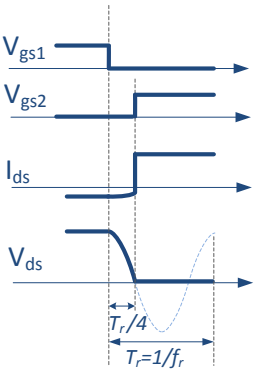

Figure 4.1

Figure 4.2 shows the circuit for the ZVS mode of switch C (Mode 3) and its equivalent resonant circuit, the equivalent resonant circuit is similar for all other ZVS transition modes (modes 5,8,10), and their resonant frequency (f_r) can be calculated as:

$$f_r = \frac{1}{2 \cdot \pi \sqrt{L_k \cdot (2 \cdot C_{\mathrm{oss(tr)}} + C_{\mathrm{XFMR}})}}$$

Notice that $C_{\mathrm{oss(tr)}}$is used for time calculation purposes, $C_{\mathrm{oss(tr)}}$ is the MOSFET's equivalent time related output capacitance as list in the datasheet, below is an example from the IPW65R310CFD datasheet to show the $C_{\mathrm{oss(tr)}}$ parameter and its definition.

Effective output capacitance, time related[2)]	$C_{o(tr)}$		204		pF	I_D = constant, V_{GS} = 0V, V_{DS} = 0 ... 400V

[2)] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

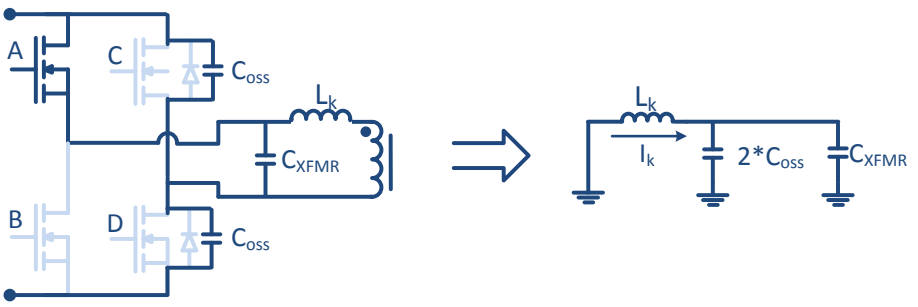

Figure 4.2

The time condition for achieving ZVS is:

$$Deadtime\ (T_D) \geq One\ fouth\ the\ resonant\ period\ (T_r/4)$$

$$Deadtime\ (T_D) \geq \frac{\pi}{2}\sqrt{L_k \cdot (2 \cdot C_{\mathrm{oss(tr)}} + C_{\mathrm{XFMR}})}$$

If we consider both energy and time ZVS design equations discussed above, we can see that increasing the leakage inductance can increase the energy available for ZVS, thus extending the ZVS load range, but on the other hand it has a side effect of decreasing the resonant frequency during voltage transition, thus increased deadtime is required, which is not desired in high switching frequency applications. For that reason, it is logical to reduce the capacitive energy in the circuit rather than increasing the inductive energy, this implies the necessity of low MOSFET's output capacitcance for this converter and for other ZVS topologies in general.

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5 Design Equations and Power Losses

The following are design equations for the full-bridge converter with current doubler, also a design example is integrated to further clarify the usage of all equations.

Since rms currents are calculated for the purpose of estimating power losses, we can neglect the waveforms details shown in Figure 3.1 such in duty cycle loss modes and ZVS modes, and only consider the power delivery modes and freewheeling modes. Also since it's a CCM operation with a low inductor current ripple (<50%) we may neglect the current ripple effect on all rms values.

Transformer

Turns ratio of the transformer is designed such that the output voltage regulation is maintained during minimum input voltage (during the holdup time of the preceding PFC stage), and at full load condition. The duty cycle loss is a term used to describe the time deducted each half switching cycle to reverse current polarity in the primary side and commute the current between the secondary side rectifiers, as shown in Figure 3.1, which reduces the period available for power delivery, therefore, duty cycle loss must be considered when calculation the turns ratio, otherwise the converter might loose regulation at heavy load conditions especially at cases of higher leakage inductance values.

Voltage gain is shown in the equation below,

$$\frac{V_o}{V_{in}} = \underbrace{\frac{N_s}{N_\mathrm{p}} \cdot ph}_{} - \underbrace{I_o \cdot \left(\frac{N_s}{N_\mathrm{p}}\right)^2 \cdot \frac{L_\mathrm{k}}{V_\mathrm{in}} \cdot f}_{}$$

Ideal voltage gain − duty cycle loss effect

If we assume leakage inductance Lk= 10 µH, and maximum phase shift ph= 0.4 at minimum input voltage, then,

$$\frac{12}{350} = \frac{N_s}{N_\mathrm{p}} \cdot 0.4 - 50 \cdot \left(\frac{N_s}{N_\mathrm{p}}\right)^2 \cdot \frac{10 \cdot 10^{-6}}{350} \cdot 150 \cdot 10^3$$

$$\rightarrow \frac{N_s}{N_\mathrm{p}} = 0.09 \rightarrow \frac{N_\mathrm{p}}{N_\mathrm{s}} = 11.1 \text{ choose } 11$$

For rms currents, power losses calculation and component selections, We may only consider effective phase shift ph_{eff} (neglect duty cycle loss), as:

$$ph_{eff} = \frac{V_o}{V_{in}} \frac{N_p}{N_\mathrm{s}}$$

$$= \frac{12}{390} \cdot 11 = 0.338$$

Selection of transformer size and shape mainly considers its efficiency and temperature rise, some transformer design experience along with few iterations are requires to reach an optimized core selection and balanced core and winding losses. For our design example, we chose core E41/17/12-3C90.

For acceptable core losses, we limit the maximum magnetic flux to 0.1 Tesla, consequently we can calculate the number of primary turns.

$$N_p = \frac{V_{in} \cdot ph_{eff}}{2 \cdot B_{max} \cdot A_c \cdot f}$$

$$= \frac{390 \cdot 0.338}{2 \cdot 0.1 \cdot 149 \cdot 10^{-6} \cdot 150 \cdot 10^3} = 29.53 \rightarrow \text{choose } 33 \text{ turns}$$

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$$\rightarrow N_s = \frac{33}{11} = 3 \text{ turns}$$

$$B_{max} = \frac{V_{in} \cdot ph_{eff}}{2 \cdot N_p \cdot A_c \cdot f}$$
$$= \frac{390 \cdot 0.338}{2 \cdot 33 \cdot 149 \cdot 10^{-6} \cdot 150 \cdot 10^3} = 0.089 \text{ Tesla}$$

For cores with 3C90 or R material, the following equation can be used to calculate core losses,

$$P_{\text{core}} = 0.036 \cdot \left(\frac{f}{10^3}\right)^{1.64} \cdot (10 \cdot B_{max})^{2.68} \cdot V_e \cdot 10^3$$
$$= 0.036 \cdot \left(\frac{150 \cdot 10^3}{10^3}\right)^{1.64} \cdot (10 \cdot 0.094)^{2.68} \cdot 11500 \cdot 10^{-9} \cdot 10^3 = 1.139 \text{ W}$$

$$I_{pri.rms} = \frac{I_o}{2} \cdot \frac{N_s}{N_p}$$
$$= \frac{50}{2} \cdot \frac{3}{33} = 2.273\ A$$
$$P_{pri.cond} = {I_{pri.rms}}^2 \cdot R_{pri}$$
$$= 2.273^2 \cdot R_{pri} = 5.17 \cdot R_{pri}\ \ Watt$$

$$I_{sec.rms} = \frac{I_o}{2} \cdot \sqrt{2 \cdot ph_{eff}}$$
$$= \frac{50}{2} \cdot \sqrt{2 \cdot 0.338} = 20.55\ A$$
$$P_{sec.cond} = {I_{sec.rms}}^2 \cdot R_{sec}$$
$$= 20.55^{\,2} \cdot R_{sec} = 422.3 \cdot R_{sec}\ \ Watt$$

Filter Inductor

Inductor current ripple

$$\Delta I_{L1} = \Delta I_{L2} = \%Ripple \cdot \frac{I_o}{2}$$
$$= 20\% \cdot \frac{50}{2} = 5\ A$$

Filter inductors values L_1 and L_2 and their peak currents are determined based on the specified inductor current ripple.

$$L_1 = L_2 = \frac{1}{\Delta I_{L1}} \cdot V_o \left(1 - ph_{eff}\right) \cdot T$$
$$= \frac{1}{5} \cdot 12(1 - 0.338) \cdot \frac{1}{150 \cdot 10^3} = 10.6\ \mu\text{H}$$

$$I_{L.pk} = \frac{I_o}{2} + \frac{\Delta I_{L1}}{2}$$

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$$= \frac{50}{2} + \frac{5}{2} = 27.5\ A$$

→ Inductor saturation current must all be rated at > 27.5A .

The inductor rms current and conduction loss are:

$$I_{L.rms} = \frac{I_o}{2}$$
$$= \frac{50}{2} = 25\ A$$
$$P_{L.cond} = {I_{L.rms}}^2 \cdot DCR$$
$$= 25^{\,2} \cdot DCR = 625 \cdot DCR \quad Watt$$

Primary MOSFET

In order to select the optimum MOSFET, one must understand the MOSFET requirements in a full-bridge converter. High voltage MOSFETS have several families based on different technologies, which each target a specific application, topology or operation. For a ZVS converter such as the full-bridge, the following are some major MOSFET selection considerations:

- Low FOMs - R_{on}*$Q_{g.}$
- Fast Turn-off switching, higher gate plateau voltage.
- Low output capacitance C_{oss} for extended ZVS range and short deadtime designs.
- VDS rating to handle spikes/overshoots.
- Low thermal resistance $R_{thJC.}$
- Package selection must consider the resulting total thermal resistance from junction to ambient.
- Robust body diode with fast reverse recovery. Although that in normal operation the body diode current/charge are softly commuted, in some conditions such as startup, load transient, light load or low leakage inductance, body diode may have hard commutation, it may not have a channel conduction following its own conduction, or channel conduction might be too short and not enough to completely sweep out the reverse recovery charge, in such case, as the MOSFET turns off with a high dv/dt while there are still residual charge in the body diode region, the charge leaving the body diode P-region may bias the parasitic npn BJT, causing false turn on and destruction of the MOSFET.

CFD2 CoolMOS™ series are recommended for ZVS applications in general, and for full-bridge converter in specific. The low reverse recovery charge Q_{rr} (illustrated in Figure 5.1), time t_{rr} and current I_{rrm} of the CFD series brings a higher margin in repetitive hard commutation of the body diode, which increases the system reliability.

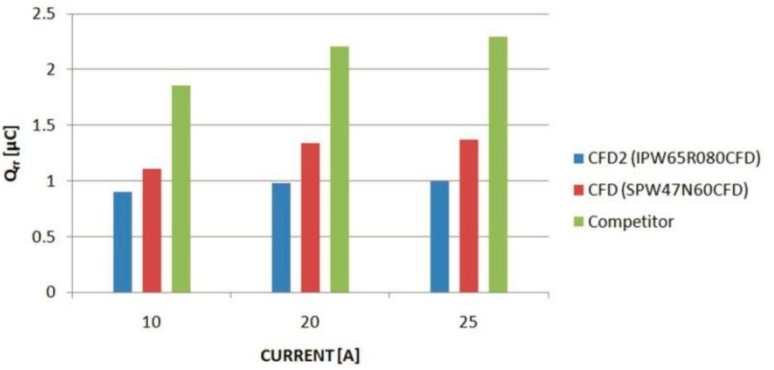

Figure 5.1

Design of Phase Shifted Full-Bridge Converter with Current Doubler Rectifier

According to the aforementioned MOSFET selection criteria and to the specification listed in Table 1, MOSFET **IPW65R310CFD** is selected, and its parameters will be used for the following calculations.

The MOSFET rms current can be calculated by the following equation, consequently the MOSFET conduction loss is obtained.

$$I_{S.rms} = \frac{I_o}{2} \cdot \frac{N_s}{N_p} \sqrt{\frac{1}{2}}$$
$$= \frac{50}{2} \cdot \frac{3}{33} \sqrt{\frac{1}{2}} = 1.607\ A$$

$$P_{S.cond} = {I_{S.rms}}^2 \cdot R_{on.pri(100℃)}$$
$$= 1.607^2 \cdot 0.5 = 1.29\ W$$

Since it's a ZVS converter, turn-on loss and output capacitance Coss switching loss are zero.

Turn-off time and loss are:

$$t_{off} = Q_{gd} \cdot \frac{R_g}{V_{pl}} + Q_{gs} \cdot \frac{V_{pl} - V_{th}}{V_{pl}} \cdot \frac{2 \cdot R_g}{V_{pl} + V_{th}}$$
$$= 22 \cdot 10^{-9} \cdot \frac{3}{6.4} + 7 \cdot 10^{-9} \cdot \frac{6.4 - 4}{6.4} \cdot \frac{2 \cdot 3}{6.4 + 4} = 11.83 \cdot 10^{-9}\ s$$

$$P_{S.off} = 0.5 \cdot I_{L.pk} \cdot \frac{N_s}{N_p} \cdot V_{in} \cdot t_{off} \cdot f$$
$$= 0.5 \cdot 27.5 \cdot \frac{3}{33} \cdot 390 \cdot 11.83 \cdot 10^{-9} \cdot 150 \cdot 10^3 = 0.865\ \mathrm{W}$$

Gate drive loss

$$P_{S.gate} = V_g \cdot Q_g \cdot f$$
$$= 12 \cdot 41 \cdot 10^{-9} \cdot 150 \cdot 10^3 = 0.074\ \mathrm{W}$$

$$\therefore \text{MOSFET total loss} = 2.229\ \mathrm{W}$$

Synchronous Rectifier (SR) MOSFET

Voltage stress of SR MOSFET in a current doubler circuit is:

$$V_{SR,stress} = V_o\ /ph_{eff}$$
$$= 12\ /\ 0.338\ = 35.5\ V \quad \rightarrow$$ we choose 75V MOSFETs to allow for ringing and input voltage overshoots.

The SR rms current is:

$$I_{SR.rms} = I_o \sqrt{\frac{ph_{eff}}{2} + \frac{1}{4}}$$

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$$= 50\sqrt{\frac{0.338}{2}+\frac{1}{4}} = 32.37\ A$$

In order to choose the optimum MOSFET in synchronous rectification, the power loss mechanism needs to be well understood. SRs do not operate as active switches; hence they have no voltage-current overlap switching losses, causing switching losses to be relatively constant across the load range, which makes conduction losses dominant in the heavy load region. For that reason, SRs are required to have low Ron in order to have a balanced switching and conduction losses and optimal operation.

Another important portion of the total switching losses is related to the output capacitance C_{oss} and the reverse recovery charge Q_{rr} of the MOSFET. Considering the turn-off moment, the Q_{rr} has to be removed and the output capacitance has to be charged up to the secondary side transformer voltage. Due to the very short on-time of the body diode of about 50ns to 100ns, Q_{rr} losses can be neglected, leaving only gate charge loss and C_{oss} loss as switching losses.

Selection of the optimal SR MOSFET that provides balanced and optimized loss can be according to following formula:

$$R_{on.sec\_optimal} = \sqrt{\frac{\left(FOM_{Qg}\cdot V_g\cdot f + 0.5\cdot FOM_{Qoss}\cdot {V_o}/{ph_{eff}}\cdot f \right)}{I_{SR.rms}{}^2}}$$

Where,

$$FOM_{Qg} = R_{on}\cdot\ Q_g \quad FOM_{Qoss} = R_{on}\cdot\ Q_{oss}$$

If we optimize the operation at mid load point, and apply the formulas above to the 75V OptiMOS 3 technology, we find that:

$$FOM_{Qg} = 2.3\ m\Omega\cdot 155\ nC$$

$$FOM_{Qoss} = 2.3\ m\Omega\cdot 160\ nC$$

$$R_{on.sec\_optimal} = \sqrt{\left(2.3\ m\Omega\cdot 155\ nC\cdot 12\cdot 150\cdot 10^3\ +\ 0.5\cdot 2.3\ m\Omega\cdot 160\ nC\cdot\frac{12}{0.338}\cdot 150\cdot 10^3\right)/(32.37/2)^2}$$

$$R_{on.sec\_optimal} = 2.487\cdot 10^{-3}\ \Omega\ \rightarrow we\ choose\ \text{IPP023NE7N3 G}$$

Another way for choosing the optimal SR MOSFET is to use the tool shown in Figure 5.2. It is a diagram that is derived from the optimization equation above with applying the Optimos technology parameters and the SR operation condition. Note that there will be different diagram for each voltage rating, more details are included in the Infineon Technologies Application Note: “Optimum MOSFET Selection for Synchronous Rectification”, that is listed in the references.

The starting point on this diagram is to determine the transformer voltage (or the SR voltage stress), in our case 35.5V, then we move down to the device we intend use (IPP023NE7N3), then we move left to the switching frequency (150kHz), then we move up to the SR rms current curve, note that we like optimize the SR selection at mid load, hence 32.37A/2= 16.19A, since there isn’t a line for 16A, we may plot an approximated one between the 10A and the 20A lines, then we may move to the right to find the optimum Rds(on) value and further to determine how many parallel FETs are required in order to obtain the optimum Rds(on). For our example we conclude that a single IPP023NE7N3 MOSFET is enough.

Design of Phase Shifted Full-Bridge Converter with Current Doubler Rectifier

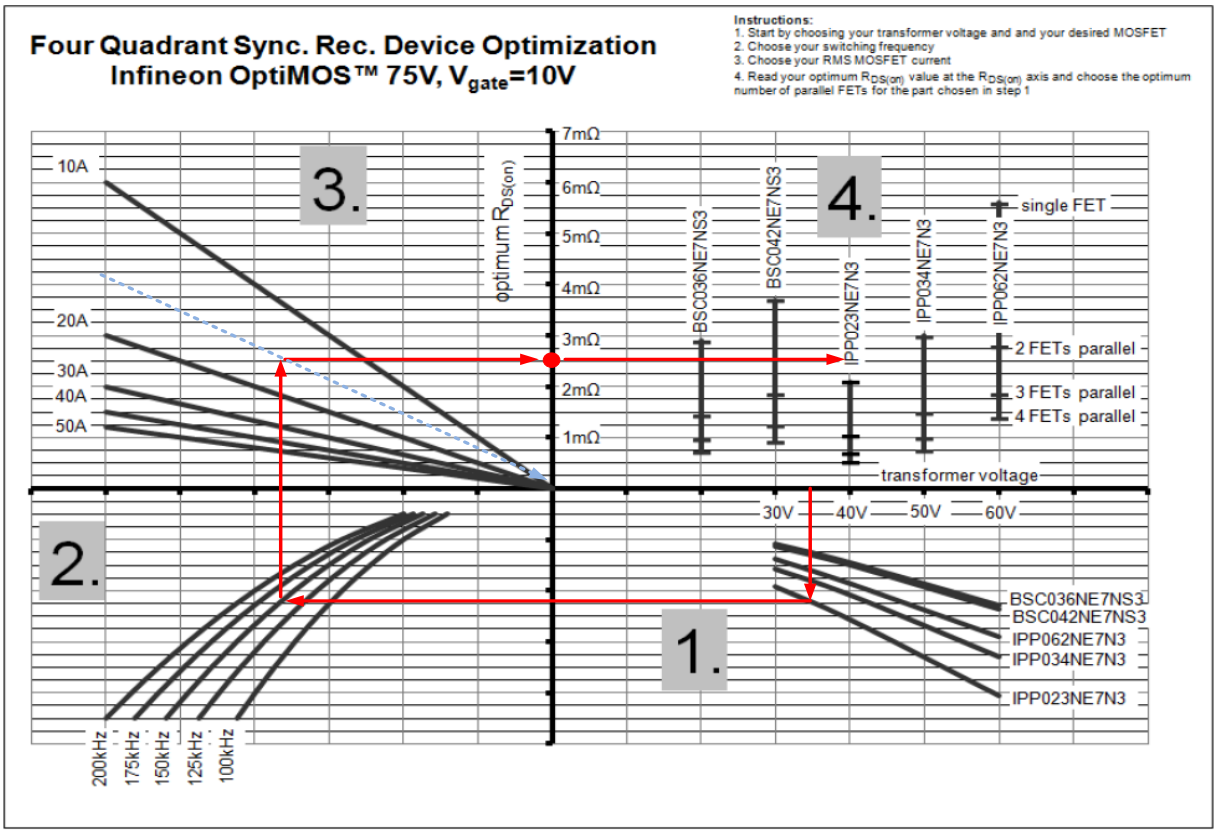

Figure 5.2

SR conduction loss

$$P_{SR.cond} = {I_{S.rms}}^2 \cdot R_{on.sec(100℃)}$$
$$= 32.37^2 \cdot 2.75 \cdot 10^{-3} = 2.88\,W$$

Output capacitance Coss switching loss

$$P_{SR.oss} = 0.5 \cdot Q_{oss} \cdot \frac{V_o}{ph_{eff}} \cdot f$$
$$= 0.5 \cdot 160 \cdot 10^{-9} \cdot \frac{12}{0.338} \cdot 150 \cdot 10^3 = 0.426\ \mathrm{W}$$

SR gate drive loss

$$P_{SR.gate} = V_g \cdot Q_g \cdot f$$
$$= 12 \cdot 155 \cdot 10^{-9} \cdot 150 \cdot 10^3 = 0.279\ \mathrm{W}$$

$\therefore$ SR MOSFET total loss $= 2.229\ \mathrm{W}$

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Output Capacitor

The output capacitor current ripple is a function othe phase shift, current doubler rectifier is able to fully cancel the current ripple in output capacitance in the case of Ph_{eff} = 0.5.

Output capacitor current ripple, rms current and ESR loss can be calculated by the following equations.

$$\Delta I_{Cout} = \frac{V_o}{L_1} \cdot T \cdot \left(1 - 2 \cdot ph_{eff}\right)$$

$$= \frac{12}{10.6 \cdot 10^{-6}} \cdot \frac{1}{150 \cdot 10^3} \cdot (1 - 2 \cdot 0.338) = 2.45 \text{ A}$$

$$I_{Cout.rms} = \sqrt{\frac{1}{12} \cdot \Delta I_{Cout}{}^2}$$

$$= \sqrt{\frac{1}{12} \cdot 2.45^2} = 0.705\ A$$

$$P_{Cout} = I_{Cout.rms}{}^2 \cdot ESR_{out}$$

$$= 0.705^2 \cdot ESR_{out} = 0.497 \cdot ESR_{out}\ \ W$$

Output capacitor voltage ripple

$$\Delta V_{Cout} = \frac{V_o \cdot \left(1 - 2 \cdot ph_{eff}\right) \cdot T^2}{16 \cdot L_1 \cdot C_{out}}$$

For 12mV capacitor voltage ripple as specified in Table 1, the capacitor value is calculate as:

$$C_{out} = \frac{V_o \cdot \left(1 - 2 \cdot ph_{eff}\right) \cdot T^2}{16 \cdot L_1 \cdot \Delta V_{Cout}}$$

$$= \frac{12 \cdot (1 - 2 \cdot 0.338)}{16 \cdot 10.6 \cdot 10^{-6} \cdot 12 \cdot 10^{-3}} \cdot \left(\frac{1}{150 \cdot 10^3}\right)^2 = 84.9 \text{ µF}$$

Input Capacitor

The input capacitor rms current can be calculated by the following equation, consequently the capacitor ESR loss is obtained.

$$I_{Cin.rms} = \sqrt{2 \cdot ph_{eff} \cdot \left(\frac{I_o}{2} \cdot \frac{N_s}{N_p} - \frac{P_o}{V_{in}}\right)^2 + 2 \cdot \left(0.5 - ph_{eff}\right)\left(\frac{P_o}{V_{in}}\right)^2}$$

$$= \sqrt{2 \cdot 0.338 \cdot \left(\frac{50}{2} \cdot \frac{3}{33} - \frac{600}{390}\right)^2 + 2 \cdot (0.5 - 0.338)\left(\frac{600}{390}\right)^2} = 1.063\ A$$

$$P_{Cin} = I_{Cin.rms}{}^2 \cdot ESR_{in}$$

$$= 1.063^2 \cdot ESR = 1.13 \cdot ESR_{in}\ \ W$$

Note that the above capacitor equations assume that the converter is supplies by a dc supply (input current is constant). If we consider the overall system architecture, we can see that the input capacitance is preceded and supplied by the PFC stage, hence the shared capacitance (bus capacitor) has two sources of ripple, the first is the switching frequency ripple caused by the interaction between the two stages, if the full bridge switching frequency is synchronized with the PFC stage, then this rms current can be minimized, this is possible as many control ICs offer the synchronization input to their internal oscillator. The second source of ripple is the 60 Hz ripple generated by the PFC stage. For better estimation of the rms current, especially in a non-synchronized application or if the PFC stage is a variable frequency operation, then simulation might be the best approach.

Design of Phase Shifted Full-Bridge Converter with Current Doubler Rectifier

Heat sink

Multiple MOSFETs can have separate heat sinks or share the same one; however, the selection of the heat sink is based on its required thermal resistivity.

In case of a separate heat sink for each MOSFET, thermal resistors are modeled as in Figure 5.3.

$$R_{thSA.FET1} = \frac{T_{J.FET1} - T_A}{P_{FET1}} - R_{thCS.FET1} - R_{thJC.FET1}$$

$$R_{thSA.FET2} = \frac{T_{J.FET2} - T_A}{P_{FET1}} - R_{thCS.FET2} - R_{thJC.FET2}$$

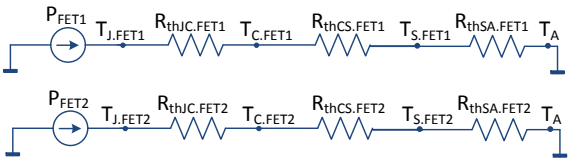

Figure 5.3

In case of a single heat sink for multiple MOSFETs, thermal resistors are modeled as in Figure 5.4.

The maximum heat sink temperature T_S allowed is the minimum outcome of the two equations below

$$T_S = T_{J.FET1} - P_{FET1} \cdot (R_{thCS.FET1} + R_{thJC.FET1})$$

$$T_S = T_{J.FET2} - P_{FET2} \cdot (R_{thCS.FET2} + R_{thJC.FET2})$$

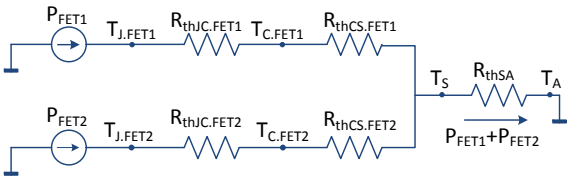

Figure 5.4

Once T_S is specified, then the heat sink thermal resistance can be calculated.

$$R_{thSA} = \frac{T_S - T_A}{P_{FET1} + P_{FET2}}$$

R_{thJC} is the thermal resistace from junction to case, this is specified in the MOSFET and Diode datasheets.

R_{thCS} is the thermal resistace from case to heatsink, typically low compared to the overall thermal resistance, its value depends on the the interface material, for example, thermal grease and thermal pad.

R_{thSA} is the thermal resistance from heatsink to ambient, this is specified in the heatsink datasheets, it depends on the heatsink size and design, and is a function of the surroundings, for example, a heatsink could have difference values for R_{thSA} for different airflow conditions.

T_S is the heatsink temperature, T_C is the case temperature , T_A is the ambient temperature.

P_{FET} is FET's total power loss.

Design of Phase Shifted Full-Bridge Converter with Current Doubler Rectifier

Table 2 shows two design examples for the CCM PFC boost converter, for different power levels and switching frequencies.

Table 2

	Design Example #1	**Design Example #2**
	600W 150kHz	**1000W 100kHz**
Transformer		
Core size/material	E41/17/12-3C90	E42/21/15-3C90
N_p	33	33
N_s	3	3
B_{max}	0.089 Tesla	0.112 Tesla
P_{core}	1.139 W	1.622 W
$I_{pri.rms}$	2.273 A	3.788 A
$P_{pri.cond}$	$5.17 \cdot R_{pri}$ W	$14.35 \cdot R_{pri}$ W
$I_{sec.rms}$	20.55 W	34.281 W
$P_{sec.cond}$	$422.3 \cdot R_{sec}$ W	$1175.19 \cdot R_{sec}$ W
Filter Inductor		
L	10.6 µH	9.53 µH
$I_{L.pk}$	27.5 A	45.833 A
$I_{L.rms}$	25 A	41.67 A
$P_{L.cond}$	$625 \cdot DCR$ W	$1736 \cdot DCR$ W
Primary MOSFET	**IPW65R310CFD**	**IPW65R190CFD**
$I_{S.rms}$	1.607 A	2.678 A
$P_{S.cond}$	1.29 W	2.152 W
t_{off}	$11.83 \cdot 10^{-9}$ s	$19.71 \cdot 10^{-9}$ s
$P_{S.off}$	0.865 W	1.602 W
$P_{S.gate}$	0.074 W	0.082 W
Synchronous Rectifier MOSFET	**IPP023NE7N3 G**	**2 x IPP023NE7N3 G**
$I_{SR.rms}$	32.37 A	53.957 A
$P_{SR.cond}$	2.88 W	4 W
$P_{SR.oss}$	0.426 W	0.567 W
$P_{SR.gate}$	0.279 W	0.372 W
Output Capacitor		
$I_{Cout.rms}$	0.705 A	1.175 A
P_{Cout}	$0.497 \cdot ESR_{out}$ W	$1.38 \cdot ESR_{out}$ W
Input Capacitor		
$I_{Cin.rms}$	1.063 A	1.771 A
P_{Cin}	$1.13 \cdot ESR_{in}$ W	$3.136 \cdot ESR_{in}$ W

Design of Phase Shifted Full-Bridge Converter with Current Doubler Rectifier

6 References

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Design of Phase Shifted Full-Bridge Converter with Current Doubler Rectifier

Symbols used in formulas

V_{in}: Input voltage
V_o: Output voltage
I_o: Output current
P_o: Output power
f: Switching frequency
T: Switching time period
Ph: Phase shift
Ph_{eff}: Effective phase shift
E_C: Capacitive energy
E_L: Inductive Energy
$I_{L1.max}$: Output inductor (L1) maximum current
$I_{L1.min}$: Output inductor (L1) minimum current
L_k: Leakage inductor
L_M: Magnetizing inductor
$I_{M.pk}$: Peak magnetizing current
N_p: Number of transformer's primary turns
N_s: Number of transformer's secondary turns
B_{max}: Peak magnetic flux
A_c: Core sectional area
P_{core}: Core loss
$I_{pri.rms}$: Transformer primary winding rms current
R_{pri}: Transformer primary winding resistance
$P_{pri.cond}$: Transformer primary winding conduction loss
$I_{sec.rms}$: Transformer secondary winding rms current
R_{sec}: Transformer secondary winding resistance
$P_{sec.cond}$: Transformer secondary winding conduction loss
$I_{L,pk}$: Peak output inductor current
%Ripple: Inductor current ripple percentage to input current
DCR: Inductor DC resistance
$I_{L,rms}$: Output inductor rms current
$P_{L.cond}$: Output inductor conduction loss
t_{off}: MOSFET switching off time
$R_{on.pri(100C)}$: Primary MOSFET on resistance at 100^oC
$I_{S,rms}$: Primary MOSFET rms current
$P_{S,cond}$: Primary MOSFET conduction loss
$P_{S.off}$: Primary MOSFET switching off power loss
$P_{S.gate}$: Primary MOSFET gate drive loss
$V_{SR,stress}$: SR MOSFET max voltage stress
$R_{on.sec(100C)}$: SR MOSFET on resistance at 100^oC
$I_{SR,rms}$: SR MOSFET rms current
$P_{SR,cond}$: SR MOSFET conduction loss
$P_{SR,gate}$: SR MOSFET gate drive loss
$P_{SR,oss}$: SR output capacitance loss
Q_{oss}: MOSFET output capacitance charge
Q_{gs}: MOSFET gate-source charge
Q_{gd}: MOSFET gate-drain charge
Q_g: MOSFET total gate charge
R_g: MOSFET gate resistance
V_{pl}: MOSFET gate plateau voltage
V_{th}: MOSFET gate threshold voltage
ESR: Capacitor resistance
$I_{Cin.rms}$: Input capacitor rms current
P_{Cin}: Input capacitor conduction loss