

Recommended External Circuitry for Transphorm GaN FETs

Table of Contents

Part I: Introduction.....	2
Part II: Solutions to Suppress Oscillation	2
Part III: The di/dt Limits of GaN Switching Devices & Solutions for High-current Operation.....	4
Part IV: Additional Design Notes	5

Application Note 0009

Part I: Introduction

Transphorm GaN FETs provide significant advantages over silicon (Si) superjunction MOSFETs by offering lower gate charge (Q_g), faster switching speeds, and lower body-diode reverse recovery charge (Q_{rr}). GaN FETs exhibit in-circuit switching speeds much higher than that of the current Si technologies. The inherent rapid switching of GaN devices reduces current/voltage cross-over power losses, enabling high frequency operation while simultaneously achieving high efficiency.

However, the accompanying high di/dt transient during switching, combined with parasitic inductances, generates noise voltages in the circuit. This noise can interfere with the gate and the driver of the device, and, in the worst case, creates sustained oscillation that must be prevented for safe operation of the circuit. This application note provides guidance on how to eliminate oscillation and how to achieve high switching current with a controlled di/dt .

Part II: Solutions to Suppress Oscillation

To avoid sustained oscillation, it is important to minimize noise generation, to minimize noise feedback, and to damp the ringing energy resulting from the high current/voltage transients. This can be achieved with the recommendations outlined below using a half-bridge switching circuit in Figure 1 as an example.

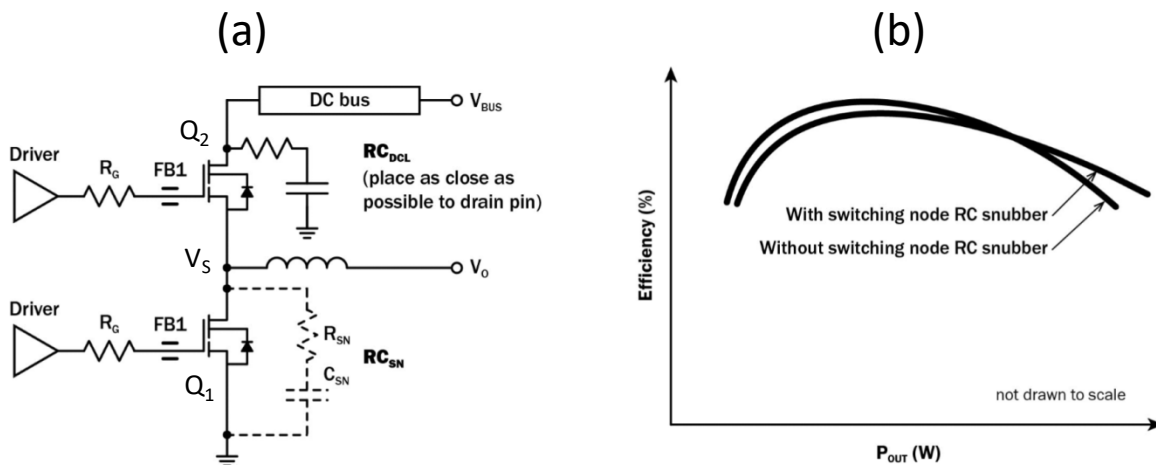


Figure 1. a) Half-bridge switching circuit and b) Efficiency vs. output power

1) Optimize the PCB layout to minimize external parasitic inductances and associated feedback. Use a large area ground plane for an overall low-noise base potential. Arrange the gate drive circuit on one side and the output circuit on the other side to minimize noise feedback from the output loop to the input loop. Place the driver circuit close to the gate of the device. Shorten the power loop by arranging the high-side and low-side devices close-by.

2) Use a gate ferrite bead [FB1 in Figure 1(a)] to prevent the high-frequency noise from entering the driver and logic circuits. This bead should be mounted close to the Gate lead of the device. NOTE: This is required even for single-ended non-half-bridge designs. The specification of the recommended gate ferrite beads are listed in Transphorm's GaN FET datasheets and also summarized in Table 2. The TO247 package includes a built-in gate ferrite bead therefore an external gate ferrite bead is not needed (see product datasheets).

Application Note 0009

3) Use a DC-link RC snubber [RC_{DCL} in Figure 1(a)]. The DC rail or DC-link, when decoupled with a low-ESR fast capacitor, can be considered a high-Q C-L network at high frequencies (with "L" being the feed inductance of the DC bus). This can interact with the devices at voltage/current transients and lead to ringing. Adding an RC snubber across the DC-link close to the drain pin of the high-side device can effectively absorb the ringing energy, suppressing potential oscillation. This effect is shown in **Figure 2** where the high-frequency ringing at 25A turn-off is substantially damped with the RC_{DCL} . Since this snubber is not inserted at the switching node, it does not add switching loss to the circuit. NOTE: This is recommended even for single-ended non-half-bridge designs. The practical values of the RC_{DCL} can be 2 sets of 6-10 Ω /0.5W SMD resistors in series with a 10nF/600-1000V ceramic SMD cap, or 1 set of 3-4 Ω /1W resistors in series with a 10-20nF/600-1000V cap if space is limited.

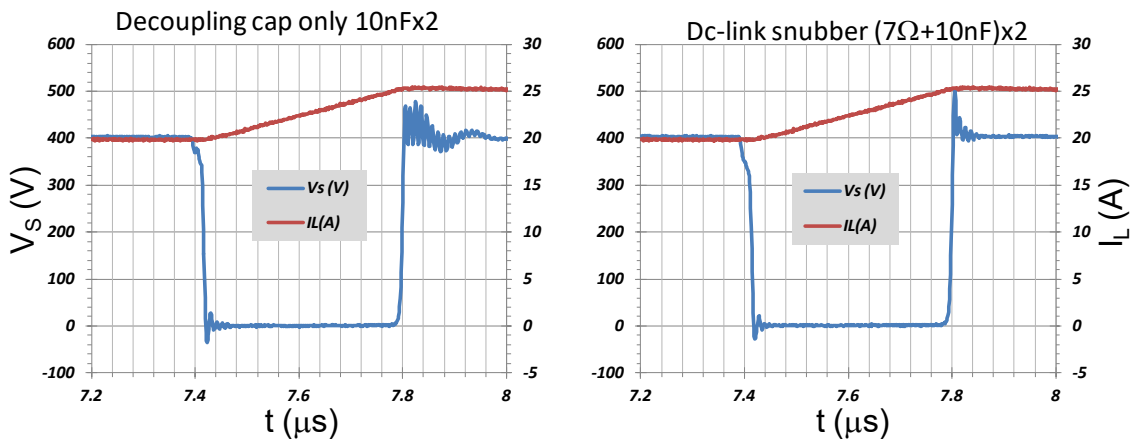


Figure 2. Half-bridge inductive switching waveforms with decoupling capacitor only and with DC-link snubber (RC_{DCL}) (Devices: TP65H050WS)

4) Adding a switching-node RC snubber [RC_{SN} in Figure 1(a)] can further reduce high-frequency ringing and help control di/dt transients at high operation currents. The effect of the RC_{SN} on switching waveform at a switching current >50A is shown in **Figure 3**. Unlike the RC_{DCL} , the capacitance of the RC_{SN} does increase switching loss. The recommended snubber parameters with little degradation in efficiency are given in the datasheet and are summarized in **Table 2**.

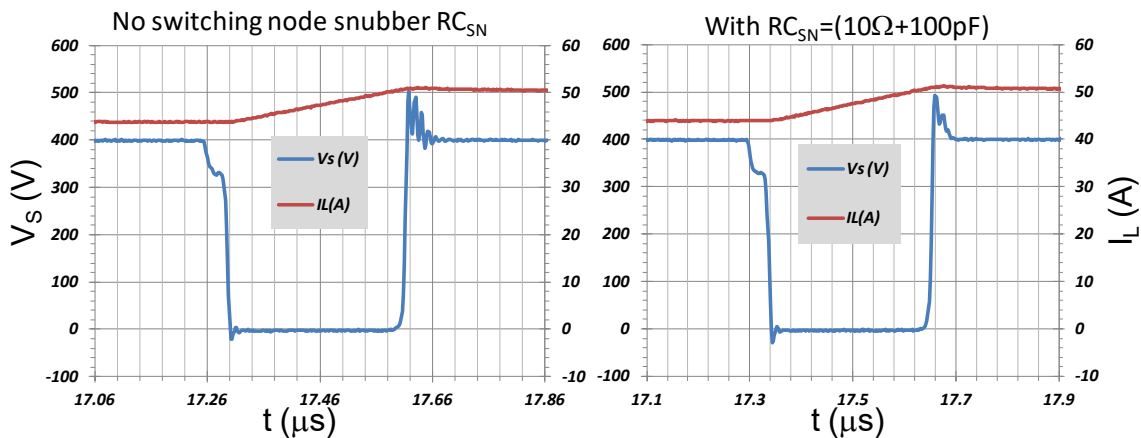


Figure 3. Effect of switching node snubber RC_{SN} on half-bridge inductive switching waveforms (Devices: TP65H035WS).

Application Note 0009

Part III: The di/dt Limits of GaN Switching Devices & Solutions for High-current Operation

Transphorm GaN FETs are designed for the highest robustness and reliability within the technology boundaries today. These devices can operate to their full voltage rating and at extremely high di/dt levels in normal operation mode (forward conduction when current enters the Drain). However, when used as a free-wheeling device in reverse conduction mode (current enters the Source when the Gate is off), there are di/dt limits beyond which the performance can be negatively affected. Although these reverse conduction di/dt limits in the range of 1200~3800 A/ μ s (depending on device & stress duration) are much greater than that of typical superjunction devices at ~60A/ μ s, care must be taken for best performance at high current levels since the di/dt value is a strong function of switching current.

It is important to note that this di/dt limit only applies to the device acting as a free-wheeling diode (FWD) and only applies to the duration when the FWD transitions from blocking voltage to reverse conducting current. Three cases are illustrated in **Figure 4**; the affected devices are the ones functioning as an FWD during dead-time when the inductor current commutates from the main switch to the reverse current of the FWD.

- 1) A boost converter that uses an SiC diode as the rectifier device – Not affected.
- 2) A synchronous boost that uses a GaN FET as the FWD – Q_2 affected.
- 3) A synchronous buck that uses a GaN FET as the FWD – Q_1 affected.

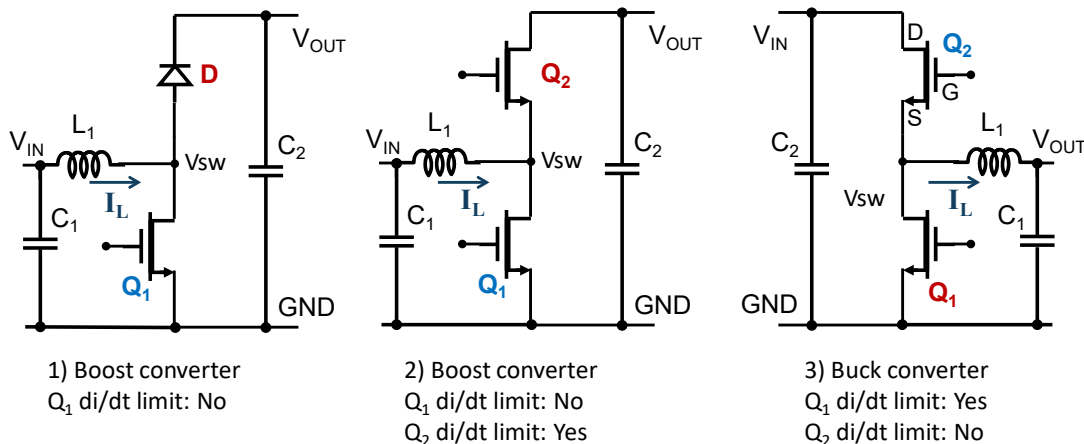


Figure 4. Identifying the device affected by the di/dt limit in three popular circuits: (1) boost converter, (2) synchronous boost converter, and (3) buck converter.

The maximum di/dt stress happens when the main switch [Q_1 in **Figure 4** (2) or Q_2 in **Figure 4** (3)] turns off and the inductor current redirects to the FWD instantly. The higher the turn-off current, the higher the reverse conduction di/dt. The reverse conduction di/dt limits and associated maximum (turn-off) switching current values are listed in the datasheet. The example for TPH320WSB is shown in **Table 1**. The $(di/dt)_{RDMC}$ and I_{RDMC1} values are for constant repetitive switching operation such as in a DC to DC converter, while I_{RDMC2} applies to DC to AC or AC to DC conversion circuits when the peak current switching is much lower than the average switching current. The $(di/dt)_{RDMT}$ and I_{RDMCT} values are for transient conditions such as in the event of power-line-disturbance (PLD) in a PFC (when one AC input cycle is missing, which forces the circuit to operate at a much higher current in the next cycle to make up for the energy loss).

Application Note 0009

Symbol	Parameter	Min	Typ	Max	Unit
$(di/dt)_{RDMC}$	Reverse diode di/dt, repetitive ^b	—	—	1500	A/ μ s
I_{RDMC1}	Reverse diode switching current, repetitive (dc) ^{c, e}	—	—	23	A
I_{RDMC2}	Reverse diode switching current, repetitive (ac) ^{c, e}	—	—	27	A
$(di/dt)_{RDMT}$	Reverse diode di/dt, transient ^d	—	—	2900	A/ μ s
I_{RDMT}	Reverse diode switching current, transient ^{d, e}	—	—	35	A

Table 1. TPH3205WSB reverse diode conduction di/dt limits and associated max switching current when using the recommended R_G and RC_{SN} .

Note that the reverse diode switching current limits were obtained with the recommended circuit parameters [Figure 1(a) and Table 2]. The gate resistor R_G is important to control the di/dt and the addition of a switching node snubber RC_{SN} offers further improvements when operation current is high. The effect of RC_{SN} is shown in Figure 1(b): a slight reduction in low-load efficiency, but a significant enhancement at high load. In applications with operation current below 70 percent of the maximum rating, the RC_{SN} can be omitted. On the other hand, one can further increase the R_G value if the operation current is higher than the maximum I_{RDM} 's in the datasheet. In all situations, care has to be taken to ensure junction temperature of the devices do not exceeding maximum rating.

Part IV: Additional Design Notes

1) Circuit and Layout Recommendations

- Place the RC_{DCL} as close as possible to the drain pin of the high-side GaN FET and ground it to the large ground plane.
- SMD mounting is recommended for all snubber components.
- A Gate resistor (R_G) is required for all devices.
- Gate ferrite beads (FB1) are only required for TO-220 and PQFN devices; TO-247 devices have built-in ferrite beads hence no external FB1 is needed.
- If the device is being driven at >70 percent of the rated I_{RDM} values, then a switching node RC snubber (RC_{SN}) is recommended in addition to the required DC-link RC snubber (RC_{DCL}).
- The gate ferrite bead and gate resistor prevent oscillation and reduce excessive di/dt when the GaN device is used in a half-bridge topology.
- The RC_{DCL} reduces the voltage ringing due to device interaction with the bypass network.
- The RC_{SN} slightly reduces light and medium load efficiency with the benefit of increased output power.
- The RC_{SN} implementation in a half-bridge has the advantage of allowing a higher peak turn-off switching current due to the reduction of the di/dt seen by the freewheeling device as the main conducting device turns off.

Application Note 0009

2) Required and Recommended External Components

The recommended components of the half-bridge circuit in **Figure 1(a)** is summarized in **Table 2**. They have tested and verified to prevent oscillation for safe, reliable operation with the recommended gate drive voltage ranges shown. Using a higher “on” voltage is not recommended and may increase the propensity for oscillation and will require a larger gate resistor. Using a lower “on” voltage may increase switching and conduction losses due to increased $R_{ds(on)}$.

Parameters \ Part Num.	TP65H035WS/WSQA	TP65H050WS	TP65H050BS	TP65H070LxG	TP65H150LSG	TP65H300G4LSG	TPH3205WSBQA	TPH3212PS	TPH3208LxG/PS	TPH3206LxGB/PSB	TP90H180PS	TP90H050WS
Package Type	TO-247	TO-247	TO-263	PQFN88	PQFN88	PQFN88	TO-247	TO-220	PQFN88/TO-220	PQFN88/TO-220	TO-220	TO-247
Recommended Gate Voltage Drive	0V, 12 V	0V, 12 V	0V, 12 V	0V, 12 V	0V, 12 V	0V, 10-12 V	0V, 10-12 V	0V, 10-12 V	0V, 10-12 V	0V, 10-12 V	0V, 10-12 V	0V, 12 V
Recommended Gate Resistor (RG)	30Ω	30-45Ω	45Ω	50-70Ω	60-70Ω	60-70Ω	15Ω	15Ω	25Ω	25Ω	25Ω	30-45Ω
Ferrite Bead Gate (FB1)	-	-	240Ω @ 100 MHz	240Ω @ 100 MHz	240Ω @ 100 MHz	240Ω @ 100 MHz	-	180Ω @ 100 MHz	330Ω @ 100 MHz	120-240Ω @ 100 MHz	180Ω @ 100 MHz	-
Recommended DCLink _{SN}	[10nF + 80] x 2	[10nF + 80] x 2	[10nF + 80] x 2	[10nF + 100] x 2	[4.7nF + 50]	[4.7nF + 50]	[10nF + 80] x 2	[10nF + 80]	[10nF + 80]	[10nF + 80]	[10nF + 80]	[10nF + 80] x 2
Recommended RC _{SN}	[200pF + 50]	[100pF + 100]	[100pF + 100]	[68pF + 150]	[22pF + 150]	-	[100pF + 100]	[22pF + 150]	[22pF + 150]	[22pF + 150]	[22pF + 150]	[100pF + 100]
Reverse diode max (di/dt), repetitive (A/μs) - di/dt _{REDC}	1800	1600	1600	1400	1200	TBD	1500	1400	1250	1200	1200	1600
Reverse diode max swiching current, dc-dc repetative (A) - I _{RDMS1}	28	24	24	19	11	TBD	23	19	13	11	11	24
Reverse diode max swiching current, ac repetative (A) - I _{RDMS2}	35	28	28	24	14	TBD	27	24	17	14	14	28
Reverse diode max (di/dt), transient (A/μs) - di/dt _{TRMT}	3800	3000	3000	2800	2400	TBD	2900	2800	2500	2400	2400	3000
Reverse diode max swiching current, transient (A) - I _{RDMT}	45	36	36	30	18	TBD	35	30	21	18	18	36

Table 2. Recommended components for half-bridge circuit in Figure 1(a).

3) To Verify GaN FET Stable Operation

To verify adequate operational margin without oscillation, as a minimum observe the V_{DS} waveforms at the turn-on and turn-off switching edges at the application’s maximum drain current. This may occur during start-up or at the application’s maximum load step. A double-pulse or multi-pulse test is highly recommended utilizing the actual layout, with current levels at or greater than 120 percent of the application’s anticipated peak current. Verify that the ringing on the V_{DS} waveform at the transition edges is adequately damped. See design guide [DG004: Multi-pulse Testing for GaN Layout Verification](#).