transphorm

Application Note 0010

GaN FETs in Parallel Using Drain Ferrite Beads and RC Snubbers for High-power Applications

Abstract

This application note provides a solution for paralleling GaN FETs in bridge power converters using drain ferrite beads and/or RC snubbers, including GaN device driver design.

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Introduction

It is challenging to parallel gallium nitride (GaN) FETs in hard-switching bridge power converter applications, especially for discrete in leaded packages. Due to the high dv/dt, di/dt switching speed, dynamic current, and transition energy, unbalance between the parallel GaN FETs is potentially greater compared to silicon (Si) MOSFETs. This application note provides a solution for paralleling GaN FETs in bridge power converters using drain ferrite beads and/or RC snubbers, including a GaN device driver design discussion.

Solution 1: Parallel two TO-220/TO-247 devices directly

In the paper Paralleling GaN HEMTs for Diode-free Bridge Power Converters[1], two GaN FETs directly paralleling was proposed. Symmetrical circuit, negative turn-off gate voltage, and RC snubber are utilized to avoid unbalanced current sharing and unstable oscillation. Figure 1 shows a basic half-bridge circuit using a single half-bridge driver.

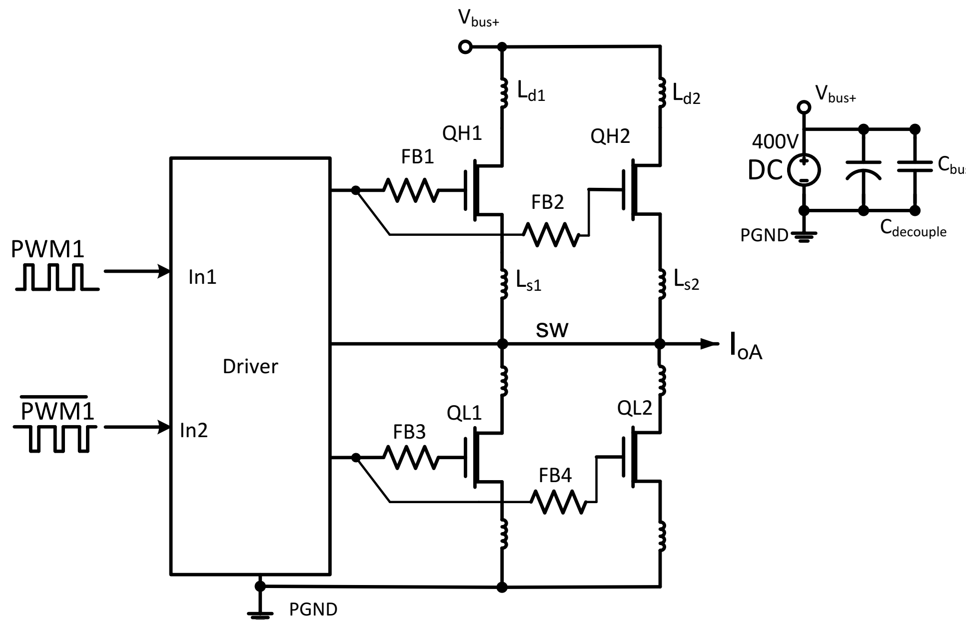


Figure 1. A half-bridge circuit using two GaN FETs in parallel

Two TO-220 in parallel

As shown in Figure 2, a half-bridge circuit with two devices directly paralleling is presented. To make the gate circuits symmetrical to each device, side-by-side layout is selected. It is seen that the gate loop area increases and switching node connection is longer than back-to-back placement, while it is good for the thermal dissipation as the two heat sources don't need to attach to the same area of heat sink. Since the parasitic inductance is higher than single device half-bridge, 10V/-4V negative biased Vgs voltage is applied to avoid the fault turn on due to the voltage ringing induced by the common source inductance. The switching node area should not overlap with power GND or high voltage layers, because the parasitic

[1] Z. Wang, Y. Wu, J. Honea, L. Zhou, Paralleling GaN HEMTs for Diode-free Bridge Power Converters. *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, pp. 752-758.

capacitance will bring additional switching loss and also unstable oscillation. A very small-value RC snubber is optional for reduce the voltage spike and improve the reliability, as shown in Figure 2.

Since the high dv/dt slew rate voltage change in switching node will be coupled to the low voltage signal side through high side isolated power supply, low isolation capacitance (< 3pF) power supply is selected and a common mode choke can effectively reduce the peak of common mode current. A common mode choke is applied on high side power supply to filter out the common mode current ripples. Another solution for avoiding high dv/dt interference is using non-isolated boot-strap circuit to generate negative voltage bias. The hard switching tests are conducted for verification. It can be seen in Figure 3 that both high and low side devices safely and repeatedly switch to 50A without slowing down the switching speed (Rg = 0).

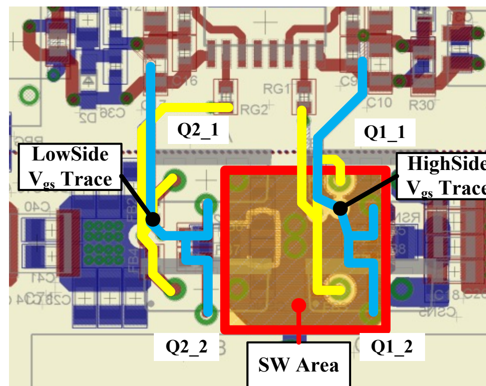
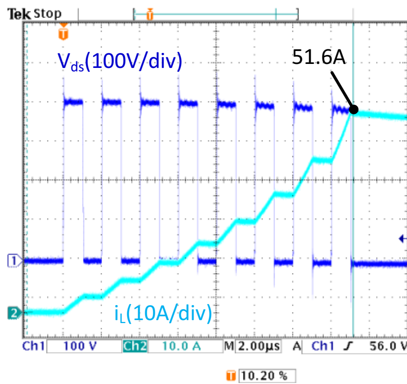
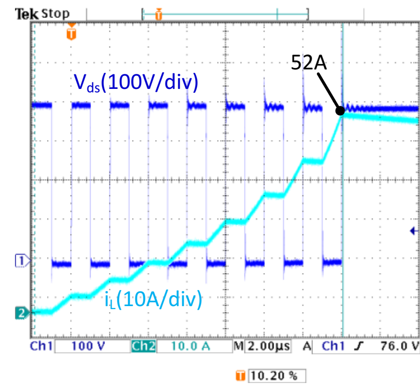


Figure 2. Layout of two TPH3206PS directly paralleling circuit



(a)

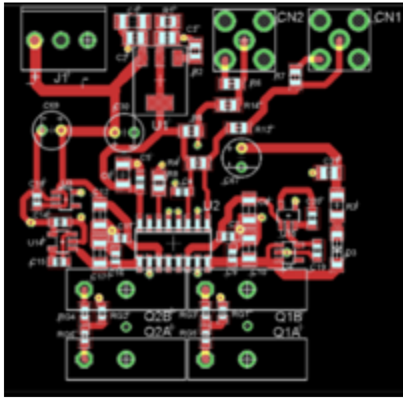


(b)

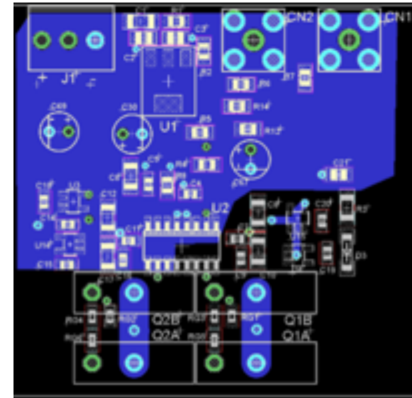
Figure 3. Switching test of paralleling TO-220 GaN FETs: (a) high side switching up to 51.6A, (b) low side switching up to 52A

Two TO-247 in parallel

The TO-247 is a bigger package that leads to large power and driving loop in parallel case. Therefore, separated driving board and power board are recommended for paralleling TO-247 devices. Figure 4 shows the driving board PCB layout and Figure 5 shows the assembled two half-bridge boards with two TO-247 in parallel. In this way, the power loop of each device can be symmetrical and compact and separated from the driving circuit.



(a)



(b)

Figure 4. Driving the daughter board for a parallel TO-247 half-bridge: (a) top layer, (b) bottom layer

Whether using a TO-247 or TO-220 style package the, recommended driving voltage is still +10V/-4V Vgs. The difference is that an RC snubber is needed for the TO-247 paralleled solution (a 47pF+10Ω snubber is suggested across each device). Figure 6 below verifies the stability of the hard switching tests to over 80A.

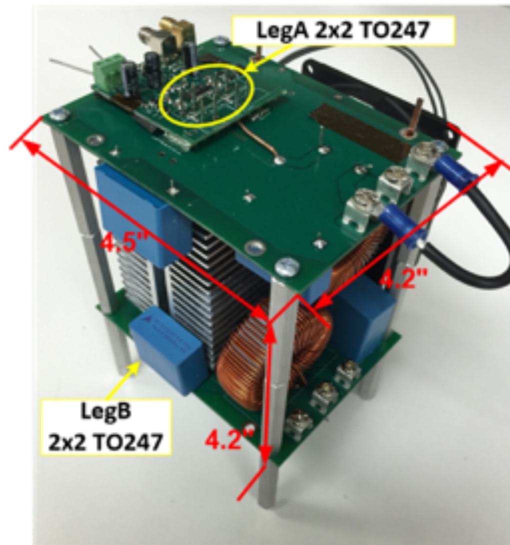


Figure 5. Assembled two-TO-247 half-bridge

Figure 6. Hard-switching to >80A: (a) high side switching to 86.8A, (b) low side switching to 93.6A

Solution 2: Parallel two TO-247 devices using drain ferrite bead

In Solution 1, we focused on the PCB layout optimization to make the direct parallel successful; however, the high frequency ringing due to the parasitic inductance and output capacitance still exists. It may not only result in the oscillation between high side and low side devices, but can also lead to the oscillation between two paralleled devices, which will make the parallel fail. Referring to the application note AN0009, Recommended External Circuitry for Transphorm GaN FETs, the ringing frequency for Transphorm's GaN FETs is around 50~200MHz, and adding proper drain ferrite beads to suppress this ringing will greatly improve the stability of half-bridge circuit. It is an additional solution for paralleling GaN FETs using drain ferrite bead.

Parallel TO-247 using a through-hole ferrite bead

Figure 7 shows the paralleled GaN FETs half-bridge circuit with drain ferrite bead for each device. The ferrite beads effectively increase the impedance between two parallel devices and prevent them from oscillation.

Since the ringing is eliminated, high side and low side devices can be arranged side-by-side although the loop inductance is higher than back-to-back. The paralleled devices are back-to-back configuration, as shown in Figure 8, for the schematic and PCB board.

Compared the non-drain ferrite bead method, the PCB layout is simple and it is not necessary to separate driving board and power board. However, the circuit symmetricity is still a very important factor for successfully paralleling.

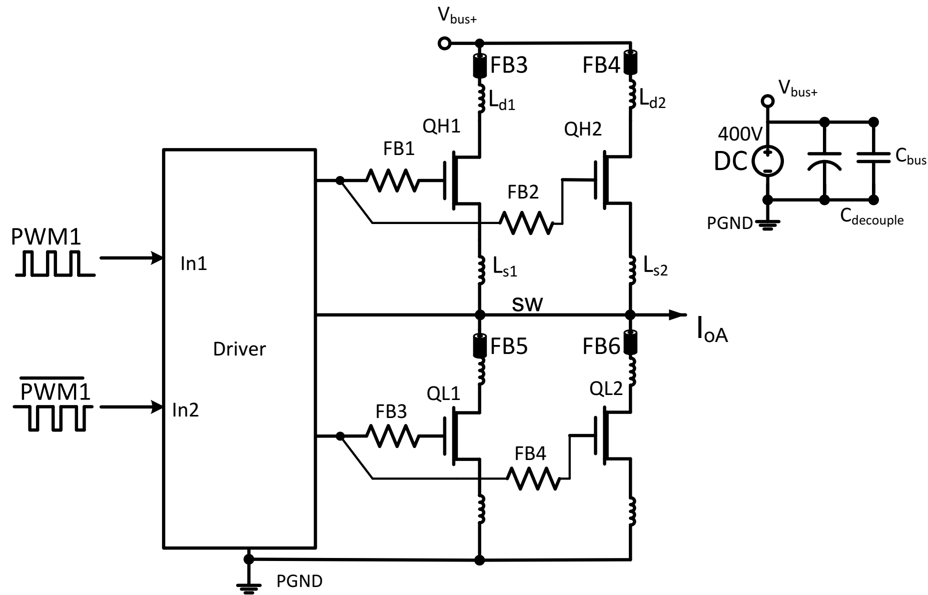
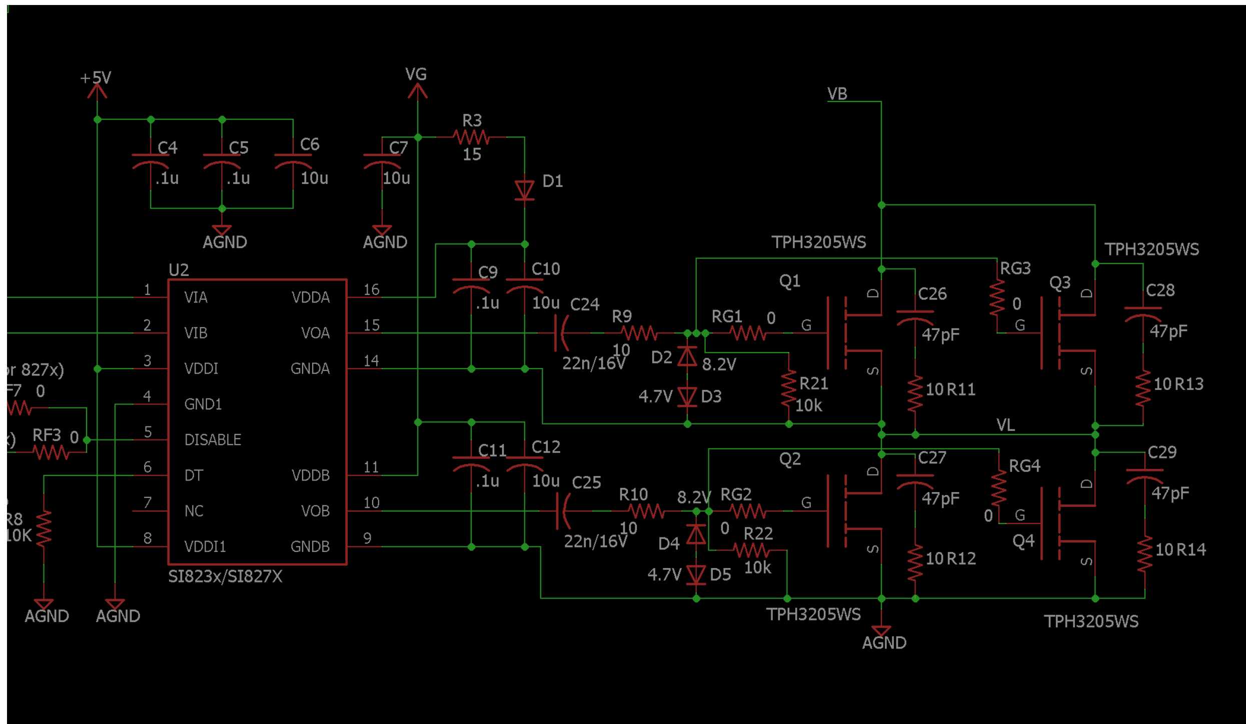
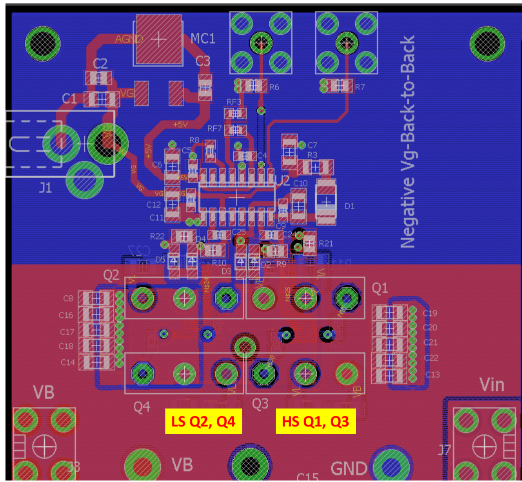


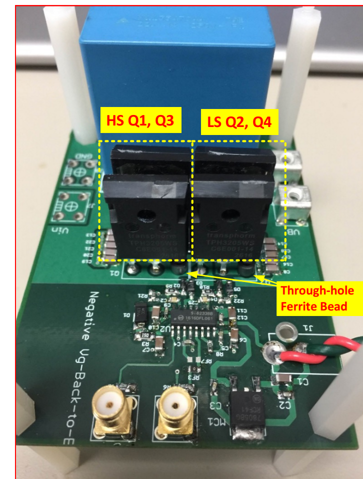
Figure 7. A half-bridge circuit with two GaN FETs in parallel using a drain ferrite bead



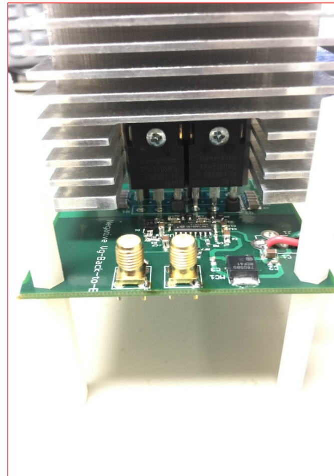
(a)



(b)



(c)



(d)

Figure 8. Two-TO-247 in parallel using a drain ferrite bead: (a) schematic, (b) layout, (c) assembled PCB board, (d) mounting heat-sink

Switching tests were verified for both high side and low side devices in different DC bus voltages. Figure 9 and Figure 10 show the low side switching test waveforms at 200–400V, respectively. It can be seen that the voltage ringing is suppressed. The RC snubber can be removed when using drain ferrite bead, so the switching loss can be reduced. Figure 11 shows the switching waveform at 50A without an RC snubber, while the voltage ringing is slightly higher than those with an RC snubber.

Figure 9. Low side switching waveforms: red = iL, yellow = Vds

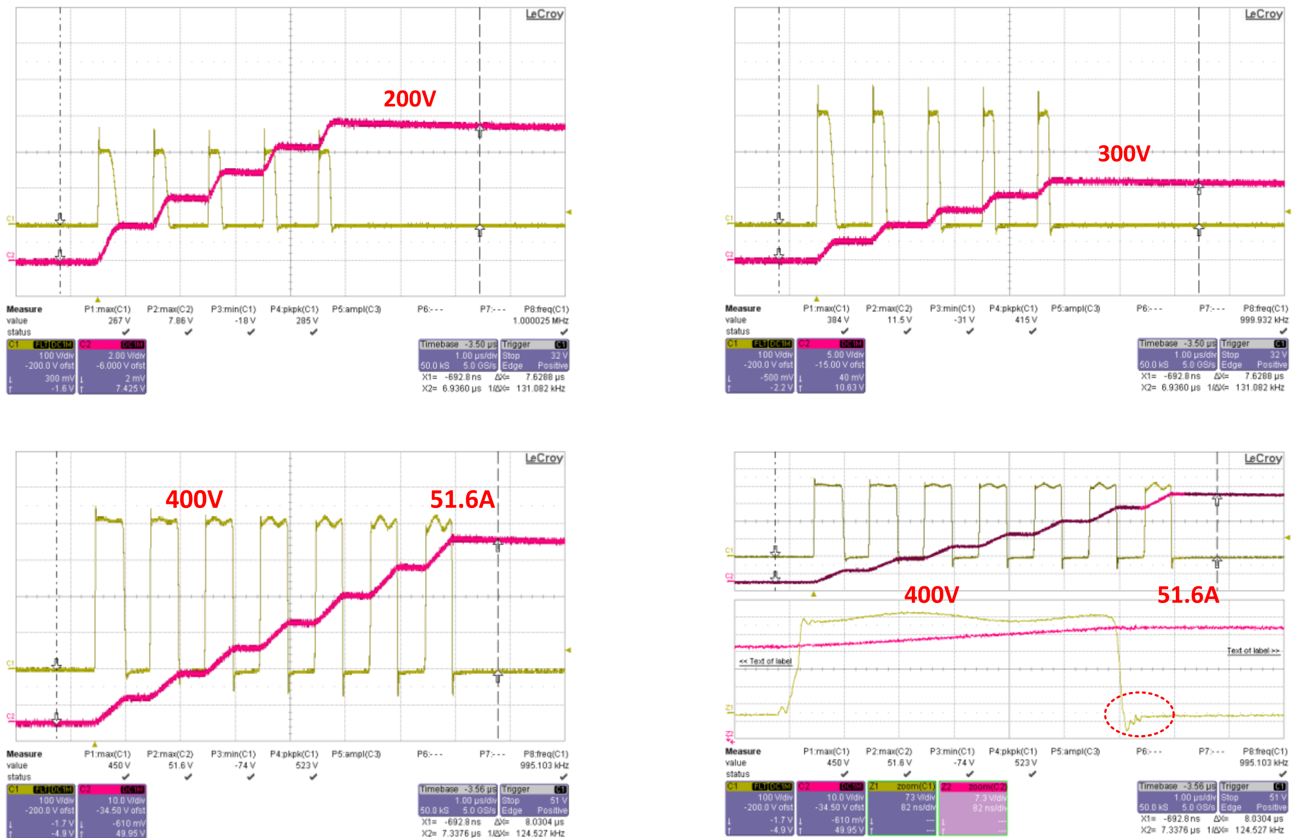
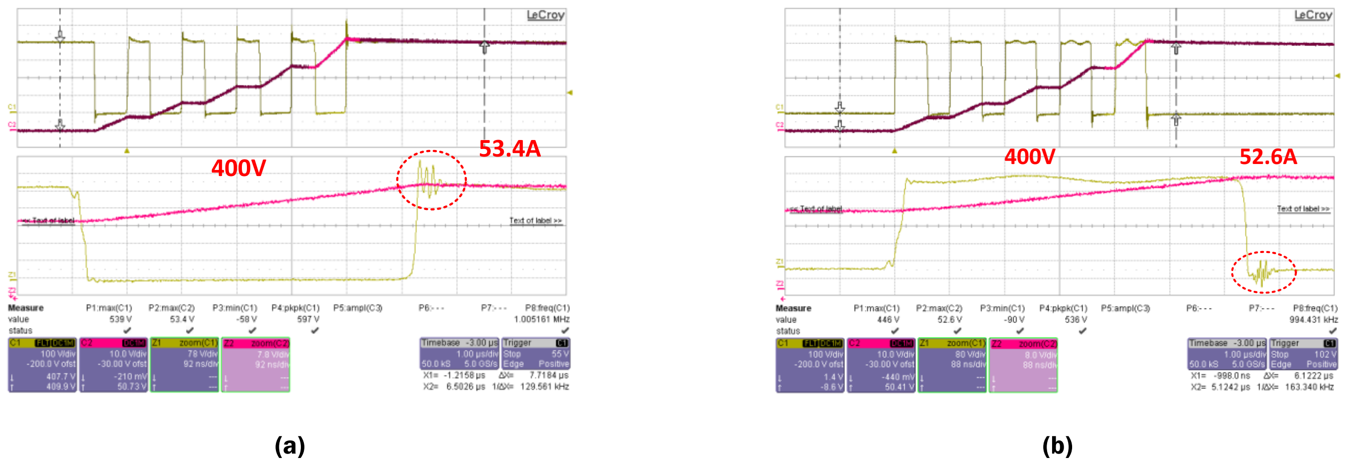


Figure 10. High side switching waveforms: red = iL, yellow= Vds



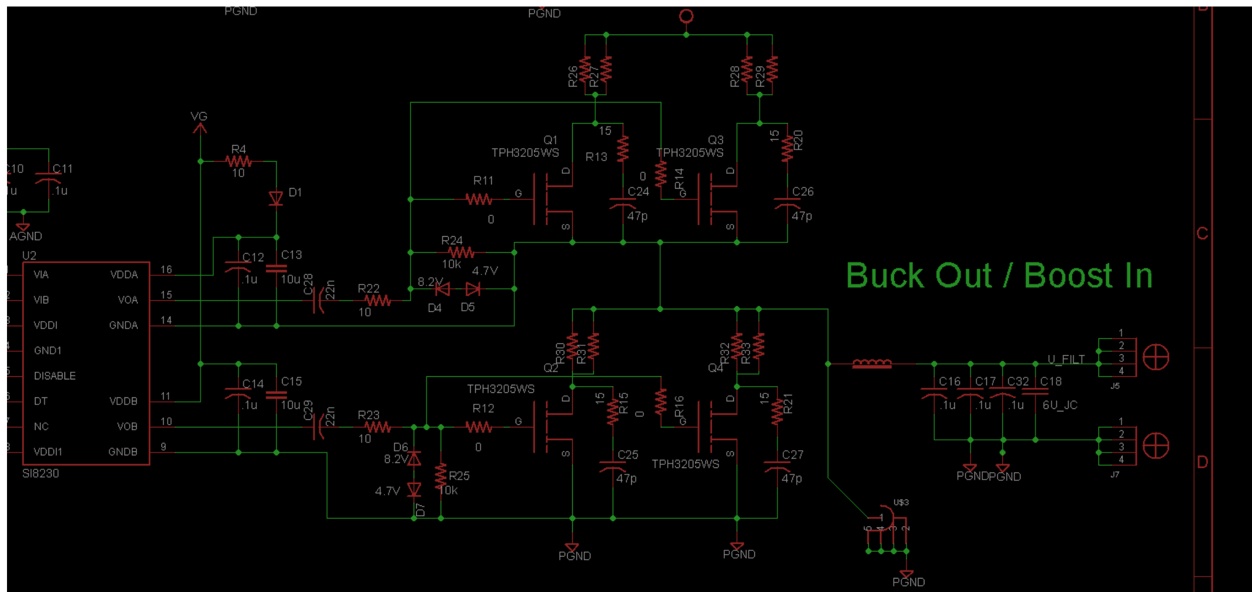
(a) (b)

Figure 11. Switching to 50A without an RC snubber: (a) low side switching to 53.4A, (b) high side switching to 52.6A

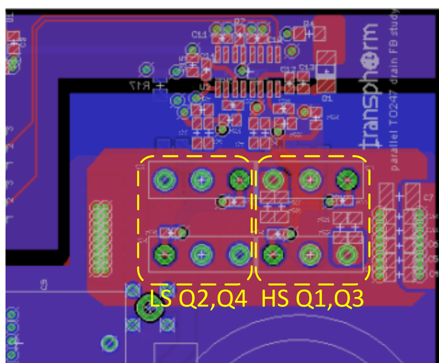
Parallel TO-247 using an SMD ferrite bead

It can be proven that a high current SMD ferrite bead has the same effect to suppress the voltage ringing as an RC snubber. Figure 12 shows the schematic, PCB layout and assembled PCB board for TO-247 parallel using an SMD ferrite bead. The PCB layout is very similar to that using through-hole. It should be noticed that the SMD ferrite bead should be close to the drain and layout is symmetrical.

The switching test is conducted to verify the switching stability. Figure 13 shows the high side/low side switching to over 100A using two 30Ω @100MHz SMD ferrite beads in parallel. The small voltage ringing also happens at high side turn-on time. By adding the RC snubber, this voltage ringing is gone, as shown in Figure 14. In the test, the Vds is 400V and Vgs is 12V.



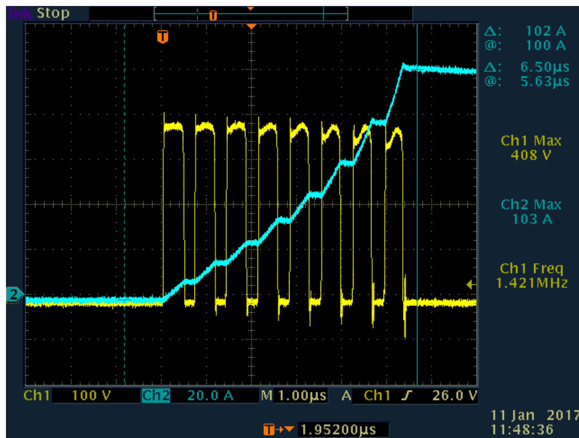
(a)

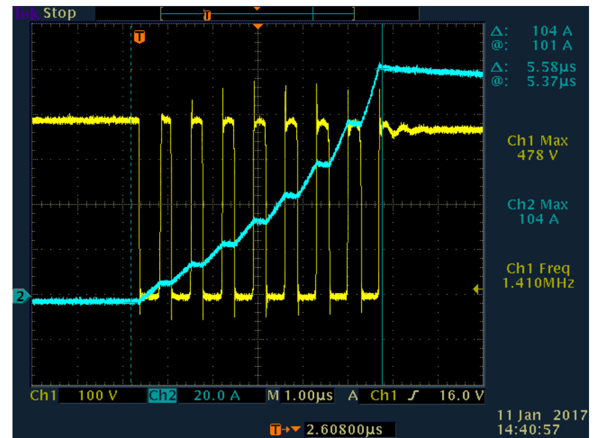


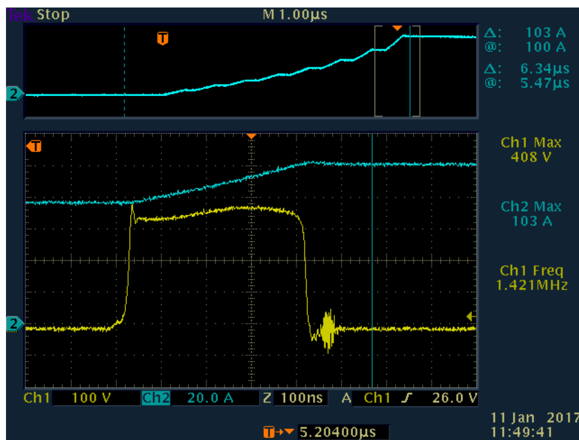
(b)

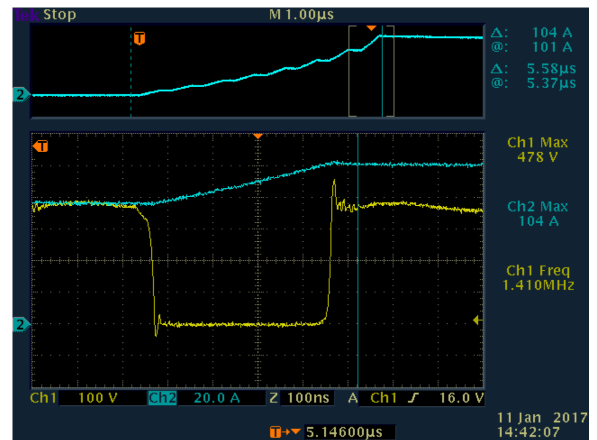
(c)

Figure 12. Two-TO-247 in parallel using and SMD ferrite bead: (a) schematic, (b) layout, (c) assembled PCB board









(a) **(b)**

Figure 13. Switching waveforms using an SMD ferrite bead only: (a) high side hard switching, (b) low side hard switching

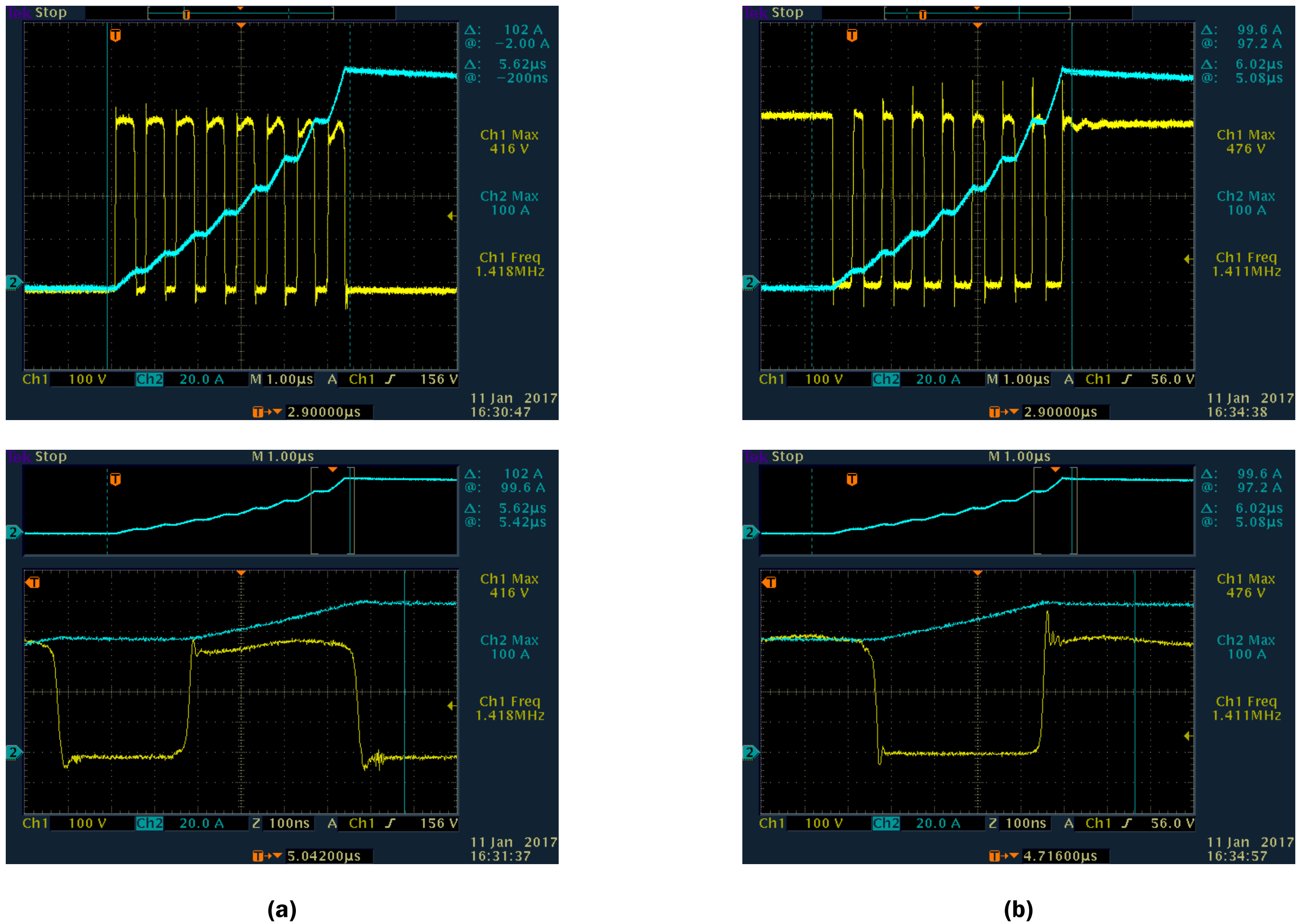


Figure 14. Switching waveforms using an SMD ferrite bead and an RC snubber: (a) high side hard switching, (b) low side hard switching

The efficiency is tested by configuring the half-bridge in synchronous rectification boost mode. The input voltage is 200V, output voltage is 400V and the circuit is switching at 100kHz with a 276µH Kool Mµ® core inductor. Figure 15 shows the efficiency curves with a 47pF+10Ω RC snubber and without an RC snubber. The peak efficiency is around 98.8% at 2.5kW~3kW. Limited by the heat sink size, it can be seen that the output power can be over 5.5kW and the case temperature is around 100°C.

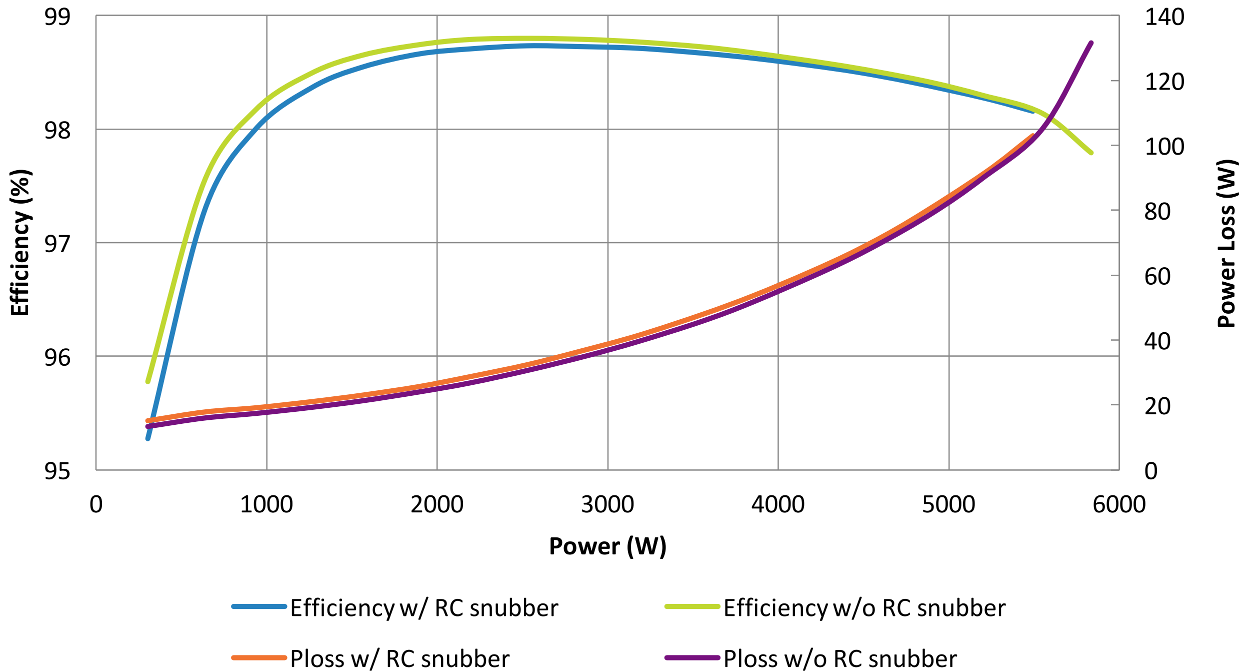


Figure 15. Efficiency measurement for a half-bridge boost converter using two TPH3205WSB in parallel

Conclusion

Design guidelines and a successful example of paralleling high-speed GaN power FETs have been presented in this application note. The driver circuit and layout design for leaded-packaged GaN FETs in parallel were discussed. A half-bridge circuit using two TPH3205WSB in parallel with and without drain ferrite beads and RC snubbers were designed and demonstrated. Both high side and low side devices were tested to 100A in hard-switching conditions, respectively. The 200V input/400V output synchronous boost mode showed that the output power can be scaled up to 5.5kW while there is still enough room for higher output power and achieves efficiency as high as 98.8% at 100kHz switching frequency.