ESP32-C6 Series

Hardware Design Guidelines

Introduction

Hardware design guidelines give advice on how to integrate ESP32-C6 into other products. ESP32-C6 is a series of ultra-low-power SoCs with support for 2.4 GHz Wi-Fi 6 (802.11 ax), Bluetooth® 5 (LE), Zigbee and Thread (802.15.4).

These guidelines will help to ensure optimal performance of your product with respect to technical accuracy and conformity to Espressif's standards.

Version 1.0

Espressif Systems

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1 Overview

Note:

Check the link or the QR code to make sure that you use the latest version of this document:
https://espressif.com/sites/default/files/documentation/esp32-c6_hardware_design_guidelines_en.pdf

ESP32-C6 series is a low-power MCU-based SoC solution that supports 2.4 GHz Wi-Fi 6 (802.11 ax), Bluetooth® 5 (LE), Zigbee 3.0 and Thread 1.3 (802.15.4). With its state-of-the-art power and RF performance, this SoC is an ideal choice for a wide variety of application scenarios relating to Internet of Things (IoT), smart home, industrial automation, health care, and consumer electronics.

ESP32-C6 has a high-performance (HP) 32-bit RISC-V processor and an low-power (LP) 32-bit RISC-V processor, operating at up to 160 MHz and 20 MHz respectively. The chip supports application development to operate without the need for a host MCU.

ESP32-C6 series provides a highly-integrated way to implement wireless communication technologies using a complete RF subsystem, including a antenna switch, RF balun, power amplifier, low noise amplifier (LNA), filter, power management unit, calibration circuits, etc. As a result, PCB size has been greatly reduced.

With its advanced calibration circuitry, ESP32-C6 series can dynamically adjust itself to remove external circuit imperfections or adapt to changes in external conditions. As such, the mass production of ESP32-C6 series does not require expensive and specialized Wi-Fi test equipment.

For more information about ESP32-C6 series, please refer to *ESP32-C6 Series Datasheet*.

2 Schematic Checklist

The core circuitry of ESP32-C6 requires only 20 electrical components (resistors, capacitors, and inductors), one crystal and one SPI flash memory chip (optional for the QFN32 package). The high integration of ESP32-C6 allows for simple peripheral circuit design. This chapter details ESP32-C6 schematics.

ESP32-C6 consists of variants in two packages, namely the QFN40 package and the QFN32 package. The main difference between these two packages is whether the flash is integrated into the chip's package.

ESP32-C6 schematics are shown in Figure 1 and Figure 2 respectively.

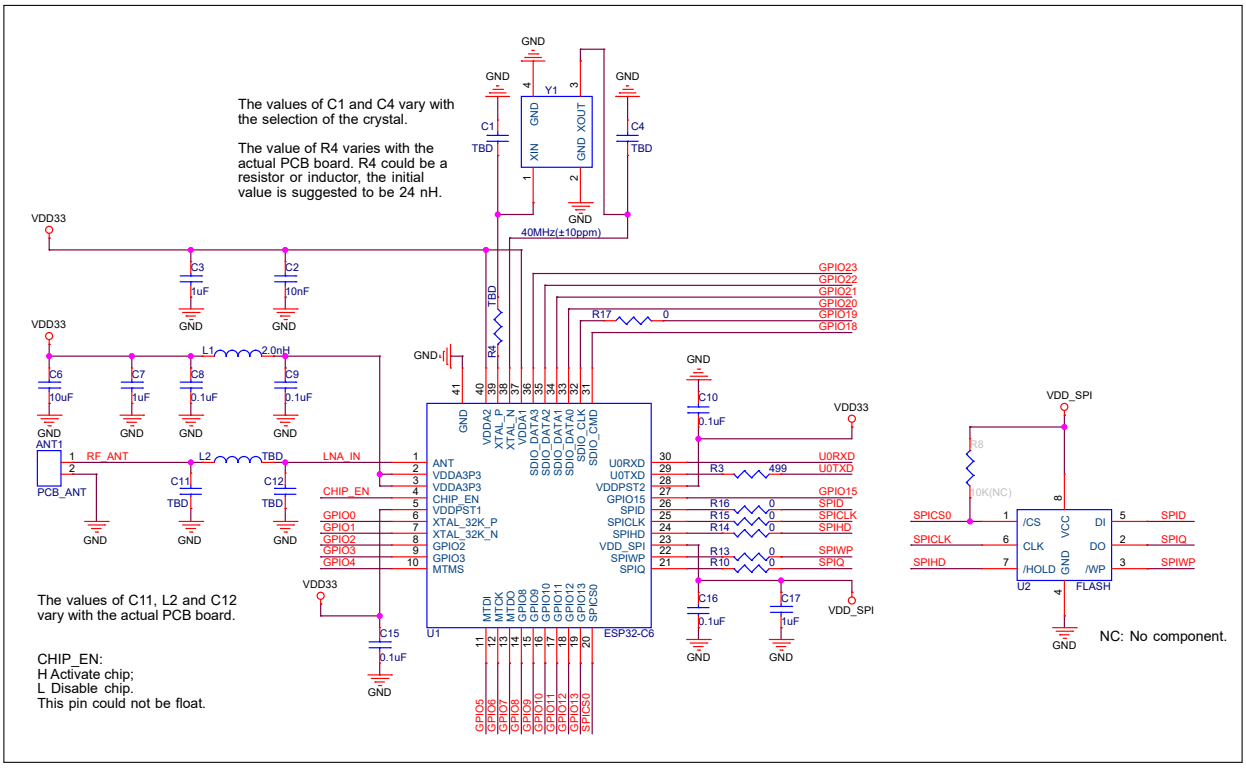

Figure 1: ESP32-C6 QFN40 Schematic

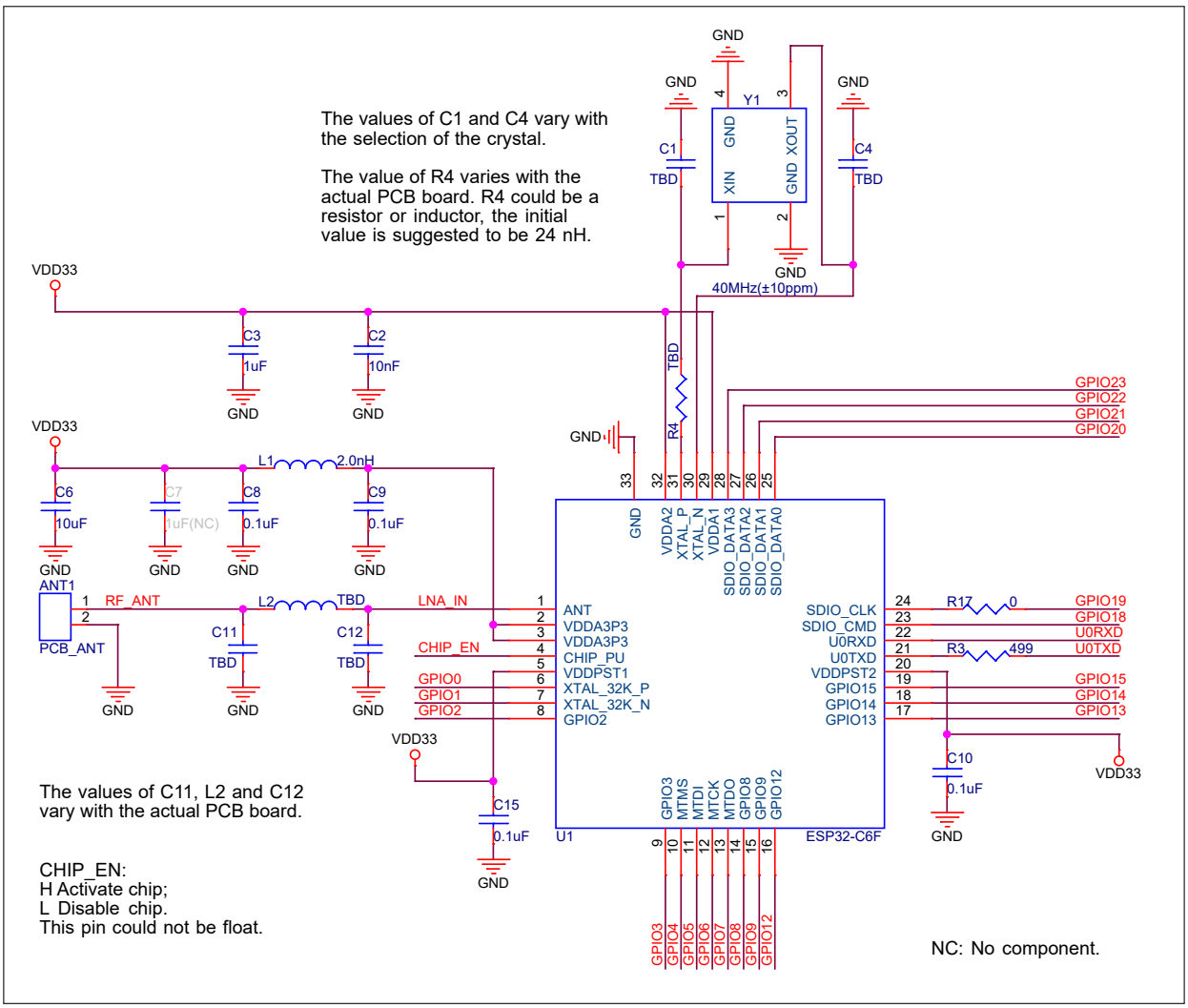

Figure 2: ESP32-C6 QFN32 Schematic

Note:

Unless otherwise specified, "ESP32-C6" used in this document refers to the QFN40 variant of ESP32-C6.

Any basic ESP32-C6 circuit design may be broken down into 11 major sections:

- Power supply
- Power-on sequence and system reset
- Flash
- Clock source
- RF
- UART
- Strapping pins
- GPIO
- ADC
- USB
- SDIO

The rest of this chapter details the specifics of circuit design for each of these sections.

2.1 Power Supply

For more information about power pins, please refer to *ESP32-C6 Series Datasheet* > Section Power Supply.

2.1.1 Digital Power Supply

ESP32-C6 has pin5 VDDPST1 and pin28 VDDPST2 that supply power to LP digital pins/part of analog pins and HP digital pins respectively, in a voltage range of 3.0 V ~ 3.6 V. It is recommended to add a 0.1 μF filter capacitor close to each digital power supply pin.

Pin23 VDD_SPI can serve as the power supply for the external device at 3.3 V (typical value), provided by VDDPST2 via R_{SPI} (For information about R_{SPI}, please refer to *ESP32-C6 Series Datasheet* > Section Power Scheme). Therefore, there will be a voltage drop on VDD_SPI to VDDPST2. It is recommended to add a 0.1 μF and a 1 μF filter capacitor close to VDD_SPI.

VDD_SPI can be connected to and powered by an external power supply.

When not serving as a power supply pin, VDD_SPI can be used as GPIO27.

Notice:

When using VDD_SPI as the power supply pin for the in-package flash or external 3.3 V flash, the supply voltage should be 3.0 V or above, so as to meet the requirements of flash's working voltage.

The schematic for the digital power supply pins is shown in Figure 3.

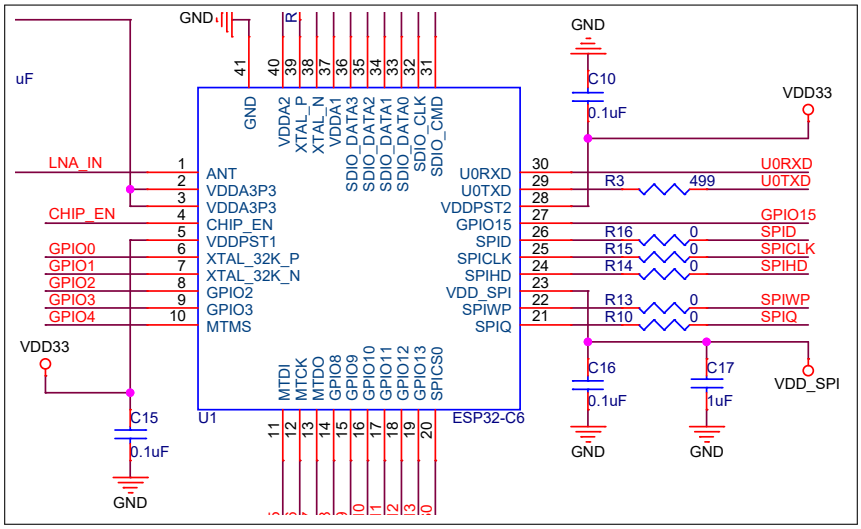

Figure 3: Schematic for the Digital Power Supply Pins

2.1.2 Analog Power Supply

Pin2 VDDA3P3, pin3 VDDA3P3, pin37 VDDA1, and pin40 VDDA2 are the analog power supply pins, working at 3.0 V ~ 3.6 V.

Please be noted that the sudden increase in current draw, when ESP32-C6 is transmitting signals, may cause a power rail collapse. Therefore, it is highly recommended to add a 10 μF capacitor to the power pin2 and pin3 VDDA3P3, which can work in conjunction with the 1 μF capacitor. In addition, a CLC filter circuit needs to be

added near VDDA3P3 pins so as to suppress high-frequency harmonics. The recommended rated current of the inductor is 500 mA or above. Refer to Figure 4 and place the appropriate decoupling capacitor near each analog power pin.

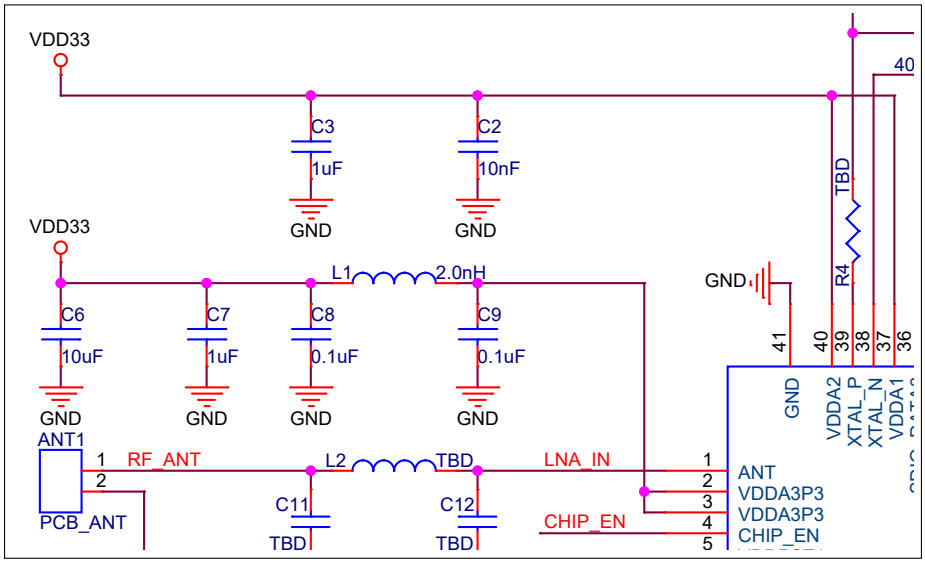

Figure 4: Schematic for the Analog Power Supply Pins

Notice:

- The recommended power supply voltage for ESP32-C6 is 3.3 V and the output current is no less than 500 mA.
- It is suggested to add another 10 μF capacitor at the power entrance. If the power entrance is close to pin2 and pin3, two 10 μF capacitors could be merged into one.
- It is suggested to add an ESD protection diode at the power entrance.

2.2 Power-up Timing and System Reset

2.2.1 Power-up Timing

When ESP32-C6 uses a 3.3 V system power supply, the power rails need some time to stabilize before CHIP_PU is pulled up and the chip is activated. Therefore, CHIP_PU needs to be powered up after the 3.3 V rails have been brought up. More details about the power-up timing can be found in Section 2.2.3.

Notice:

To ensure the correct power-up timing, it is advised to add an RC delay circuit at the CHIP_PU pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 μF. However, specific parameters should be adjusted based on the characteristics of the actual power supply and the power-up and reset sequence timing of the chip.

2.2.2 System Reset

CHIP_PU serves as the reset pin of ESP32-C6. The reset voltage (V_{IL_nRST}) should be in the range of (–0.3 ~ 0.25 × VDDPST1) V. To avoid reboots caused by external interferences, make the CHIP_PU trace as short as possible. Also, add a pull-up resistor as well as a capacitor to the ground whenever possible. More details can be found in Section 2.2.3.

Notice:

CHIP_PU pin must not be left floating.

2.2.3 Power-up and Reset Timing

Figure 5 shows the power-up and reset timing of ESP32-C6 series of chips. Details about the parameters are listed in Table 1.

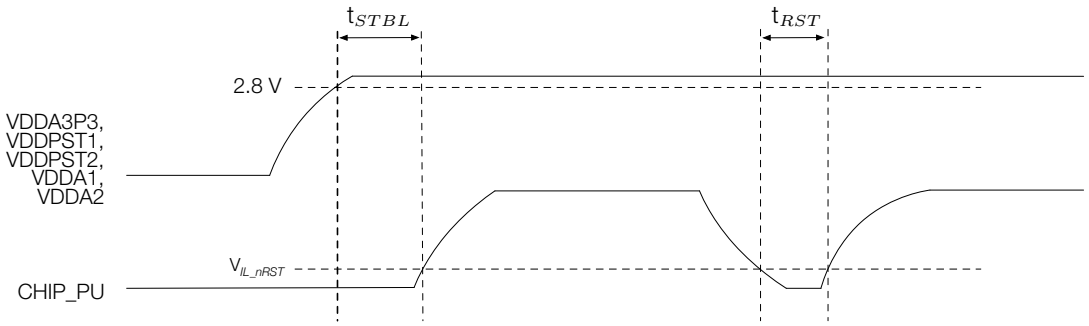

Figure 5: Visualization of Timing Parameters for Power-up and Reset

Table 1: Description of Timing Parameters for Power-up and Reset

Parameter	Description	Min (μs)
t_{STBL}	Time reserved for the power rails of VDDA3P3, VDDPST1, VDDPST2, VDDA1 and VDDA2 to stabilize before the CHIP_PU pin is pulled high to activate the chip	50
t_{RST}	Time reserved for CHIP_PU to stay below V_{IL_nRST} to reset the chip	50

Notice:

If your device needs to be frequently powered on and off, the power supply ramps up slowly, or the power supply such as solar photovoltaic is not stable, adding a single RC circuit might not meet the requirements for power-up and reset timing, and consequently the chip will not boot correctly. In this case, it is advised to take other approaches, such as adding an external reset chip or a watchdog timer IC. For chips with a 3.3 V flash, the reset threshold is suggested to be around 3.0 V.

2.3 Flash

ESP32-C6 series in QFN40 package can support up to 16 MB external flash, powered by VDD_SPI. It is recommended to add a zero-ohm series resistor on the SPI lines as shown in Figure 6, to lower the driving current, reduce interference to RF, adjust timing, and better shield from interference.

ESP32-C6 series of chips in QFN32 package have in-package SPI flash. The pins for flash are not bonded out.

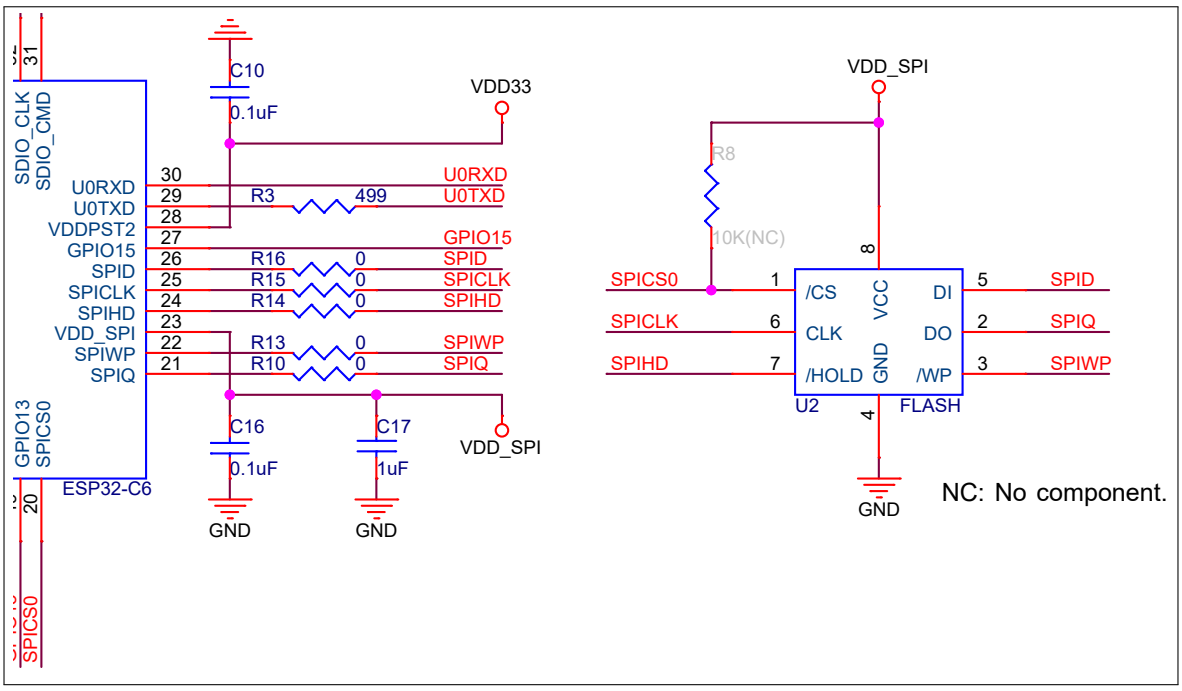

Figure 6: Schematic for the External Flash and RAM (PSRAM)

2.4 Clock Source

ESP32-C6 has two clock sources:

- External clock source
- RTC clock source

2.4.1 External Clock Source (compulsory)

Currently, the ESP32-C6 firmware only supports 40 MHz crystal.

Crystal

The circuit for the crystal is shown in Figure 7. The initial values of external capacitors C1 and C4 can be determined according to the formula:

$$C_L = \frac{C1 \times C4}{C1 + C4} + C_{stray}$$

where the value of C_L (Load Capacitance) can be found in the crystal's datasheet, and the value of C_{stray} refers to the PCB's stray capacitance. The values of C1 and C4 need to be further adjusted after an overall test.

In order to reduce the impact of high-frequency crystal harmonics on RF performance, please add a series component (resistor or inductor) on the XTAL_P clock trace. Initially it is suggested to use an inductor of 24 nH, and the value should be adjusted after an overall test. Note that the accuracy of the selected crystal should be within ±10 ppm.

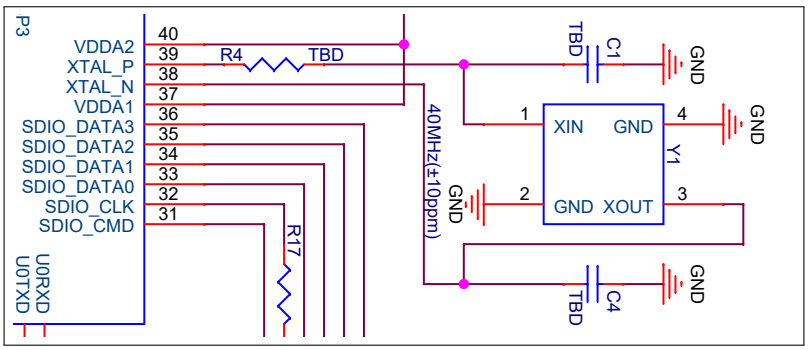

Figure 7: Schematic for the Crystal

Notice:

- Defects in the manufacturing of crystal and oscillators (for example, large frequency deviation of more than ±10 ppm, unstable performance within operating temperature range, etc) may lead to the malfunction of ESP32-C6, resulting in a decrease of the RF performance.
- When Wi-Fi or Bluetooth connection fails, after ruling out software problems, you may measure the frequency offset in 2.4 GHz via a radio communication analyzer or a spectrum analyzer and see if it is too large. If yes, adjust capacitors at the two sides of the crystal to reduce frequency offset.

2.4.2 RTC (optional)

ESP32-C6 supports main crystal division, an external 32.768 kHz crystal, or an external signal e.g. an oscillator to act as the RTC sleep clock, suitable for applications that require high-precision RTC clocks such as scenario which requires the Bluetooth wake-up function.

Figure 8 shows the schematic for the external 32.768 kHz crystal.

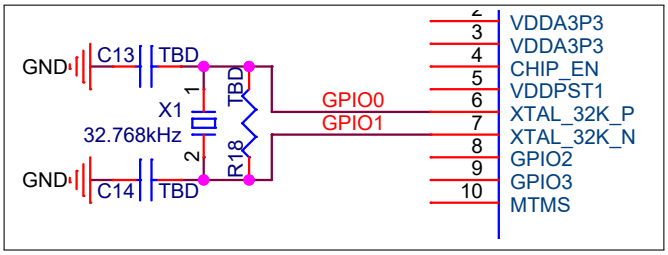

Figure 8: Schematic for the External Crystal (RTC)

Notice:

- Please note the requirements for the 32.768 kHz crystal.
  - Equivalent series resistance (ESR) $\leqslant 70\ k\Omega$.
  - Load capacitance at both ends should be configured according to the crystal's specification. For reference, see Section 2.4.1.
- The parallel resistor R is used for biasing the crystal circuit ($5\ M\Omega < R \leqslant 10\ M\Omega$). In general, you do not need to populate the resistor.
- If the RTC source is not required, then the pins for the external 32.768 kHz crystal can be used as GPIOs.

Figure 9 shows the schematic of the external signal.

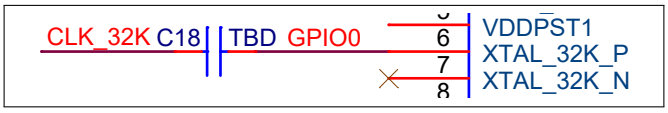

Figure 9: Schematic for ESP32-C6's External Oscillator

The external signal can be input to the XTAL's P end through a DC blocking capacitor (about 20 pF). The XTAL's N end can be floating. The signal should meet the following requirements:

Input to XTAL's P End	Amplitude (Vpp, unit: V)
Sine wave or square wave	0.6 < Vpp < VDD

2.5 RF

The RF circuit of the ESP32-C6 series of chips is mainly composed of three parts, the RF traces on the PCB board, the chip matching circuit, the antenna and the antenna matching circuit.

For the RF traces on the PCB board, 50 Ω impedance control is required.

Chip matching circuit must be placed close to the chip. It is mainly used to adjust the impedance point and suppress harmonics. The CLC structure is preferred, and a set of LC can be added if space permits. The CLC matching circuit is shown in Figure 10.

For the antenna and the antenna matching circuit, to ensure the radiation performance, the antenna's characteristic impedance must be around 50 Ω. Adding a CLC matching circuit near the antenna is recommended to adjust the antenna. However, if the available space is limited and the antenna impedance point can be guaranteed to be 50 Ω by simulation, then there is no need to add a matching circuit near the antenna.

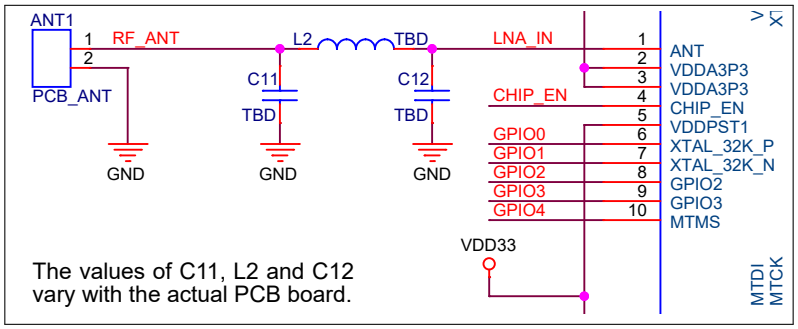

Figure 10: Schematic for RF Matching

Figure 11 shows the general process of RF tuning. Please be noted the matching parameters are subject to the RF tuning of PCB board, which depends greatly on the antenna and PCB layout. The initial value of the resistor can be 0 Ω. For ESP32-C6 series of chips, it is recommended to set the S11 parameter in the figure below to 30+j0 Ω and the center frequency is 2442 MHz.

If the RF function is not required, the RF pin can be left floating.

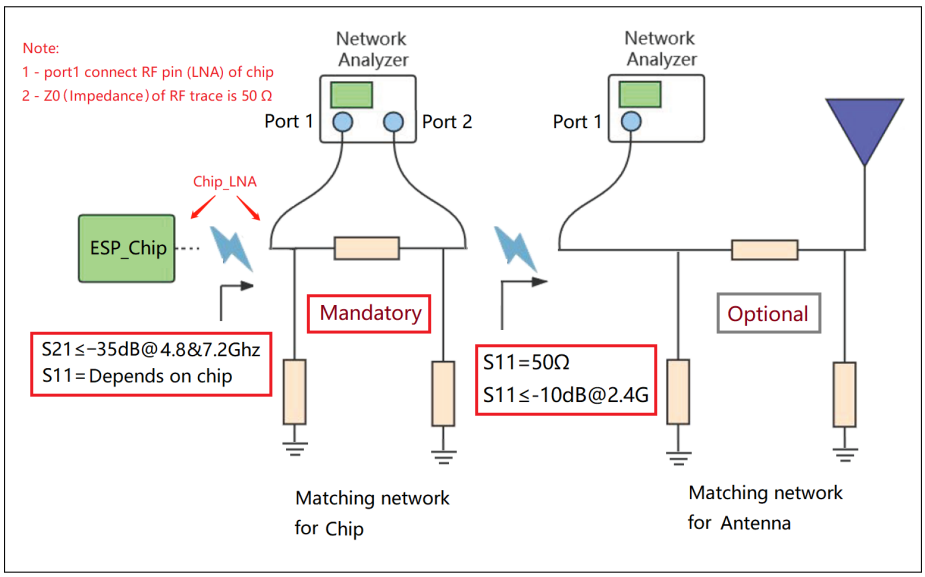

Figure 11: RF Tuning Diagram

Notice:
The matching parameters vary with board, so the ones used in our modules could not be applied directly.

2.6 UART

It is recommended to connect a 499 Ω series resistor to the U0TXD line in order to suppress the 80 MHz harmonics.

Usually UART0 is used as the serial port for download and log printing, and UART0 pins are fixed. For instructions on download over UART0, please refer to Section 4.3.

Other UART interfaces can be used as serial ports for communication, which could be mapped to any available GPIO by software configurations. For these interfaces, it is also recommended to add a series resistor to the TX line to suppress harmonics.

2.7 Strapping Pins

At each startup or reset, a chip requires some initial configuration parameters, such as in which boot mode to load the chip, etc. These parameters are passed over via the strapping pins. After reset, the strapping pins operate as regular IO pins.

All the information about strapping pins is covered in *ESP32-C6 Series Datasheet* > Section Strapping Pins.

In this document we will mainly cover the strapping pins related to boot mode.

GPIO8 and GPIO9 control the boot mode after the reset is released. See Table 3 Boot Mode Control Boot Mode Control.

Table 3: Boot Mode Control

Boot Mode	GPIO8	GPIO9
Default Configuration	– (Floating)	1 (Pull-up)
SPI Boot (default)	Any value	1
Download Boot	1	0
Invalid combination[1]	0	0

[1] This combination triggers unexpected behavior and should be avoided.

Regarding the timing requirements for the strapping pins, there are such parameters as *setup time* and *hold time*. For more information, see Table 4 and Figure 12.

Table 4: Description of Timing Parameters for the Strapping Pins

Parameter	Description	Min (ms)
t_{SU}	*Setup time* is the time reserved for the power rails to stabilize before the CHIP_PU pin is pulled high to activate the chip.	0
t_H	*Hold time* is the time reserved for the chip to read the strapping pin values after CHIP_PU is already high and before these pins start operating as regular IO pins.	3

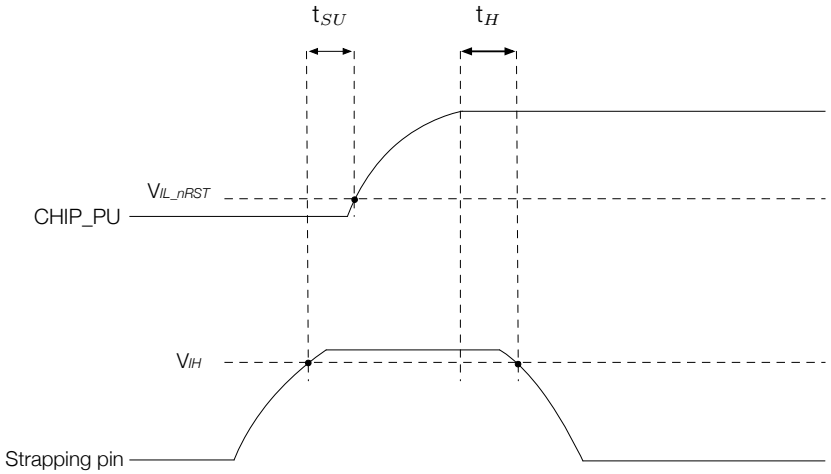

Figure 12: Visualization of Timing Parameters for the Strapping Pins

Notice:
Please do not add high-value capacitors at GPIO9, otherwise the chip might enter Download Boot mode when booted for the first time.

2.8 GPIO

Note:
The content below is excerpted from *ESP32-C6 Series Datasheet* > Section Pins.

The pins of ESP32-C6 series can be configured via IO MUX or GPIO matrix. IO MUX provides the default pin

configurations, whereas the GPIO matrix is used to route signals from peripherals to GPIO pins. For more information about IO MUX and GPIO matrix, please refer to *ESP32-C6 Technical Reference Manual* > *IO MUX and GPIO Matrix (GPIO, IO_MUX)*.

Some peripheral signals can only be routed to certain GPIO pins, while some can be routed to any available GPIO pins. For details, please refer to *ESP32-C6 Series Datasheet* > Section Peripheral Pin Configurations.

When using GPIOs,

- Please pay attention to their default configurations after reset, as shown in Table 5. It is recommended to add a pull-up or pull-down to pins in high-impedance state.
- Avoid using the pins already occupied by flash.
- Pay attention to the states of strapping pins during power-up.

Table 5: ESP32-C6 Pin Overview

Pin No.	Pin Name	Pin Type	Pin Providing Power	Pin Settings		Pin Function Sets		
				At Reset	After Reset	IO MUX	LP IO MUX	Analog
1	ANT	Analog						
2	VDDA3P3	Power						
3	VDDA3P3	Power						
4	CHIP_PU	Analog	VDDPST1					
5	VDDPST1	Power						
6	XTAL_32K_P	IO	VDDPST1			**IO MUX**	LP IO MUX	Analog
7	XTAL_32K_N	IO	VDDPST1			**IO MUX**	LP IO MUX	Analog
8	GPIO2	IO	VDDPST1	IE	IE	**IO MUX**	LP IO MUX	Analog
9	GPIO3	IO	VDDPST1	IE	IE	**IO MUX**	LP IO MUX	Analog
10	MTMS	IO	VDDPST1	IE	IE	**IO MUX**	LP IO MUX	Analog
11	MTDI	IO	VDDPST1	IE	IE	**IO MUX**	LP IO MUX	Analog
12	MTCK	IO	VDDPST1		IE, WPU [6]	**IO MUX**	LP IO MUX	Analog
13	MTDO	IO	VDDPST1		IE	**IO MUX**	LP IO MUX	
14	GPIO8	IO	VDDPST2	IE	IE	**IO MUX**		
15	GPIO9	IO	VDDPST2	IE, WPU	IE, WPU	**IO MUX**		
16	GPIO10	IO	VDDPST2		IE	**IO MUX**		
17	GPIO11	IO	VDDPST2		IE	**IO MUX**		
18	GPIO12	IO	VDDPST2		IE	IO MUX		**Analog**
19	GPIO13	IO	VDDPST2		IE, WPU	IO MUX		**Analog**
20	SPICS0	IO	VDD_SPI	WPU	IE, WPU	**IO MUX**		
21	SPIQ	IO	VDD_SPI	WPU	IE, WPU	**IO MUX**		
22	SPIWP	IO	VDD_SPI	WPU	IE, WPU	**IO MUX**		
23	VDD_SPI	Power/IO	—			IO MUX		**Analog**
24	SPIHD	IO	VDD_SPI	WPU	IE, WPU	**IO MUX**		
25	SPICLK	IO	VDD_SPI	WPU	IE, WPU	**IO MUX**		

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Pin No.	Pin Name	Pin Type	Pin Providing Power	Pin Settings		Pin Function Sets		
				At Reset	After Reset	IO MUX	LP IO MUX	Analog
26	SPID	IO	VDD_SPI	WPU	IE, WPU	**IO MUX**		
27	GPIO15	IO	VDDPST2	IE	IE	**IO MUX**		
28	VDDPST2	Power						
29	U0TXD	IO	VDDPST2		WPU [7]	**IO MUX**		
30	U0RXD	IO	VDDPST2		IE, WPU	**IO MUX**		
31	SDIO_CMD	IO	VDDPST2	WPU	IE	**IO MUX**		
32	SDIO_CLK	IO	VDDPST2	WPU	IE	**IO MUX**		
33	SDIO_DATA0	IO	VDDPST2	WPU	IE	**IO MUX**		
34	SDIO_DATA1	IO	VDDPST2	WPU	IE	**IO MUX**		
35	SDIO_DATA2	IO	VDDPST2	WPU	IE	**IO MUX**		
36	SDIO_DATA3	IO	VDDPST2	WPU	IE	**IO MUX**		
37	VDDA1	Power						
38	XTAL_N	Analog						
39	XTAL_P	Analog						
40	VDDA2	Power						
41	GND	Power						

Column **Pin Settings** shows predefined settings at reset and after reset with the following abbreviations:

- IE – input enabled
- WPU – internal weak pull-up resistor enabled
- WPD – internal weak pull-down resistor enabled

2.9 ADC

Please add a 0.1 μF filter capacitor between pins and ground when using the ADC function to improve accuracy.

2.10 USB

ESP32-C6 has a USB Serial/JTAG controller. GPIO12 and GPIO13 can be used as D- and D + of USB respectively. It is recommended to reserve a series resistor and a capacitor to ground on each trace, and place them close to the chip side.

ESP32-C6 supports download and log printing over USB. For instructions on download over USB, please refer to Section 4.3.

2.11 SDIO

ESP32-C6 series has only one SDIO slave controller that conforms to the industry-standard SDIO Specification Version 2.0. SDIO should be connected to specific GPIOs, namely SDIO_CMD, SDIO_CLK, SDIO_DATA0,

SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3. Please add a pull-up resistor to these GPIOs, and preferably reserve a series resistor on each trace.

3 PCB Layout Design

This chapter introduces the key points of how to design an ESP32-C6 PCB layout using the ESP32-C6-WROOM-1 module as an example.

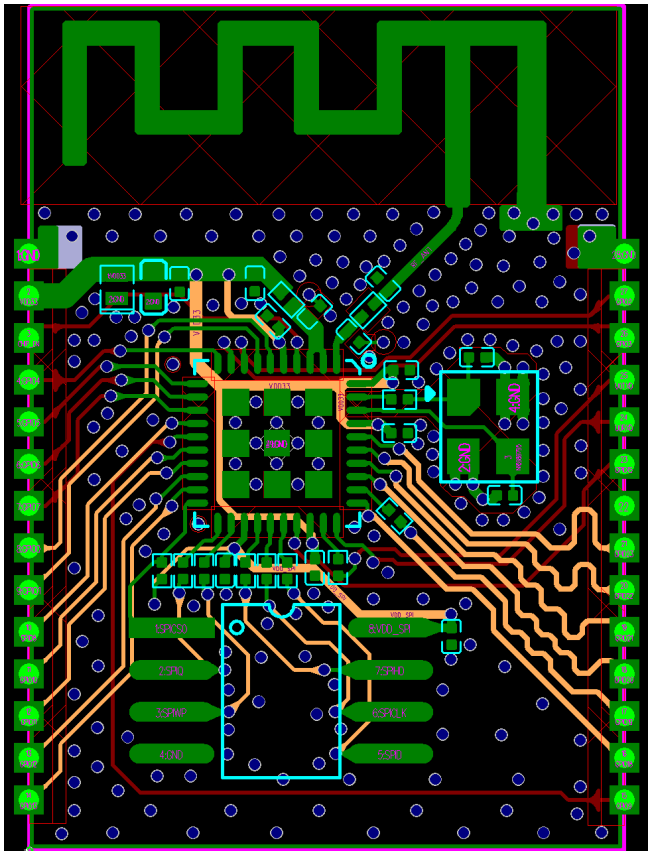

Figure 13: ESP32-C6 PCB Layout

3.1 General Principles of PCB Layout

It is recommended to use a four-layer PCB design:

- Layer 1 (TOP): Signal traces and components
- Layer 2 (GND): No signal traces here to ensure a complete GND plane
- Layer 3 (POWER): GND plane should be applied to better isolate the RF and crystal. Route power traces and a few signal traces on this layer, provided that there is a complete GND plane under the RF and crystal.
- Layer 4 (BOTTOM): Route power traces here. It is not recommended to place any components on this layer.

A two-layer PCB design can also be used:

- Layer 1 (TOP): Signal traces and components
- Layer 2 (BOTTOM): Do not place any components on this layer and keep traces to a minimum. Please make sure there is a complete GND plane for the chip, RF and crystal.

3.2 Positioning a Module on a Base Board

If module-on-board design is adopted, attention should be paid while positioning the module on the base board. The interference of the base board on the module's antenna performance should be minimized.

It is suggested to place the module's on-board PCB antenna outside the base board, and the feed point of the antenna closest to the board. In the following example figures, positions with mark ✓are strongly recommended, while positions without a mark are not recommended.

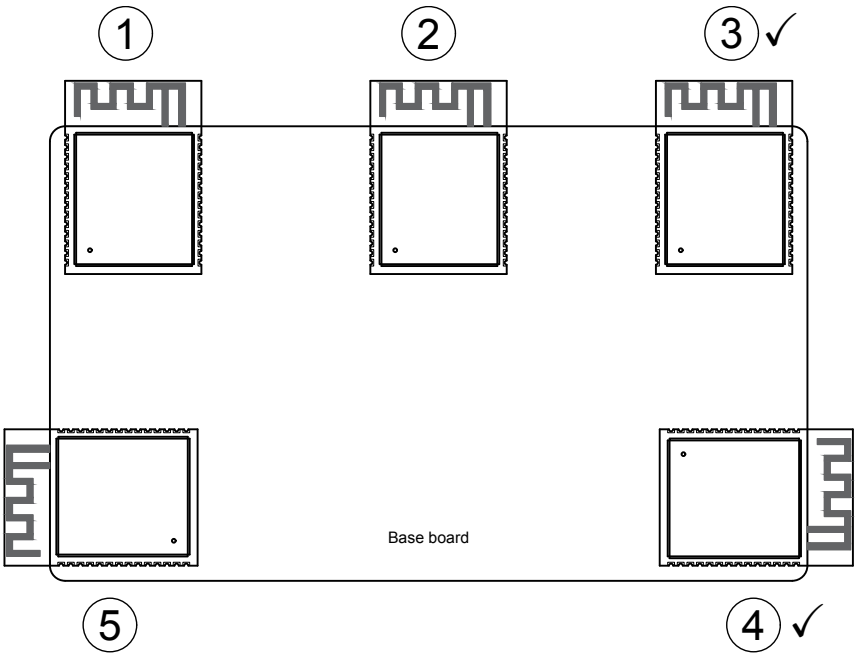

Figure 14: Placement of ESP32-C6 Modules on Base Board (antenna feed point on the right)

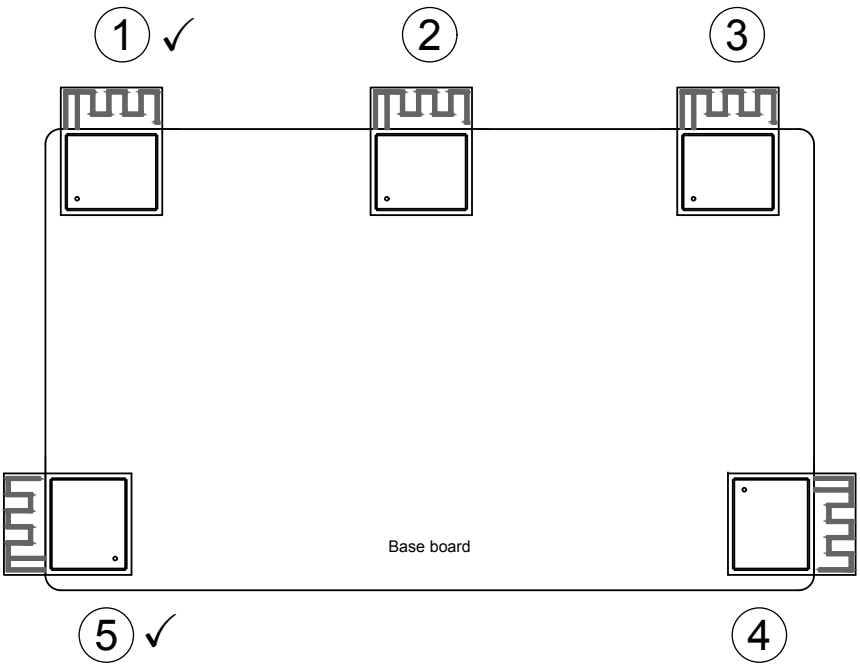

Figure 15: Placement of ESP32-C6 Modules on Base Board (antenna feed point on the left)

If PCB antenna could not be placed outside the board, please ensure a clearance of at least 15 mm around antenna area (no copper, routing, components on it), and place the feed point of the antenna closest to the board. If there is base board under the antenna area, it is recommended to cut it off to minimize its impact on the antenna. Figure 16 shows the suggested clearance for modules whose antenna feed point is on the right.

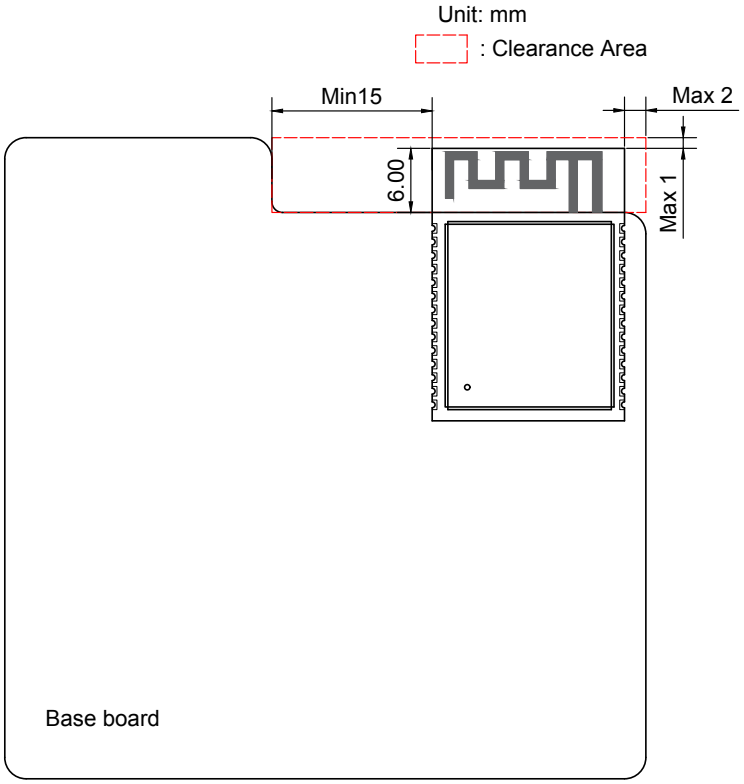

Figure 16: Keep-out Zone for ESP32-C6 Module's Antenna on the Base Board (antenna feed point on the right)

When designing an end product, attention should be paid to the interference caused by the housing of the antenna and it is recommended to carry out RF verification.

As a conclusion, please be noted it is necessary to test the throughput and communication signal range of the whole product to ensure the product's actual RF performance.

3.3 Power Supply

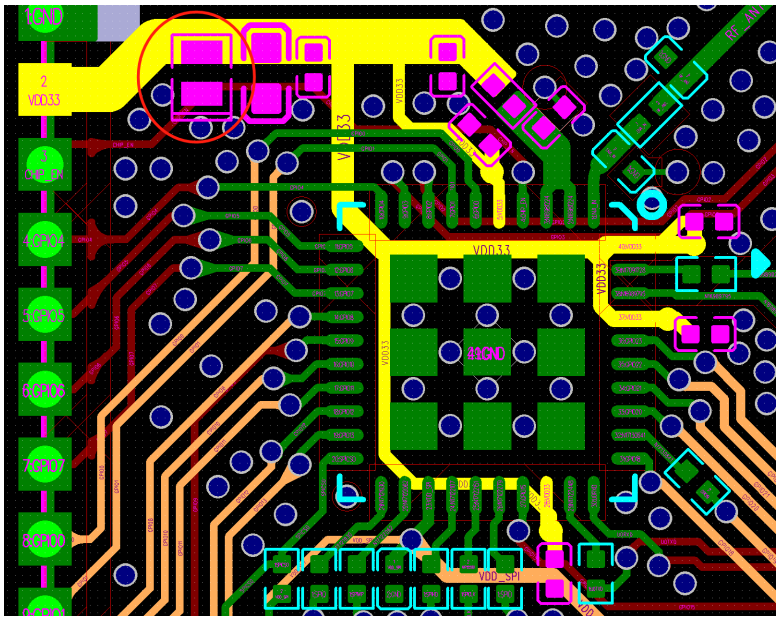

Figure 17: ESP32-C6 Power Traces in a Four-layer PCB Design

- Four-layer PCB design is preferred. The power traces should be routed on inner third layer whenever possible. Vias are required for the power traces to go through the layers and get connected to the pins on the top layer. There should be at least two vias if the main power traces need to cross layers. The drill diameter on other power traces should be no smaller than the width of the power traces.
- The 3.3 V power traces, highlighted in yellow, are routed as shown in Figure 17. The width of the main power traces should be no less than 25 mil. The width of the power traces for VDDA3P3 pins should be no less than 20 mil. Recommended width of other power traces is 10 mil.
- The ESD protection diode is placed next to the power port (circled in red in the top left quarter of Figure 17). The power trace should have a 10 µF capacitor on its way before entering into the chip, and a 0.1 or 1 µF capacitor could also be used in conjunction with this 10 µF capacitor. After them, the power traces are divided into several branches using a star-shape topology, which reduces the coupling between different power pins. Note that all decoupling capacitors should be placed close to the corresponding power pin, and ground vias should be added close to the capacitor's ground pad to ensure a short return path.

  Notice:
  The analog power pin VDDA3P3 are close to the chip's power entrance as shown in Figure 17 (in Figure 17 the power entrance is the starting point of VDD33 highlighted in yellow), so we only use one 10 μF capacitor at VDDA3P3 and the power entrance. If they are not close to each other, please add one 10 μF capacitor at VDDA3P3, and another 10 μF capacitor at the power entrance. If space allows, please also reserve two 1 μF capacitors.

- As shown in Figure 18, it is recommended to connect the capacitor to ground in the CLC filter circuit near VDDA3P3 to the fourth layer through a via, and maintain a keep-out area on other layers. The purpose is to further reduce harmonic interference.
- VDDA3P3 should be surrounded by grounding copper on both sides, and isolated by GND from the RF and GPIO traces nearby. Vias should be placed whenever possible.

- The ground pad at the bottom of the chip should be connected to the ground plane through at least nine ground vias.
- If you need to add a thermal pad EPAD under the chip on the bottom of the module, it is recommended to employ a square grid on the EPAD, cover the gaps with ink, and place ground vias in the gaps, as shown in Figure 17. This can avoid tin leakage when soldering the module EPAD to the substrate.

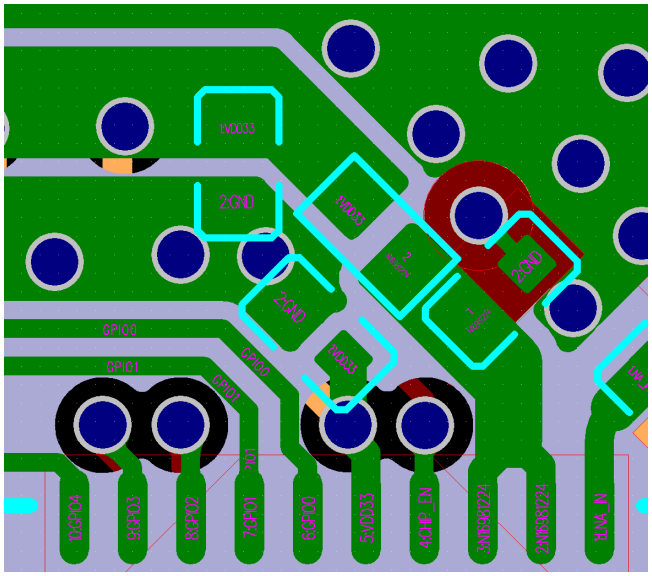

Figure 18: ESP32-C6 Analog Power Traces in a Four-layer PCB Design

3.4 Crystal

Figure 19 is the crystal layout for reference. Please only maintain a keep-out area around the crystal on the top layer, and:

- The crystal should be placed far from the clock pin to avoid the interference on the chip. **The gap should be at least 2.4 mm**. It is good practice to add high-density ground vias stitching around the clock trace for better isolation.
- There should be no vias for the clock input and output traces, which means the traces cannot cross layers.
- Components in series to the crystal trace should be placed close to the chip side.
- The external matching capacitors should be placed on the two sides of the crystal, not connected directly to the series components, and at the end of the clock trace, to make sure the ground pad of the capacitor is close to that of the crystal.
- Do not route high-frequency digital signal traces under the crystal. It is best not to route any signal trace under the crystal. The vias on the power traces on both sides of the crystal clock trace should be placed as far away from the clock trace as possible, and the two sides of the clock trace should be surrounded by grounding copper.
- As the crystal is a sensitive component, do not place any magnetic components nearby that may cause interference, for example large inductance component, and ensure that there is a clean large-area ground plane around the crystal.

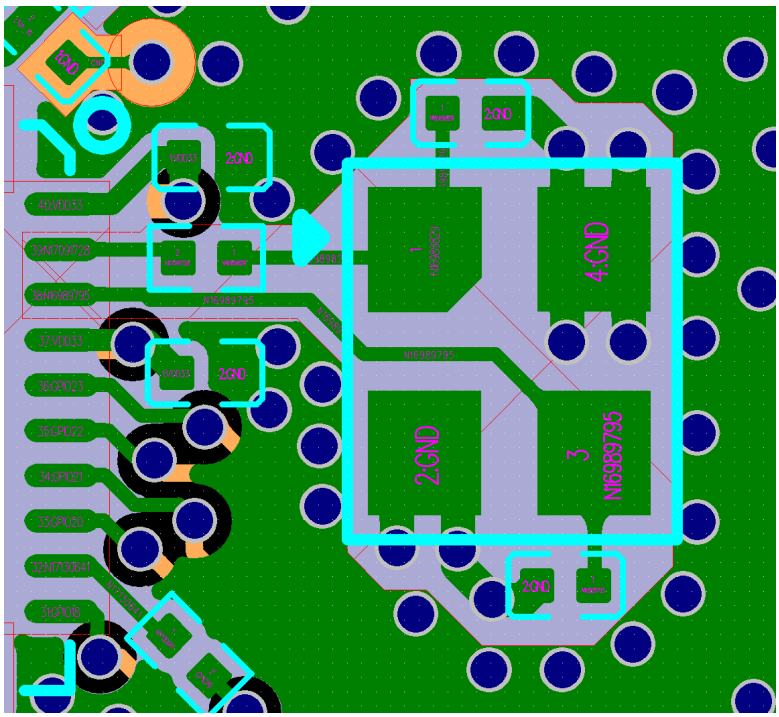

Figure 19: ESP32-C6 Crystal Layout

3.5 RF

The RF trace is routed as shown highlighted in pink in Figure 20.

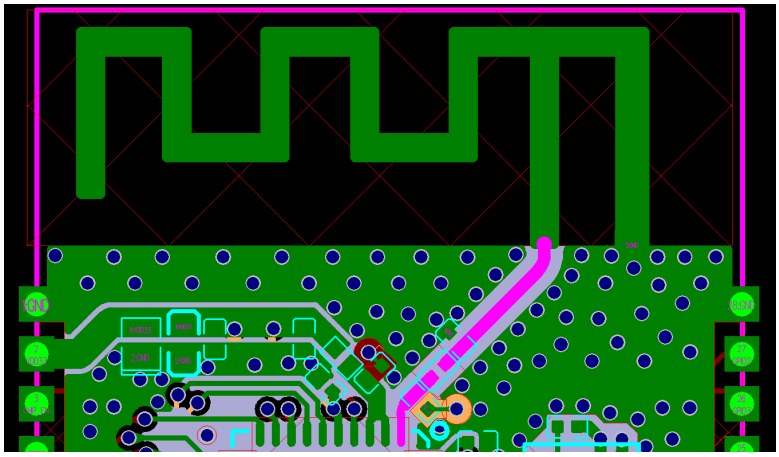

Figure 20: ESP32-C6 RF Layout in a Four-layer PCB Design

- The RF trace should have 50 Ω characteristic impedance. The reference plane is the second layer. A π-type matching circuit should be added on the RF trace and placed close to the chip, in a zigzag.
- For designing the RF trace at 50 Ω impedance, you could refer to the PCB stack-up design shown in Figure 21.

Thickness (mm)	Impedance (Ohm)	Gap (mil)	Width (mil)	Gap (mil)
-	50	12.2	12.6	12.2

Stack up	Material	Base copper (oz)	Finished Layer Thickness (mil)	DK
SM			0.4	4
L1_Top	Finished Copper 1 oz	0.33	0.8	
PP	7628 TG150 RC50%		8	4.39
L2_Gnd		1	1.2	
Core	Core		Adjustable	4.43
L3_Power		1	1.2	
PP	7628 TG150 RC50%		8	4.39
L4_Bottom	Finished Copper 1 oz	0.33	0.8	
SM			0.4	4

Figure 21: ESP32-C6 PCB Stack up Design

- The RF trace should have consistent width and not branch out. It should be as short as possible with dense ground vias around for inteference shielding.
- The RF trace should be routed on the outer layer without vias, i.e., should not cross layers. The RF trace should be routed at a 135° angle, or with circular arcs if trace bends are required.
- Please add a stub to ground at the ground pad of the first matching capacitor to suppress second harmonics. It is preferable to keep the stub length 15 mil, and determine the stub width according to the PCB stack-up, so that the characteristic impedance of the stub is 100 Ω ± 10%. In addition, please connect the stub via to the third layer, and maintain a keep-out area on the first and second layers. The trace highlighted in Figure 22 is the stub. Note that a stub is not required for package types above 0201.
- The ground plane on the adjacent layer needs to be complete. Do not route any traces under the RF trace whenever possible.
- There should be no high-frequency signal traces routed close to the RF trace. The RF antenna should be placed away from high-frequency components, such as crystals, DDR, high-frequency clocks, etc. In addition, the USB port, USB-to-serial chip, UART signal lines (including traces, vias, test points, header pins, etc.) must be as far away from the antenna as possible. The UART signal line should be surrounded by ground copper and ground vias.

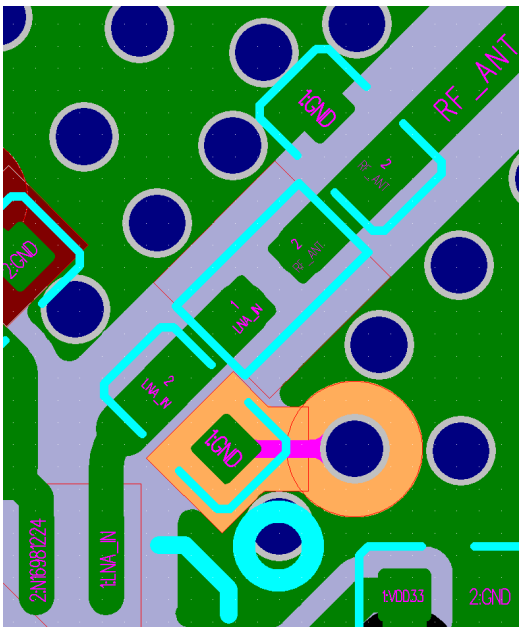

Figure 22: ESP32-C6 Stub in a Four-layer PCB Design

3.6 Flash

Place the zero-ohm series resistors on the SPI lines close to the chip. Route the SPI traces on the inner layer (e.g., the third layer), add ground copper and ground vias around the clock and data traces of SPI separately whenever possible.

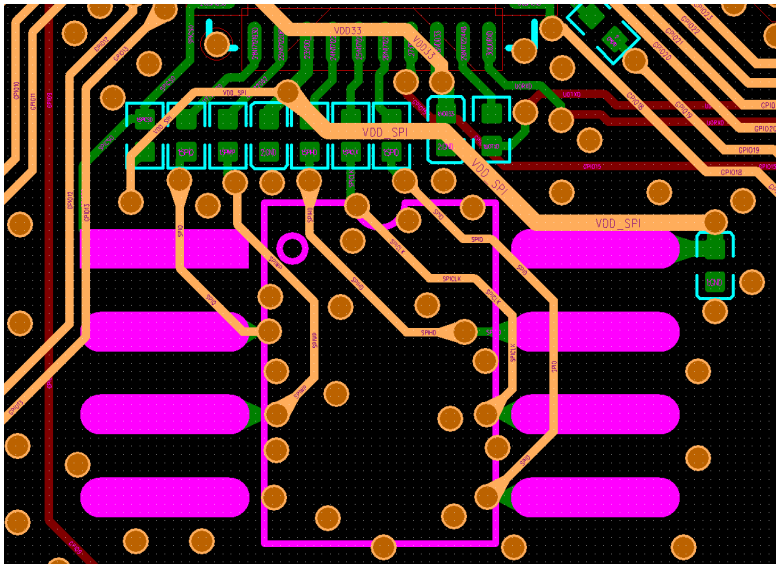

Figure 23: ESP32-C6 Flash Layout

3.7 UART

The series resistor on the U0TXD trace needs to be placed close to the chip and away from the crystal. The U0TXD and U0RXD traces on the top layer should be as short as possible, surrounded by ground copper and ground vias.

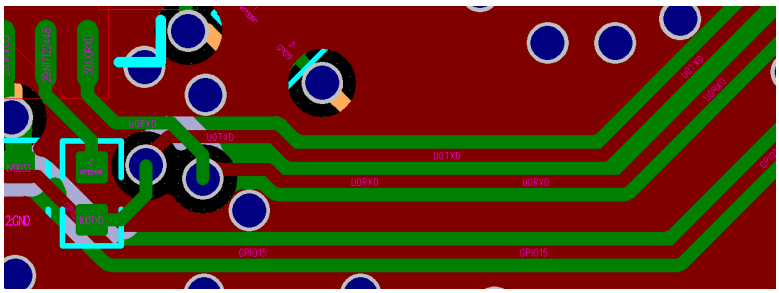

Figure 24: ESP32-C6 UART0 Layout

3.8 USB

Place the RC circuit on the USB traces closer to the chip. Please use differential pairs and route them in parallel at equal lengths. Make sure there is a complete reference ground plane and surround the USB traces with ground copper.

3.9 SDIO

Because SDIO traces have a high speed, it is necessary to control the parasitic capacitance.

The trace length for SDIO_CMD, SDIO_DATA0 ∼ SDIO_DATA3 should be 3 mil longer or shorter than the trace length for SDIO_CLK. If necessary, use serpentine routing. It is better to surround the SDIO_CLK trace with ground. The path from SDIO GPIOs to the master SDIO interface should be as short as possible and no more than 2500 mil or even 2000 mil.

Do not place SDIO traces across planes.

3.10 Typical Layout Problems and Solutions

3.10.1 Q: The current ripple is not large, but the TX performance of RF is rather poor.

Analysis:

The current ripple has a strong impact on the RF TX performance. It should be noted that the ripple must be tested when ESP32-C6 is in the normal working mode. The ripple increases when the power gets high in a different mode.

Generally, the peak-to-peak value of the ripple should be <80 mV when ESP32-C6 sends MCS7@11n packets, and <120 mV when ESP32-C6 sends 11m@11b packets.

Solution:

Add a 10 μF filter capacitor to the branch of the power trace (the branch powering the chip's analog power pin). The 10 μF capacitor should be as close to the analog power pin as possible for small and stable current ripples.

3.10.2 Q: The power ripple is small, but RF TX performance is poor.

Analysis:

The RF TX performance can be affected not only by power ripples, but also by the crystal itself. Poor quality and big frequency offsets of the crystal decrease the RF TX performance. The crystal clock may be corrupted by other interfering signals, such as high-speed output or input signals. In addition, high-frequency signal traces, such as the SDIO traces and UART traces under the crystal, could also result in the malfunction of the crystal. Besides, sensitive components or radiating components, such as inductors and antennas, may also decrease the RF performance.

Solution:

This problem is caused by improper layout and can be solved by re-layout. Please see Section 3.4 for details.

3.10.3 Q: When ESP32-C6 sends data packages, the power value is much higher or lower than the target power value, and the EVM is relatively poor.

Analysis:

The disparity between the tested value and the target value may be due to signal reflection caused by the impedance mismatch on the transmission line connecting the RF pin and the antenna. Besides, the impedance mismatch will affect the working state of the internal PA, making the PA prematurely access the saturated region in an abnormal way. The EVM becomes poor as the signal distortion happens.

Solution:

Match the antenna's impedance with the π-type circuit on the RF trace, so that impedance of the antenna as seen from the RF pin matches closely with that of the chip. This reduces reflections to the minimum.

3.10.4 Q: TX performance is not bad, but the RX sensitivity is low.

Analysis:

Good TX performance indicates proper RF impedance matching. Poor RX sensitivity may result from external coupling to the antenna. For instance, the crystal signal harmonics could couple to the antenna. If the TX and RX traces of UART cross over with RF trace, they will affect the RX performance, as well. If there are many high-frequency interference sources on the board, signal integrity should be considered.

Solution:

Keep the antenna away from crystals. Do not route high-frequency signal traces close to the RF trace. Please see Section 3.5 for details.

4 Hardware Development

4.1 ESP32-C6 Modules

For a list of ESP32-C6 modules please check Modules section of Espressif website.

To review module reference designs please check Documentation section of Espressif website.

4.2 ESP32-C6 Development Boards

For a list of the latest designs of ESP32-C6 boards please check Development Boards section of Espressif website.

4.3 Download Instructions

You can download firmware to ESP32-C6 either via UART or USB.

To download via UART:

1. Set the chip/module to Download Boot mode by pulling IO8 (floating by default) high and IO9 low (pulled up by default).
2. Power on the chip/module and check whether the chip/module has entered Download Boot mode via UART0 through serial tools.
3. Download your firmware into flash using Flash Download Tool via UART.
4. After firmware has been downloaded, keep IO9 floating or pull it high so that it returns back to high state and the chip enters SPI Boot mode.
5. Power on the chip/module again. The chip will read and execute the new firmware during initialization.

To download via USB:

1. If the flash is empty, set the chip/module to Download Boot mode by pulling IO8 (floating by default) high and IO9 low (pulled up by default).
2. Power on the chip/module and check whether the chip/module has entered Download Boot mode via USB.
3. Download your firmware into flash using Flash Download Tool via USB.
4. After firmware has been downloaded, pull IO9 high or keep it floating to enter SPI Boot mode.
5. Power on the chip/module again. The chip will read and execute the new firmware during initialization.
6. If the flash is not empty, start directly from Step 3.

Notice:

- Before downloading the firmware, it is advised to check if the chip has entered Download Boot mode or not via serial tools.
- Serial tools cannot be used simultaneously with the Flash Download Tool.
- If USB GPIOs are configured to other functions in the firmware, or the USB function is disabled in the firmware, you cannot download directly via USB for download next time, and need to set the chip to Download Boot mode first.
- It is recommended to reserve UART0 connector as an alternative way to download.

5 Related Documentation and Resources

Related Documentation

- ESP32-C6 Series Datasheet – Specifications of the ESP32-C6 hardware.
- ESP32-C6 Technical Reference Manual – Detailed information on how to use the ESP32-C6 memory and peripherals.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP32-C6 Series SoCs* – Browse through all ESP32-C6 SoCs.
  https://espressif.com/en/products/socs?id=ESP32-C6
- *ESP32-C6 Series Modules* – Browse through all ESP32-C6-based modules.
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- *ESP32-C6 Series DevKits* – Browse through all ESP32-C6-based devkits.
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- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  https://products.espressif.com/#/product-selector?language=en

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  https://espressif.com/en/contact-us/sales-questions

Glossary

CLC	Capacitor-Inductor-Capacitor
DDR	Double-Data Rate
ESD	Electrostatic Discharge
LC	Inductor-Capacitor
PA	Power Amplifier
RC	Resistor-Capacitor
RTC	Real-Time Clock
SiP	System-in-Package
Zero-ohm resistor	A zero-ohm resistor is a placeholder on the circuit so that another higher ohm resistor can replace it, depending on design cases.

Revision History

Date	Version	Release Notes
2023-03-09	v1.0	First release

www.espressif.com

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