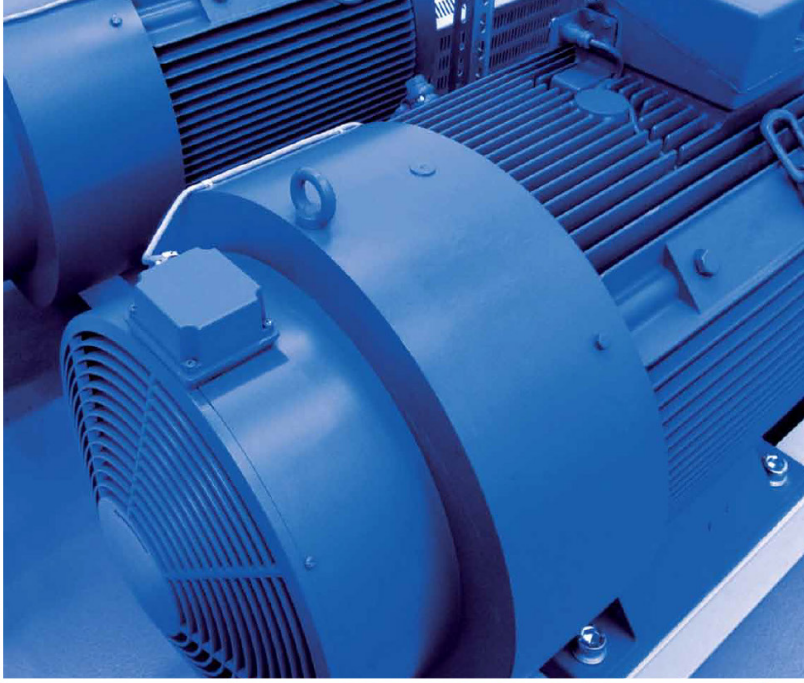

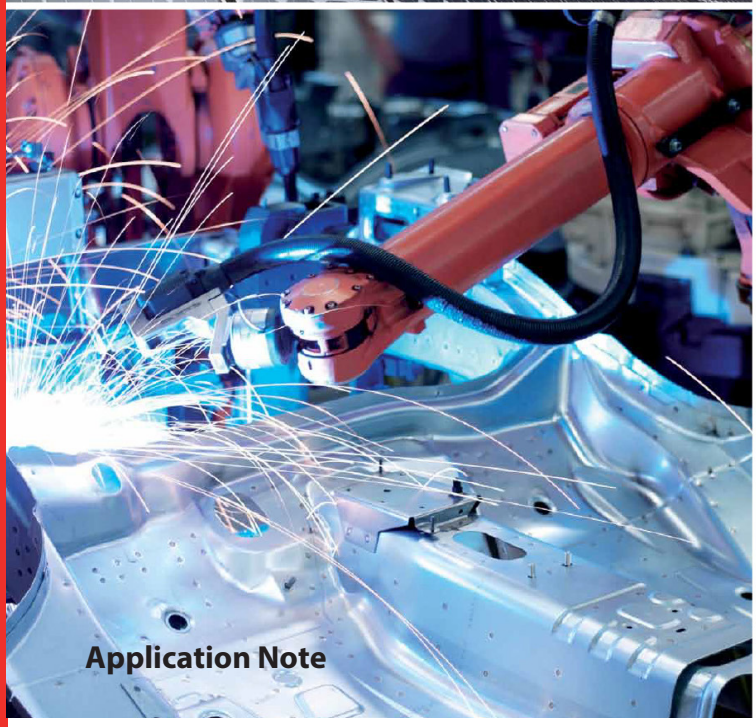

Application Note

EMC/EMI Filter Design with RB Common-Mode Chokes: Part 2

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Content

In this paper, we will look at a theoretical approach to determining the amount of EMC noise that will occur, and how to determine the appropriate filter component values to mitigate that noise.

Filter design example

A simple example was chosen to explain the design approach for an EMC/EMI filter with RB chokes. Assuming our application is a 1.6 kW half bridge push-pull converter running on 115 V AC single phase like shown in figure 1. The switching frequency is 20 kHz, the duty cycle is 50 % and IEC/EN61000-6-3, – the generic emission standard for residential, commercial and light-industrial environments – should be fulfilled. The switching components are displayed as switches T1 and T2.

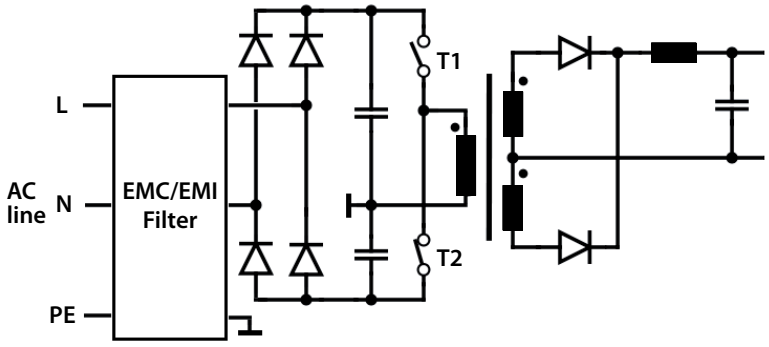

Fig. 1: Half bridge push-pull power supply

1. Determine AC current

To design an EMC/EMI line filter with RB chokes, the highest AC current is expected at minimum input voltage (115 V–10 %) Iac = 1600 W/103.5 V = 15.5 amps. RB chokes can operate up to an ambient temperature of 60 °C without derating. In this case a 16 A RB choke is selected.

2. Estimate the EMI noise level

RB chokes are available as low and high inductance versions. For this application with non-sinusoidal current, the low inductance version (all RB6x22) is the preferred type. To identify the needed attenuation performance, we estimate the EMI noise level as demonstrated in the next step.

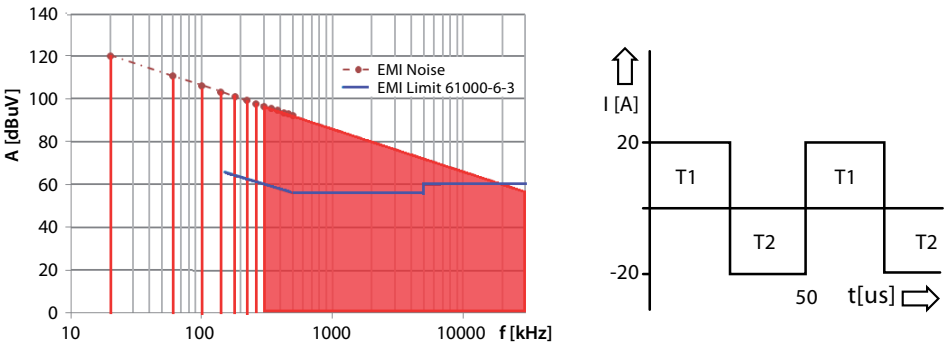

Fig. 2: Estimated trend of DM noise

The DM noise going to the line is mainly caused by the voltage drop across the impedance Z of the DC link capacitors resulting from the current blocks of the switching transistors. A very simplified EMI noise estimation (neglecting the ramp up time of the current, the needed dead time between the current blocks of the push-pull converter, the non-conducting phase of the diodes, the frequency dependence of Z, etc.) delivers a voltage drop U of about 0.76 volts with current blocks of 20 A and an impedance Z of 38 mΩ.

$$a_n = \frac{4\,U}{\pi\,n}\ [V] \quad A_n = 20 \log \frac{a_n}{1\mu V}\ [dB\mu V] \quad \text{for } n = 1, 3, 5\ldots$$

Equ. 1: Fourier analysis

The Fourier analysis according to equation 1 delivers the harmonics for this symmetrical signal. For the fundamental we receive 0.97 V (120 dBµV) as displayed in figure 2. DM noise can be described as an envelope curve starting at 20 kHz with 120 dBµV and decreases with 20 dB per decade. As a symmetrical signal is only causing odd harmonics, the 9th (180 kHz) with 0.11 V (101 dBµV) would be the first harmonic to be damped to comply with the quasi peak limits of IEC/EN61000-6-3.

For PWM modulated signals with a steady variation of the on time like with drives or PFC converters, the envelope curve is more complex. For an estimation of DM noise with variable duty cycle like for PFC stages, the envelope curve can also be reduced to a simple model. The amplitude of the fundamental remains on the same level up to frequency f1, which can be calculated with equation 2:

$$f_1 = \frac{f_s}{\sin(\pi\, d_{min})}$$

d_{min} smallest duty cycle [RAD]
f_s switching frequency

Equ. 2: Frequency f1 for EMI noise envelope curve

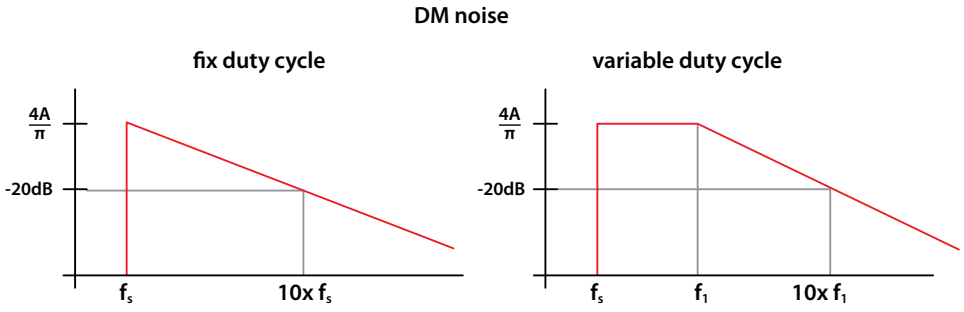

Fig. 3: Simplified envelope curves of DM noise

Figure 3 shows the simplified models of DM noise in both cases. Starting at the fundamental with a fix duty cycle of 50%, the envelope curve of DM noise immediately decreases with 20 dBµV per decade. For applications with variable duty cycle the envelope curve remains on the starting level up to f1 and then decreases with 20 dBµV per decade like shown at the right side diagram of figure 3.

CM noise is mainly transferred to ground via the small parasitic capacitance of the insulation between the chip and the ground of the switching power component (excluded motor drive applications with shielded motor power cords).

In our example with a fixed duty cycle of 50% CM noise is a symmetrical signal with the switching frequency period. The decay time of the pulses depends on the size of the coupling capacity and the impedance of the circuit which closes the loop to balance the leap. Assuming a coupling with several 10 pF and a line impedance of 25 Ω of the LISN for CM noise and no further ringing effects, the simplified response signal would look like shown in figure 4:

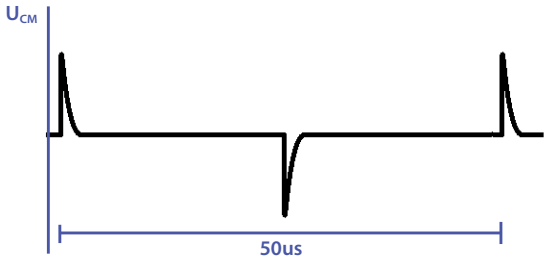

Fig. 4: Simplified CM noise signal

If one of the transistors switches, the voltage leap of 80 V would lead to current flowing through the parasitic capacitance to ground. The contact to ground can be considered as a capacitive voltage divider of parasitic capacitor of the power components (transistors, diodes) mounted to the heat sink. Assuming the switching transistor transfers 20 V to ground, we receive 25 V (148 dBµV) for the fundamental A1 according to equation 1.

For the subsequent harmonics, CM noise decreases much more strongly compared to DM noise. CM noise rises again for frequencies above 1MHz. To get specifications for the required CM attenuation, a low pass behavior of –40 dBµV / decade (low pass consisting out of coupling capacity and wire inductivity) is assumed. Hence amplitude A9 is expected to be about 1% of the fundamental (0.5 V = 108 dBµV).

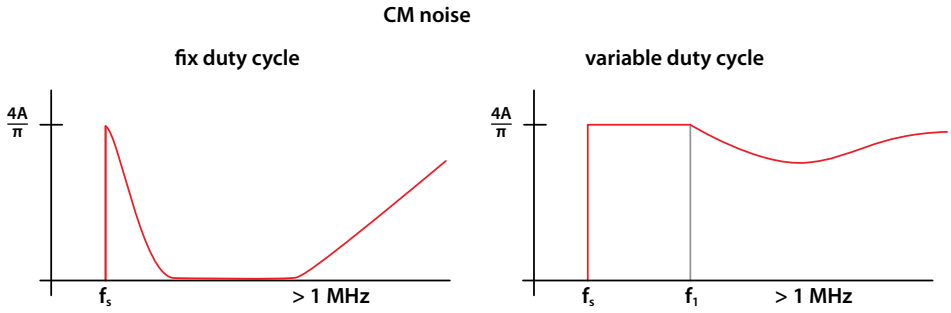

Fig.5: Simplified envelope curves of CM noise

Predicting the CM noise is more difficult, because parasitic couplings and resonances have more impact. Figure 5 shows the possible trend of harmonics. For applications with variable duty cycle, the noise level does not decrease up to f1, similar as with the DM noise. In both cases CM noise levels increase in the higher frequency range.

CM noise also depends more on design details of the power unit. A poor system design can raise the conducted noise level and also cause emissions in the radiated range. CM currents can flow through housing and power cords and use them as antenna to radiate EMI noise. Thus it is important to keep the loop of asymmetric current between the noise source and the EMI filter short.

3. Determine required filter attenuation

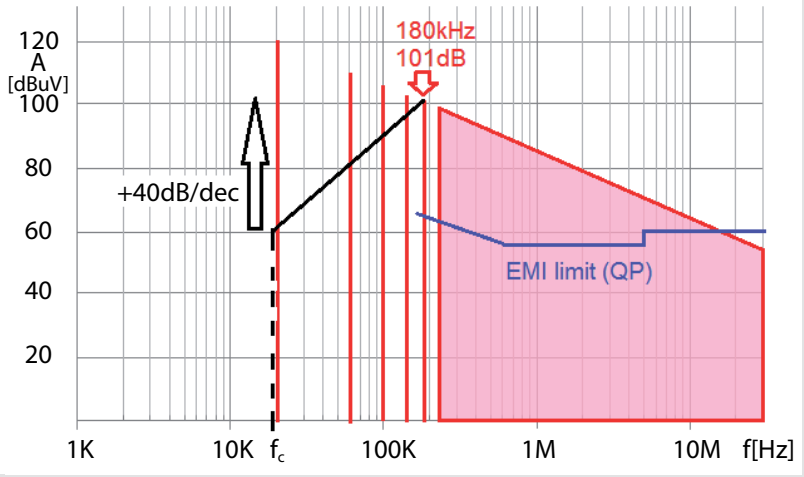

Fig. 6: Principle of EMC/EMI filter design determination

Figure 6 shows the principle to determine the required DM attenuation A. It can be looked at as a subtraction between the DM noise level (red) and the limits (blue). Considering an additional safety margin m to keep the EMI noise below the limits with respect to tolerances in series production, the required attenuation A can be derived from equation 3:

$$A[dBuV] = An - L_{QP} + m$$

An	EMI amplitude of the n^{th} harmonic (first harmonic above 150kHz)
L_{QP}	EMI Quasi Peak limit at the n^{th} harmonic (first harmonic above 150kHz)
m	safety margin (e.g. 3dB)

Equ. 3: Required filter attenuation A

To comply with the QP limit (65 dBµV) of IEC/EN61000-6-3 and to reduce the DM noise of 101 dBµV at 180 kHz, the filter needs a DM attenuation of 39 dBµV with a safety margin of 3 dB.

With the assumed CM noise of 108 dBµV at 180 kHz and a safety margin of 3 dBµV, a CM attenuation of 46 dBµV is required.

4. Specify the filter corner frequency f_c

With the knowledge that the attenuation of a LC-filter starts at the corner frequency and the attenuation is rising with 40 dB per decade, the needed corner frequency can be specified according to equation 4:

$$A[dBuV] = 40 \log\left(\frac{f}{f_c}\right) \Rightarrow f_c = 10^{\frac{-A}{40}} f$$

Equ. 4: Calculation of corner frequency f_C

The relative filter performance trend curve is also displayed in figure 6 (black). Where the start of the trend curve with 40 dB rise is below the EMI limit, is the required corner frequency f_C of the filter. With the required DM attenuation of 39 dBµV, equation 4 delivers a DM corner frequency f_C of 19 kHz.

With a required CM attenuation of 46 dBµV at 180 kHz the CM corner frequency f_C results to 12.7 kHz.

5. Select the RB choke

As our example has a non-sinusoidal current consumption like shown in figure 7, the low inductance version RB6x22-126-1M0 should be preferred. If there is no sufficient attenuation achievable or a low leakage current design is needed, the high inductance version RB8522-16-3M0 can be used, if inrush and line current of the application do not exceed the saturation limits given in table 1.

Designation	convection cooling nominal current I@60 °C [A]	forced cooling 3 m/s nominal current I@60 °C [A]	Nominal Inductance L_N@25 °C [mH/path]	Typical stray Inductance L_S@25 °C [µH/path]	Resistance R@25 °C [mΩ/path]	max. DM peak current 25 °C IDM_{max}@25 °C [A]	max. DM peak current 100 °C IDM_{max}@100 °C [A]	max. CM peak current 25 °C ICM_{max}@25 °C [A]	max. CM peak current 100 °C IDM_{max}@100 °C [A]
RB6122-16-1M0	16	25	1.00	6.3	4.8	135	95	0.24	0.16
RB6122-25-0M6	25	39	0.64	4.0	2.7	160	112	0.31	0.21
RB6122-36-0M5	36	53	0.45	3.6	1.5	185	130	0.41	0.28
RB6122-50-0M3	50	80	0.25	1.8	0.9	270	189	0.58	0.40
RB6522-16-1M0	16	25	1.00	6.2	4.6	135	95	0.24	0.16
RB6522-25-0M6	25	39	0.64	3.9	2.6	160	112	0.31	0.21
RB6522-36-0M5	36	53	0.45	3.6	1.5	185	130	0.41	0.28
RB6522-50-0M3	50	80	0.25	2.0	0.9	270	189	0.58	0.40
RB8522-16-3M0	16	25	3.00	22.2	8.4	73	51	0.17	0.11
RB8522-25-2M0	25	39	2.00	13.6	4.2	126	88	0.27	0.18
RB8522-36-1M5	36	58	1.50	12.8	3.0	165	116	0.40	0.27
RB8522-50-0M8	50	83	0.75	6.5	1.7	225	158	0.55	0.36
RB6132-16-0M8	16	26.5	0.80	5.8	4.6	155	109	0.32	0.22
RB6132-25-0M5	25	41	0.47	3.3	2.4	225	158	0.41	0.28
RB6132-36-0M4	36	60	0.42	2.9	1.4	330	231	0.59	0.39
RB6132-50-0M2	50	81	0.18	1.9	0.9	335	235	0.88	0.59
RB6532-16-0M8	16	26.5	0.80	6.9	4.7	155	109	0.32	0.22
RB6532-25-0M5	25	41	0.47	3.6	2.4	225	158	0.41	0.28
RB6532-36-0M4	36	60	0.42	4.2	1.5	330	231	0.59	0.39
RB6532-50-0M5	50	81	0.18	1.5	0.8	335	235	0.88	0.59
RB8532-16-1M3	16	27	1.30	9.1	5.7	128	90	0.26	0.17
RB8532-25-0M9	25	41	0.94	6.7	3.0	195	137	0.39	0.26
RB8532-36-0M8	36	58	0.83	7.3	2.3	260	182	0.55	0.36
RB8532-50-0M3	50	82	0.33	3.1	1.2	395	277	0.88	0.59

Table 1: RB chokes saturation parameters

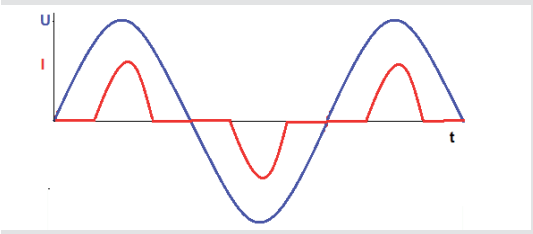

Fig.7: Non-sinusoidal line current

RB6x22-16-1M0 is selected as a preferred solution and RB8522-16-3M0 as an option.

6. Calculate the values of the capacitors

Derived from the common equations to calculate the corner frequency f_C, the required values of C_x and C_y can be calculated according to equation 5:

$$f_{C_{DM}} = \frac{1}{2\pi\sqrt{2 L_S C_X}} \qquad f_{C_{CM}} = \frac{1}{2\pi\sqrt{2 L_N C_Y}}$$

$$C_X = \frac{1}{8\pi^2 L_S f_{C_{DM}}^2} \qquad C_y = \frac{1}{8\pi^2 L_N f_{C_{CM}}^2}$$

Equ. 5: Calculation values for C_x and C_y

Assuming we use the vertical versions of RB chokes, we can get the stray inductivity values L_S out of table 1 and receive L_S = 6.3 µH for RB6522-16-1M0 and LS = 22.2 µH for RB8522-16-3M0.

With equation 5 we receive:

For RB6x22-16-1M0

C_x = 5.6 µF with f_{CDM} = 19 kHz and C_y = 79 nF with f_{CCM} = 12.7 kHz
We select RB6x22-16-1M0 with C_x = 4.7 µF and C_y = 100 nF as preferred filter solution

For RB8x22-16-3M0

C_x = 1.6 µF with f_{CDM} = 19 kHz and C_y = 26 nF with f_{CCM} = 12.7 kHz
We select RB8522-16-1M0 with C_x = 1.5 µF and C_y = 33 nF as optional filter solution.

(Selections are closest values according E6 series)

7. Design note for X- and Y-capacitors

As mentioned, the filter capacitors have to handle the ripple and leakage current.

Y-capacitors have limitations to consider:

- Thermal limit for high frequency switching currents, in particular with power electronics with no galvanic insulation or shielded motor cables
- Leakage current requirements of the application.
- Sufficient dielectric strength to withstand burst, surge, Hi-pot test voltage from active line to ground

For Class I applications Y2 types should be used.

X-capacitors also have limitations to consider:

- Thermal limit with current caused by switching voltage ripple
- Dielectric strength for burst and surge
- Hi-pot test between active lines (if applied)

Thermal tests with the application running under worst case conditions prove that the EMC design works under all conditions.

For Class I applications, X2 types should be used.

8. Check the leakage current limit

As mentioned, the value of C_y can be limited by safety standard requirements. The leakage current caused by the line voltage for this single phase application can be calculated according to equation 6:

$$I_{lk} = 2\pi f_R U_R C_y$$

f_R rated frequency
U_R rated voltage

Equ. 6: Calculating leakage current I_{lk}

With a voltage rating of 250 V, we receive I_{lk} = 2.6 mA for C_y = 33 nF and 7.9 mA for C_y = 100 nF. More details about the calculation can be found in the application note **"Leakage current of power line filters".**

9. Consider to use RB choke evaluation boards for a test set-up

For the fast design-in of RB choke based EMC/EMI filters Schaffner offers various evaluation boards to test and try the filter design before doing the PCB layout:

order description	fits for
EVA-BOARD FOR RB6122 SERIES	all RB6122
EVA-BOARD FOR RB6132-16/25	RB6132-16-0M8 RB6132-25-0M5
EVA-BOARD FOR RB6132-36/50	RB6132-36-0M4 RB6132-50-0M2
EVA-BOARD FOR RB6522 SERIES	all RB6522
EVA-BOARD FOR RB6532 SERIES	all RB6532
EVA-BOARD FOR RB8522 SERIES	all RB8522
EVA-BOARD FOR RB8532 SERIES	all RB8532

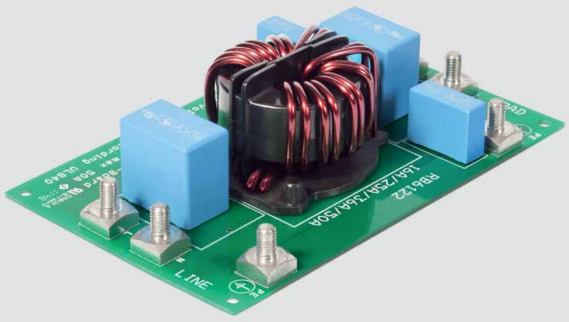

Fig. 8: Evaluation board for RB chokes

10. Designing the filter

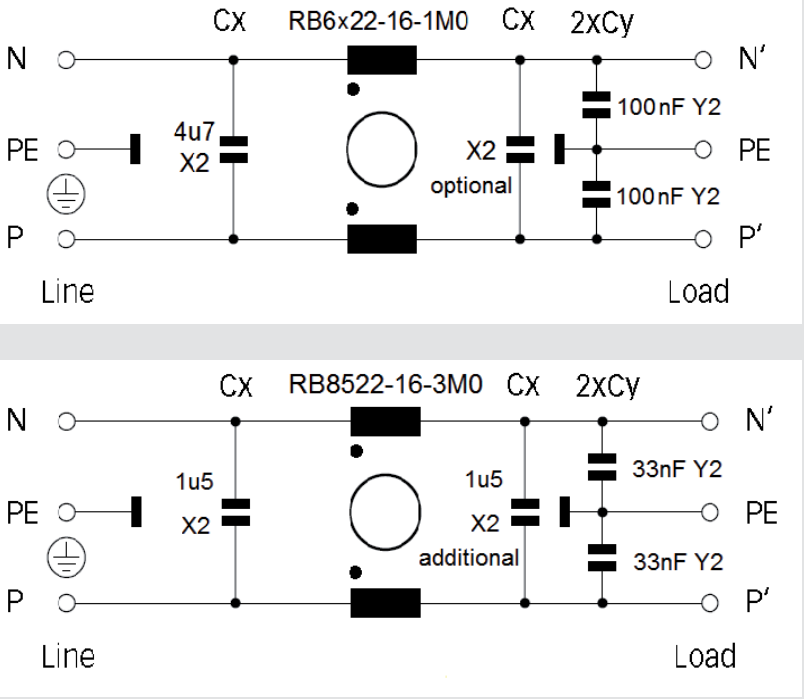

Fig. 9: Schematics of filter design with high and low inductance RB chokes

Figure 9 shows the schematics of the designed filter solutions. If a leakage current of 7.9 mA is not acceptable due to the limit of the applied safety standard (e.g. DIN VDE 0701-0702) the size of the C_y has to be reduced or the high inductance filter solution has to be selected. Additional C_x on the load-side improves the DM attenuation as shown with the CISPR17 measurements in the next section.

11. Verification of the filter attenuation

The first filter design with RB6522-16-1M0 has been assembled according to figure 8 with an RB choke evaluation board, and the attenuation has been tested according CISPR 17 in the Schaffner test lab:

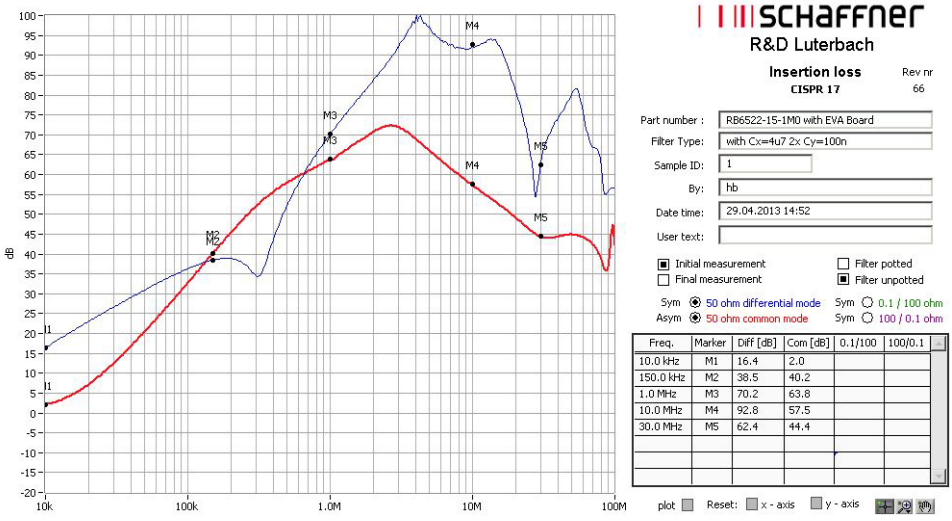

Fig.10: Insertion loss test with RB6522-16-1M0, C_x = 4.7 µF, C_y = 100 nF

Figure 10 shows that the filter design theory is in compliance with the practical evaluation for the 9th harmonics. We receive DM attenuation (blue line) of 39 dBµV. But the impact of other effects (e.g. parasitic elements of the components, inductive coupling between CM choke and line side C_x etc.) can already be seen in the area above 300 kHz, leading to slow-down of expected DM attenuation rise. The measured CM attenuation at 180 kHz is, as expected, about 45 dBµV. From a theoretical scope there are no further filtering components needed to fulfill the attenuation performance of the application example.

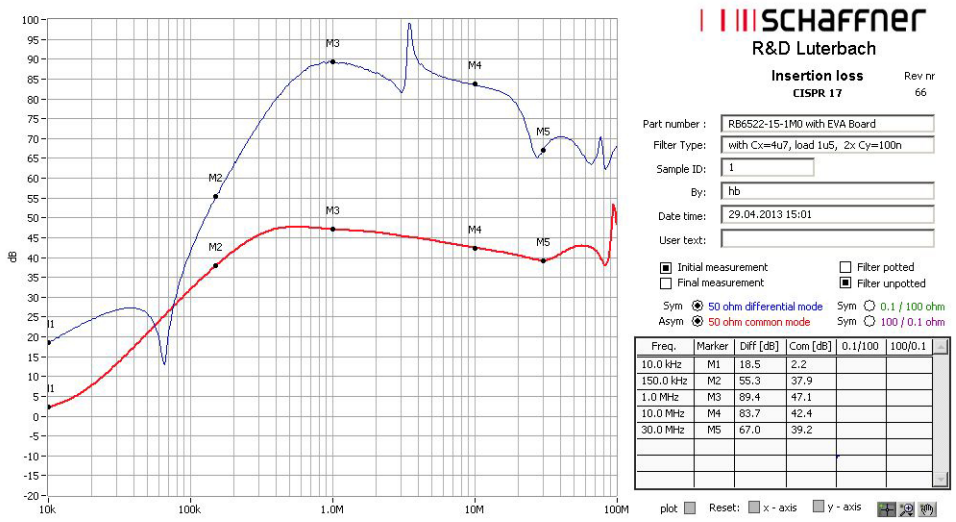

Fig.11: Insertion loss test with RB6522-16-1M0, C_x = 4.7 µF line side, C_x = 1.5 µF load side, C_y = 100 nF

If the DM performance is insufficient for the following harmonics or for applications with variable duty cycle, there is a "quick and dirty" method to boost it up: an additional C_x on the load side can improve DM attenuation like shown in figure 11. In real life the performance is not always so apparent depending on the noise impedance.
To fulfill the leakage current requirement of 3.5mA, a second filter design with RB8522-16-3M0 had been assembled with an evaluation board and also tested according CISPR 17 in the Schaffner test lab:

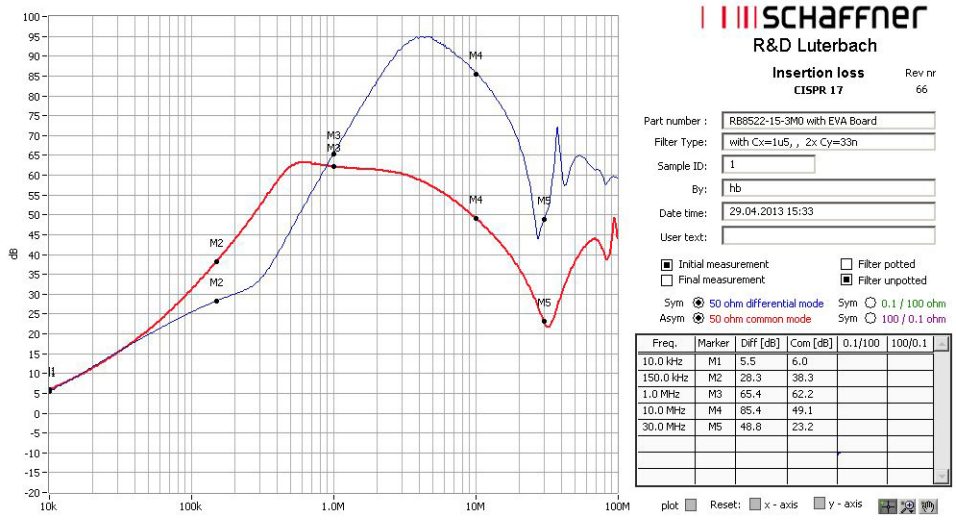

Fig.12: Insertion loss test with RB8522-16-3M0, C_x = 1.5 µF, C_y = 33 nF

Figure 12 shows the result of the CISPR17 test. The projected DM attenuation of 39 dBµV was not achieved (30 dBµV at 180 kHz). As discussed already with the results shown in figure 9, the parasitic impacts of other effects can be seen more pronounced this time. Now an additional C_x on the load side is mandatory to achieve the projected filter performance. The CM attenuation is almost as expected at about 44 dBµV.

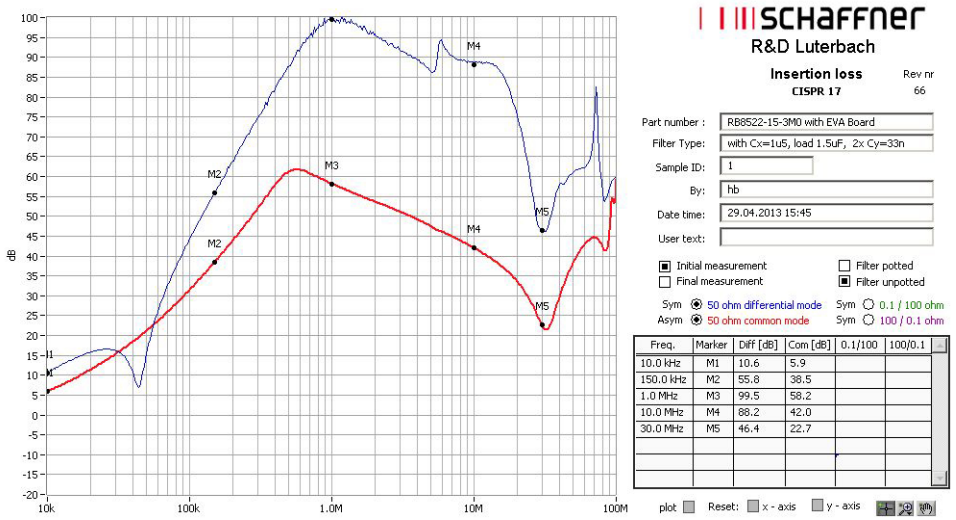

Fig.13: Insertion loss test with RB6522-16-1M0, C_x = 1.5µF, additional C_x = 1.5 µF on line side, C_y = 33 nF

Figure 13 shows the improvement of DM attenuation with a load-side C_x = 1.5 µF. DM attenuation is now about 63 dBµV at 180 kHz. The CM attenuation remained at 44 dBµV at 180 kHz.
Finally, the filter has to be inserted to the test setup and the conducted emissions have to be tested:

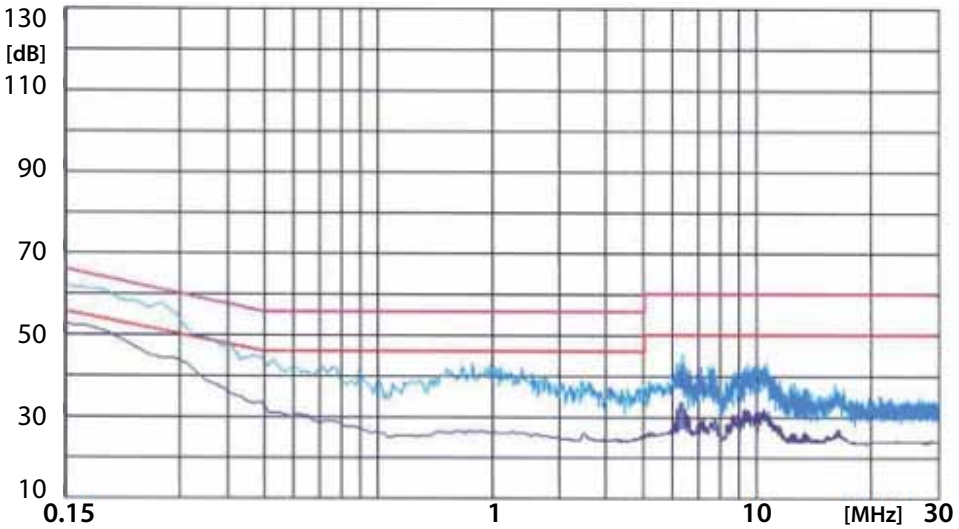

Fig. 14: EMI noise curve complies with the limits of IEC/EN61000-6-3 after filter insertion

The example shows that EMC/EMI filter design can not only be done on theoretical basis, but understanding of the theory is needed to adapt the filter to the individual needs of the application. If you would like to obtain a better understanding, please contact Schaffner EMC

PCB design details

Besides the arrangement recommendation of the components shown with the schematics above, mind the rules of PCB EMC/EMI design:

- Consider the creepage and clearance distances needed in your application.
- Design circuit paths adequate to the maximum current. High current crest factors lead to higher losses. The higher the current density, the higher the possible stray fields.
- Minimize the area in between current flowing backward and forward, otherwise it can operate as a "coil" inducing magnetic fields to other components or as a dipole antenna radiating emissions to the environment.
- For best performance, the power flow of the circuit paths has to go directly to the pins of the X-caps. A restriction of the circuit path forces the HF current flowing to the pins. Consider the thermal impacts of this measure as well.
- Plan a load side C_x if possible, to have the chance to modify DM performance if required.
- Do not intersect filtered and unfiltered paths. Keep the noisy and filtered areas separated in your design, including the wiring. The pin-out of the horizontal 3-wire RB chokes are designed to enable optimum separation (see figure 15)

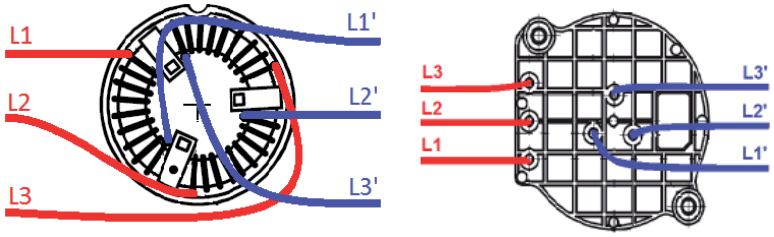

Fig. 15: left side: PCB layout with conventional horizontal 3-wire choke; right side: Layout with RB6132

On the left side figure 15 shows a pin arrangement of conventional horizontal 3-wire chokes, where an EMC-conscious PCB layout is difficult. No broad design of the circuit path is possible and the coupling risk is high due to input output crossing. A lot of chokes also have no extra fixation possibility and the wiring is done directly on coated cores.

The horizontal 3-wire versions of RB chokes have an innovative arrangement of pins to make the PCB layout work easier. This enables sufficient space to design broad circuit paths and a clear separation of filter input and output side. All RB chokes have an outstanding insulation due to the core bobbin design and the efficient choke fixation with two screws prevents against transport and vibration damages.

To support an efficient design-in process of RB chokes for the PCB layout, 3D CAD files (format STEP) and PCB layout files (format EAGLE) are as well available from Schaffner.

Summary

EMC/EMI filter design on PCB level requires a systematic step-by-step approach for achieving the desired results. Often, common-mode choke selection is limited to the comparison of individual parameters like the inductivity, which in many cases is insufficient. By following the recommendations in this application note, and by utilizing the RB choke evaluation boards, the overall design process and time to market can be accelerated. In addition, Schaffner field application engineers are available for individual support.

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