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XDS510 USB
JTAG Emulator

Technical
Reference

XDS510 USB
JTAG Emulator
Installation Guide

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Contents

About This Manual

This document describes the module level operations of the XDS510 USB JTAG Emulator. This emulator is designed to be used with digital signal processors (DSPs) and microcontrollers designed by Texas Instruments.

The XDS510 USB JTAG Emulator is a table top module that attaches to a personal computer or laptop to allow hardware engineers and software programmers to develop applications with DSPs and microcontrollers.

Notational Conventions

This document uses the following conventions.

The XDS510 USB JTAG Emulator will sometimes be referred to as the XDS510 USB, JTAG Emulator, or Emulator.

Program listings, program examples, and interactive displays are shown is a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments Code Composer and Code Composer Studio Users Guide

Chapter 1

Introduction to the XDS510
USB JTAG Emulator

This chapter provides you with a description of the XDS510 USB JTAG Emulator along with the key features.

1.0 Overview of the XDS510 USB JTAG Emulator

The XDS510 USB JTAG Emulator is designed to be used with digital signal processors (DSPs) and microprocessors which operate with +3.3 or +5 volt levels on the JTAG interface This emulator is powered from USB line. This means no power is drawn from the target system.

The XDS510 USB is designed to be compatible with the existing Texas Instruments XDS510 emulator and operate with debuggers provided by Texas Instruments.

1.1 Key Features of the XDS510 USB JTAG Emulator

The XDS510 USB JTAG Emulator has the following features:

- Supports Texas Instrument's Digital Signal Processors (C2xxx, C54xx, C55xx, C67xx, C64xx, TMS470, OMAP) with JTAG interface (IEEE 1149.1)

- Compatible with Texas Instrument's XDS510 emulator.

- Advanced emulation controller provides high performance.

- Compatible with USB 1.x and USB 2.0 (full speed)

- Supports USB interface with host PC, no adapter card required.

- Supports +3.3 volt and +5 volt JTAG interfaces (+3.3V to +1.8V with Low Voltage Adapter).

- One status LED for operational status.

- Power provided by host USB port or USB hub

- Compatible with Texas Instruments Code Composer Studio

- Compatible with Spectrum Digital's Flash programming utility

- Compatible with Windows 98, Windows 2000, and Windows XP Operating Systems

1.2 Key Items on the XDS510 USB JTAG Emulator

Figure 1-1 shows the XDS510 USB. The key items identified are:

- Status LEDs
- JTAG connector
- Tail
- USB connector to the host PC or hub

Figure 1-1, KEY ITEMS ON THE XDS510 USB
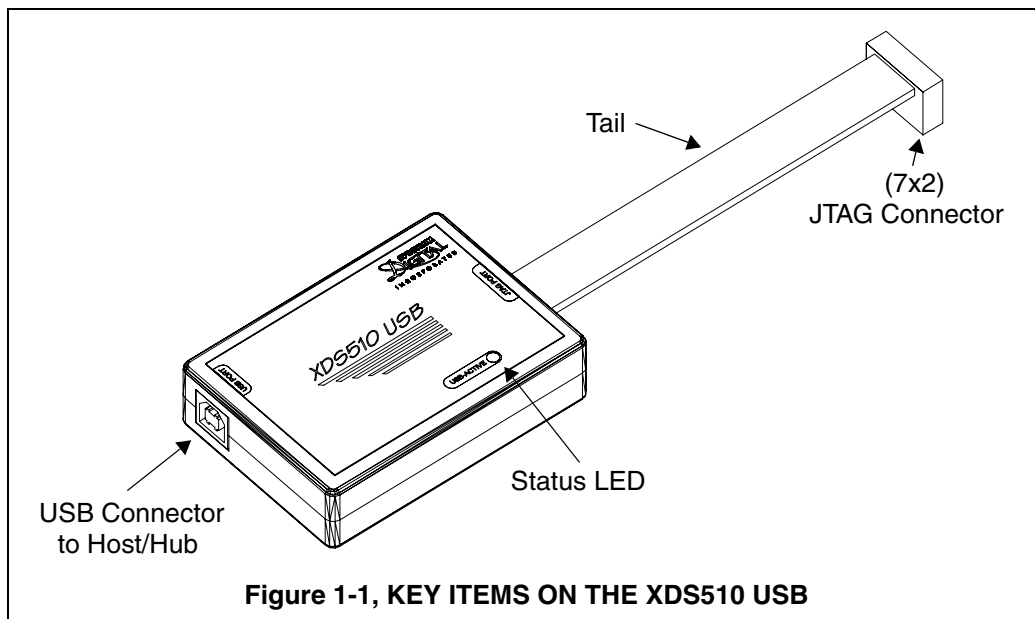
1.3 Support for Low Power DSPs

The XDS510 USB JTAG emulator was designed to interface to target boards with +3.3 or +5 volt I/O levels. However many new DSPs operate at lower I/O voltage levels (e.g. +1.8V). To support operation with the lower voltage devices Spectrum Digital has designed the Low Voltage Adapter, part # 701208. This adapter plugs onto the emulator's 2x7 female connector on one side and the target's 2x7 male connector on the other. This adapter resolves the voltage differences required for correct operation.

Chapter 2 describes the operation of the Low Voltage Adapter with the XDS510 USB.

Chapter 2

Installing the XDS510
USB JTAG Emulator

This chapter helps you install the XDS510 USB JTAG Emulator. For use with specific software packages such as the TI's Code Composer/Studio refer to their respective documentation.

2.1   What You'll Need

The following checklists detail items that are shipped with the XDS510 USB JTAG emulator and additional items you'll need to use these tools.

Hardware checklist

___ **host**   An IBM PC/AT or 100% compatible PC or laptop with a hard-disk system and CD-ROM disk drive with a USB port

___ **memory**   Minimum of 32MB

___ **display**   Color VGA or LCD

___ **emulator module**   XDS510 USB JTAG emulator

___ **target system**   A board with a TI DSP or Microcontroller and power supply

___ **connector to**   14-pin connector (two rows of seven pins) --- see Chapter 3 for
    target system   more information about this connector

Software checklist

___ **operating system** Win 98, Win 2000, Win XP

___ **software tools**   Compiler/assembler/linker for DSP or Microcontroller

___ **debugger**   Code Composer or Code Composer Studio

___ **drivers**   Spectrum Digital drivers for TI Code Composer (included with XDS510 USB emulator or available from Spectrum digital's website)

2.2 Installing the XDS510 USB JTAG Emulator

This section contains the steps for installing the XDS510 USB JTAG Emulator.

WARNING

Target Cable Connectors:

Be very careful with the target cable connectors. connect them gently; don't force them into position, or you may damage the connectors.

Do **not** connect or disconnect the 14-pin cable while the target system is powered up.

### 2.2.1 XDS510 USB Installation Checklist

To install the XDS510 USB JTAG emulator execute the following checklist:

❏ Turn off the power to your target board.

❏ Insert the Spectrum Digital USB Driver CD-ROM in the computers CD-ROM drive and install the device drivers. Code Composer/Studio should be installed already.

❏ Connect the supplied USB cable to your PC or laptop. If you connect the USB cable to a USB hub be sure the hub is connected to the PC or laptop and power is applied to the hub.

❏ Connect the supplied USB cable to your XDS510 USB emulator.

❏ Your system configuration should now look like that in Figure 2-1or Figure 2-2 After a few moments windows will detect new hardware and prompt you with "New Hardware Found" screens. Follow the instructions on the screens and let Windows find the USB driver files "sdusbemu.inf" and sdusbemu.sys" on your CD-ROM drive.

If you want to verify a successful USB driver install, right mouse on Control Panel, then select Properties -> Hardware -> Device Manager. You should see a new class "SD USB Based Debug Tools" and one Spectrum Digital XDS510 USB emulator installed.

❏ Now connect the tail of the emulator to the 2 x 7 header on your target board. Apply power to the target board

Figures 2-1 and 2-2 show two typical configurations in which the XDS510 USB can be used with a host PC and target board.

Figure 2-1, Connecting the XDS510 USB To Your Target System

**Figure 2-2, Connecting the XDS510 USB Through a USB Hub**
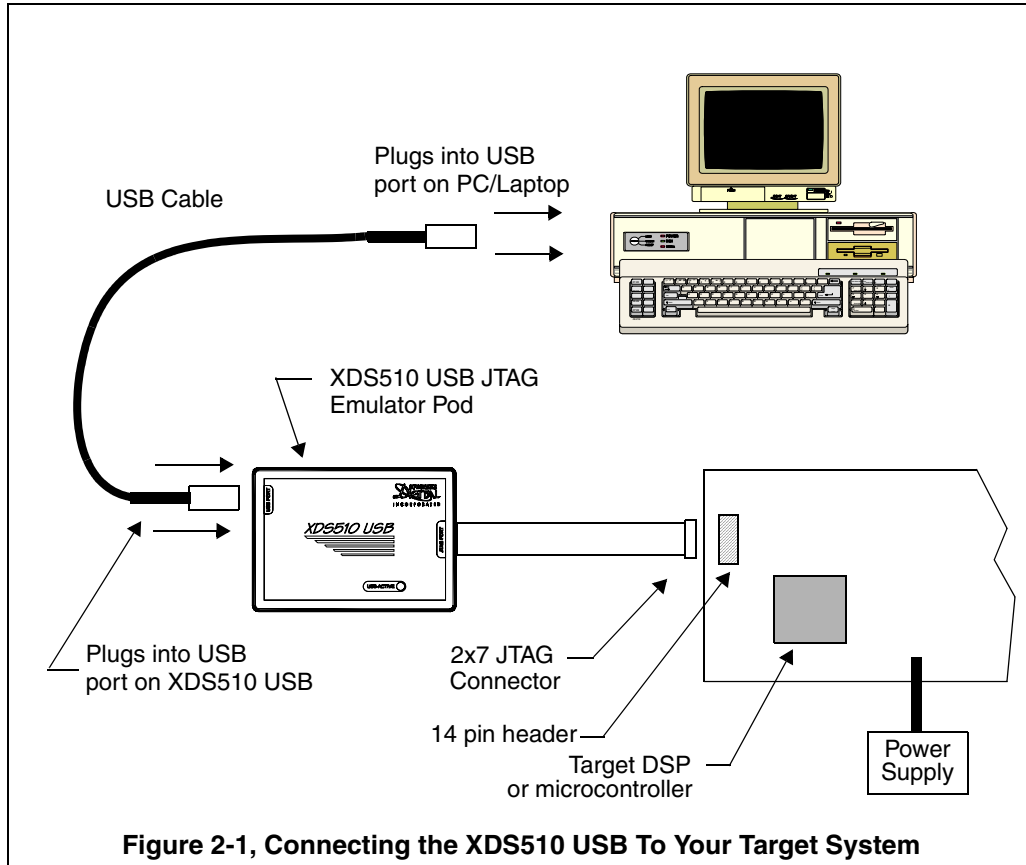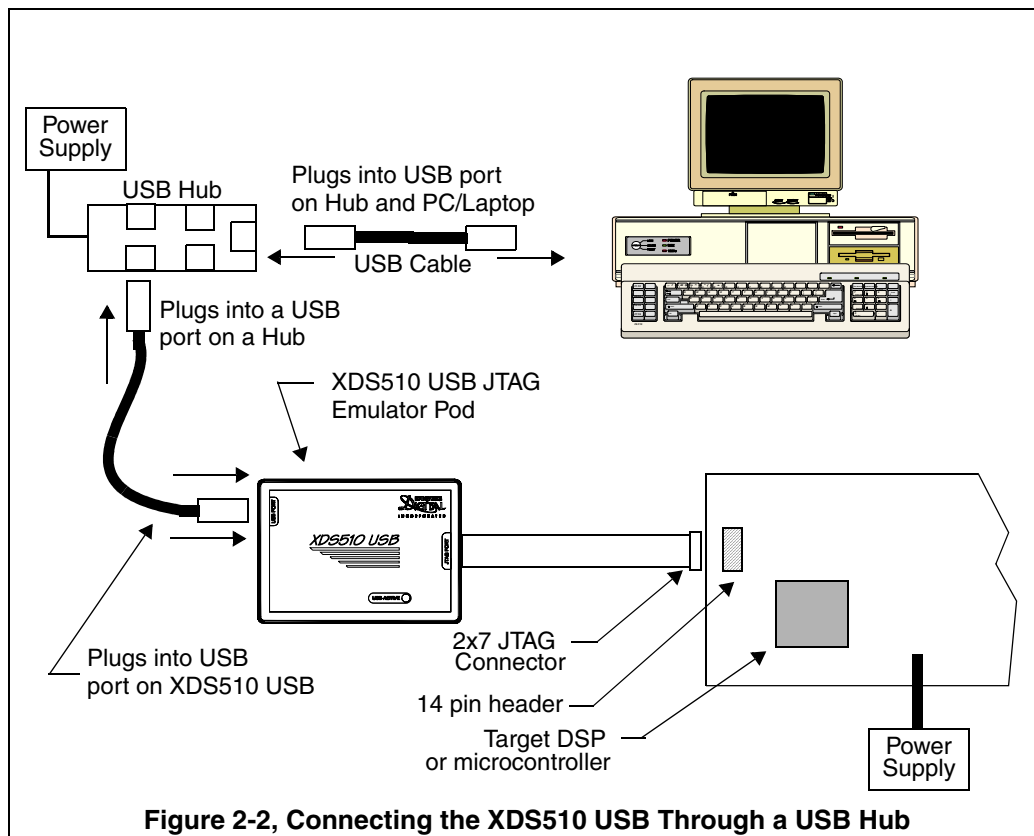
2.3 Using the XDS510 USB with the Low Voltage Adapter

The Low Voltage Adapter, part # 701208, is used with the XDS510 USB JTAG emulator when the I/O voltage on the target DSP is between +2.8V and +1.8V. This adapter resolves the voltage differences required for correct operation.

Additional uses of the Low Votage Adapter are:

> • Signal buffering in noisy target environments
> • Emulator header metal wear protection

This adapter plugs onto the emulator's 2x7 female connector on one side and the target's 2x7 male connector on the other. The figure below shows how the Low Voltage Adapter plugs on to the target board and subsequently how the emulator attaches to the Low Voltage Adapter.

**Figure 2-3, Connecting the XDS510 USB to the
Low Voltage Adapter, and DSP Target Board**
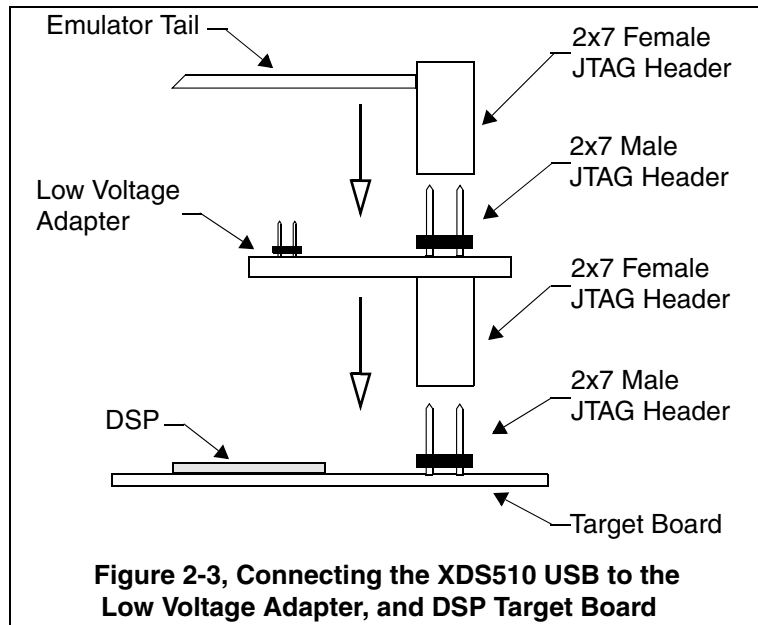
The figure below shows the system configuration using the Low Voltage Adapter with the XDS510 USB JTAG Emulator.

Figure 2-4, Using the Low Voltage Adapter with the XDS510 USB
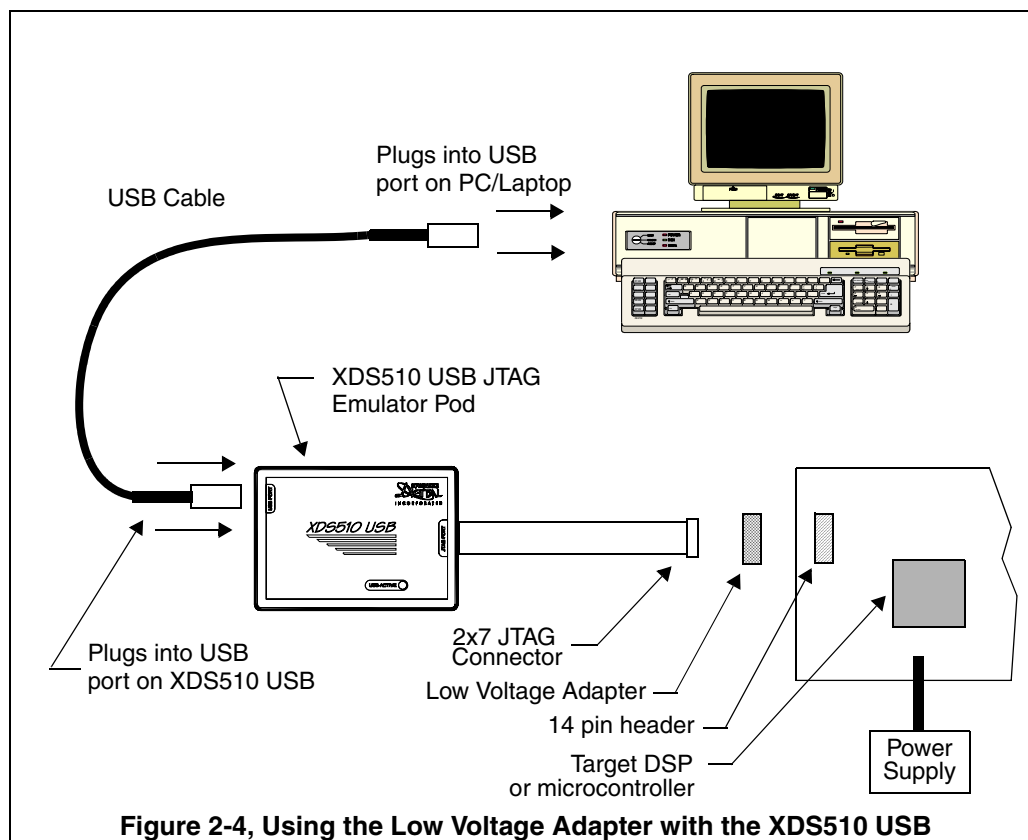
2.4 XDS510 USB LED

The XDS510 USB has one (1) red Light Emitting Diode (LED). This LED provides the user with the status of the emulator. The meaning of the LED is described in the table below.

Table 1: XDS510 USB LEDs

LED Name	Function
USB ACTIVE	Indicates activity over the USB Bus

Chapter 3

Specifications For Your Target System's Connection to the Emulator

This chapter contains information about connecting your target system to the emulator. Your target system must use a special 14-pin connector for proper communication with the emulator.

3.1 Designing Your Target System's Emulator Connector (14-pin Header)

Certain devices support emulation through a dedicated emulation port. This port is a superset of the IEEE 1149.1 (JTAG) standard and is accessed by the emulator. To perform emulation with the emulator, your target system must have a 14-pin header 2 rows of 7 pins) with the connections that are shown in Figure 3-1. Table 1 describes the emulation signals.
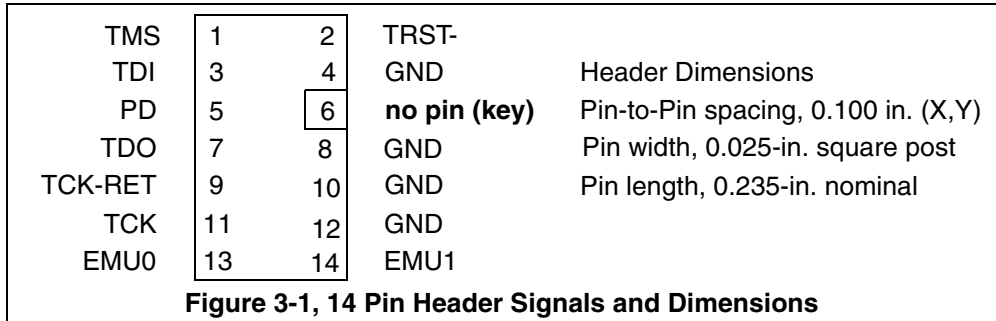
TMS	1	2	TRST-	
TDI	3	4	GND	Header Dimensions
PD	5	6	**no pin (key)**	Pin-to-Pin spacing, 0.100 in. (X,Y)
TDO	7	8	GND	Pin width, 0.025-in. square post
TCK-RET	9	10	GND	Pin length, 0.235-in. nominal
TCK	11	12	GND	
EMU0	13	14	EMU1	

Figure 3-1, 14 Pin Header Signals and Dimensions

Table 1: 14-Pin Header Signal Description

Pin #	Signal	Description	Emulator State	Target State
1	TMS	JTAG test mode select.	Output	Input
3	TDI	JTAG test data input.	Output	Input
7	TDO	JTAG test data output.	Input	Output
11	TCK	JTAG test clock. TCK is a 12-MHz clock source from the emulation pod. This signal can be used to drive the system test clock.	Output	Input
2	TRST-	JTAG test reset.	Output	Input
13	EMU0	Emulation pin 0.	I/O	I/O
14	EMU1	Emulation pin 1.	I/O	I/O
5	PD	Presence detect. Indicates that the emulation cable is connected and that the target is powered up. PD should be tied to the target processor's I/O pins Vcc.	Input	Output
9	TCK_RET	JTAG test clock return. Test clock input to the emulator. May be a buffered or unbuffered version of TCK.	Input	Output

Although you can use other headers, recommended parts include:

straight header, unshrouded   DuPont Connector Systems
                                      part # 67996-114

right-angle header, unshrouded   DuPont Connector Systems
                                      part # 68405-114

3.2 Bus Protocol

The IEEE 1149.1 specification covers the requirements for JTAG bus slave devices (such as the TMS320C5x family) and provides certain rules, summarized as follows:

__ The TMS/TDI inputs are sampled on the rising edge of the TCK signal of the device.

__ The TDO output is clocked from the falling edge of the TCK signal of the device

When JTAG devices are daisy-chained together, the TDO of one device has approximately a half TCK cycle set up to the next device's TDI signal. This type of timing scheme minimizes race conditions that would occur if both TDO and TDI were timed from the same TCK edge. The penalty for this timing scheme is a reduced TCK frequency.

The IEEE 1149.1 specification does not provide rules for JTAG bus master (emulator) devices.

3.3 Emulator Cable Pod Logic

Figure 3-2 shows a portion of the emulator cable pod. These are the functional features of the emulator pod:

___ Signals TMS and TDI are generated from the rising edge of TCK_RET.

___ Signals TMS, TDI, TCK, and TRST- are series-terminated to reduce signal reflections.

___ A 12-MHz test clock source is provided. You may also provide your own test clock for greater flexibility.

Figure 3-2, Emulator Pod Interface
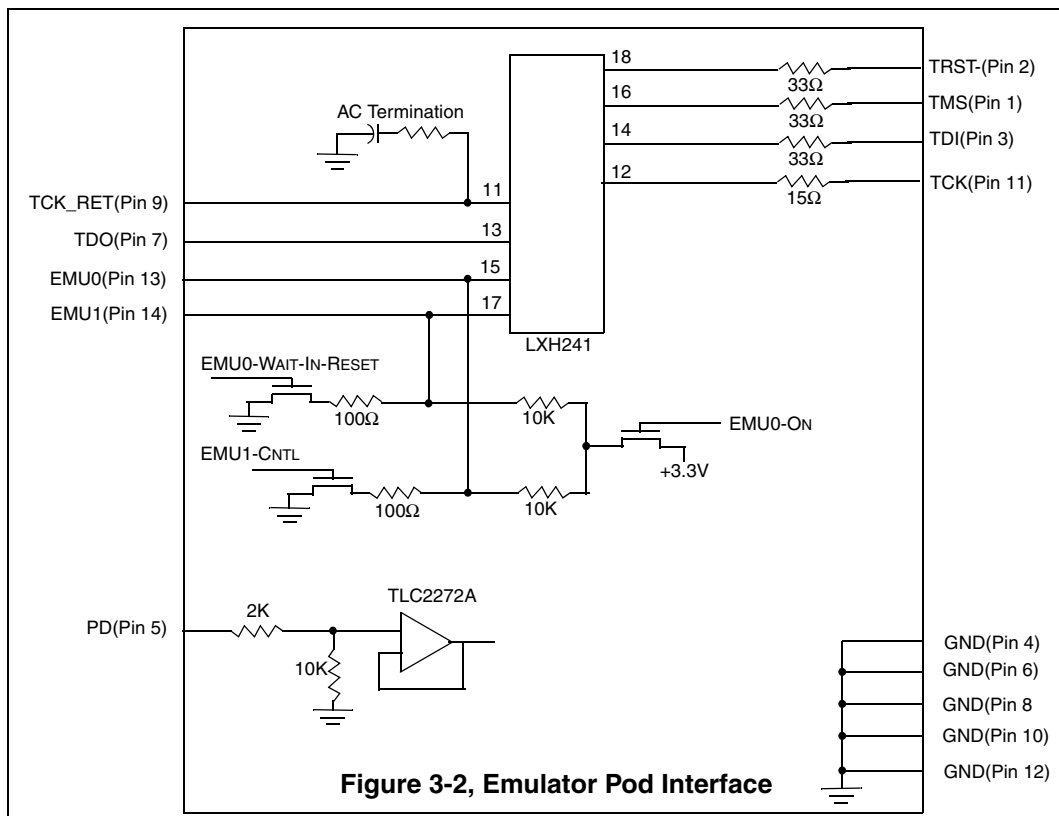
3.4 Emulator Cable Pod Signal Timing

Figure 3-3 shows the signal timings for the emulator. Table 2 defines the timing parameters for the emulator. The timing parameters are calculated from standard data sheet parts used in the emulator and cable pod. These parameters are for reference only. Spectrum Digital does not test or guarantee these timings.
The emulator pod uses TCK_RET as its clock source for internal synchronization. TCK is provided as an optional target system test clock source.
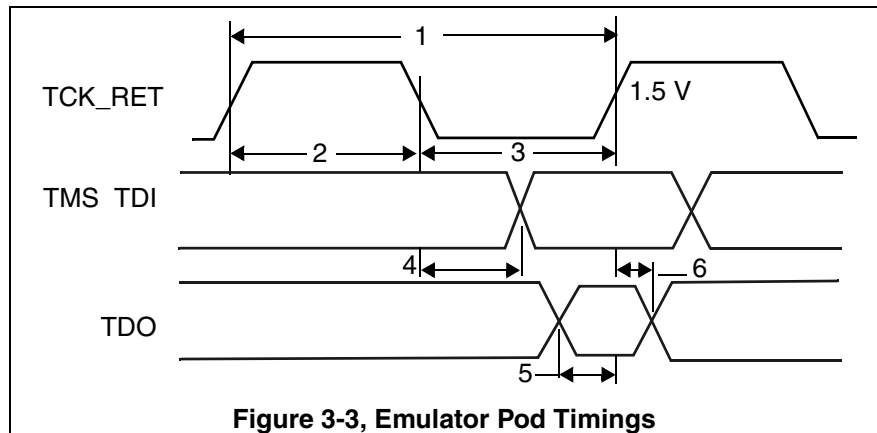

Figure 3-3, Emulator Pod Timings

Table 2: Emulator Pod Timing Parameters

| No	Reference	Description	Min	Max	Units
1	t_{TCKmin}	TCK_RET period	50	10000	ns
2	$t_{TCKhighmin}$	TCK_RET high pulse duration	15		ns
3	$t_{TCKlowmin}$	TCK_RET low pulse duration	15		ns
4	$td_{(XTMX)}$	TMS/TDI valid from TCK_RET low	5	22	ns
5	$tsu_{(XTDOmin)}$	TDO setup time to TCK_RET high	5		ns
6	$thd_{(XTDOmin)}$	TDO hold time from TCK_RET high	5		ns

3.5 Buffering Signals Between the Emulator and the Target System

It is extremely important to provide high-quality signals between the emulator and the target device on the target system. If the distance between the emulation header and the target device is greater than 6 inches, the emulation signals must be buffered. The need for signal buffering and placement of the emulation header can be divided into two categories:

— **No signal buffering.** As shown in figure 3-4, the distance between the header and the target device should be no more than 6 inches.

Figure 3-4, No Signal Buffering
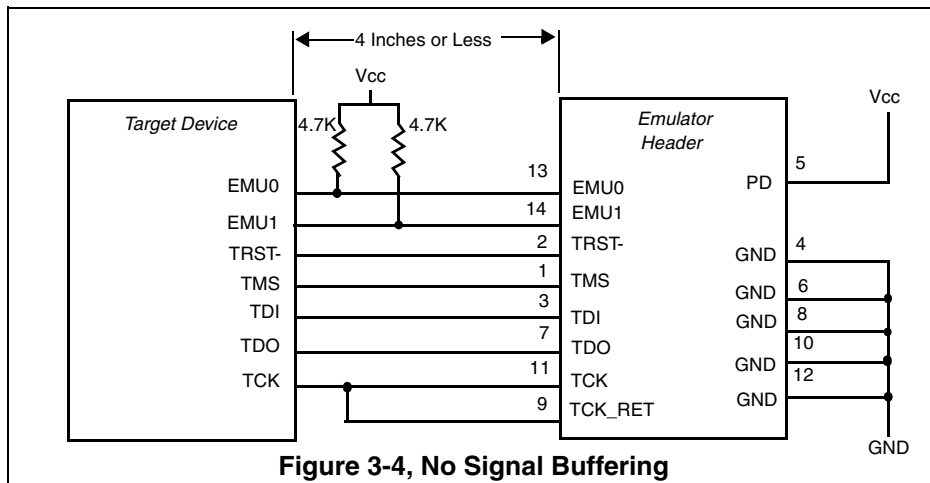
— **Buffered emulation signals.** Figure 3-5 shows the distance between the emulation header and the target device is greater than 6 inches. The target device signals--TMS, TDI, TDO, and TCK_RET are buffered through the same package.

Figure 3-5, Buffered Emulation Signals
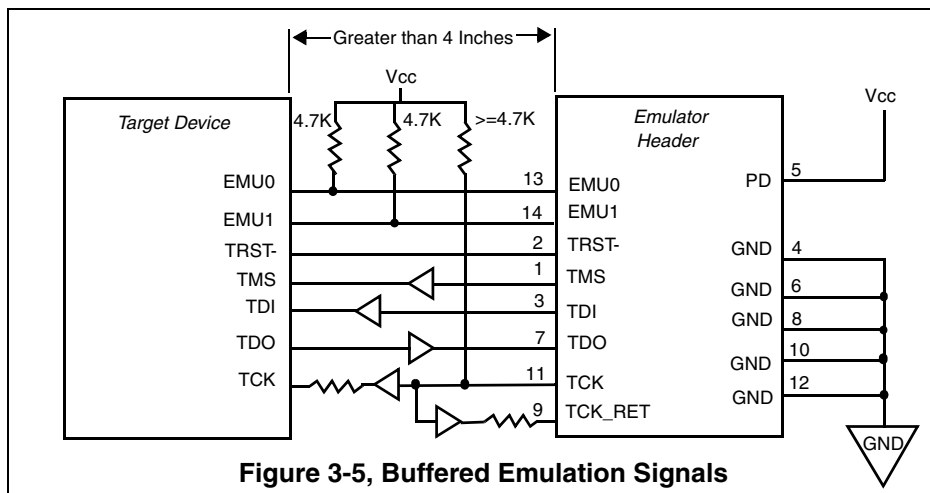
___ The EMU0 and EMU1 signals must have pullups to Vcc. The pullup resistor value should be chosen to provide a signal rise time less than 10 uS. A 4.7k ohm resistor is suggested for most applications. EMU0-1 are I/O pins on the target device, however, they are only inputs to the emulator. In general, these pins are used in multiprocessor systems to provide global run/stop operations.

___ It is extremely important to provide high quality signals, especially on the processor TCK and the emulator TCK_RET signal. In some cases, this may require you to provide special PWB trace routing and to use termination resistors to match the trace impedance. The emulator pod does provide fixed series termination on the TMS, TCK, and TDI signals.

Figure 3-6 shows an application with the system test clock generated in the target system. In this application the TCK signal is left unconnected.
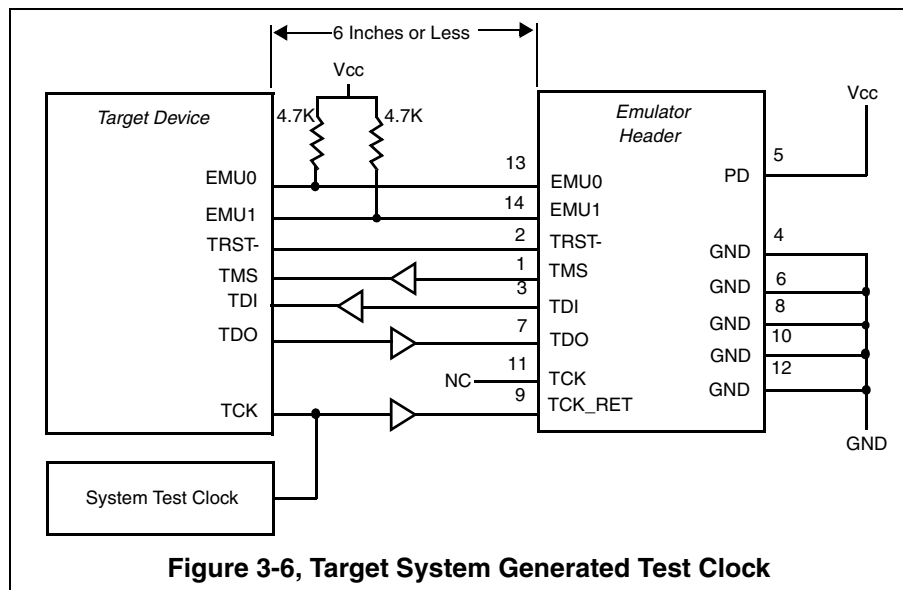

Figure 3-6, Target System Generated Test Clock

There are two benefits to having the target system generate the test clock:

___ The emulator provides only a single 12-MHz test clock. If you generate your own test clock, you can set the frequency to match your system requirements.

___ In some cases, you may have other devices in your system that require a test clock when the emulator is not connected.
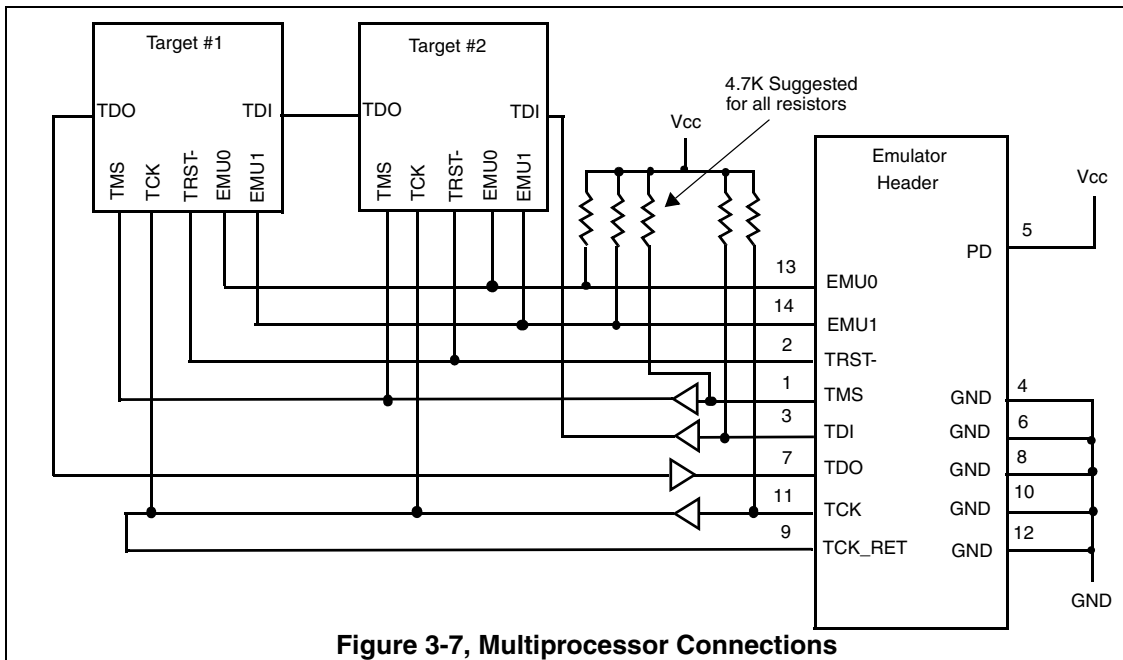
Figure 3-7, Multiprocessor Connections

Figure 3-7 shows a typical multiprocessor configuration. This is a daisy chained configuration (TDO-TDI daisy-chained), which meets the minimum requirements of the IEEE 1149.1 specification. The emulation signals in this example are buffered to isolate the processors from the emulator and provide adequate signal drive for the target system. One of the benefits of a JTAG test interface is that you can generally slow down the test clock to eliminate timing problems. Several key points to multiprocessor support are as follows:

___ The processor TMS, TDI, TDO, and TCK should be buffered through the same physical package to better control timing skew.

___ The input buffers for TMS, TDI, and TCK should have pullups to Vcc. This will hold these signals at a known value when the emulator is not connected. A pull up resistor of 4.7k ohms is suggested.

3.6 Emulation Timing Calculations

The following are a few examples on how to calculate the emulation timings in your system. For actual target timing parameters, see the appropriate device data sheets.

Assumptions:

$t_{su(TTMS)}$	Target TMS/TDI setup to TCK high	5	ns
$t_{h(TTMS)}$	Target TMS/TDI hold from TCK high	5	ns
$t_{d(TTDO)}$	Target TDO delay from TCK low	10	ns
$t_{d(bufmax)}$	Target buffer delay maximum	7	ns
$t_{d(bufmin)}$	Target buffer delay minimum	1	ns
$t_{(bufskew)}$	Target buffer skew between two devices in the same package: $[t_{d(bufmax)} - t_{d(bufmin)}]$ x 0.15	.9	ns
$t_{tckfactor}$	Assume a 40/60 duty cycle clock	0.4	

Given in Table 2:

$t_{d(XTMSmax)}$	Emulator TMS/TDI delay from TCK_RET high, max	22	ns
$t_{su(XTDOmin)}$	TDO setup time to emulator TCK_RET high	5	ns

There are two key timing paths to consider in the emulation design:

__   the TCK_RET/TDI(t_{prdtck_TMS}) path, and
__   the TCK_RET/TDO(t_{prdtck_TDO}) path.

In each case, the worst case path delay is calculated to determine the maximum system test clock frequency.

Case 1:   Single processor, direct connection, TMS/TDI timed from TCK_RET.

t_{prdtck_TMS} $= (t_{d(XTMSmax)} + t_{su(TTMS)})\ ^{*}\ 2$
                      $= (22ns + 5ns) * 2$
                      $= 54ns\ (18.5\ MHz)$

t_{prdtck_TDO} $= [t_{d(TTDO)} + t_{su(XTDOmin)}]\,/\,t_{tckfactor}$
                      $= (10ns + 5ns)\,/\,0.4$
                      $= 37.5ns\ (26.6\ MHz)$

In this case, the TCK/TMS-TDI path is the limiting factor.

Case 2:   Single/multiple processor, TMS/TDI buffered input; TCK_RET/TDO buffered output, TMS/TDI timed from TCK_RET.
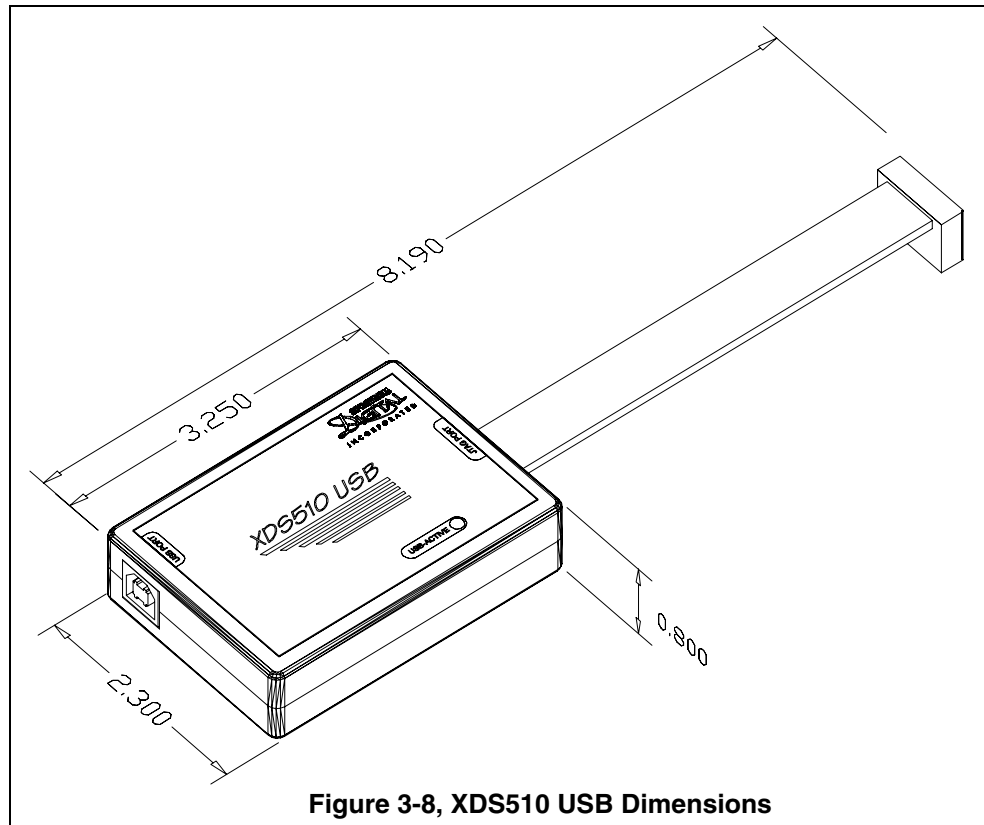
t_{prdtck_TMS} $= (t_{d(XTMSmax)} + t_{su(TTMS)} + 2t_{d(bufmax)})\ ^{*}\ 2$
                      $= (22ns + 5ns + 2(7ns)) * 2$
                      $= 82ns\ (12.2\ MHz)$

t_{prdtck_TDO} $= (t_{d(TTDO)} + t_{su(XTDOmin)} + t_{bufskew})\,/\,t_{tckfactor}$
                      $= (10ns + 5ns + 0.9\ ns)\,/\,0.4$
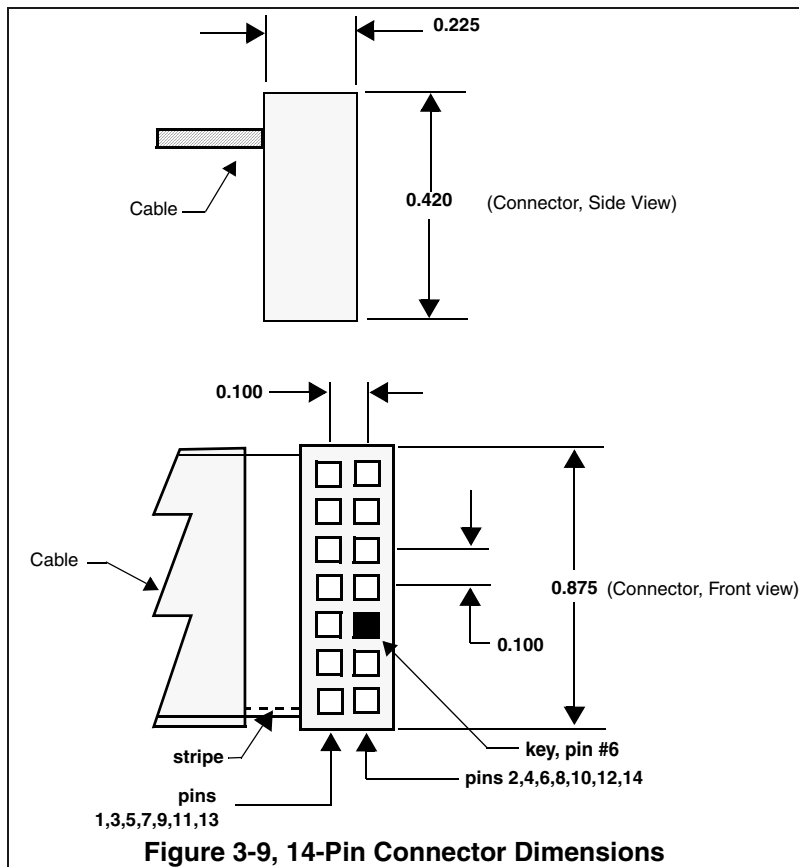 $= 39.8ns\ (25.1\ MHz)$

In this case, the TCK/TMS-TDI path is the limiting factor.

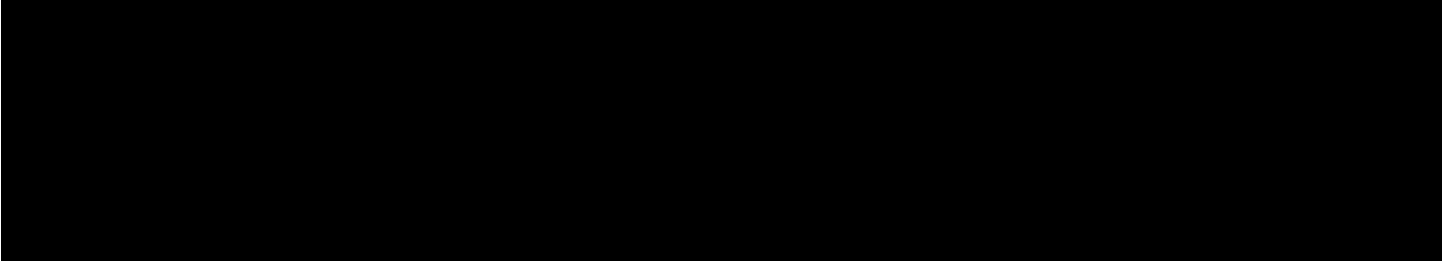### 3.7 Mechanical Dimensions of the XDS510 USB JTAG Emulator

The XDS510 USB JTAG Emulator consists of a 6-foot USB cable, the **XDS510 USB** emulator pod, and a short section of cable (tail) that connects to the target system. The overall cable length is approximately 6 feet, 10 inches. Figure 3-8 and Figure 3-9 (page 3-12) show the mechanical dimensions for the **XDS510 USB** emulator pod and short cable. Note that the pin-to-pin spacing on the connector is 0.100 inches in both the X and Y planes. The **XDS510 USB** JTAG emulator enclosure is nonconductive plastic with one recessed metal screw.

Figure 3-8, XDS510 USB Dimensions

Note: All dimensions are in inches and are nominal dimensions, unless otherwise specified.

Figure 3-9, 14-Pin Connector Dimensions

Note: All dimensions are in inches and are nominal dimensions, unless otherwise specified.