TB3283

Using the Universal Timer (UTMR) Module as Legacy PIC16/PIC18 Timers

Introduction

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The Universal Timer (UTMR) module is a timer module introduced in the newer PIC® devices, which combines most of the operations of all the legacy timers (TMR0/1/2, SMT, CCP) into one single timer. The inbuilt capture and compare features along with customizable Start, Reset, and Stop options make the UTMR universal. Additionally, multiple UTMR modules can be chained together to form a larger size timer.

This document shows how to configure the UTMR to operate in different modes available in legacy timer peripherals (TMR0, TMR1, TMR2, SMT, CCP). In the cases where a mode in the legacy timer is not supported, suggestions are given about combining the UTMR with other peripherals to perform those functions. Features new to UTMR that are not supported in the legacy timers are beyond the scope of this document. Refer to the device specific data sheet or TB3264 for more information.

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1. Commonly Used UTMR Settings

As a reference, the following table describes the selections for the most commonly used settings for the UTMR configuration used throughout this document. Refer to the device specific data sheet or TB3264 for more information.

Table 1-1. Commonly Used UTMR Settings

UTMR Bit Setting	Description	Possible Selections
START	Start condition of the timer	00 = None (ON = 1) 01 = Either ERS Edge 10 = Rising ERS Edge 11 = ERS Level - 1
RESET	Reset condition of the timer	00 = None 01 = ERS Level - 0 + PR Match 10 = at Start + PR Match 11 = at PR Match
STOP	Stop condition of the timer	00 = None 01 = Either ERS Edge 10 = Rising ERS Edge 11 = at PR Match
CPOL	Clock polarity – selects the active clock edge	0 = Falling Clock Edge (default) 1 = Rising Clock Edge
EPOL	ERS polarity – inverts the polarity of ERS signals	0 = True ERS Levels (default) 1 = Inverted ERS Levels
OSEN	One-shot mode enable – stops the timer and then disables it (ON = 0)	0 = Disabled (default) 1 = Enabled
LIMIT	Limit mode enable - prevents the counter from exceeding the PR value	0 = Disabled (default) 1 = Enabled
CAPT	Capture command bit – captures the current counter value in the capture register	0 = Capture is complete (or not started) 1 = Counter value capture in progress
CLR	Clear command bit – clears the counter and prescaler counter values	0 = Clearing is complete (or not started) 1 = Counter/Prescaler counter value clear in progress
OM	Output mode – chooses the type of output	0 = Pulse Output (default) 1 = Level Output
OPOL	Output polarity – chooses the polarity of the output	0 = Low output when idle (default) 1 = High output when idle

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UTMR Bit Setting	**Description**	**Possible Selections**
CSYNC	Clock synchronization – synchronizes ERS and other input/output signals and commands to timer clock	0 = Disabled/Async 1 = Enabled/Sync (default)
TUCHAIN	Chains two UTMR instances to form a bigger timer	Refer to device specific data sheet

1.1 UTMR Size and Buffered Access

UTMR is available in different sizes: 8, 16, 24, and 32-bit. The exact size configuration is specific to the device; refer to the device data sheet for more information. Regardless of the timer size, the TUxyTMR timer/counter register is not guarded for atomic access. However, the TUxyPR period register is double-buffered.

The raw TUxyTMR timer/counter register is not double-buffered and no read/write protection is offered in hardware. The user is encouraged to access or alter the timer value only using the capture and period registers described below. The raw counter may be directly accessed, but the access is not double-buffered and may corrupt the data if the operation is performed with a running timer.

To read the timer value, use CAPT command to capture the current counter value in TUxyCR capture register. To clear the raw timer register, use CLR command. Synchronization delay may apply while using CAPT and CLR commands based on CSYNC bit setting.

The TUxyPR period register is double-buffered and hardware protection is offered to alter the value of the register while the timer is running. To change the period of the timer, it is recommended to update the TUxyPR register, rather than to change the counter value. Refer to device data sheet on more details about updating period for a running timer.

Important: The size of UTMR is specific to the device. To increase the size of the UTMR, two timer instances can be chained using TUCHAIN register. Refer to device data sheet for specific details.

2. Using UTMR as Timer0 (TMR0)

TMR0 is a basic timer module that can operate in either 8-bit or 16-bit mode. In 8-bit mode, the value in TMR0L register is compared to the value in TMR0H register. When the two values match, TMR0L is reset and timer output toggles. In 16-bit mode, TMR0H:L together forms a 16-bit counter. The timer output toggles when the timer rolls over. The following table shows the UTMR settings needed to operate in different TMR0 modes:

Table 2-1. UTMR Settings for Different TMR0 Modes

TMR0 Mode	UTMR Settings		
	START	RESET	STOP
8-bit	None (ON = 1)	At PR Match	None
16-bit		None	

2.1 Other TMR0 Features

The following table shows how some of the other features of TMR0 can be applied using UTMR:

Table 2-2. Features comparison between TMR0 and UTMR

Feature	TMR0	UTMR
Active Clock Edge	TMR0 increments at every rising edge of clock.	Set CPOL = Rising Clock Edge to increment UTMR at rising clock edges.
Synchronization	TMR0 can operate either synchronous or asynchronous to instruction clock (F_{osc}/4) based on ASYNC bit setting.	UTMR always operates asynchronous to the system clock. The CSYNC bit is used to synchronize signals and commands going in and out of the UTMR module.
Buffered Read/ Write	Buffered read and write is available in 16-bit mode.	The TUxyTMR timer/counter register is not guarded for atomic access. However, the TUxyPR period register is double-buffered. Refer to section 1.1 UTMR Size and Buffered Access for details on UTMR buffered access to registers.
Prescaler	TMR0 has 16 programmable input prescaler options ranging from 1:1 to 1:32768, which can be selected using CKPS bits.	UTMR has 256 programmable clock prescaler options ranging from 1:1 to 1:256, which can be selected using TUxyPS register.
Postscaler	TMR0 has a programmable postscaler ranging from 1:1 to 1:16, which can be selected using OUTPS bits.	UTMR does not has any postscaler because the module is not supposed to be used as a time base for PWM.
Output	TMR0 output toggles on every match between TMR0L and TMR0H in 8-bit mode, or when TMR0H:TMR0L rolls over in 16-bit mode. If the output postscaler is used, the output is scaled by the ratio selected.	Use OM = Pulse output to pulse the output at every PR match for one timer clock period. To pulse the output at timer overflow (for 16-bit TMR0 mode), set TUxyPR to the maximum value. Toggle output feature is not available in UTMR.
Interrupt	TMR0IF interrupt occurs every time TMR0 output toggles.	ZIF zero interrupt can be used to identify when the timer resets or rolls-over to zero. Alternatively, PRIF period interrupt can be used to identify a PR match (as in 8-bit TMR0 mode) and a roll-over (as in 16-bit TMR0 mode) when TUxyPR is set to the maximum value.

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Feature	TMR0	UTMR
Sleep Mode Operation	TMR0 halts when operating synchronously. In Asynchronous mode, TMR0 continues operating as long as the clock is active, and wakes up the CPU if interrupts are enabled.	UTMR continues to operate as long as the clock is active, and wakes up the CPU if interrupts are enabled.

3. Using UTMR as Timer 1 (TMR1) with Gate Control

TMR1 is a 16-bit timer which adds gate control features to the timer functionality. To implement the same gate control features in UTMR, the ERS signal acts as the gate. The Start and Stop conditions are tied to specific ERS events which signify the gate start and completion events, respectively. At every gate completion event (Stop condition), the current timer value is captured into the TUxyCR capture register and CIF capture interrupt occurs. The following table shows UTMR settings in different TMR1 modes:

Table 3-1. UTMR Settings for Different TMR1 Modes

TMR1 Mode	UTMR Settings				Comments
	START	RESET	STOP	Other	
GE - Gate Enable	Rising ERS Edge	None	Either ERS Edge	—	—
GPOL - Gate Polarity	Rising ERS Edge	None	Either ERS Edge	EPOL = Inverted	—
GTM - Gate Toggle Mode	Rising ERS Edge	None	Rising ERS Edge	—	The CLC or NCO is used as a 1:2 frequency divider, which feeds into UTMR as ERS source.
GSPM - Gate Single Pulse Mode	Rising ERS Edge	None	Either ERS Edge	OSEN = Enabled	—
GSPM + GTM	Rising ERS Edge	None	Rising ERS Edge	OSEN = Enabled	—

3.1 Other TMR1 Features

The following table shows how some of the other features of TMR1 can be applied using UTMR:

Table 3-2. Features comparison between TMR1 and UTMR

Feature	TMR1	UTMR
Active Clock Edge	TMR1 increments at every rising edge of clock. In some cases, a falling edge must be registered before the timer starts incrementing.	Set CPOL = Rising Clock Edge to increment UTMR at rising clock edges.
Synchronization	TMR1 can operate either synchronous or asynchronous to the system clock based on SYNC bit setting.	UTMR always operates asynchronous to the system clock. The CSYNC bit is used to synchronize signals and commands going in and out of the UTMR module.
Buffered Read/ Write	RD16 bit can be used to read/write 16-bits of TMRxH:L register in one atomic operation.	The TUxyTMR timer/counter register is not guarded for atomic access. However, the TUxyPR period register is double-buffered. Refer to section 1.1 UTMR Size and Buffered Access for details on UTMR buffered access to registers.
Prescaler	TMR1 has 4 programmable input prescaler options ranging from 1:1 to 1:8, which can be selected using CKPS bits.	UTMR has 256 programmable clock prescaler options ranging from 1:1 to 1:256, which can be selected using TUxyPS register.
Gate Source and Polarity	The gate source is selected using GSS bits and the polarity of the gate source is selected using GPOL bit.	The ERS signal acts as the gate source and can be selected using TUxyERS register. The ERS polarity can be selected using EPOL bit.

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Feature	TMR1	UTMR
Gate Value Status	The most current value of gate level can be read using GVAL bit.	Use OM = Level output to represent the current run/stop state of UTMR, i.e. when the gate is activated and when it is not active. This is also represented using the RUN status bit.
Output	TMR1 output pulses every roll-over for one instruction clock.	Set TUxyPR to the maximum value and set OM = Pulse Output mode. This will cause a pulse for one timer clock period when the timer rolls over.
Interrupts	The TMRxGIF gate event interrupt occurs at the completion of a gate event. The TMRxIF timer interrupt occurs when the counter rolls-over to zero.	CIF capture interrupt can be used to signify completion of a gate event. ZIF zero interrupt can be used to signify a counter roll-over.
Sleep Mode Operation	TMR1 halts when operating synchronously. In asynchronous mode, TMR1 continues operating as long as the clock is active, and wakes up the CPU if interrupts are enabled.	UTMR continues to operate as long as the clock is active, and wakes up the CPU if interrupts are enabled.

4. Using UTMR as Timer2 (TMR2) with Hardware Limit Timer (HLT)

TMR2 is an 8-bit timer with separate counter and period registers. It has Hardware Limit Timer (HLT) capabilities based on an External Reset Source (ERS) input. TMR2 can operate in three different modes:

- Free-Running Period mode
- One-Shot mode
- Monostable mode

The following sections describe how the UTMR can be used as a TMR2 in each of the three modes.

4.1 Free-Running Period Mode

In the Free-Running Period mode of TMR2, the value of the T2TMR timer register is compared to the T2PR period register on each clock cycle. Upon a period match, the T2TMR timer register is reset in the next clock cycle, and continues counting. The UTMR operates in a similar way: the TUxyTMR timer/counter register is compared to the TUxyPR period register on each timer clock cycle. The RESET bits can be set to reset the counter upon a period register match (PR match). The following table shows UTMR settings in different TMR2 Free-Running Period modes:

Table 4-1. UTMR Settings for Different TMR2 Free-Running Period Modes

TMR2 MODE[4:0]	TMR2 Mode					UTMR Settings				Comments
	Output	Operation	Start	Reset	Stop	START	RESET	STOP	Other	
00000	Period Pulse	Software gate	ON = 1	—	ON = 0	None (ON = 1)	At PR Match	None	—	—
00001		Hardware gate, active-high	ON = 1 (and) ERS = 1	—	ON = 0 (or) ERS = 0	ERS Level - 1		Either ERS Edge	—	—
00010		Hardware gate, active-low	ON = 1 (and) ERS = 0	—	ON = 0 (or) ERS = 1				EPOL = Inverted	—

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TMR2 MODE[4:0]	TMR2 Mode					UTMR Settings				Comments
	Output	Operation	Start	Reset	Stop	START	RESET	STOP	Other	
00011	Period Pulse with Hardware Reset	Rising or falling edge Reset	ON = 1	Either ERS Edge	ON = 0	Either ERS Edge	At Start + PR Match	None	—	UTMR requires an edge to start for the very first time.
00100		Rising edge Reset		Rising ERS Edge		Rising ERS Edge			—	
00101		Falling edge Reset		Falling ERS Edge					EPOL = Inverted	
00110		Low level Reset		ERS = 0	ON = 0 (or) ERS = 0	None (ON = 1)	ERS Level - 0 + PR Match	None	—	—
00111		High level Reset		ERS = 1	ON = 0 (or) ERS = 1				EPOL = Inverted	—

4.2 One-Shot Mode

In TMR2, the One-Shot mode is identical to the Free-Running Period mode except that the ON bit is cleared and the timer is stopped when T2TMR matches T2PR and will not restart until the ON bit is cycled off and on. This can easily be achieved in UTMR using the One-Shot Enable (OSEN) bit. The following table shows UTMR settings in different TMR2 One-Shot modes:

Table 4-2. UTMR Settings for Different TMR2 One-Shot Modes

TMR2	TMR2 Mode					UTMR Settings			
MODE[4:0]	Output	Operation	Start	Reset	Stop	START	RESET	STOP	Other
01000	One-shot	Software start	ON = 1	—	ON = 0 (or) Next clock after PR match	None (ON = 1)	At PR Match	At PR Match	OSEN = Enabled
01001	Edge-Triggered Start	Rising edge start	ON = 1 (and) Rising ERS Edge	—		Rising ERS Edge			
01010		Falling edge start	ON = 1 (and) Falling ERS Edge	—					OSEN = Enabled (and) EPOL = Inverted
01011		Any edge start	ON = 1 (and) Either ERS Edge	—		Either ERS Edge		At PR Match	OSEN = Enabled
01100	Edge-Triggered Start and Hardware Reset	Rising edge start and Rising edge Reset	ON = 1 (and) Rising ERS Edge	ERS = Rising ERS Edge	ON = 0 (or) Next clock after PR match	Rising ERS Edge	At Start + PR Match	At PR Match	OSEN = Enabled
01101		Falling edge start and Falling edge Reset	ON = 1 (and) Falling ERS Edge	ERS = Falling ERS Edge				At PR Match	OSEN = Enabled (and) EPOL = Inverted
01110		Rising edge start and Low-level Reset	ON = 1 (and) Rising ERS Edge	ERS = 0			ERS Level - 0 + PR Match		OSEN = Enabled
01111		Falling edge start and High-level Reset	ON = 1 (and) Falling ERS Edge	ERS = 1					OSEN = Enabled (and) EPOL = Inverted

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TMR2 MODE[4:0]	TMR2 Mode					UTMR Settings			
	Output	Operation	Start	Reset	Stop	START	RESET	STOP	Other
10110	Level Triggered Start and Hardware Reset	High-level start and Low-level Reset	ON = 1	ERS = 0	ON = 0 (or) Next clock after PR match (or) Held in Reset	ERS Level - 1	ERS Level - 0 + PR Match	At PR Match	OSEN = Enabled
10111		Low-level start and High-level Reset	ON = 1	ERS = 1					OSEN = Enabled (and) EPOL = Inverted

4.3 Monostable Mode

In TMR2, Monostable modes are similar to One-Shot modes except that the ON bit is not cleared and the timer can be restarted by an external Reset event. This can be achieved in UTMR by stopping the counter at every PR match. The following table shows UTMR settings in different TMR2 Monostable modes:

Table 4-3. UTMR Settings for Different TMR2 Monostable Modes

TMR2 MODE[4:0]	TMR2 Mode					UTMR Settings			
	Output	Operation	Start	Reset	Stop	START	RESET	STOP	Other
10001	Edge-Triggered Start	Rising edge start	ON = 1 (and) Rising ERS Edge	—	ON = 0 (or) Next clock after PR match	Rising ERS Edge	At PR Match	At PR Match	—
10010		Falling edge start	ON = 1 (and) Falling ERS Edge	—					EPOL = Inverted
10011		Any edge start	ON = 1 (and) Either ERS Edge	—		Either ERS Edge			—

4.4 Other TMR2 Features

The following table shows how some of the other features of TMR2 can be applied using UTMR:

Table 4-4. Features Comparison between TMR2 and UTMR

Feature	TMR2	UTMR
Active Clock Edge	TMR2 increments at every rising edge of clock by default. The CPOL bit can use used to change the active clock edge.	Use CPOL bit to select the active clock edge. By default, CPOL = Falling Clock Edge.

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Feature	TMR2	UTMR
Synchronization	The prescaler output can be synchronized to Fosc/4 by setting the PSYNC bit. The ON bit can be synchronized to Fosc/4 by setting the CSYNC bit.	Synchronizing prescaler output is not required for UTMR because the timer is completely asynchronous to the system clock. The CSYNC bit is used to synchronize signals and commands going in and out of the UTMR module.
Prescaler	TMR2 has 8 programmable input prescaler options ranging from 1:1 to 1:128, which can be selected using CKPS bits.	UTMR has 256 programmable clock prescaler options ranging from 1:1 to 1:256, which can be selected using TUxyPS register.
Postscaler	TMR2 has a programmable postscaler ranging from 1:1 to 1:16, which can be selected using OUTPS bits. The internal postscaler counter is incremented at every period match.	UTMR does not has any postscaler because the module is not supposed to be used as a time base for PWM.
Output	The TMR2 output pulses for a single timer clock period upon each time the internal postscaler counter matches with the OUTPS bits postscaler selection.	Use OM = Pulse mode to pulse the output for one single timer clock period upon each PR match.
Interrupts	The TMR2IF interrupt is generated every time an output pulse is generated, i.e. when the internal postscaler counter matches with the OUTPS bits postscaler selection.	PRIF period interrupt can be used to signify when a PR match happens.
Sleep Mode Operation	TMR2 halts when PSYNC = `1`. When PSYNC = `0`, TMR2 continues operating, as long as the clock is active, and wakes up the CPU if interrupts are enabled.	UTMR continues to operate as long as the clock is active, and wakes up the CPU if interrupts are enabled.

5. Using UTMR as Signal Measurement Timer (SMT)

SMT is a 24-bit counter with advanced clock and gating logic, which can be configured for measuring a variety of digital signal parameters, such as pulse width, frequency and duty cycle, and the time difference between edges on two signals. A key feature that differentiates SMT from UTMR is the presence of two input signals (SMT signal and window) and two capture registers (SMTxCPW and SMTxCPR). UTMR has only one input signal (ERS) and one capture register. Thus, the UTMR might need to be reconfigured multiple times to measure different attributes in the same application. The following table shows UTMR settings in different SMT modes:

Table 5-1. UTMR Settings for Different SMT Modes

SMT MODE[3:0]	SMT Mode	UTMR Settings				Comments
		START	RESET	STOP	Other	
0000	Timer	None (ON = 1)	At PR Match	None	—	—
0001	Gated Timer	Rising ERS Edge	At PR Match	Either ERS Edge	—	Use SMT signal as ERS input.
0010	Period and Duty Cycle Measurement	Rising ERS Edge	At Start + PR Match	None (measures pulse-width) Rising ERS Edge (measures period)	—	Use SMT signal as ERS input. TUxyCR capture register will capture either pulse-width or period based on the Stop condition, but not both simultaneously.
0011	High and low time Measurement	Either ERS Edge	At Start + PR Match	Either ERS Edge	—	Use SMT signal as ERS input. TUxyCR capture register will capture high time, then low time, then high time, and so on. TUxyCR must be read before it is overwritten with new data.
		Rising ERS Edge	At Start + PR Match	Either ERS Edge	EPOL = True level for high time EPOL = Inverted level for low time	Use SMT signal as ERS input. TUxyCR capture register will capture either high time or low time based on EPOL bit setting.
0100	Windowed Measurement	Rising ERS Edge	At Start + PR Match	Rising ERS Edge	—	Use SMT window as ERS input.TUxyCR capture register will capture period of the window signal.

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SMT MODE[3:0]	SMT Mode	UTMR Settings				Comments
		START	RESET	STOP	Other	
0101	Gated Windowed Measurement	Rising ERS Edge	At PR Match	Either ERS Edge	—	Use SMT signal as ERS input. Use software to poll SMT window signal and reset counter manually using CLR command at every rising edge. Alternatively, interrupt-on-change can be used to monitor SMT window signal in software.
0110	Time of Flight Measurement	Rising ERS Edge	At Start + PR Match	Either ERS Edge	—	Use CLC to send an XOR of SMT window and SMT signal via ERS. TUxyCR capture register captures the time of flight measurement.
0111	Capture	None	At PR Match	Either ERS Edge	—	Use SMT signal as ERS input. TUxyCR capture register will first capture rising edge of ERS, then the falling edge of ERS, then the rising edge, and so on. TUxyCR must be read before it is overwritten with new data. PRAIF and PWAIF are both captured via CIF.
1000	Counter	None (ON = 1)	At PR Match	None	CSYNC = Async for using external clock source EPOL = Inverted for capturing at rising edge of ERS	Use SMT signal as UTMR clock input. Use SMT window as ERS input. TUxyCR capture register will capture counter value at falling edge of ERS (or rising edge when EPOL = Inverted).
1001	Gated Counter	Rising ERS Edge	At PR Match	Either ERS Edge	CSYNC = Async for using external clock source	Use SMT signal as UTMR clock input. Use SMT window as ERS input. TUxyCR capture register will capture counter value at falling edge of ERS. PWAIF is equivalent to CIF.
1010	Windowed Counter	Rising ERS Edge	At Start + PR Match	None (measures pulse-width) Rising ERS Edge (measures period)	CSYNC = Async for using external clock source	Use SMT signal as UTMR clock input. Use SMT window as ERS input. TUxyCR capture register will capture either pulse-width or period based on the Stop condition, but not both simultaneously.

5.1 Other SMT Features

The following table shows how some of the other features of SMT can be applied using UTMR:

Table 5-2. Features Comparison between SMT and UTMR

Feature	SMT	UTMR
Active Clock Edge	SMT increments at every rising edge of clock by default. The CPOL bit can use used to change the active clock edge.	Use CPOL bit to select the active clock edge. By default, CPOL = Falling Clock Edge.
Synchronization	SMT operates asynchronous to the system clock. All input and output signals are synchronized to the SMT clock.	UTMR also operates asynchronous to the system clock. Set CSYNC = Sync to synchronize signals and commands going in and out of the UTMR module.
Prescaler	TMR2 has 4 programmable input prescaler options ranging from 1:1 to 1:8, which can be selected using PS bits.	UTMR has 256 programmable clock prescaler options ranging from 1:1 to 1:256, which can be selected using TUxyPS register.
Input Source and Polarity	SMT signal and window sources are selected using SSEL and WSEL bits. The polarity is selected using SPOL and WPOL bits.	UTMR has only one ERS input selectable using TUxyERS register and polarity controlled using EPOL bit. Refer to Table 5-1 UTMR Settings for Different STM Modes for details on how the SMT signal and window inputs are mapped to ERS and/or UTMR clock.
Buffered Read/ Write	The 24-bit SMTxTMR timer/counter register is not guarded for atomic access and should not be accessed when GO = 1.	The TUxyTMR timer/counter register is not guarded for atomic access. However, the TUxyPR period register is double-buffered. Refer to section 1.1 UTMR Size and Buffered Access for details on UTMR buffered access to registers.
Manual Reset	Setting RST bit clears the timer atomically.	Setting CLR command bit clears the timer atomically.
Limit Mode	The counter can be prevented from resetting at the end of the timer period by using the STP bit. When STP = 1, the SMTxTMR will stop and remain equal to the SMTxPR register. When STP = 0, the SMTxTMR register resets at the end of the period.	Set RESET = None and LIMIT = Enabled to prevent the TUxyTMR counter from advancing beyond PR. Even though the counter does not advance, the timer is still “running” (RUN status bit and Level Output remain asserted) unless a Stop event occurs.
Capture Registers	The SMTxCPW and SMTxCPR capture registers capture the value of the SMTxTMR register based on the SMT mode of operation. These registers can also be updated with the current SMTxTMR value by setting the CPWUP and CPRUP bits respectively.	UTMR has only one TUxyCR capture register. Refer to Table 5-1 UTMR Settings for Different STM Modes for details on how this capture register can be used in different modes. The TUxyCR capture register can be updated with the current value of the TUxyTMR counter register by setting the CAPT command bit.
Status Information	Timer run status is indicated by TS bit. Signal status is indicated by AS bit. Window status is indicated by WS bit. All status bits are subject to synchronization delays.	Timer run status is indicated by RUN bit. CLC can be configured as a latch to indicate signal and window status.

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Feature	SMT	UTMR
Acquisition Mode	When REPEAT = 0, SMT operates in single acquisition mode, timer stops incrementing and GO bit is cleared after each acquisition. Set REPEAT = 1 to operate continuously.	Enable One-Shot mode (OSEN = Enabled) to operate in single acquisition mode, the timer stops and ON bit is cleared. Disable One-Shot mode to operate continuously.
Output	SMT output pulses every period match for one instruction clock.	Use OM = Pulse mode to pulse the output for one single timer clock period upon each PR match.
Interrupts	SMTxPWAIF pulse-width acquisition interrupt triggers when SMTxCPW register is updated with SMTxTMR register value. SMTxPRAIF period acquisition interrupt triggers when SMTxCPR register is updated with SMTxTMR register value. SMTxIF period match interrupt occurs when SMTxTMR register equals SMTxPR register.	SMTxPWAIF and SMTxPRAIF interrupts are represented as CIF capture interrupt in UTMR, which is triggered any time a capture event happens. SMTxIF interrupt can be represented as PRIF period interrupt in UTMR, which is triggered at every PR match.
Sleep Mode Operation	SMT continues to operate as long as the clock is active, and wakes up the CPU if interrupts are enabled.	UTMR continues to operate as long as the clock is active, and wakes up the CPU if interrupts are enabled.

6. Using UTMR as CCP (Capture/Compare/PWM)

The CCP (Capture/Compare) module is a peripheral which uses TMR1/TMR2 as the time base to perform Capture/Compare/PWM operations. The Capture/Compare modes use TMR1 as time base, whereas PWM mode uses TMR2 as time base. The following table shows UTMR settings in different CCP modes:

Table 6-1. UTMR Settings for Different CCP Modes

CCP MODE[3:0]	CCP Mode	CCP Operation	UTMR Settings If START/RESET/STOP = <blank>, set based on use case				Comments
			START	RESET	STOP	Other	
0001	Compare	Toggle output; clear TMR1	—	At PR Match	—	—	Use OM = Pulse mode and OPOL to generate appropriate output. Set/Clear/Toggle output features are not available in UTMR.
0010		Toggle output	—	—	—	—	
1000		Set output	—	—	—	—	
1001		Clear output	—	—	—	—	
1010		Pulse output	—	—	—	OM = Pulse output	—
1011		Pulse output; clear TMR1	—	At PR Match	—	OM = Pulse output	—
0011	Capture	Every edge of CCPx input	—	—	Either ERS Edge	—	—
0100		Every falling edge of CCPx input	—	—	Rising ERS Edge	EPOL = Inverted	—
0101		Every rising edge of CCPx input	—	—		—	—
0110		Every 4th rising edge of CCPx input	—	—		—	Use CLC or NCO as a frequency divider and use that as ERS input.
0111		Every 16th rising edge of CCPx input	—	—		—	
11xx	PWM	PWM operation	Rising ERS Edge	At Start + PR Match	At PR Match	OM = Level output OPOL = 0 for left-aligned PWM OPOL = 1 for right-aligned PWM	UTMR requires a periodic ERS input to act as the PWM period. The PR value determines the PWM duty cycle.

6.1 Other CCP Features

The following table shows how some of the other features of CCP modes can be applied using UTMR:

Table 6-2. Features Comparison between CCP (Capture/Compare Modes) and UTMR

Feature (Capture/ Compare modes)	CCP	UTMR
Capture Sources	The capture source can be selected using CTS bits.	The ERS input is used as a capture trigger and can be selected using TUxyERS register.
Timer Mode	TMR1 must be running in Timer mode or Synchronized counter mode. The Capture/ Compare may not work in Asynchronous Counter mode.	UTMR can operate in any mode for Capture/ Compare operation to happen.
Prescaler	Outside of the prescalers associated with the different time bases, the CCPx input has 4 prescaler settings available for Capture operation.	UTMR has 256 programmable clock prescaler options ranging from 1:1 to 1:256, which can be selected using TUxyPS register. CLC and/or NCO can be used to prescale the ERS input.
Output	CCP output can be set, cleared, toggled, or pulsed based on the mode of operation.	Use OM = Pulse mode to pulse the output for one single timer clock period upon each PR match.
Interrupts	CCPxIF interrupt is triggered when either a capture event occurs, or a compare match occurs.	CIF capture interrupt represents a captured event. PRIF period interrupt represents a compare match event.
Sleep Mode Operation	CCP module operates as long as the underlying time base is active.	UTMR continues to operate as long as the clock is active, and wakes up the CPU if interrupts are enabled.

Table 6-3. Features Comparison between CCP (PWM mode) and UTMR

Feature (PWM mode)	CCP	UTMR
Timer Mode	TMR2 must be running at $F_{OSC}/4$ clock for correct operation.	UTMR requires a periodic ERS input of the desired PWM period as the time base. The UTMR rollover period must be greater than or equal to the ERS input period for correct operation.
PWM Period	The PWM period is specified by the T2PR register of TMR2 resource.	The PWM period is the period of the ERS input signal.
PWM Duty Cycle	The PWM duty cycle is determined by the 10-bit value in the CCPRx register. FMT bit controls the alignment of the 10-bit data in the CCPRx register. The CCPRx register double buffers the PWM duty cycle to avoid glitches when changing the duty cycle.	The PWM duty cycle is determined by the PR value in the TUxyPR period register. The TUxyPR period register is also double-buffered to avoid glitches when changing the duty cycle.
PWM Resolution	The maximum PWM resolution is 10 bits when T2PR = 0xFF.	The maximum PWM resolution is the size of the UTMR when the UTMR rollover period matches the ERS input period.

.....continued

Feature (PWM mode)	CCP	UTMR
PWM Output	The CCPx output is a left-aligned PWM signal.	Use OM = Level mode to generate a PWM output. Set OPOL = 0 to generate a left-aligned PWM signal and OPOL = 1 to generate a right-aligned PWM signal. **Note:** The PR value might differ based on left-aligned or right-aligned PWM signal.
Sleep Mode Operation	PWM is not functional in Sleep mode because TMR2 is derived from F_{OSC}.	UTMR continues to operate in Sleep mode as long as the periodic ERS input is available and the UTMR clocks are active.

The period of the PWM is dependent on the period of the ERS input signal:

$$PWM\ Period\ =\ ERS\ Input\ Period$$

When OPOL = 0 (left-aligned PWM), the PR value determines the ON time. Hence, the pulse width of the signal is:

$$Pulse\ \ Width\ =\ (PR\ value\ +\ 1)\ \times TUCLK\ period$$

When OPOL = 1 (right-aligned PWM), the PR value determines the OFF time. Hence, the pulse width of the signal is:

$$Pulse\ \ Width\ =\ PWM\ Period\ -\ ((PR\ value\ +\ 1)\ \times TUCLK\ period)$$

The duty cycle ratio is a function of the pulse width and period of the PWM signal:

$$Duty\ Cycle\ \ Ratio\ =\ \frac{Pulse\ Width}{PWM\ Period}$$

The resolution of the PWM is a function of the PWM period, UTMR rollover period, and UTMR size. The maximum PWM resolution is the size of the UTMR, when the UTMR rollover period matches the PWM period.

$$PWM\ Resolution\ =\ \left\lfloor \log_2\left(\frac{PWM\ Period}{UTMR\ Rollover\ Period}\times 2^{UTMR\ Size}\right)\right\rfloor bits$$

Important: The UTMR rollover period must be greater than or equal to the ERS input period for proper PWM operation.

7. Conclusion

The UTMR module can be configured in multiple ways and be customized to operate in a variety of applications, such as periodic operation, external clock gating, hardware limit timer, and external clock operation. The inbuilt capture, compare features and customizable Start, Reset, Stop conditions make the Universal Timer is quite versatile.

8. Revision History

Revision	Date	Description
A	09/2020	Initial document release

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