
PCIe Switch with Integrated USB 3.2 Gen 2 Host Controller, Ethernet MAC & Programmable I/O

Highlights

- PCIe Gen 4 (8GT/s) switch fabric
- 1-lane PCIe Gen 4 (8GT/s) expansion port
- USB 3.2 Gen 2 (10Gbps) xHCI host
- 2.5Gbps Ethernet MAC (RGMII/SGMII/SGMII+)
- 802.3bz reference design to achieve 10/100/1000/2500Base-T networking
- I/O Multiplexer (SMBus/SPI/UART/GPIO)

Target Applications

- Single-Board Computers (SBC)
- AIoT Edge computing
- Industrial PC (IPC)
- Edge appliances
- Storage extensions

Features

- Integrated PCI switching fabric
 - 512byte maximum payload size
- Integrated PCIe physical interfaces
 - 4-lane (4x8GT/s) upstream port
 - Allowing single, dual, or four lane links
 - 1-lane (1x8GT/s) downstream port
- Integrated USB 3.2 Gen 2 (10Gbps) physical interfaces
- Integrated xHCI USB 3.2 Gen 2 (10Gbps) USB host controller
 - 2x 10Gbps Gen 2 PHY
 - 4x USB HS/FS/LS PHY
- Multiple config. options for Type-C® or Type-A2.5Gbps Ethernet MAC
 - IEEE 802.3 compliant
 - RGMII support for 10/100/1000Mbps
 - SGMII support for 1Gbps
 - SGMII+ support for 2.5Gbps
 - Jumbo frame support
- Precision Time Protocol
 - IEEE 1588-2008 E2E and P2P one and two step support
 - IEEE 1588-2008 Programmable Time Compare output (e.g., 1PPS)

- Comprehensive power management features
 - PCIe 3.1 LPSS (Low Power Sub States): L2 (with aux. power supply)
- Power and I/O
 - Integrated power-on reset circuit with configurable under/over voltage protection
 - Latch-up performance exceeds 150mA per EIA/JESD78, Class II
 - JEDEC Class 3A ESD performance
- UARTs
 - RS232/RS485
 - Auto-direction control
 - Standard and advanced speed support
 - Basic or comprehensive signal support
- Additional features
 - Multifunction GPIOs
 - Programmable pin multiplexer
 - Ability to use low-cost 25MHz crystal or clock for reduced BOM
 - SPI peripheral interface
 - SMBus target interface
 - SMBus controller interface
 - PVT Sensor
 - JTAG TAP
- Packaging
 - Pb-free RoHS compliant 164-pin DRQFN package
- Environmental
 - Available in commercial and industrial temperature grades

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1.0 INTRODUCTION

1.1 General Description

The Microchip PCI11414 is a single-chip PCIe switch with an integrated USB 3.2 Gen 2 host controller, Ethernet MAC and programmable I/O. The integrated PCIe physical interfaces provide a 4-lane (4x8GT/s) upstream port and a 1-lane (1x8GT/s) downstream port. The device is targeted to address customer requests for higher bandwidth PCIe sub-systems within embedded applications. The maximum line rate is 8GT/s and it is certified against the GEN4 compliance program as defined in the PCIe Revision 4.x specifications. PCIe upstream can be delivered across a single or multiple lanes to accommodate best system architecture. The PCI11414 includes a compliant PCIe implementation from external facing physical interfaces through to switch fabric and endpoint controllers.

The PCI11414 includes a USB-IF and xHCI compliant USB 3.2 Gen 2 host controller which provides one USB 3.2 Gen 2 (USB Type-C) port, and three USB 2.0 HS/FS/LS (USB Type-A) ports. USB-C support is provided, with CC1 & CC2 (Configuration Control) being managed by the PCI11414. Overcurrent Sense (OCS) and Port Control are provided for control of Vbus.

The PCI11414 also includes an IEEE 802.3 compliant 2.5Gbps Ethernet MAC. The integrated RGMII and SGMII interfaces support 10/100/1000Mbps and 1/2.5Gbps operation, respectively.

A programmable pin multiplexer is used to map I/O functions to package pins. This enables designers to work with either a default configuration or modify signals to best fit their application. Example signals include those associated with USB operation, through to GPIO or SMBus, which are accessed via a dedicated PCIe Endpoint Controller.

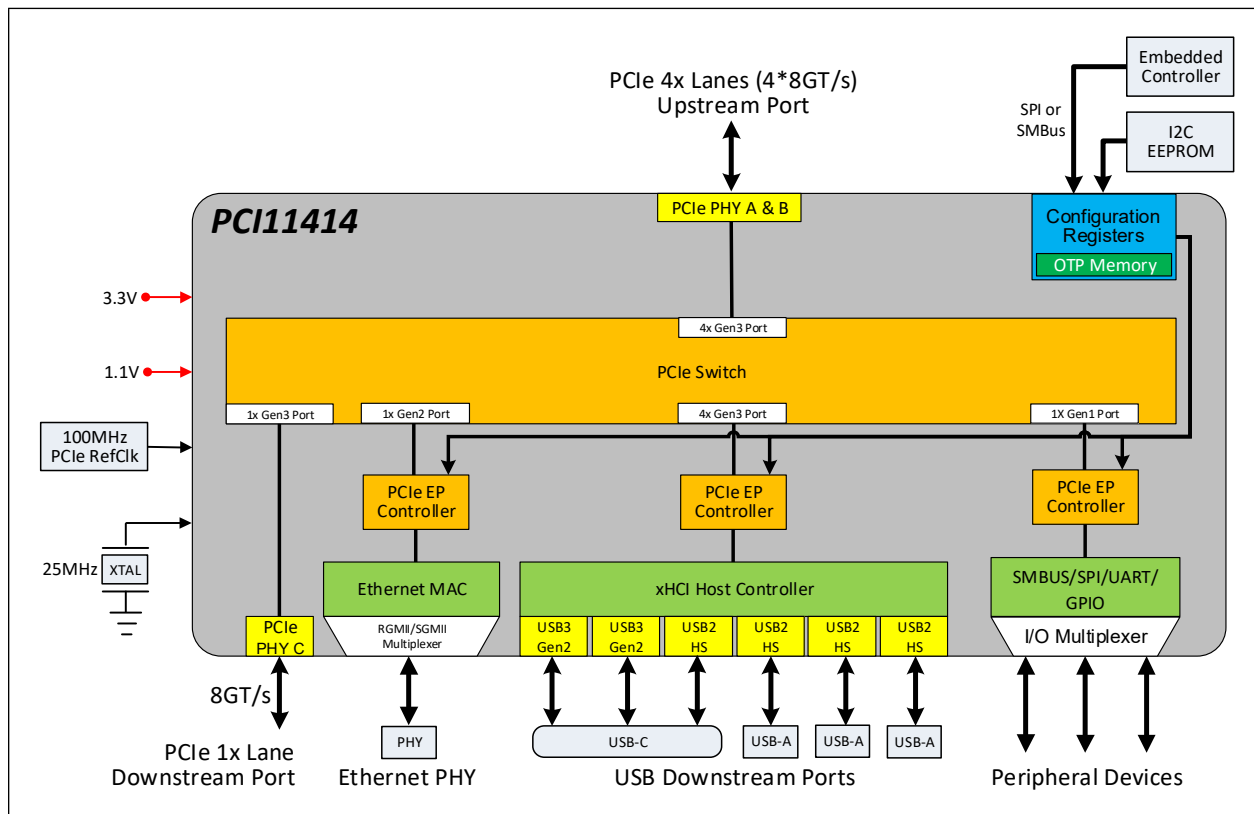
Though many clocks are required for PCI11414 operation, these are generated within an integrated clock farm. Only a single-ended 25MHz clock or crystal is required externally together with a PCIe reference clock.

PCI11414 software presentation is enabled using standard abstractions to major operating systems.

The PCI11414 is available in a 164-pin DRQFN package in commercial (0°C to +70°C) or industrial (-40°C to +85°C) temperature ranges.

An internal block diagram of the PCI11414 is shown in [Figure 1-1](#).

FIGURE 1-1: INTERNAL BLOCK DIAGRAM



PCI11414

2.0 PACKAGE INFORMATION

FIGURE 2-1: 164-DRQFN PACKAGE (DRAWING)

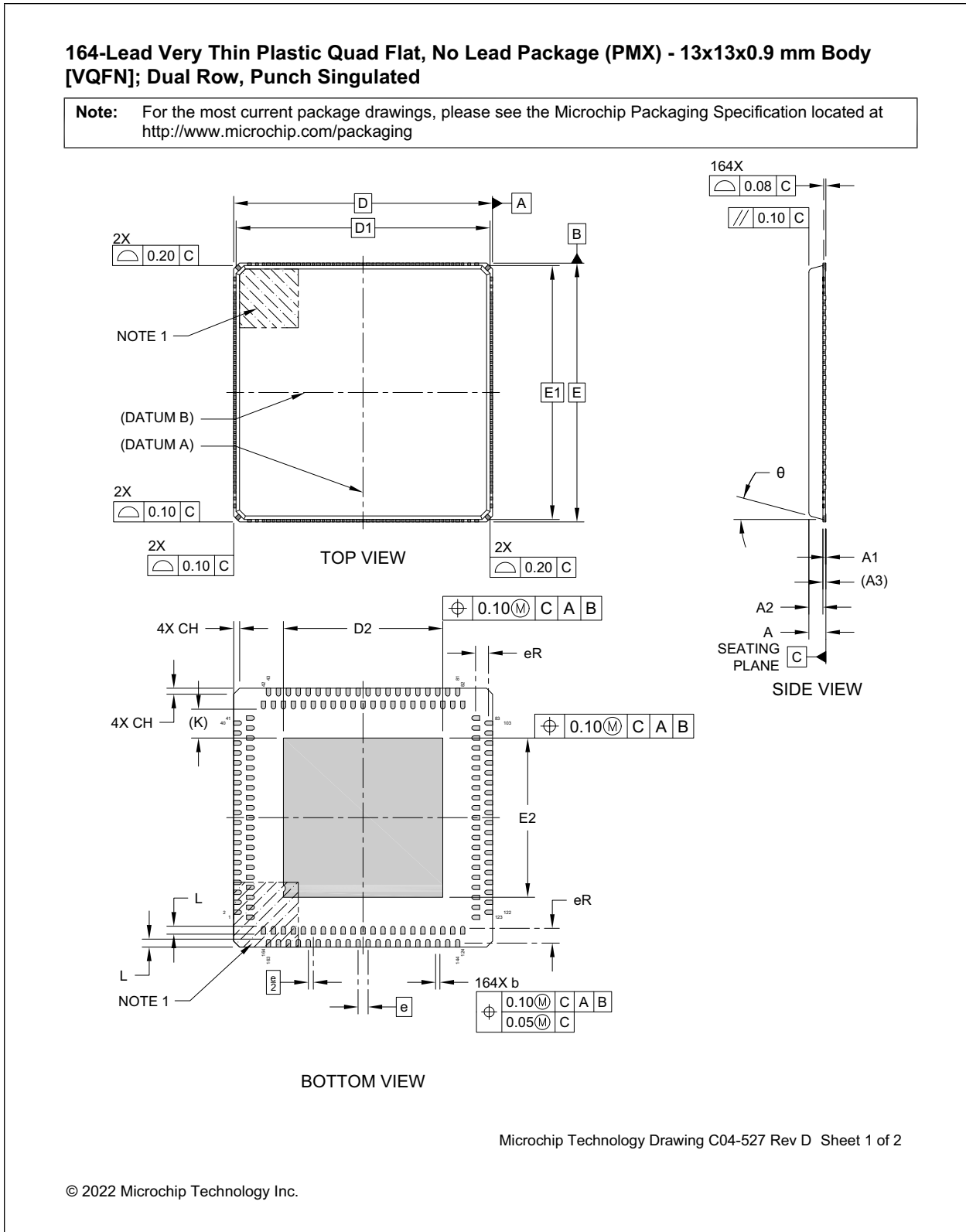
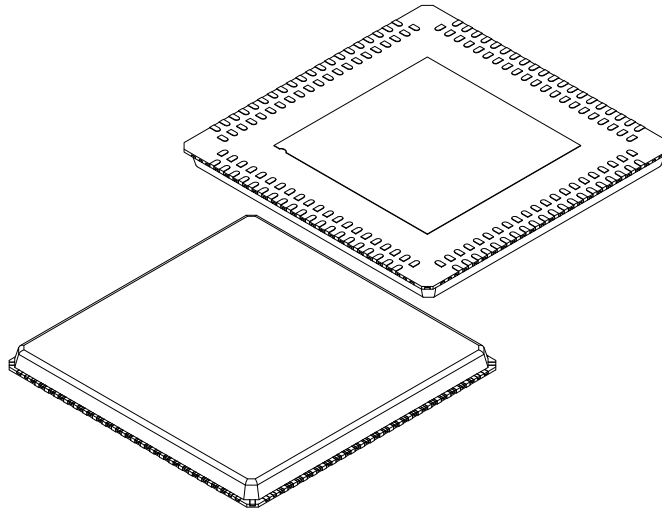


FIGURE 2-2: 164-DRQFN PACKAGE (DIMENSIONS)

164-Lead Very Thin Plastic Quad Flat, No Lead Package (PMX) - 13x13x0.9 mm Body [VQFN]; Dual Row, Punch Singulated

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	164		
Pitch	e	0.50 BSC		
Overall Height	A	–	–	0.90
Standoff	A1	0.00	0.02	0.05
Molded Package Height	A2	–	0.70	0.75
Terminal Thickness	A3	0.152 REF		
Overall Length	D	13.00 BSC		
Molded Package Length	D1	12.75 BSC		
Exposed Pad Length	D2	7.90	8.00	8.10
Overall Width	E	13.00 BSC		
Molded Package Width	E1	12.75 BSC		
Exposed Pad Width	E2	7.90	8.00	8.10
Terminal Row Spacing	eR	0.65 BSC		
Terminal Width	b	0.18	0.22	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	1.45 REF		
Package Corner Chamfer	CH	–	–	0.60
Mold Draft Angle	θ	5°	–	15°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is punch singulated
- Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.

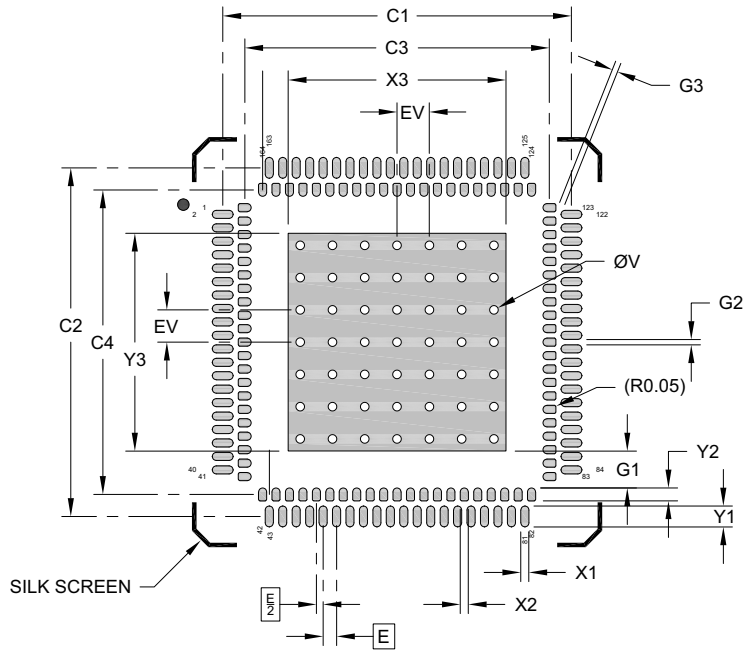
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FIGURE 2-3: 164-DRQFN PACKAGE (LAND PATTERN)

164-Lead Very Thin Plastic Quad Flat, No Lead Package (PMX) - 13x13x0.9 mm Body [VQFN]; Dual Row, Punch Singulated

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X3			8.10
Center Pad Length	Y3			8.10
Outer Row Contact Pad Spacing	C1		12.96	
Outer Row Contact Pad Spacing	C2		12.96	
Inner Row Contact Pad Spacing	C3		11.32	
Inner Row Contact Pad Spacing	C4		11.32	
Outer Contact Pad Width (X80)	X1			0.30
Outer Contact Pad Length (X80)	Y1			0.78
I84er Contact Pad Width (X84)	X2			0.30
I84er Contact Pad Length (X84)	Y2			0.48
Contact Pad to Center Pad	G1	1.35		
Contact Pad to Contact Pad	G2	0.20		
Outer Contact Pad to Inner Contact Pad	G3	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		0.20	

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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APPENDIX A: PRODUCT BRIEF REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00003792B (05-17-23)	Highlights	Updated cover bullets for clarity.
	Section 1.1, General Description	Added the following sentence to the first paragraph: "The maximum line rate is 8GT/s and it is certified against the GEN4 compliance program as defined in the PCIe Revision 4.x specifications."
	Figure 1-1	Updated port names for clarity.
	Section 2.0, "Package Information"	Updated package drawing, dimensions and land pattern.
DS00003792A (01-08-21)	All	Initial Release.

PCI11414

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>[X]⁽¹⁾</u>	<u>-</u>	<u>X</u>	<u>/</u>	<u>XXX</u>
Device	Tape and Reel Option		Temperature Range		Package
Device:	PCI11414= PCIe Switch with USB Host, Ethernet MAC, I/O				
Tape and Reel Option:	Blank = Standard packaging (tray) T = Tape and Reel (Note 1)				
Temperature Range:	Blank = 0°C to +70°C (Commercial) I = -40°C to +85°C (Industrial)				
Package:	PMX = 164-pin DRQFN				

Examples:

- a) PCI11414/PMX
Tray, 0°C to +70°C, 164-pin DRQFN
- b) PCI11414T/PMX
Tape & reel, 0°C to +70°C, 164-pin DRQFN
- c) PCI11414-I/PMX
Tray, -40°C to +85°C, 164-pin DRQFN
- d) PCI11414T-I/PMX
Tape & reel, -40°C to +85°C, 164-pin DRQFN

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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