S32G2

S32G2 Data Sheet

Rev. 3 — 04/2021

Data Sheet: Technical Data

- This document provides electrical specifications for the S32G2.
- For functional characteristics and the programming model, see the S32G Reference Manual.

Contents

1 Introduction

1.1 Overview

S32G2 is a family of high-performance vehicle network processors that combine controller area network (CAN), local interconnect network (LIN), and FlexRay networking with high-data-rate Ethernet networking. It also combines a functional safe-core infrastructure with MPU cores and includes high-level security features.

S32G2 family includes the following variants:

- S32G234M
- S32G233A
- S32G254A
- S32G274A

This document primarily represents the features offered by the superset S32G274A. To compare the features of the S32G2 family variants, please see the Feature comparison.

1.2 Applications

The S32G2 chip family targets the following applications:

- Central gateways and domain controllers connecting various networks and translating their protocols
- Safety processor for ADAS and autonomous driving
- High-performance central compute nodes
- FOTA masters controlling secure software image downloads and their distribution to the ECUs in the network
- Secure key management
- Smart antennas

2 Block diagram

The following figure shows the block diagram for S32G274A, the superset chip in the S32G2 family.

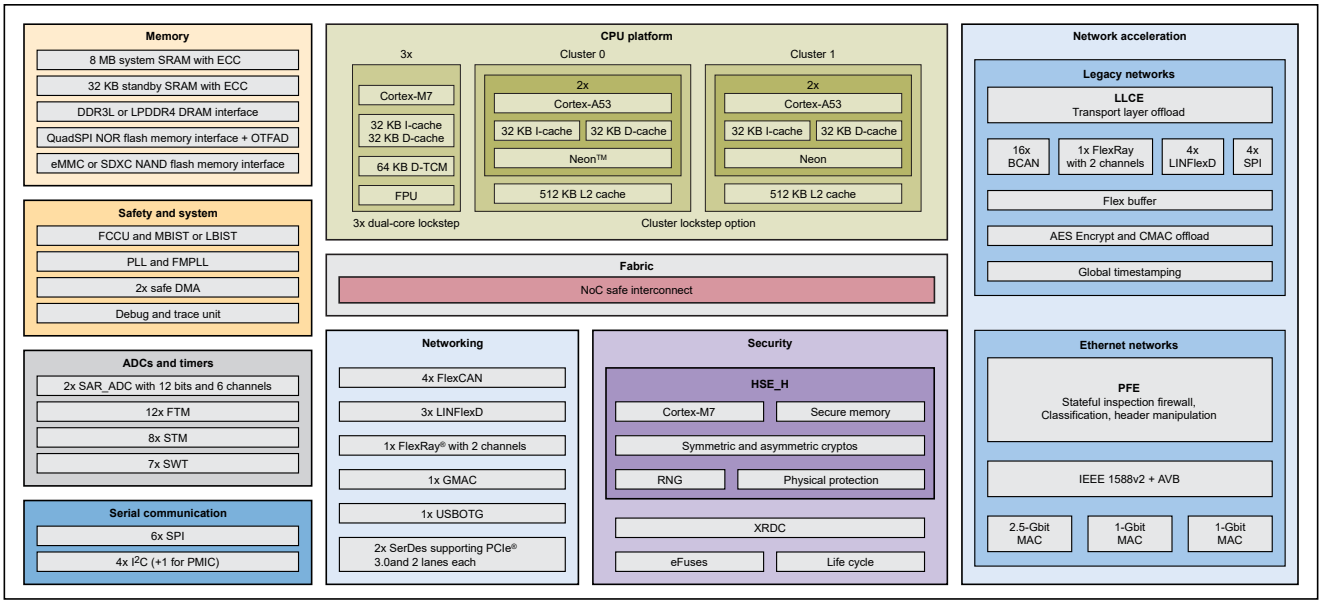

Figure 1. Block diagram

3 Feature comparison

The following table compares the features of chips in the S32G2 family.

Table 1. Feature comparison

Feature	S32G234M	S32G233A	S32G254A	S32G274A
Compute and bus modules				
CPUs: applications	N/A	Cluster 0: single Cortex-A53 core (only core 0 is available on these chips)		Cluster 0: dual Cortex-A53 core
		Cluster 1: single Cortex-A53 core (only Core 0 is available on these chips)		Cluster 1: dual Cortex-A53 core
L1 cache	N/A	32 KB I-cache and 32 KB D-cache per Cortex-A53 core		
L2 cache	N/A	512 KB per cluster		
Cache coherency interconnect	N/A	Yes		
Interrupt controller for Cortex-A53 core	N/A	Generic interrupt controller (CoreLink™ GIC-500)		
Core maximum frequencies	Cortex-M7 core: 400 MHz	Cortex-A53 core: 1 GHz Cortex-M7 core: 400 MHz		
Lockstep support for Cortex-A53 cores	N/A	Configurable: lockstep clusters or two independent clusters		
CPUs: real-time	3 Cortex-M7 cores in lockstep	1 Cortex-M7 core in lockstep (only the	3 Cortex-M7 cores in lockstep	

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Table 1. Feature comparison (continued)

Feature	S32G234M	S32G233A	S32G254A	S32G274A
		Cortex-M7 core 0 is avaialable on these chips)		
L1 cache	32 KB I-cache and 32 KB D-cache per Cortex-M7 core			
DTCM	64 KB per Cortex-M7 core			
Interrupt controller for Cortex-M7 core	3 NVICs	1 NVIC	3 NVICs	
DMA	2 eDMA (supporting lockstep), each with 32 channels			
DMAMUX inputs	128 per DMA			
Debug run control	Arm CoreSight™ JTAG (IEEE 1149.1)			
Debug trace	Aurora 4-lane			
SWT	7			
STM	8			
Memory modules				
System RAM	8 MB	6 MB	8 MB	
System RAM ports	16 ports, interleaved 64-byte			
DRAM	N/A	LPDDR4 and DDR3L		
DRAM physical interface (PHY)	N/A	×32		
QuadSPI	1 (supports two identical devices)			
uSDHC	1			
Fuses	8 KB bank			
Standby SRAM with ECC	32 KB			
Security modules				
Security subsystem	HSE_H			
Resource isolation	XRDC supporting 8 domains			
Arm TrustZone®	N/A	Yes		
Life cycle	Yes			
Secure debug	Yes			
OTFAD	Yes			
Communication interface modules				
Comms acceleration	LLCE			
CAN with flexible data rate	16 (in LLCE) + 4			

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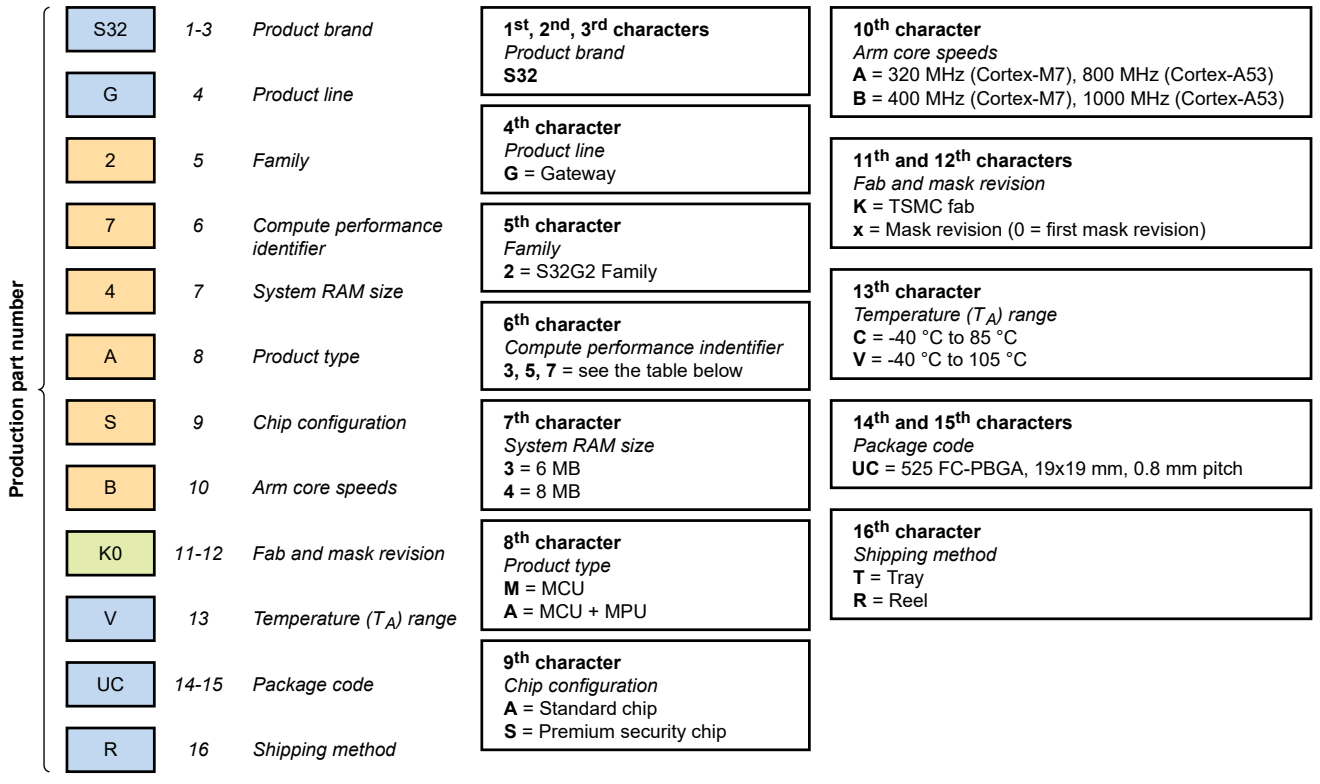
Table 1. Feature comparison (continued)

Feature	S32G234M	S32G233A	S32G254A	S32G274A
FlexRay with dual-channel support for protocol version 2.1	1 (in LLCE) + 1			
LINFlexD	4 (in LLCE) + 3			
SPI	4 (in LLCE, can be enabled with firmware) + 6			
Ethernet acceleration	PFE			
MAC	4 (3 PFE_MAC + 1 GMAC_0)			
Supported Ethernet interfaces	MII, RMII, RGMII, and SGMII			
SerDes subsystem with PCIe	1 supporting Gen2 in X1 and X2 modes (PCIe_1 only)	2 supporting Gen3 in X1 and X2 modes		
SerDes subsystem lanes	2 configurable for PCIe or SGMII (SerDes_1 only)	4 configurable for PCIe or SGMII		
USBOTG	N/A	1 supporting USB 2.0 and ULPI interfaces		
I^2C	5			
CRC	1			
Generic modules				
PIT	2			
SAR_ADC	2, each supporting 12 bits and 6 channels			
FTM	2, each supporting 6 channels			
CTU	1			
SEMA42	1			
Clocking, power, and reset				
FIRC frequency	48 MHz			
SIRC frequency	32 kHz			
FXOSC frequency	20–40 MHz			
PLL	5			
Low-power mode	Yes			
RTC	1 with API function			
Wake-up sources	24			
Miscellaneous				
Package	525 flip chip plastic ball grid array (525 FC-PBGA), 19 mm × 19 mm, 0.8 mm pitch			

4 Ordering Parts

4.1 Ordering information



	S32G234M	S32G233A	S32G254A	S32G274A
Arm Cortex-M7 cores	3	1	3	3
Arm Cortex-A53 cores	-	2	2	4
System RAM size (MB)	8	6	8	8

Figure 2. Ordering information

5 Electrostatic Discharge (ESD) Characteristics

The following table gives the ESD ratings and test conditions for the device.

Table 2. Electrostatic Discharge (ESD) Characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	ESD Human Body Model (HBM) [1, 2, 3]	—	—	2000	V	All pins	—
—	ESD Charged Device Model (CDM) [1, 3, 4]	—	—	250	V	All pins	—

1. Device failure is defined as: "If after exposure to ESD pulses, the device does not meet the device specification requirements."

2. This parameter is tested in conformity with AEC-Q100-002
3. All ESD testing conforms with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
4. This parameter is tested in conformity with AEC-Q100-011.

6 Maximum Ratings

6.1 Absolute Max Ratings

This table defines the absolute maximum ratings for the device in terms of reliability characteristics. Absolute maximum rating specifications are stress ratings only, and functional operation is not guaranteed under these conditions. Functional operating conditions are given in the Operating Conditions section of this document.

Table 3. Absolute Max Ratings

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD	Core voltage Supply [1, 2]	-0.3	—	0.96	V	—	—
VSS	Ground Supply [1]	-0.3	—	0.3	V	—	—
VDD_STBY	Standby domain supply voltage [1, 2]	-0.3	—	0.96	V	—	—
VDD_LV_PLL	PLL digital voltage supply [1, 2, 3]	-0.3	—	0.96	V	—	—
VDD_LV_PLL_AUR	Aurora PLL digital voltage supply [1, 2]	-0.3	—	0.96	V	—	—
VDD_LV_PLL_DDR0	DDR0 PLL digital voltage supply [1, 2]	-0.3	—	0.96	V	—	—
VDD_VP_PCIEn	PCIE0/1 core voltage supply (n=0, 1) [1, 2]	-0.3	—	0.96	V	—	—
VDD_FIRC	FIRC high voltage supply [1, 4]	-0.3	—	2.16	V	—	—
VDD_EFUSE	EFUSE high voltage supply [1, 4]	-0.3	—	2.16	V	—	—
VDD_IO_x	GPIO 3.3V supply [1, 5]	-0.3	—	4	V	—	—
VDD_IO_A	GPIO A 3.3V supply [1, 5]	-0.3	—	4	V	—	—
VDD_IO_B	GPIO B 3.3V supply [1, 5]	-0.3	—	4	V	—	—
VDD_IO_GMAC0	GMAC0 I/O voltage supply [1, 5]	-0.3	—	4	V	—	—
VDD_IO_GMAC1	GMAC1 I/O voltage supply [1, 5]	-0.3	—	4	V	—	—
VDD_IO_QSPI	QSPI A I/O voltage supply [1, 4]	-0.3	—	2.16	V	—	—

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Table 3. Absolute Max Ratings (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_IO_SDHC	uSDHC / QSPI B I/O voltage supply [1, 5]	-0.3	—	4	V	—	—
VDD_IO_CLKOUT	CLKOUT 1.8V I/O supply [1, 4]	-0.3	—	2.16	V	—	—
VDD_IO_AUR	Aurora 1.8V I/O supply [1, 4]	-0.3	—	2.16	V	—	—
VDD_IO_DDR0	DDR0 I/O voltage supply [1]	-0.3	—	2.16	V	—	—
VDD_IO_USB	USB I/O voltage supply [1, 5]	-0.3	—	4	V	—	—
VDD_IO_STBY	Standby domain I/O voltage supply [1, 5]	-0.3	—	4	V	—	—
VDD_VREF	Supply detector high voltage supply [1, 4]	-0.3	—	2.16	V	—	—
VDD_ADC	ADC voltage supply [1, 4]	-0.3	—	2.16	V	Reference to VSS_ADC	—
VSS_ADC	ADC ground supply [1]	-0.3	—	0.3	V	Reference to VSS	—
VDD_HV_PLL	PLL high voltage supply [1, 4]	-0.3	—	2.16	V	—	—
VDD_HV_PLL_AUR	Aurora PLL high voltage supply [1, 4]	-0.3	—	2.16	V	—	—
VDD_HV_PLL_DDR0	DDR PLL voltage supply [1, 4]	-0.3	—	2.16	V	—	—
VDD_DDR0	DDR0 high voltage supply [1, 4]	-0.3	—	2.16	V	DDR PHY PLL	—
VDD_FXOSC	FXOSC high voltage supply [1, 4]	-0.3	—	2.16	V	Reference to VSS_FXOSC	—
VSS_FXOSC	FXOSC ground supply [1]	-0.3	—	0.3	V	Reference to VSS	—
VEXTAL	FXOSC EXTAL input voltage range [1, 4, 6]	-0.3	—	2.16	V	—	—
VXTAL	FXOSC XTAL input voltage range [1, 4, 6]	-0.3	—	2.16	V	—	—
VDD_IO_PCIEn	PCIE0/1 high voltage supply (n=0, 1) [1, 4]	-0.3	—	2.16	V	—	—

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Table 3. Absolute Max Ratings (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_TMU	Thermal Monitoring Unit (TMU) high voltage supply [1, 4]	-0.3	—	2.16	V	—	—
VREFH_ADC	ADC reference high voltage [1, 4]	-0.3	—	2.16	V	Reference to VREFL_ADC	—
VREFL_ADC	ADC reference low voltage [1]	-0.3	—	0.3	V	Reference to VSS	—
VAD_INPUT	ADC input voltage range [1, 7, 8]	VREFL_ADC -0.6	—	VREFH_ADC + 0.5	V	—	—
VIN	GPIO input voltage range [1, 9, 10]	VSS - 0.3	—	VDD_IO_* + 0.3	V	—	—
IINJ_D	Maximium DC current injection digital I/O pin [1, 11]	-3	—	3	mA	—	—
IINJ_A	Maximum DC current injection analog input pin [1, 8, 12]	-1	—	1	mA	—	—
IMAXSEG	Maximum RMS current per GPIO supply domain (VDD_IO_*) [1]	—	—	140	mA	—	—
TSTG	Storage temperature range [1]	-55	—	150	C	—	—
TSDR	Maximum solder temperature [1, 13]	—	—	260	C	Pb free	—
MSL	Moisture Sensitivity Level [1, 14]	—	—	3	—	—	—
—	Voltage at 10 % of tSIGNAL	-0.4	—	3.7	V	See input overshoot/ undershoot voltage for each GPIO pad type figure below	—
—	Voltage at 7.50 % of tSIGNAL	-0.5	—	3.8	V	See input overshoot/ undershoot voltage for each GPIO pad type figure below	—
—	Voltage at 2.50 % of tSIGNAL	-0.6	—	3.9	V	See input overshoot/ undershoot voltage for each GPIO pad type figure below	—

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Table 3. Absolute Max Ratings (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	Voltage at 1.60 % of tSIGNAL	-0.7	—	4	V	See input overshoot/ undershoot voltage for each GPIO pad type figure below	—

1. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device. See the operating conditions table for functional specifications.
2. Allowed 0.88V – 0.96V for 60 seconds cumulative over lifetime with no operating restrictions, 2.0 hours cumulative over lifetime with device in reset, at maximum Tj = 125 °C
3. VDD_LV_PLL must be connected to VDD, and not powered independently. It must share any filters with VDD.
4. Allowed 1.92V - 2.16V for 60 seconds cumulative over lifetime with no operating restrictions, 2.6 hours cumulative over lifetime with device in reset, at maximum Tj = 125 °C
5. Allowed 3.52V - 4.0V for 60 seconds cumulative over lifetime with no operating restrictions, 2.6 hours cumulative over lifetime with device in reset, at maximum Tj = 125 °C
6. VEXTAL/ VXTAL (min) is for powered condition. VEXTAL/VXTAL (min) can be lower in unpowered condition.
7. The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage equals the supply plus the voltage drop across the internal ESD diode from I/O pin to supply.
8. Allowed for a cumulative duration of 50 hours operation over the lifetime of the device at maximum Tj, with VREFH_ADC <= 1.92V, VREFL_ADC = 0V. Allowed for unlimited duration if the device is unpowered.
9. Absolute maximum rating VIN max levels are 3.82V and 2.22V for 3.3V and 1.8V supplies respectively.
10. Absolute minimum level for VIN signal is -0.3V.
11. IINJ_D specifications are per pin for an unpowered condition of the associated supply. The maximum simultaneous injection per supply is 30mA.
12. Non-disturb of ADC channels during current injection cannot be guaranteed. The degradation in channel performance cannot be specified due to the dynamic operation of the ADC input mux and potential for varying charge distribution. For the max +/-1mA DC injection quoted here, VAD_INPUT would be +0.5/-0.6V relative to VREFH_ADC/VREFL_ADC at -40 Tj. ADC Output of the channel into which injection occurs will saturate depending on the direction of injection and for the channels not subject to current injection Offset error would be -12 LSB to 6 LSB and TUE would be -12 LSB to 8 LSB.
13. Solder profile per IPC/JEDEC J-STD-020D.
14. Moisture sensitivity per JEDEC test method A112.

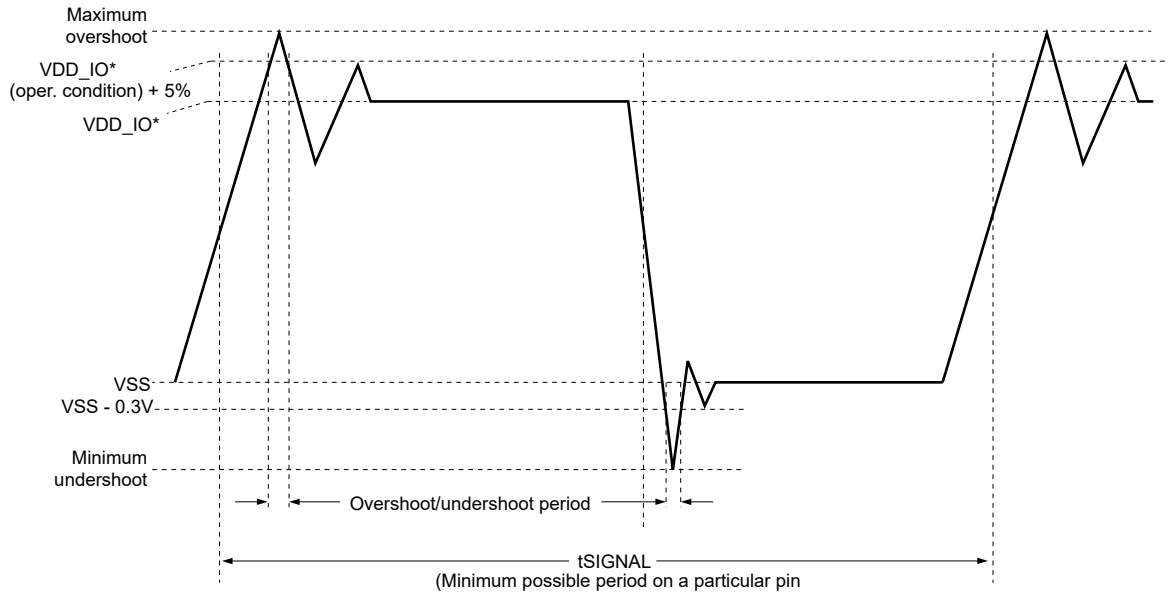

Figure 3. Input overshoot/undershoot voltage for each GPIO pad type

7 Operating Conditions

7.1 Operating Conditions

The following table describes the functional operating conditions for the device, and for which all specifications in this datasheet are valid, except where explicitly noted. Device behavior is not guaranteed for operation outside of the conditions in this table.

Table 4. Operating Conditions

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSYS_A53	Cortex-A53 core operating frequency [1, 2]	—	—	1000	MHz	—	—
fSYS_CM7	Cortex-M7 core operating frequency [1, 2]	—	—	400	MHz	—	—
fSYS_PFE_PE	PFE PE operating frequency [1, 2]	—	—	600	MHz	—	—
Tj	Junction Temperature Range [1, 3]	-40	—	125	C	—	—
Ta	Ambient Temperature Range [1]	-40	—	105	C	—	—
VDD	Core voltage Supply [1, 4]	0.72	0.77	0.87	V	DIE_PROCESS[1:0] fuse setting = b01	—

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Table 4. Operating Conditions (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD	Core voltage Supply [1, 4]	0.75	0.8	0.87	V	DIE_PROCESS[1:0] fuse setting = b00	—
VSS	Ground Supply [1]	—	0	—	V	—	—
VDD_STBY	Standby domain suppy voltage [1, 5, 6]	0.72	0.77	0.87	V	DIE_PROCESS[1:0] fuse setting = b01	—
VDD_STBY	Standby domain suppy voltage [1, 5, 6]	0.75	0.8	0.87	V	DIE_PROCESS[1:0] fuse setting = b00	—
VDD_LV_PLL	PLL digital voltage supply [1, 7, 8]	0.72	0.77	0.87	V	DIE_PROCESS[1:0] fuse setting = b01	—
VDD_LV_PLL	PLL digital voltage supply [1, 7, 8]	0.75	0.8	0.87	V	DIE_PROCESS[1:0] fuse setting = b00	—
VDD_LV_PLL_AUR	Aurora PLL digital voltage supply [1, 8]	0.72	0.77	0.87	V	DIE_PROCESS[1:0] fuse setting = b01	—
VDD_LV_PLL_AUR	Aurora PLL digital voltage supply [1, 8]	0.75	0.8	0.87	V	DIE_PROCESS[1:0] fuse setting = b00	—
VDD_LV_PLL_ DDR0	DDR0 PLL digital voltage supply [1, 8]	0.72	0.77	0.87	V	DIE_PROCESS[1:0] fuse setting = b01, reference PLL only - DDR PLL LV supply tied to LV power grid.	—
VDD_LV_PLL_ DDR0	DDR0 PLL digital voltage supply [1, 8]	0.75	0.8	0.87	V	DIE_PROCESS[1:0] fuse setting = b00, reference PLL only - DDR PLL LV supply tied to LV power grid.	—
VDD_VP_PCIEn	PCIE0/1 core voltage supply [1, 8, 9]	0.72	0.77	0.87	V	DIE_PROCESS[1:0] fuse setting = b01	—
VDD_VP_PCIEn	PCIE0/1 core voltage supply [1, 8, 9]	0.75	0.8	0.87	V	DIE_PROCESS[1:0] fuse setting = b00	—
VDD_IO_A	GPIO A 3.3V supply [1]	3.08	3.3	3.52	V	—	—
VDD_IO_B	GPIO B 3.3V supply [1]	3.08	3.3	3.52	V	—	—
VDD_IO_GMAC0	GMAC0 I/O voltage supply [1]	1.68	1.8	1.92	V	1.8V	—
VDD_IO_GMAC0	GMAC0 I/O voltage supply [1]	3.08	3.3	3.52	V	3.3V	—
VDD_IO_GMAC1	GMAC1 I/O voltage supply [1]	1.68	1.8	1.92	V	1.8V	—

Table continues on the next page...

Table 4. Operating Conditions (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_IO_GMAC1	GMAC1 I/O voltage supply [1]	3.08	3.3	3.52	V	3.3V	—
VDD_IO_QSPI	QuadSPI A I/O voltage supply [1, 10]	1.68	1.8	1.92	V	1.8V	—
VDD_IO_SDHC	uSDHC / QSPI B I/O voltage supply [1]	1.68	1.8	1.92	V	1.8V	—
VDD_IO_SDHC	uSDHC I/O voltage supply [1]	3.08	3.3	3.52	V	3.3V	—
VDD_IO_CLKOUT	CLKOUT 1.8V I/O supply [1]	1.68	1.8	1.92	V	—	—
VDD_IO_AUR	Aurora 1.8V I/O supply [1]	1.68	1.8	1.92	V	Aurora LVDS Tx + ref clock	—
VDD_IO_STBY	Standby domain I/O voltage supply [1, 5]	3.08	3.3	3.52	V	Min 2.91V supported in low-power standby mode	—
VDD_IO_USB	USB I/O voltage supply [1]	1.68	1.8	1.92	V	1.8V	—
VDD_IO_USB	USB I/O voltage supply [1]	3.08	3.3	3.52	V	3.3V	—
VDD_IO_DDR0	DDR3L I/O voltage supply [1]	1.283	1.35	1.45	V	—	—
VDD_IO_DDR0	LPDDR4 I/O voltage supply [1]	1.06	—	1.17	V	—	—
δVDD_IO_DDR0	DDR I/O supply ripple voltage [1]	-5	—	5	%	DDR3L	—
δVDD_IO_DDR0	LPDDR4 I/O supply ripple voltage [1]	-2.5	—	2.5	%	—	—
VDD_DDR0	DDR0 high voltage supply [1]	1.68	1.8	1.92	V	—	—
VDD_FIRC	FIRC high voltage supply [1]	1.68	1.8	1.92	V	—	—
VDD_VREF	PMC high voltage supply [1]	1.68	1.8	1.92	V	—	—
VDD_EFUSE	EFUSE high voltage supply [1, 11, 12, 13]	1.68	1.8	1.92	V	—	—
VDD_ADC	ADC high voltage supply [1]	1.68	1.8	1.92	V	—	—
VDD_HV_PLL	PLL high voltage supply [1]	1.68	1.8	1.92	V	—	—

Table continues on the next page...

Table 4. Operating Conditions (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_HV_PLL_AUR	Aurora PLL high voltage supply [1]	1.68	1.8	1.92	V	—	—
VDD_HV_PLL_DDR0	DDR PLL voltage supply [1]	1.68	1.8	1.92	V	—	—
ðVDD_HV_PLL_DDR0	DDR PLL supply ripple voltage [1]	-2.5	—	2.5	%	—	—
VDD_FXOSC	FXOSC high voltage supply [1]	1.68	1.8	1.92	V	—	—
VDD_IO_PCIEn	PCIE0/1 high voltage supply [1, 9]	1.68	1.8	1.92	V	—	—
VDD_TMU	Thermal Monitoring Unit (TMU) high voltage supply [1]	1.68	1.8	1.92	V	—	—
VREFH_ADCn	ADC reference high voltage (n=0, 1) [1]	1.68	1.8	1.92	V	—	—
VREFL_ADCn	ADC reference low voltage (n=0, 1) [1]	VSS_HV_ADC - 0.025	—	VSS_HV_ADC + 0.025	V	DC value	—
VIN_33	3.3V GPIO input voltage range [1, 14, 15]	VSS - 0.3	—	VDD_IO_* + 0.3	V	—	—
VIN_18	1.8V GPIO input voltage range [1, 14, 15]	VSS - 0.3	—	VDD_IO_* + 0.3	V	—	—
ΔVDD	0.8V supply voltage differential [1, 16]	-25	—	25	mV	Applies to all 0.8V supplies on the device.	—
ΔVDD_HV_18_IO	1.8V I/O supply voltage differential group [1, 16]	-25	—	25	mV	Applies to VDD_IO_QSPI, VDD_IO_SDHC, VDD_IO_GMAC0, VDD_IO_GMAC1, VDD_IO_USB	—
ΔVDD_HV_18_ANA	1.8V analog supply voltage differential group [1, 16]	-25	—	25	mV	Applies to VDD_IO_CLKOUT, VDD_IO_AUR, VDD_TMU, VREFH_ADC*, VDD_ADC, VDD_HV_PLL*, VDD_VREF, VDD_FXOSC, VDD_FIRC, VDD_EFUSE, VDD_DDR0, VDD_IO_PCIE0, VDD_IO_PCIE1	—

Table continues on the next page...

Table 4. Operating Conditions (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
ΔVDD_HV_33_IO	3.3V I/O supply voltage differential group [1], [16]	-25	—	25	mV	VDD_IO_A, VDD_IO_B	—
ΔVDD_IO_DDR	DDR I/O supply voltage differential group [1], [16]	-25	—	25	mV	VDD_IO_DDR0	—
ΔVSS_HV_18	1.8V supply ground voltage differential [1], [16]	-25	—	25	mV	Applies to VSS, VREFL_ADCn, VSS_ADC, VSS_FXOSC	—
VRAMP_LV	LV supply voltage ramp-up rate [1], [17]	0.001	—	24	V / ms	Applies to 0.8V supplies	—
VRAMP_HV	HV supply voltage ramp-up rate [1]	0.001	—	24	V / ms	Applies to 1.8V supplies and DDR I/O supplies.	—
VRAMP_HV_33_IO	3.3V I/O supply voltage ramp-up rate [1]	0.001	—	50	V / ms	Applies to 3.3V I/O supplies.	—
TDISCHARGE_STDBY	Supply discharge time during Standby mode entry [1]	100	—	—	us	Applies to all switchable supplies during Standby mode entry	—
VAD_INPUT	ADC input voltage range [1], [18]	VREFL_ADC - 0.35	—	VREFH_ADC + 0.25	V	—	—
IINJ_D	GPIO Input DC Injection Current [1], [19]	-3	—	3	mA	—	—
IINJ_A	SAR ADC Input DC Injection Current [1], [20]	-20	—	20	uA	—	—
IMAXSEG	Maximum RMS current per GPIO supply domain [1]	—	—	120	mA	—	—

1. The operating conditions in this table apply as required conditions for all other specifications in this document, unless explicitly noted as an exception in another section of this document.
2. The stated maximum operating frequency must be observed when using the PLL with frequency modulation enabled. Center-spread modulation is supported in cases where the nominal operating frequency plus the modulation depth (max 1.5%) is less than the stated maximum frequency.
3. Lifetime operation at Tj max not guaranteed. Standard automotive temperature profile assumed for performance and reliability guarantees.
4. If static voltage scaling is not used in the application on the VDD supply, then the voltage range for DIE_PROCESS[1:0] fuse setting = b00 applies for the device.
5. A minimum of 2.91V is supported on the VDD_IO_STBY supply when the device is in low-power standby mode.
6. The operating voltage range applies when the device is not in standby mode.
7. VDD_LV_PLL must be connected to VDD, and not powered independently. It must share any filters with VDD.
8. The minimum operating voltage applies when SVS is enabled. SVS guidelines apply to all LV supplies on the device. See power management chapter of device reference manual for details on SVS.

9. Both PCIe supplies must ramp for the SerDes PHY to safely power up into its reset state. Until both supplies are ramped, the SerDes PHY will be in an undefined state.
10. The device supports QSPI interface to 3.3V memories on the QSPI B bank, which is multiplexed with uSDHC functions on the VDD_IO_SDHC supply. QSPI A signals on VDD_IO_QSPI are limited to 1.8V.
11. The VDD_EFUSE supply must be maintained within specification during fuse programming. Failure to do this may result in improper functionality of the device after fuse programming.
12. Refer to the Power Sequencing section for the relationship of VDD_EFUSE powering up/down relative to the core, high-voltage, and I/O supplies.
13. VDD_EFUSE must be grounded when not actively programming the fuses. This supply is not required to be powered for fuse reads.
14. Additional +0.3V are supported for DC signal.
15. Absolute minimum level for VIN signal is -0.3V.
16. The "voltage differential" refers to the difference between the lowest and highest voltages across all supplies within the supply group as defined under Condition column.
17. On slow ramps, the RESET_B pin may be observed to be asserted multiple times during the supply ramping if the RESET_B pin is not being driven low by the PMIC during this time as recommended.
18. The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage equals the supply plus the voltage drop across the internal ESD diode from I/O pin to supply.
19. IINJ_D specifications are per pin for an unpowered condition of the associated supply. The maximum simultaneous injection per supply is 30mA.
20. The SAR ADC electrical specifications are not guaranteed during any period when the operating injection current limit is violated. These specifications are at maximum Tj and VREFH_ADC=1.8V; the injected current will reduce with reduced Tj.

The “fuse setting” values/conditions in above table correspond with the DIE_PROCESS[1:0] fuses which NXP programs during manufacturing. See Reference Manual and it’s Fuse Map for further details about the purpose. Example: Value “b01” represents DIE_PROCESS[1]=0 and DIE_PROCESS[0]=1”.

The device hardware design guide summarizes mandatory board design rules in table “Decoupling caps values” and section “PDN (Power Delivery Network) Guidelines".

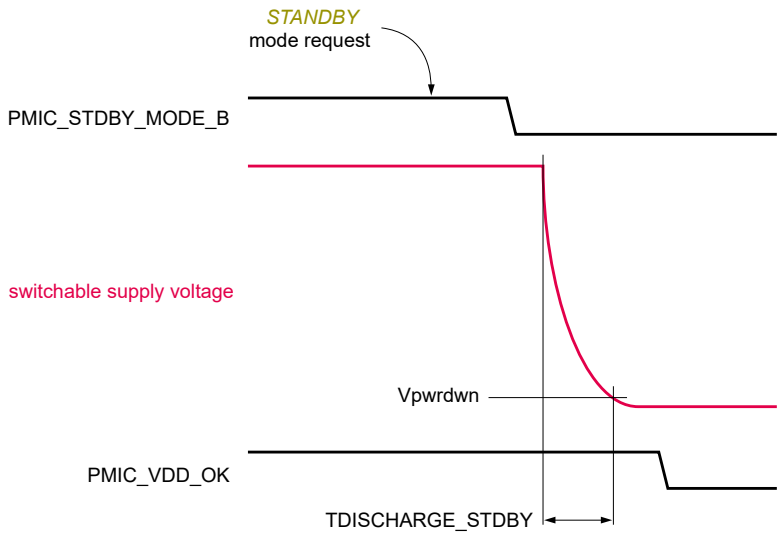

Figure 4. TDISCHARGE STDBY definition

7.2 Clock frequency ranges

The following table gives the frequency range minimum and maximums to use when programming the clock dividers on the device.

Table 5. Clock frequency ranges

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fA53_CORE_DIV2_CLK	Cortex-A53 core div2 clock frequency	24	—	500	MHz	A53_CORE_DIV2_CLK	—
fA53_CORE_DIV10_CLK	Cortex-A53 core div10 clock frequency	4.8	—	100	MHz	A53_CORE_DIV10_CLK	—
fLBIST_CLK	LBIST[7:0] clock frequency	—	—	50	MHz	LBIST_CLK[7:0]	—
fXBAR_CLK	XBAR clock frequency	24	—	400	MHz	XBAR_CLK	—
fXBAR_DIV2_CLK	XBAR div2 clock frequency	12	—	200	MHz	XBAR_DIV2_CLK	—
fXBAR_DIV3_CLK	XBAR div3 clock frequency	8	—	133	MHz	XBAR_DIV3_CLK	—
fXBAR_DIV4_CLK	XBAR div4 clock frequency	6	—	100	MHz	XBAR_DIV4_CLK	—
fDAPB_CLK	Debug clock frequency	—	—	133	MHz	fDAPB_CLK	—
fFRAY_CHI	FlexRay CHI clock frequency	—	—	133	MHz	—	—
fXBAR_DIV6_CLK	XBAR div6 clock frequency	4	—	66.7	MHz	XBAR_DIV6_CLK	—
fSERDES_REF_CLK	SERDES reference clock frequency	100	—	125	MHz	SERDES_REF_CLK	—
fPER_CLK	Peripheral clock frequency	—	—	80	MHz	PER_CLK	—
fFTM_0_EXT_CLK	FlexTimer 0 external clock frequency	—	—	20	MHz	FTM_0_EXT_CK	—
fFTM_1_EXT_CLK	FlexTimer 1 external clock frequency	—	—	20	MHz	FTM_1_EXT_CLK	—
fFLEXRAY_PE_CLK	FlexRay PE clock frequency	—	—	40	MHz	FLEXRAY_PE_CLK	—
fCAN_PE_CLK	CAN PE clock frequency	40	—	80	MHz	CAN_PE_CLK	—
fLIN_BAUD_CLK	LIN baud clock frequency	—	—	133	MHz	LIN_BAUD_CLK	—
fLINFLEXD_CLK	LIN clock frequency	—	—	66.7	MHz	LINFLEXD_CLK	—
fGMAC_TS_CLK	GMAC timestamp clock frequency	5	—	200	MHz	GMAC_TS_CLK	—

Table continues on the next page...

Table 5. Clock frequency ranges (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fGMAC_0_TX_CLK	GMAC_0 transmit clock frequency	2.5	—	125	MHz	GMAC_0_TX_CLK	—
fGMAC_0_RX_CLK	GMAC_0 receive clock frequency	2.5	—	125	MHz	GMAC_0_RX_CLK	—
fGMAC_0_REF_CLK	GMAC_0 reference clock frequency	—	—	50	MHz	GMAC_0_REF_CLK	—
fPFE_MAC_0_TX_CLK	PFE MAC_0 transmit clock frequency	2.5	—	312.5	MHz	PFE_MAC_0_TX_CLK	—
fPFE_MAC_0_RX_CLK	PFE MAC_0 receive clock frequency	2.5	—	312.5	MHz	PFE_MAC_0_RX_CLK	—
fPFE_MAC_0_REF_CLK	PFE MAC_0 reference clock frequency	—	—	50	MHz	PFE_MAC_0_REF_CLK	—
fPFE_MAC_1_TX_CLK	PFE MAC_1 transmit clock frequency	2.5	—	125	MHz	PFE_MAC_1_TX_CLK	—
fPFE_MAC_1_RX_CLK	PFE MAC_1 receive clock frequency	2.5	—	125	MHz	PFE_MAC_1_RX_CLK	—
fPFE_MAC_1_REF_CLK	PFE MAC_1 reference clock frequency	—	—	50	MHz	PFE_MAC_1_REF_CLK	—
fPFE_MAC_2_TX_CLK	PFE MAC_2 transmit cloc k frequency	2.5	—	125	MHz	PFE_MAC_2_TX_CLK	—
fPFE_MAC_2_RX_CLK	PFE MAC_2 receive clock frequency	2.5	—	125	MHz	PFE_MAC_2_RX_CLK	—
fPFE_MAC_2_REF_CLK	PFE MAC_2 reference clock frequency	—	—	50	MHz	PFE_MAC_2_REF_CLK	—
fSPI_CLK	SPI clock frequency	10	—	100	MHz	SPI_CLK	—
fQSPI_2X_CLK	QSPI 2X clock frequency	—	—	400	MHz	QSPI_2X_CLK - DDR 200MHz	—
fQSPI_2X_CLK	QSPI 2X clock frequency	—	—	333	MHz	QSPI_2X_CLK - DDR 166MHz	—
fQSPI_2X_CLK	QSPI 2X clock frequency	—	—	266	MHz	QSPI_2X_CLK - DDR / SDR 133MHz	—
fQSPI_2X_CLK	QSPI 2X clock frequency	—	—	208	MHz	QSPI_2X_CLK - SDR 104MHz	—

Table continues on the next page...

Table 5. Clock frequency ranges (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fQSPI_2X_CLK	QSPI 2X clock frequency	—	—	200	MHz	QSPI_2X_CLK - SDR 100MHz	—
fQSPI_2X_CLK	QSPI 2X clock frequency	—	—	133	MHz	QSPI_2X_CLK - DDR 66MHz	—
fQSPI_1X_CLK	QSPI 1X clock frequency	—	—	200	MHz	QSPI_1X_CLK - DDR 200MHz	—
fQSPI_1X_CLK	QSPI 1X clock frequency	—	—	166	MHz	QSPI_1X_CLK - DDR 166MHz	—
fQSPI_1X_CLK	QSPI 1X clock frequency	—	—	133	MHz	QSPI_1X_CLK - DDR / SDR 133MHz	—
fQSPI_1X_CLK	QSPI 1X clock frequency	—	—	104	MHz	QSPI_1X_CLK - SDR 104MHz	—
fQSPI_1X_CLK	QSPI 1X clock frequency	—	—	100	MHz	QSPI_1X_CLK - SDR 100MHz	—
fQSPI_1X_CLK	QSPI 1X clock frequency	—	—	66	MHz	QSPI_1X_CLK - DDR 66MHz	—
fSDHC_CLK	uSDHC clock frequency	133	—	200	MHz	SDHC_CLK - DDR HS400	—
fSDHC_CLK	uSDHC clock frequency	—	—	200	MHz	SDHC_CLK - SDR HS200	—
fSDHC_CLK	uSDHC clock frequency	—	—	100	MHz	SDHC_CLK - SDR 100MHz	—
fSDHC_CLK	uSDHC clock frequency	—	—	52	MHz	SDHC_CLK - DDR / SDR 52MHz	—
fPFE_PE_CLK	PFE PE clock frequency	—	—	600	MHz	PFE_PE_CLK	—
fPFE_SYS_CLK	PFE system clock frequency	—	—	300	MHz	PFE_SYS_CLK	—

8 Thermal Characteristics

Thermal characteristics are targets based on simulation from preliminary die and package definitions. The specified characteristics are subject to change per final device design and characterization. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

Table 6. Thermal Resistance

Board type [1]	Symbol	Description	Value	Unit
JESD51-9, 2s2p	$R_{\theta JA}$	Junction to ambient Thermal Resistance[2]	16.5	°C/W

Table continues on the next page...

Table 6. Thermal Resistance (continued)

Board type [1]	Symbol	Description	Value	Unit
JESD51-9, 2s2p	Ψ_{JT}	Junction to Lid Top Thermal Resistance[3]	0.1	°C/W

1. Thermal test board meets JEDEC specification for this package (JESD51-9).
2. Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
3. Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

9 DC Electricals

9.1 Total power specifications for 0.8V and 1.8V Analog Domains

The following table contains the individual max and thermal 0.8V power figures for each device in the S32G2 family as well as a 1.8V analog total which applies to all devices. For I/O power specifications please see dedicated I/O table.

Table 7. Total power specifications for 0.8V and 1.8V Analog Domains

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	0.8V Supply Rail Power: S32G274A Max Usecase [1]	—	—	4.5	W	Tj=125C, Sum of VDD, VDD_STBY, VDD_VP_PCIE0/1, VDD_LV_PLL, VDD_LV_PLL_DDR0, VDD_LV_PLL_AUR	—
—	0.8V Supply Rail Power: S32G274A Thermal Usecase [2]	—	—	4.36	W	Tj=125C, Sum of VDD, VDD_STBY, VDD_VP_PCIE0/1, VDD_LV_PLL, VDD_LV_PLL_DDR0, VDD_LV_PLL_AUR	—
—	0.8V Supply Rail Power: S32G254A Max Usecase [1, 3]	—	—	4.37	W	Tj=125C, Sum of VDD, VDD_STBY, VDD_VP_PCIE0/1, VDD_LV_PLL, VDD_LV_PLL_DDR0, VDD_LV_PLL_AUR	—
—	0.8V Supply Rail Power: S32G254A Thermal Usecase [2, 3]	—	—	4.22	W	Tj=125C, Sum of VDD, VDD_STBY, VDD_VP_PCIE0/1, VDD_LV_PLL, VDD_LV_PLL_DDR0, VDD_LV_PLL_AUR	—

Table continues on the next page...

Table 7. Total power specifications for 0.8V and 1.8V Analog Domains (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	0.8V Supply Rail Power: S32G233A Max Usecase [1, 3]	—	—	4.25	W	Tj=125C, Sum of VDD, VDD_STBY, VDD_VP_PCIE0/1, VDD_LV_PLL, VDD_LV_PLL_DDR0, VDD_LV_PLL_AUR	—
—	0.8V Supply Rail Power: S32G233A Thermal Usecase [2, 3]	—	—	4.16	W	Tj=125C, Sum of VDD, VDD_STBY, VDD_VP_PCIE0/1, VDD_LV_PLL, VDD_LV_PLL_DDR0, VDD_LV_PLL_AUR	—
—	0.8V Supply Rail Power: S32G234M Max Usecase [1, 3]	—	—	3.79	W	Tj=125C, Sum of VDD, VDD_STBY, VDD_VP_PCIE0/1, VDD_LV_PLL, VDD_LV_PLL_DDR0, VDD_LV_PLL_AUR	—
—	0.8V Supply Rail Power: S32G234M Thermal Usecase [2, 3]	—	—	3.67	W	Tj=125C, Sum of VDD, VDD_STBY, VDD_VP_PCIE0/1, VDD_LV_PLL, VDD_LV_PLL_DDR0, VDD_LV_PLL_AUR	—
—	1.8V Analog Supply Rail power: All devices [4]	—	—	0.135	W	Tj=125C, Sum of VDD_FXOSC, VDD_HV_PLL_AUR, VDD_HV_PLL_DDR0, VDD_ADC, VREFH_ADC0/1, VDD_FIRC, VDD_VREF, VDD_HV_PLL, VDD_TMU, VDD_DDR0	—

1. Max usecase: This is provided for power supply design. It is the realistic peak power consumption in an application. Shall only be maintained for a very short time (approx. 100us).
2. Thermal usecase: This is provided for designing a thermal solution. This is a realistic maximum sustained usecase which would be maintained for a longer duration.
3. Note that during Self Test execution, the power consumption for this device could exceed the stated spec. The S32G274A device Max Usecase spec will apply for the duration of the self test.
4. 1.8V total does not include additional consumption during a fuse programming operation. See IDD_EFUSE_PGM spec for max additional current.

NOTE

If SVS is used then VDD can be 0.77V. The MAX and THERMAL specs will be unchanged.

9.2 Static power specifications for I/O Domains

The following table contains the static power consumption for each I/O power domain. This data does not include the usage dependent dynamic current of GPIO-pins. To estimate the dynamic GPIO current for a specific use-case, an IO calculator tool is available. For IO calculator, contact your NXP sales representative. The "Device Power and Operating Current Specifications" table contains pre-calculated total I/O power (static + dynamic) for common usecases.

Table 8. Static power specifications for I/O Domains

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
SPVDD_IO_A	3.3V Static Power on VDD_IO_A	—	—	1	mW	VDD_IO_A = 3.3V	—
SPVDD_IO_B	3.3V Static Power on VDD_IO_B	—	—	1.3	mW	VDD_IO_B = 3.3V	—
SPVDD_IO_STBY	3.3V Static Power on VDD_IO_STBY	—	—	2.4	mW	VDD_IO_STBY = 3.3V	—
SPVDD_IO_SDHC	3.3V Static Power on VDD_IO_SDHC	—	—	155	mW	VDD_IO_SDHC = 3.3V	—
SPVDD_IO_SDHC	1.8V Static Power on VDD_IO_SDHC	—	—	58	mW	VDD_IO_SDHC = 1.8V	—
SPVDD_IO_ GMAC0	3.3V Static Power on VDD_IO_GMAC0	—	—	154	mW	VDD_IO_GMAC0 = 3.3V	—
SPVDD_IO_ GMAC0	1.8V Static Power on VDD_IO_GMAC0	—	—	55	mW	VDD_IO_GMAC0 = 1.8V	—
SPVDD_IO_ GMAC1	3.3V Static Power on VDD_IO_GMAC1	—	—	150	mW	VDD_IO_GMAC1 = 3.3V	—
SPVDD_IO_ GMAC1	1.8V Static Power on VDD_IO_GMAC1	—	—	55	mW	VDD_IO_GMAC1 = 1.8V	—
SPVDD_IO_USB	3.3V Static Power on VDD_IO_USB	—	—	147	mW	VDD_IO_USB = 3.3V	—
SPVDD_IO_USB	1.8V Static Power on VDD_IO_USB	—	—	53.5	mW	VDD_IO_USB = 1.8V	—
SPVDD_IO_QSPI	1.8V Static Power on VDD_IO_QSPI	—	—	0.9	mW	VDD_IO_QSPI = 1.8V	—
SPVDD_IO_ CLKOUT	1.8V Static Power on VDD_IO_CLKOUT	—	—	0.9	mW	VDD_IO_CLKOUT = 1.8V	—
SPVDD_IO_PCIE0	1.8V Static Power on VDD_IO_PCIE0	—	—	2.6	mW	VDD_IO_PCIE0 = 1.8V	—
SPVDD_IO_PCIE1	1.8V Static Power on VDD_IO_PCIE1	—	—	2.6	mW	VDD_IO_PCIE1 = 1.8V	—
SPVDD_IO_AUR	1.8V Static Power on VDD_IO_AUR	—	—	1.1	mW	VDD_IO_AUR = 1.8V	—

Table continues on the next page...

Table 8. Static power specifications for I/O Domains (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
SPVDD_IO_DDR	1.1V Static Power on VDD_IO_DDR - LPDDR4	—	—	8.2	mW	VDD_IO_DDR = 1.1V	—
SPVDD_IO_DDR	1.35V Static Power on VDD_IO_DDR - DDR3L	—	—	10.1	mW	VDD_IO_DDR = 1.35V	—

9.3 Device Power and Operating Current Specifications

The device power consumption, operating current, and applicable conditions are given in the following table.

NOTE

All measurements are at Tj=125C, unless otherwise specified.

Table 9. Device Power and Operating Current Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
PVDD_STBY	Standby mode core supply power	—	48	—	uW	Ta = 25C, VDD = 0.8V, typical silicon, all pull up/down disabled	—
PVDD_IO_STBY	Standby mode I/O supply power [1]	—	120	—	uW	Ta = 25C, VDD_IO_STBY = 3.0V, typical silicon, all pull up/down disabled	—
IDD_FXOSC	VDD_FXOSC operating current	—	0.6	—	mA	1.8V, 40MHz	—
IDD_HV_PLL_AUR	VDD_HV_PLL_AUR operating current	—	4.3	—	mA	1.8V, fPLL_VCO = 5GHz	—
IDD_HV_PLL_DDR0	VDD_HV_PLL_DDR0 operating current (DDR reference PLL only)	—	2	—	mA	fPLL_DDR_PHI0 = 800MHz, fDDR_PLL = 1600MHz, 1.8V	—
IDD_ADC	VDD_ADC operating current	—	1.8	—	mA	1.8V, 2 ADCs @ 1Msps	—
IDD_ADC	VDD_ADC operating current	—	200	—	uA	1.8V, Disabled (per ADC)	—
IVREFH_ADC	VREFH_ADC operating current	—	210	—	uA	VREFH_ADC = 1.8V	—
IDD_FIRC	VDD_FIRC operating current	—	0.6	—	mA	FIRC trimmed frequency (48MHz typical)	—

Table continues on the next page...

Table 9. Device Power and Operating Current Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IDD_VREF	VDD_VREF operating current	—	0.7	—	mA	1.8V	—
IDD_HV_PLL	VDD_HV_PLL operating current	—	8.9	—	mA	1.8V, fPLL_VCO = 2GHz, Core / Peripheral/Acclerator PLLs	—
IDD_EFUSE_PGM	VDD_EFUSE programming current	—	—	140	mA	VDD_EFUSE=1.8V, VDD=0.8V	—
IDD_TMU	VDD_TMU operating current	—	4.6	—	mA	1.8V, central unit and remote sensors operating	—
IDD_DDR0	VDD_DDR0 operating current	—	5.0	—	mA	1.8V, fPLL_DDR_PHI0 = 800MHz, fDDR_PLL = 1600MHz	—
PVDD_IO_PCIEn	VDD_IO_PCIE0 operating power	—	—	76	mW	All circuits enabled, VDD_IO_PCIEn=1.8V, Gen3 8Gbps, 2 lanes. Per IP instance	—
PVDD_IO_PCIEn	VDD_IO_PCIE0 operating power	—	—	72	mW	All circuits enabled, VDD_IO_PCIEn=1.8V, Gen2.1 5Gbps, 2 lanes. Per IP instance	—
PVDD_IO_PCIEn	VDD_IO_PCIE0 operating power	—	—	68	mW	All circuits enabled, VDD_IO_PCIEn=1.8V, Gen1.1 2.5Gbps, 2 lanes. Per IP instance	—
PVDD_IO_PCIEn	VDD_IO_PCIE0 operating power	—	—	1.4	mW	Powered down state, VDD_IO_PCIEn=1.8V, Per IP instance	—
PVDD_IO_DDR	VDD_IO_DDR 100% write operating power	—	—	625	mW	LPDDR4, VDD_IO_DDR = 1.1V, 3200 MT/s, 100% write, 1/2 data lines switching, 60 Ohm transmit termination driving a 60 Ohm load	—
PVDD_IO_DDR_IDLE	VDD_IO_DDR idle power	—	55	—	mW	LPDDR4, VDD_IO_DDR = 1.1V, Tj = 25C	—
PVDD_IO_DDR_RET	VDD_IO_DDR data retention power	—	0.02	—	mW	LPDDR4, VDD_IO_DDR = 1.1V, Standby mode and DRAM in self-refresh, Tj=25C.	—

Table continues on the next page...

Table 9. Device Power and Operating Current Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
PVDD_IO_DDR_RET	VDD_IO_DDR data retention power	—	0.030	—	mW	DDR3L, VDD_IO_DDR = 1.35V, Standby mode and DRAM in self-refresh, Tj=25C.	—
PVDD_IO_DDR	VDD_IO_DDR 100% write operating power	—	—	598	mW	DDR3L, VDD_IO_DDR = 1.35V, 1600 MT/s, 100% Write operation, 1/2 data lines switching, 60 Ohm transmit termination driving a 60 ohm load	—
PVDD_IO_DDR_IDLE	VDD_IO_DDR idle power	—	57	—	mW	DDR3L, VDD_IO_DDR = 1.35V, Tj=25C	—
PVDD_IO_QSPI	QSPI A I/O voltage supply operating power	—	58	—	mW	1.8V, 200MHz - clocks 100% activity rate, 50% data rate, 1/2 data switching per cycle, does not include power for other I/O ins on the VDD_IO_QSPI supply. 15.5pF.	—
PVDD_IO_SDHC	VDD_IO_SDHC operating power	—	128	—	mW	1.8V, HS400, SD_CLK 100%, SD_D(8) 50%, 1/2 data switching per cycle, does not include power for other I/O pins on the VDD_IO_SDHC supply, 15.5pF	—
PVDD_IO_GMACn	VDD_IO_GMACn operating power	—	81	—	mW	1.8V, RGMII 125MHz, 100% clock rate, 50% data rate, 1/2 data switching per cycle, per IP instance, does not include power for other I/O pins on the VDD_IO_GMACn supply. 15.5pF	—
PVDD_IO_GMACn	VDD_IO_GMACn operating power	—	292	—	mW	3.3V, RGMII 125MHz, 100% clock rate, 50% data rate, 1/2 data switching per cycle, per IP instance, does not include power for other I/O pins on	—

Table continues on the next page...

Table 9. Device Power and Operating Current Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
						the VDD_IO_GMACn supply, 15.5pF.	
PVDD_IO_USB_TYP	USB I/O voltage supply operating power	—	59	—	mW	1.8V, modem - 8 outputs @60MHz, 50% data rate, 1/2 data switching per cycle, does not include power for other I/O pins on the VDD_IO_USB supply. 15.5pF.	—
PVDD_IO_USB_TYP	USB I/O voltage supply operating power	—	174	—	mW	3.3V, modem - 8 outputs @60MHz, 50% data rate, 1/2 data switching per cycle, does not include power for the other I/O pins on the VDD_IO_USB supply. 15.5pF	—
PVDD_IO_AUR	Aurora I/O voltage supply operating power	—	164	—	mW	1.8V, 5Gbps on 4 lanes, 50% Activity Rate, 1/2 data switching per cycle	—

1. This spec includes the consumption on pins in VDD_STBY_IO domain only. See the hardware design guide for more details.

10 Power Sequencing

The following sequence has been validated by NXP and is to be followed when powering up the device. Each supply within a step must be within its specified operating voltage range before the next step in the sequence is started, except as noted below.

1. Set POR_B input to low value.

2. Ramp up VDD_IO_STBY supply.

VDD_IO_B can optionally be included with VDD_IO_STBY in the first step.

3. Ramp up all GPIO supplies powered to 3.3V.

4. Ramp up all 1.8V supplies including GPIO supplies powered to 1.8V

Step 5 and 6 can commence in the following sequence prior to all 1.8V supplies reaching DC tolerance. Step 5 must still reach DC tolerance before Step 6.

5. Ramp up VDD_DDR_IO supply

6. Ramp up all 0.8V supplies

7. Set POR_B and PMIC_VDD_OK inputs to high value once all supplies have reached their specified levels.

NOTE

It is acceptable for the 1.8V supplies to not yet be within their specified range at the time of asserting the PMIC_VDD_OK input when exiting Standby mode if it is ensured that they are within their specified range no later than 140 us after the PMIC_VDD_OK input assertion.

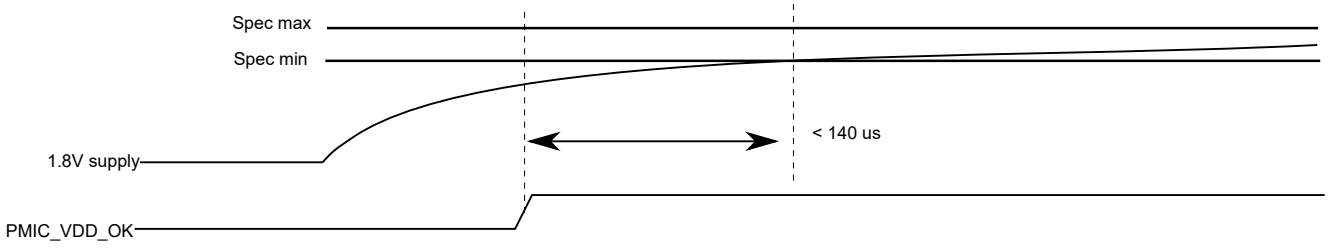

Figure 5. 1.8V supply timing with respect to PMIC_VDD_OK during Standby Mode Exit

NOTE

W hile powering up the device, the VDD_EFUSE supply pin must be kept powered down. While the device is already powered up, the VDD_EFUSE supply pin can be powered up/down independent of the other supplies on the device. The VDD_EFUSE supply pin must be powered down prior to Standby mode entry or, at the latest, powered down together with the other 1.8V supplies during Standby mode entry.

Table 10. Power Sequencing

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Vpwrdwn	Maximum voltage on a supply pin in powerdown mode	—	—	100	mV	—	—

The power-up sequence on Standby exit is the same except that only the switchable supplies that were powered down during Standby mode are ramped up again, and the POR_B input is kept high throughout the sequence.

11 Electromagnetic compatibility (EMC)

EMC measurements to IC-level IEC standards are available from NXP Semiconductor on request.

12 I/O Pad Characteristics

12.1 GPIO Pads

Table 11. GPIO Pads

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIH	Input high level DC voltage threshold	0.7 * VDD_IO_*	—	—	V	1.8V / 3.3V	—
VIL	Input low level DC voltage threshold	—	—	0.3 * VDD_IO_*	V	1.8V / 3.3V	—
VHYS_33	3.3V GPIO input hysteresis voltage	100	—	—	mV	Always enabled.	—
ILKG_18	1.8V GPIO pad input leakage current	-17	—	17	uA	1.8V, Tj = 125C	—

Table continues on the next page...

Table 11. GPIO Pads (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
ILKG_33	3.3V GPI / GPIO pad input leakage current	-30	—	30	uA	3.3V, Tj = 125C	—
ILKG_3318	1.8V/3.3V GPIO pad input leakage current (3.3V)	-50	—	50	uA	3.3V, Tj = 125C	—
ILKG_3318	1.8V/3.3V GPIO pad input leakage current (1.8V)	-17	—	17	uA	1.8V, Tj = 125C	—
CIN_18	Input capacitance (1.8V GPIO)	—	6	8	pF	—	—
CIN_33	Input capacitance (3.3V GPI / GPIO)	—	7	11	pF	—	—
CIN_3318	Input capacitance (1.8V/3.3V GPIO)	—	7	11	pF	—	—
ISLEW	Input signal slew rate [1]	1	—	4	V/ns	—	—
ITR_TF	Input signal rise/fall time [1, 2]	0.5	—	2	ns	—	—
TPW_MIN	Input minimum pulse width	2	—	—	ns	—	—
FMAX_IN_18	1.8V GPIO maximum input frequency [3]	—	—	50	MHz	CMOS Receiver	—
FMAX_IN_18	1.8V GPIO maximum input frequency [3]	—	—	208	MHz	VREF Receiver	—
FMAX_IN_3318	1.8V/3.3V GPIO maximum input frequency [3]	—	—	208	MHz	1.8V	—
FMAX_IN_3318	1.8V/3.3V GPIO maximum input frequency [3]	—	—	166.7	MHz	3.3V	—
FMAX_IN_33	3.3V GPIO maximum input frequency [3]	—	—	50	MHz	—	—
IPU_18	1.8V GPIO pull up/ down resistance	9	18	23	kΩ	pull up @ 0.3 * VDD_HV_IO, pull down @ 0.7 * VDD_HV_IO	—
IPU_33	3.3V GPIO pull up/ down resistance	9	18	23	kΩ	pull up @ 0.3 * VDD_HV_IO, pull down @ 0.7 * VDD_HV_IO	—

Table continues on the next page...

Table 11. GPIO Pads (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IPU_3318	1.8V/3.3V GPIO pull up/down resistance	9	18	23	kΩ	pull up @ 0.3 * VDD_HV_IO, pull down @ 0.7 * VDD_HV_IO	—
RDSON_18	1.8V GPIO output impedance (NMOS & PMOS) [4]	27.0	36.3	48.0	Ω	SRE[2:0] = xxx, 50% * VDD_IO_*	—
RDSON_3318	1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 1.8V [4]	18.0	30.0	43.0	Ω	SRE[2:0] = 000, 50% * VDD_IO_*	—
RDSON_3318	1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 1.8V [4]	19.0	30.0	44.0	Ω	SRE[2:0] = 100, 50% * VDD_IO_*	—
RDSON_3318	1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 1.8V [4]	21.0	33.0	49.0	Ω	SRE[2:0] = 101, 50% * VDD_IO_*	—
RDSON_3318	1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 1.8V [4]	23.0	37.5	58.0	Ω	SRE[2:0] = 110, 50% * VDD_IO_*	—
RDSON_3318	1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 1.8V [4]	24.0	37.5	57.0	Ω	SRE[2:0] = 111, 50% * VDD_IO_*	—
RDSON_3318	1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 3.3V [4]	18.0	30.0	43.0	Ω	SRE[2:0] = 000, 50% * VDD_IO_*	—
RDSON_3318	1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 3.3V [4]	19.0	30.0	44.0	Ω	SRE[2:0] = 100, 50% * VDD_IO_*	—
RDSON_3318	1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 3.3V [4]	21.0	33.4	50.0	Ω	SRE[2:0] = 101, 50% * VDD_IO_*	—
RDSON_3318	1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 3.3V [4]	23.0	39.5	61.0	Ω	SRE[2:0] = 110, 50% * VDD_IO_*	—

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Table 11. GPIO Pads (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
RDSON_3318	1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 3.3V [4]	26.0	39.5	61.0	Ω	SRE[2:0] = 111, 50% * VDD_IO_*	—
RDSON_33	3.3V GPIO output impedance (NMOS & PMOS) [4]	16.5	26.5	42.0	Ω	SRE[2:0] = 000, 50% * VDD_IO_*	—
RDSON_33	3.3V GPIO output impedance (NMOS & PMOS) [4]	16.5	26.5	42.0	Ω	SRE[2:0] = 100, 50% * VDD_IO_*	—
RDSON_33	3.3V GPIO output impedance (NMOS & PMOS) [4]	19.2	30.5	49.5	Ω	SRE[2:0] = 101, 50% * VDD_IO_*	—
RDSON_33	3.3V GPIO output impedance (NMOS & PMOS) [4]	24.5	38.0	61.5	Ω	SRE[2:0] = 110, 50% * VDD_IO_*	—
RDSON_33	3.3V GPIO output impedance (NMOS & PMOS) [4]	32.0	48.0	75.5	Ω	SRE[2:0] = 111, 50% * VDD_IO_*	—
IOH_18	1.8V GPIO output high current [4]	-15.0	—	-6.0	mA	SRE[2:0] = xxx, 80% * VDD_IO_*	—
IOL_18	1.8V GPIO output low current [4]	6.0	—	15.0	mA	SRE[2:0] = xxx, 20% * VDD_IO_*	—
IOH_3318	1.8V/3.3V GPIO output high current at 1.8V [4]	-22	—	-8	mA	SRE[2:0] = 000, 80% * VDD_IO_*	—
IOH_3318	1.8V/3.3V GPIO output high current at 1.8V [4]	-21	—	-8	mA	SRE[2:0] = 100, 80% * VDD_IO_*	—
IOH_3318	1.8V/3.3V GPIO output high current at 1.8V [4]	-19	—	-6	mA	SRE[2:0] = 101, 80% * VDD_IO_*	—
IOH_3318	1.8V/3.3V GPIO output high current at 1.8V [4]	-17	—	-6	mA	SRE[2:0] = 110, 80% * VDD_IO_*	—
IOH_3318	1.8V/3.3V GPIO output high current at 1.8V [4]	-17	—	-6	mA	SRE[2:0] = 111, 80% * VDD_IO_*	—
IOL_3318	1.8V/3.3V GPIO output low current at 1.8V [4]	8	—	22	mA	SRE[2:0] = 000, 20% * VDD_IO_*	—

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Table 11. GPIO Pads (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IOL_3318	1.8V/3.3V GPIO output low current at 1.8V [4]	8	—	21	mA	SRE[2:0] = 100, 20% * VDD_IO_*	—
IOL_3318	1.8V/3.3V GPIO output low current at 1.8V [4]	6	—	20	mA	SRE[2:0] = 101, 20% * VDD_IO_*	—
IOL_3318	1.8V/3.3V GPIO output low current at 1.8V [4]	6	—	18	mA	SRE[2:0] = 110, 20% * VDD_IO_*	—
IOL_3318	1.8V/3.3V GPIO output low current at 1.8V [4]	6	—	17	mA	SRE[2:0] = 111, 20% * VDD_IO_*	—
IOH_3318	1.8V/3.3V GPIO output high current at 3.3V [4]	-40	—	-14	mA	SRE[2:0] = 000, 80% * VDD_IO_*	—
IOH_3318	1.8V/3.3V GPIO output high current at 3.3V [4]	-40	—	-14	mA	SRE[2:0] = 100, 80% * VDD_IO_*	—
IOH_3318	1.8V/3.3V GPIO output high current at 3.3V [4]	-35	—	-10	mA	SRE[2:0] = 101, 80% * VDD_IO_*	—
IOH_3318	1.8V/3.3V GPIO output high current at 3.3V [4]	-32	—	-10	mA	SRE[2:0] = 110, 80% * VDD_IO_*	—
IOH_3318	1.8V/3.3V GPIO output high current at 3.3V [4]	-32	—	-10	mA	SRE[2:0] = 111, 80% * VDD_IO_*	—
IOL_3318	1.8V/3.3V GPIO output low current at 3.3V [4]	15	—	40	mA	SRE[2:0] = 000, 20% * VDD_IO_*	—
IOL_3318	1.8V/3.3V GPIO output low current at 3.3V [4]	15	—	40	mA	SRE[2:0] = 100, 20% * VDD_IO_*	—
IOL_3318	1.8V/3.3V GPIO output low current at 3.3V [4]	13	—	36	mA	SRE[2:0] = 101, 20% * VDD_IO_*	—
IOL_3318	1.8V/3.3V GPIO output low current at 3.3V [4]	12	—	33	mA	SRE[2:0] = 110, 20% * VDD_IO_*	—
IOL_3318	1.8V/3.3V GPIO output low current at 3.3V [4]	11	—	32	mA	SRE[2:0] = 111, 20% * VDD_IO_*	—

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Table 11. GPIO Pads (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IOH_33	3.3V GPIO output high current [4]	-40.1	—	-14.0	mA	SRE[2:0] = 000, 80% * VDD_IO_*	—
IOH_33	3.3V GPIO output high current [4]	-40.1	—	-14.0	mA	SRE[2:0] = 100, 80% * VDD_IO_*	—
IOH_33	3.3V GPIO output high current [4]	-36.2	—	-12.1	mA	SRE[2:0] = 101, 80% * VDD_IO_*	—
IOH_33	3.3V GPIO output high current [4]	-32.0	—	-10.3	mA	SRE[2:0] = 110, 80% * VDD_IO_*	—
IOH_33	3.3V GPIO output high current [4]	-29.0	—	-9.0	mA	SRE[2:0] = 111, 80% * VDD_IO_*	—
IOL_33	3.3V GPIO output low current [4]	14.6	—	39.4	mA	SRE[2:0] = 000, 20% * VDD_IO_*	—
IOL_33	3.3V GPIO output low current [4]	14.6	—	39.4	mA	SRE[2:0] = 100, 20% * VDD_IO_*	—
IOL_33	3.3V GPIO output low current [4]	13.0	—	35.5	mA	SRE[2:0] = 101, 20% * VDD_IO_*	—
IOL_33	3.3V GPIO output low current [4]	11.2	—	32.0	mA	SRE[2:0] = 110, 20% * VDD_IO_*	—
IOL_33	3.3V GPIO output low current [4]	10.0	—	29.0	mA	SRE[2:0] = 111, 20% * VDD_IO_*	—
FMAX_18	1.8V GPIO maximum output frequency [4, 5]	—	—	208	MHz	SRE[2:0] = 000	—
FMAX_18	1.8V GPIO maximum output frequency [4, 5]	—	—	150	MHz	SRE[2:0] = 100	—
FMAX_18	1.8V GPIO maximum output frequency [4, 5]	—	—	133	MHz	SRE[2:0] = 101	—
FMAX_18	1.8V GPIO maximum output frequency [4, 5]	—	—	100	MHz	SRE[2:0] = 110	—
FMAX_18	1.8V GPIO maximum output frequency [4, 5]	—	—	50	MHz	SRE[2:0] = 111	—
FMAX_33	3.3V GPIO maximum output frequency [4, 5]	—	—	50	MHz	SRE[2:0] = 100	—

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Table 11. GPIO Pads (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
FMAX_33	3.3V GPIO maximum output frequency [4, 5]	—	—	50	MHz	SRE[2:0] = 101, reduced slew relative to the SRE[2:0] = 100 setting for the same output load.	—
FMAX_33	3.3V GPIO maximum output frequency [4, 5]	—	—	50	MHz	SRE[2:0] = 110	—
FMAX_33	3.3V GPIO maximum output frequency [4, 5]	—	—	1	MHz	SRE[2:0] = 111	—
FMAX_3318	1.8V/3.3V GPIO maximum output frequency [4, 5]	—	—	208	MHz	SRE[2:0] = 000, 1.8V	—
FMAX_3318	1.8V/3.3V GPIO maximum output frequency [4, 5]	—	—	166.7	MHz	SRE[2:0] = 100, 1.8V	—
FMAX_3318	1.8V/3.3V GPIO maximum output frequency [4, 5]	—	—	150	MHz	SRE[2:0] = 101, 1.8V	—
FMAX_3318	1.8V/3.3V GPIO maximum output frequency [4, 5]	—	—	133.3	MHz	SRE[2:0] = 110, 1.8V	—
FMAX_3318	1.8V/3.3V GPIO maximum output frequency [4, 5]	—	—	100	MHz	SRE[2:0] = 111, 1.8V	—
FMAX_3318	1.8V/3.3V GPIO maximum output frequency [4, 5]	—	—	166.7	MHz	SRE[2:0] = 000, 3.3V	—
FMAX_3318	1.8V/3.3V GPIO maximum output frequency [4, 5]	—	—	150	MHz	SRE[2:0] = 100, 3.3V	—
FMAX_3318	1.8V/3.3V GPIO maximum output frequency [4, 5]	—	—	133.3	MHz	SRE[2:0] = 101, 3.3V	—
FMAX_3318	1.8V/3.3V GPIO maximum output frequency [4, 5]	—	—	100	MHz	SRE[2:0] = 110, 3.3V	—
FMAX_3318	1.8V/3.3V GPIO maximum output frequency [4, 5]	—	—	83.3	MHz	SRE[2:0] = 111, 3.3V	—

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Table 11. GPIO Pads (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TR_TF_3318	1.8V/3.3V GPIO rise/fall time at 1.8V [4, 5, 6]	1.0	—	5.5	V/ns	SRE[2:0] = 000	—
TR_TF_3318	1.8V/3.3V GPIO rise/fall time at 1.8V [4, 5, 6]	1.0	—	5.75	V/ns	SRE[2:0] = 100	—
TR_TF_3318	1.8V/3.3V GPIO rise/fall time at 1.8V [4, 5, 6]	0.75	—	4.75	V/ns	SRE[2:0] = 101	—
TR_TF_3318	1.8V/3.3V GPIO rise/fall time at 1.8V [4, 5, 6]	0.5	—	4.5	V/ns	SRE[2:0] = 110	—
TR_TF_3318	1.8V/3.3V GPIO rise/fall time at 1.8V [4, 5, 6]	0.5	—	4.0	V/ns	SRE[2:0] = 111	—
TR_TF_3318	1.8V/3.3V GPIO rise/fall time at 3.3V [4, 5, 6]	2.0	—	10.5	V/ns	SRE[2:0] = 000	—
TR_TF_3318	1.8V/3.3V GPIO rise/fall time at 3.3V [4, 5, 6]	2.0	—	9.25	V/ns	SRE[2:0] = 100	—
TR_TF_3318	1.8V/3.3V GPIO rise/fall time at 3.3V [4, 5, 6]	1.5	—	9.5	V/ns	SRE[2:0] = 101	—
TR_TF_3318	1.8V/3.3V GPIO rise/fall time at 3.3V [4, 5, 6]	0.75	—	7.5	V/ns	SRE[2:0] = 110	—
TR_TF_3318	1.8V/3.3V GPIO rise/fall time at 3.3V [4, 5, 6]	0.75	—	7.25	V/ns	SRE[2:0] = 111	—
TR_TF_18	1.8V GPIO rise/fall time [4, 5, 6]	0.75	—	3.75	V/ns	SRE[2:0] = 000	—
TR_TF_18	1.8V GPIO rise/fall time [4, 5, 6]	0.75	—	3.75	V/ns	SRE[2:0] = 100	—
TR_TF_18	1.8V GPIO rise/fall time [4, 5, 6]	0.75	—	3.25	V/ns	SRE[2:0] = 101	—
TR_TF_18	1.8V GPIO rise/fall time [4, 5, 6]	0.75	—	3.25	V/ns	SRE[2:0] = 110	—
TR_TF_18	1.8V GPIO rise/fall time [4, 5, 6]	0.25	—	3.25	V/ns	SRE[2:0] = 111	—
TR_TF_33	3.3V GPIO rise/fall time [4, 5, 6]	1.75	—	9.0	V/ns	SRE[2:0] = 000	—
TR_TF_33	3.3V GPIO rise/fall time [4, 5, 6]	1.75	—	9.0	V/ns	SRE[2:0] = 100	—
TR_TF_33	3.3V GPIO rise/fall time [4, 5, 6]	0.05	—	8.25	V/ns	SRE[2:0] = 101	—
TR_TF_33	3.3V GPIO rise/fall time [4, 5, 6]	0.01	—	7.0	V/ns	SRE[2:0] = 110	—

Table continues on the next page...

Table 11. GPIO Pads (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TR_TF_33	3.3V GPIO rise/fall time [4, 5, 6]	0.005	—	5.5	V/ns	SRE[2:0] = 111	—
VISE_33	3.3V GPIO pad indeterminate state end threshold	—	2.35	—	V	See 1.8V and 3.3V GPIO pad detailed behavior diagram below	—
VISE_3318	1.8V/3.3V GPIO pad indeterminate state end threshold	—	1.53	—	V	See 1.8V/3.3V GPIO pad detailed behavior diagram below	—
VISE_18	1.8V GPIO pad indeterminate state end threshold	—	0.6	—	V	See 1.8V and 3.3V GPIO pad detailed behavior diagram below	—

1. Fastest slew rate and lowest rise/fall time constraint required to meet high-speed interface timing such as QSPI, RGMII, and uSDHC. Slower input transitions can be used for input signals with slow switching rates (<40 MHz).
2. The ISLEW has precedence over ITR_TF if the ITR_TF violates the implied range for a given ISLEW.
3. Input slew rate and rise/fall time limits must be adhered to in conjunction with the max input frequency limits given for proper operation.
4. GPIO output transistion time information can be obtained from the device IBIS model. IBIS models are recommended for system level simulations, as discrete values for I/O transition times are not representative of the I/O pad behavior when connected to an actual transmission line load.
5. I/O timing specifications are valid for the un-terminated 50ohm transmission line reference load given in the figure below. A lumped 8pF load is assumed at the end of a 5 inch microstrip trace on standard FR4 with approximately 1.5pF/inch. For signals with frequency greater than 63MHz, a maximum 2 inch PCB trace is assumed. For best signal integrity, the series resistance in the transmission line should be matched closely to the selected RDSON of the I/O pad output.
6. Rise/fall time specifications are derived from simulation model for the defined operating points (between 20% and 80% of VDD_HV_IO level). Actual application rise/fall time should be extracted from IBIS model simulations with the microcontroller models and application PCB.

NOTE

In the Standby mode exit case, the rising edge of the PMIC_VDD_OK pin determines when the pads enter their 'POR value' state instead of the POR_B pin.

NOTE

VOH/VOL values should be calculated based on the provided RDSON, IOH/IOL values and IBIS models.

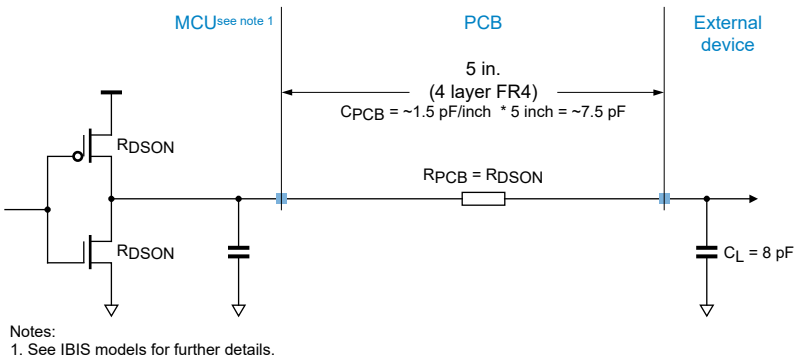


Figure 6. Reference Load Diagram

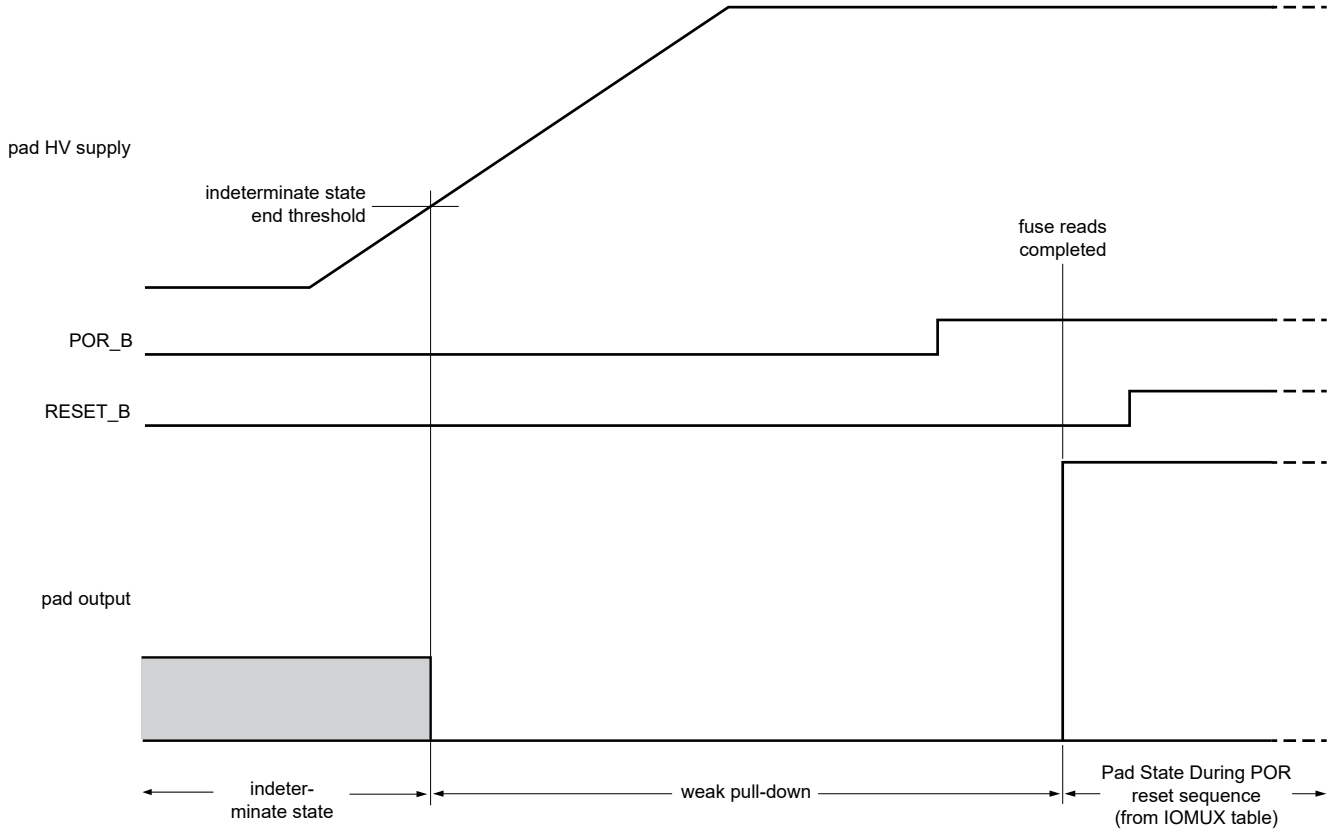


Figure 7. 1.8V/3.3V GPIO pad detailed behavior during power up

The weak pull-down is 100 Kohm and is separate from the usual selectable 12Kohm internal pull resistor. If the pad is in 3.3V mode and the IOMUX sheet defines the 'Pad State During POR reset sequence' as 'Hi-Z', the 100Kohm pull-down remains engaged until RESET_B is released.

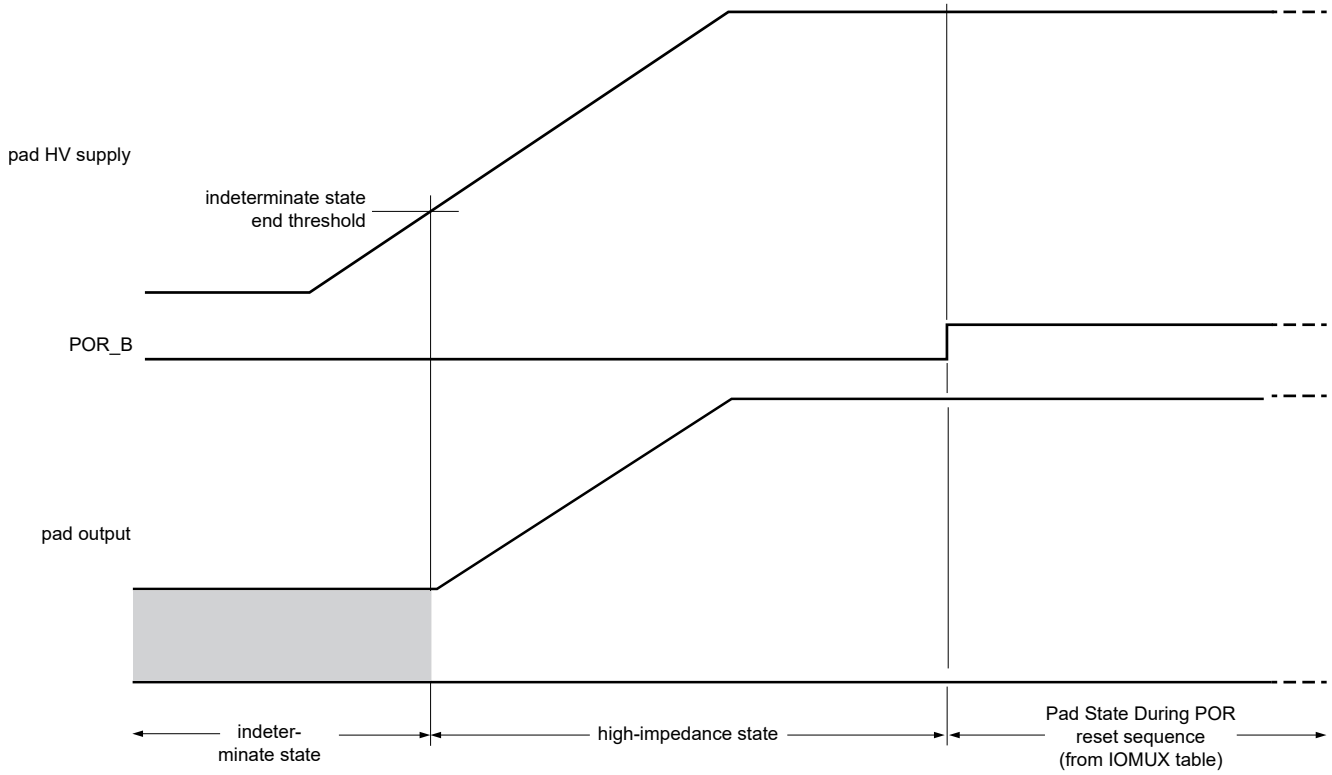


Figure 8. 1.8V and 3.3V GPIO pad detailed behavior during power up

The high-impedance state level is shown based on the external pull-up being on the corresponding pad supply.

13 Aurora specifications

13.1 Aurora Pads

Table 12. Aurora Pads

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fAURORA	Data Rate	0.05	—	5.0	Gbps	100Ω external termination (Not on board but inside receiver after AC coupling)	—
IDD_HV_AUR	Transmitter HV supply current consumption (No pre-emphasis)	18	22	31	mA	max fAURORA per active transmit lane	—
IDD_HV_AUR	Transmitter HV supply current consumption (pre-emphasis enabled ,	25	30	40	mA	max fAURORA per active transmit lane	—

Table continues on the next page...

Table 12. Aurora Pads (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	pre-emphasis gain=11)						
VOD_AURORA_AC	Transmitter Differential output voltage (end termination) [1, 2, 3]	400	600	900	mV	max fAURORA, 100Ω termination, 100Ω differential transmission line delay, matched network	—
VOD_AURORA_DC	DC range for the VOD (Transmitter Differential Output Voltage)	800	—	—	mV	ipp_obe=1 DC condition	—
VOD_AURORA_AC_PRE_EMPH	Transmitter Differential output voltage (end termination, preemph=11) [1, 2, 4]	600	900	1200	mV	max fAURORA, 100Ω termination, 100Ω differential transmission line delay, matched network	—
VCM_AURORA	Transmitter Common mode voltage	0.775	—	1.025	V	—	—
VCM_LVDS_RX	Receiver input signal common mode range	0.6	—	1.0	V	—	—
VDIFF_LVDS_RX	Receiver input differential signal	400	—	—	mV	—	—
CLOAD_AURORA	Maximum transmission line load (Lumped Load at any point on Tline)	—	—	0.1	pF	—	—
RTERM_AURORA	Internal termination resistance	80	100	130	Ohm	enabled	—
VSLEW_AURORA	Differential output slew rate	—	30	50	ps / 200mV	max fAURORA	—
TSTARTUP_AURORA	Transmitter startup time (assertion of ipp_obe to common mode settling of differential output)	—	—	500	ns	—	—
TEYE_AURORA	Valid data region (Including PLL Jitter for Aurora) [5]	0.55	—	—	UI	max fAURORA	—

Table continues on the next page...

Table 12. Aurora Pads (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VOH_AURORA	Transmitter output high indicator [6]	VDD_IO/ 2 + 0.2	—	—	V	100Ω termination at receiver end	—
VOL_AURORA	Transmitter output low indicator [6]	—	—	VDD_IO/ 2 - 0.2	V	100Ω termination at receiver end	—
PAD_P_BIAS	Pad_p voltage output level when Tx disabled	—	—	0.6	V	Ipp_obe_lv=0 Ipp_ term_en_lv=0	—
PAD_N_BIAS	Pad_n voltage output level when Tx disabled	1.1	—	—	V	Ipp_obe_lv=0 Ipp_ term_en_lv=0	—

1. When operating at max speed, there will be losses and differential output will be smaller as against DC condition. Aurora Interface Min differential swing is 400mV which is always guaranteed but the max limit is dependent on board design/ losses. For boards with negligible losses , if differential output (P-N) goes higher than 800mV (Aurora max differential input spec) , user must use “dual termination” scheme as highlighted in the Source Termination Circuit Figure to get the differential swing back within Range. The termination in the source side can be enabled through software in the transmitter pad design. Direct end termination without AC coupling is not allowed.
2. Termination scheme as shown in the End Termination Circuit Figure. Direct end termination without AC coupling is not allowed.
3. Differential output is with pre-emphasis disabled, and a 10mA output stage current.
4. Differential output is with pre-emphasis enabled, and a ~15mA avg output stage current
5. UI @ 5Gbps equals 200ps. The valid eye is expected to be > 110ps in width. ISI jitter spec is 20-30ps for the LVDS transmitter across PVT in a delay matched differential transmission line impedance of 100Ω.
6. VDD_IO maps to corresponding supply name on the device.

Termination scheme as shown in “End Termination Circuit” applies to debug tool hardware and is not recommended to be placed on the PC.

Source termination Circuit – Transmitter side 100 ohm termination is present inside the Tx pad and should not be placed on the PCB.

Direct 100 ohm board termination not allowed between AUR_TXn_N and AUR_TXn_N (n=0,1,2,3). Source termination is only allowed through the internal termination inside LVDS Tx pad.

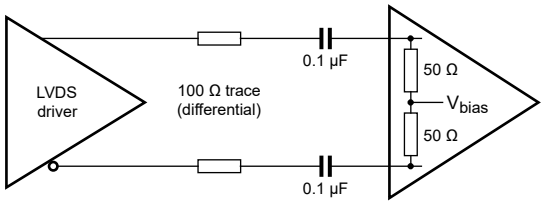


Figure 9. End Termination Circuit

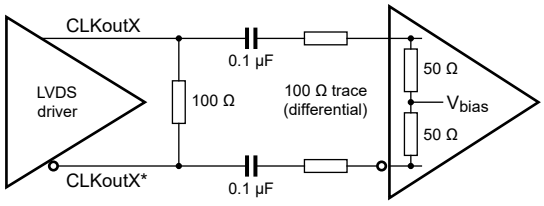


Figure 10. Source Termination Circuit

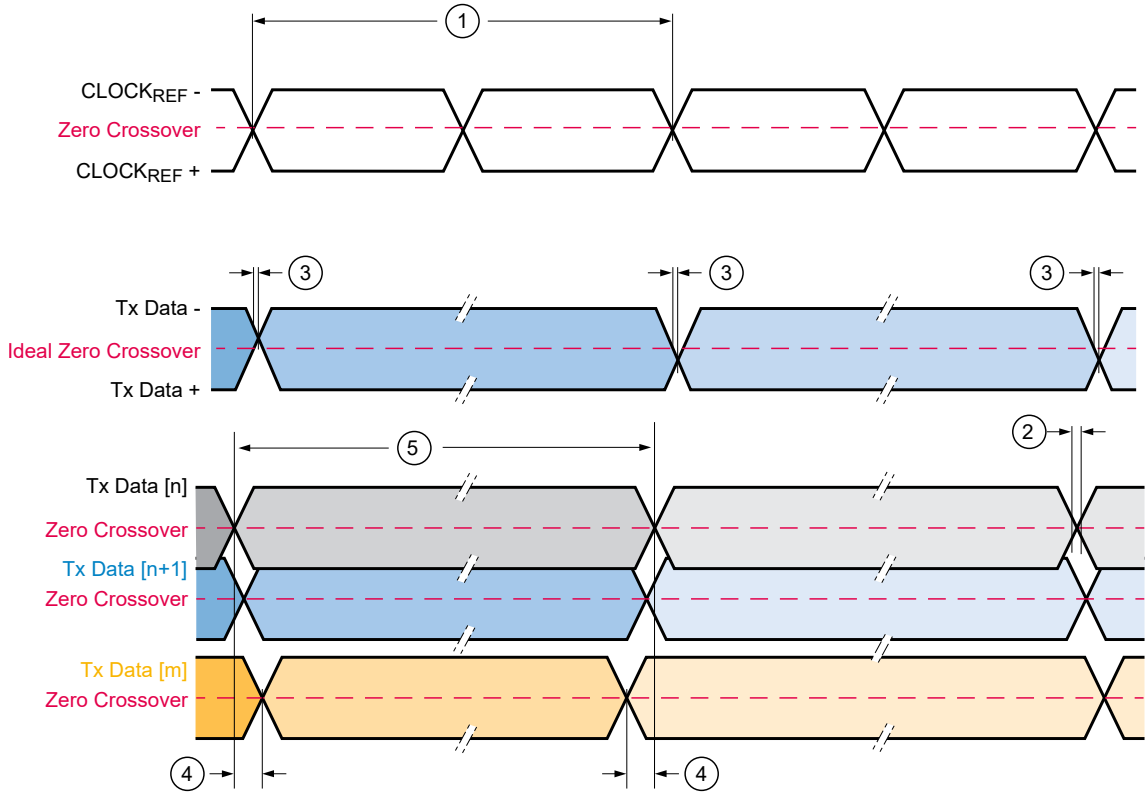
13.2 Aurora Port Timing

The following table gives the Aurora Port interface timing specifications for the device.

Table 13. Aurora Port Timing

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
BER	Bit Error Rate	—	—	10e-12	—	—	—
JD	Transmit line deterministic jitter	—	—	0.17	OUI	data rate <=3.0 Gbps	—
JD	Transmit line deterministic jitter	—	—	0.25	OUI	3.0Gbps < data rate <= 5.0Gbps	—
JT	Transmit line total jitter	—	—	0.35	OUI	data rate <= 3.0 Gbps	2
JT	Transmit line total jitter	—	—	0.45	OUI	3.0Gbps < data rate <= 5.0Gbps	2
SO	Differential output skew	—	—	20	ps	—	3
SMO	Lane to lane output skew	—	—	1000	ps	—	4
OUI	Aurora lane unit interval [1, 2]	—	500	—	ps	2.0 Gbps	5
OUI	Aurora lane unit interval [1, 2]	—	400	—	ps	2.5 Gbps	5
OUI	Aurora lane unit interval [1, 2]	—	333	—	ps	3.0 Gbps	5
OUI	Aurora lane unit interval [1, 2]	—	294	—	ps	3.4 Gbps	5
OUI	Aurora lane unit interval [1, 2]	—	250	—	ps	4.0 Gbps	5
OUI	Aurora lane unit interval [1, 2]	—	200	—	ps	5.0 Gbps	5

1. +/- 100 PPM.
2. The Aurora interface supports data rates of 2.0, 2.5, 3.0, 3.4, 4.0, and 5.0 Gbps.



For spec number 1, see Aurora PLL specifications
For rest, see Aurora port specifications

Figure 11. Aurora Debug Port Timing

13.3 Aurora PLL

The following table gives the operating frequencies and characteristics of the Aurora PLL. The operating frequencies correspond to the supported Aurora data trace lane speed. The Aurora PLL works from an external 100MHz input reference clock, and achieves a maximum output frequency of 5GHz.

Table 14. Aurora PLL

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fPLL_CLKIN	Aurora PLL Input Reference Clock Frequency [1, 2]	—	100	—	MHz	—	—
fPLL_CLKIN_PFD	Aurora PLL Phase Detector Clock Frequency [3]	—	100	—	MHz	—	—
ΔfPLL_CLKIN	Aurora PLL Input Reference Clock Duty Cycle [1]	40	—	60	%	—	—

Table continues on the next page...

Table 14. Aurora PLL (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
JRCDC	Reference clock period jitter	—	—	5	ps	RMS, 0.5MHz - 20MHz	—
fPLL_VCO	Aurora PLL VCO Frequency Range	3000	—	5000	MHz	—	—
fPLL_CLKOUT0	Aurora PLL Output Clock 0 Frequency Range [4]	—	—	5000	MHz	5.0Gbps Aurora lane data rate, VCO frequency divided by 1	—
fPLL_CLKOUT0	Aurora PLL Output Clock 0 Frequency Range [4]	—	—	4000	MHz	4.0Gbps Aurora lane data rate, VCO frequency divided by 1	—
fPLL_CLKOUT0	Aurora PLL Output Clock 0 Frequency Range [4]	—	—	3400	MHz	3.4Gbps Aurora lane data rate, VCO frequency divided by 1	—
fPLL_CLKOUT0	Aurora PLL Output Clock 0 Frequency Range [4]	—	—	3000	MHz	3.0Gbps Aurora lane data rate, VCO frequency divided by 1	—
fPLL_CLKOUT0	Aurora PLL Output Clock 0 Frequency Range [4]	—	—	2500	MHz	2.5Gbps Aurora lane data rate, VCO frequency divided by 2.	—
fPLL_CLKOUT0	Aurora PLL Output Clock 0 Frequency Range [4]	—	—	2000	MHz	2.0Gbps Aurora lane data rate, VCO frequency divided by 2.	—
fPLL_CLKOUT0	Aurora PLL Output Clock 0 Frequency Range	—	—	500	MHz	No tool connected - trace logic clock with FXOSC reference clock.	—
tLOCK	Aurora PLL Lock Time	—	—	150	us	—	—
PER_jitter	Aurora PLL Period Jitter	-21	—	21	ps	fPLL_CLKIN = 100MHz, VCO = 5GHz, fPLL_CLKOUT = 5GHz, 6-sigma	—
LT_jitter	Aurora PLL Long Term Jitter	-120	—	120	ps	Saturated, 6-sigma	—

1. Refer to the LVDS Pad specifications for additional Aurora PLL reference clock electrical specifications. Also see " Aurora Debug Port Timing" figure for fPLL_CLKIN as spec number 1.
2. 100MHz is the only input reference frequency supported for the Aurora PLL.
3. It is Aurora PLL Input Reference Clock Frequency after pre-divider.
4. The Aurora PLL is only validated at the frequencies specified within this table - these frequencies correspond to the limited set of Aurora data lane rates that are supported for the device.

14 Power Management Controller (PMC)

14.1 PMC Bandgap

Table 15. PMC Bandgap

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VBG_SCALED	Scaled version of bandgap reference voltage measured by SAR ADC [1]	1.127	1.150	1.173	V	Both bandgap and buffer are trimmed	—

1. ADC conversion error must be included when reading the bandgap reference voltage via the chip ADC.

15 Reset

15.1 Reset Duration

The diagrams in this section are not to scale.

Table 16. Reset Duration

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TFR	Functional Reset Sequence Duration	—	—	545	us	FIRC_CLK, trimmed	—
TDR	Destructive Reset Sequence Duration	—	—	1370	us	FIRC_CLK, trimmed during destructive reset phase	—
POR	Power On Reset Sequence Duration	—	—	1500	us	FIRC_CLK, trimmed during destructive reset phase	—

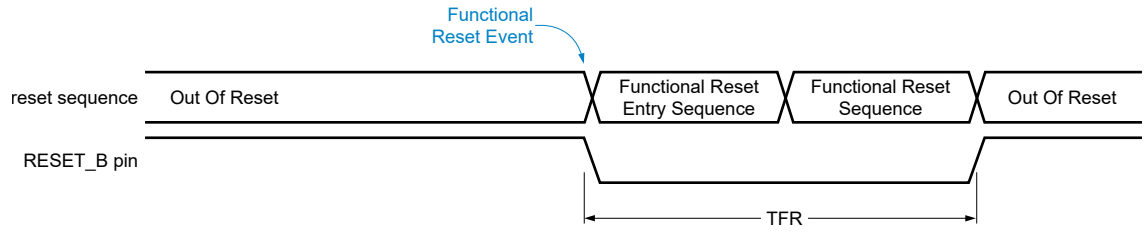


Figure 12. Functional reset

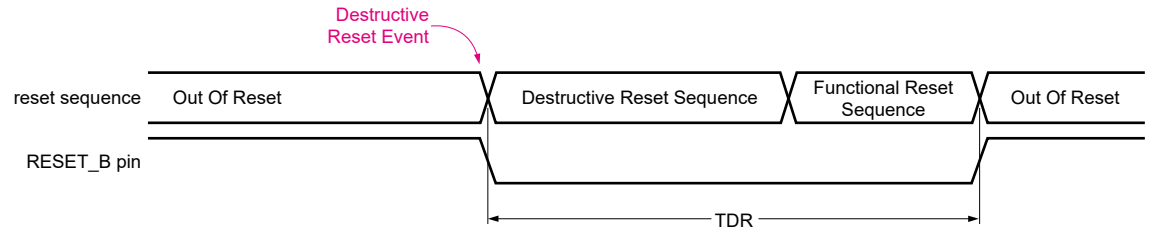


Figure 13. Destructive reset

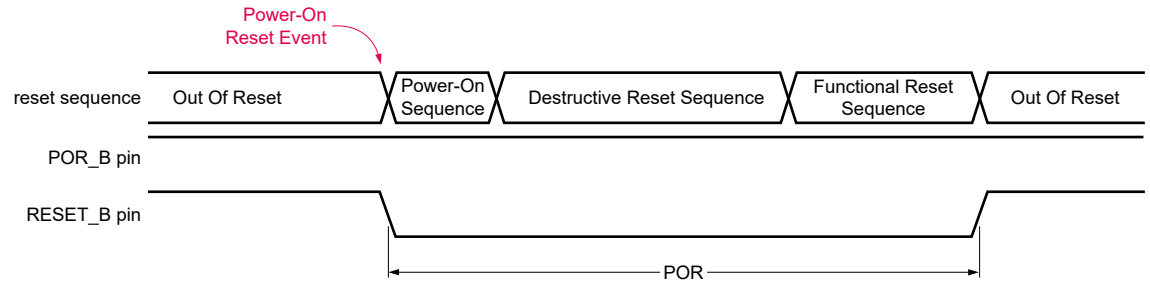


Figure 14. POR due to internal POR event

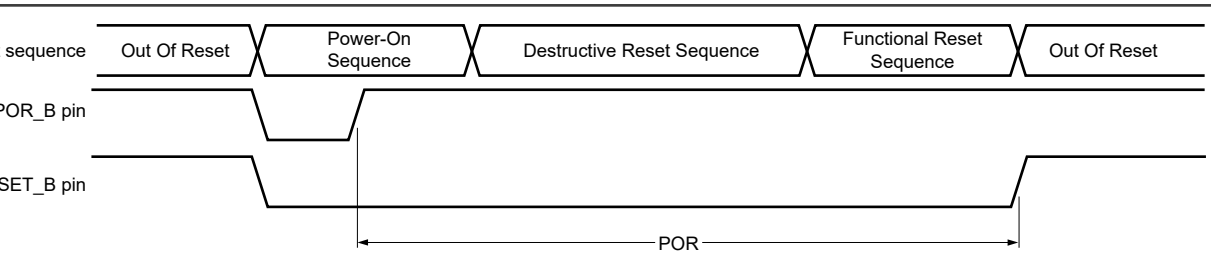


Figure 15. POR due to POR_B pin assertion

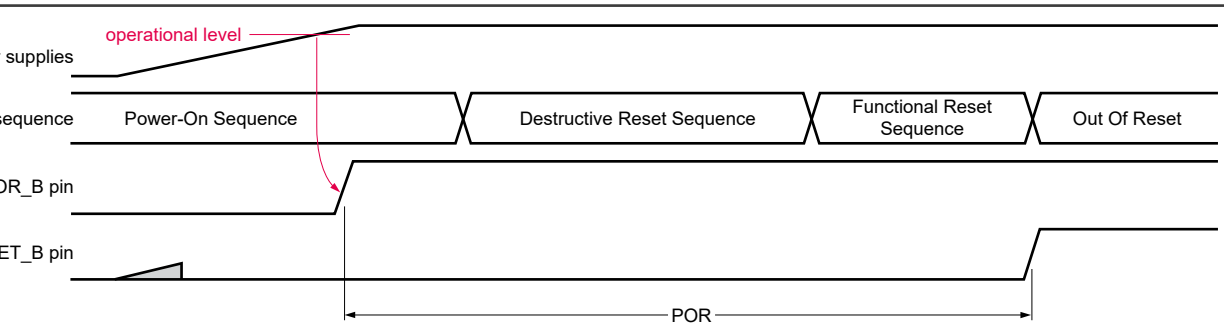


Figure 16. Initial power-up

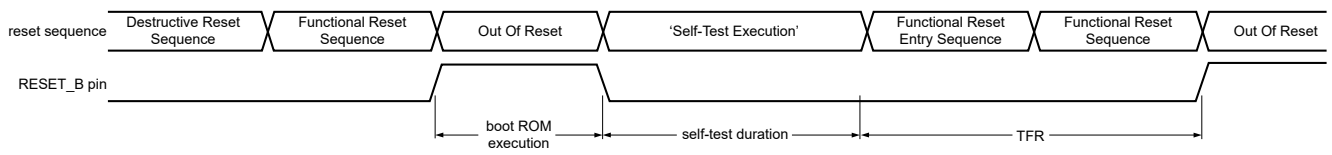


Figure 17. Start-up self-test

15.2 Reset and Standby related pad electrical characteristics

The following table gives the characteristics of the POR_B, RESET_B, PMIC_STBY_MODE_B, and PMIC_VDD_OK pads.

Values not explicitly listed in this table can be found in the 'GPIO Pads' section.

Table 17. Reset and Standby related pad electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
ISLEW_POR_B	POR_B slew rate	30e-06	—	4	V/ns	—	—
ISLEW_RESET_B	RESET_B slew rate [1]	30e-06	—	4	V/ns	Noise on RESET_B <100mV peak-peak.	—
VISE_RESET_B	RESET_B pad indeterminate state end threshold	—	2.35	—	V	See RESET_B pad detailed behavior diagram below	—
VRSE_RESET_B	RESET_B pad ramp-up state end threshold	—	460	—	mV	See RESET_B pad detailed behavior diagram below	—
WF_RESET_B	RESET_B input filtered pulse	—	—	17	ns	—	—
WNF_RESET_B	RESET_B input not filtered pulse	400	—	—	ns	—	—
MLP_POR_B	POR_B minimum low pulse	5	—	—	us	—	—
MLP_PMIC_VDD_OK	PMIC_VDD_OK minimum low pulse	36	—	—	us	during Standby mode entry	—
MHP_PMIC_VDD_OK	PMIC_VDD_OK minimum high pulse	36	—	—	us	during Standby mode exit	—

1. ISLEW_RESET_B(Min) = MAX[30e-06, 0.002 * Vnoise_p_p * Fnoise], where Vnoise_p_p is peak-peak noise magnitude (in V) and Fnoise is max noise frequency (in MHz).

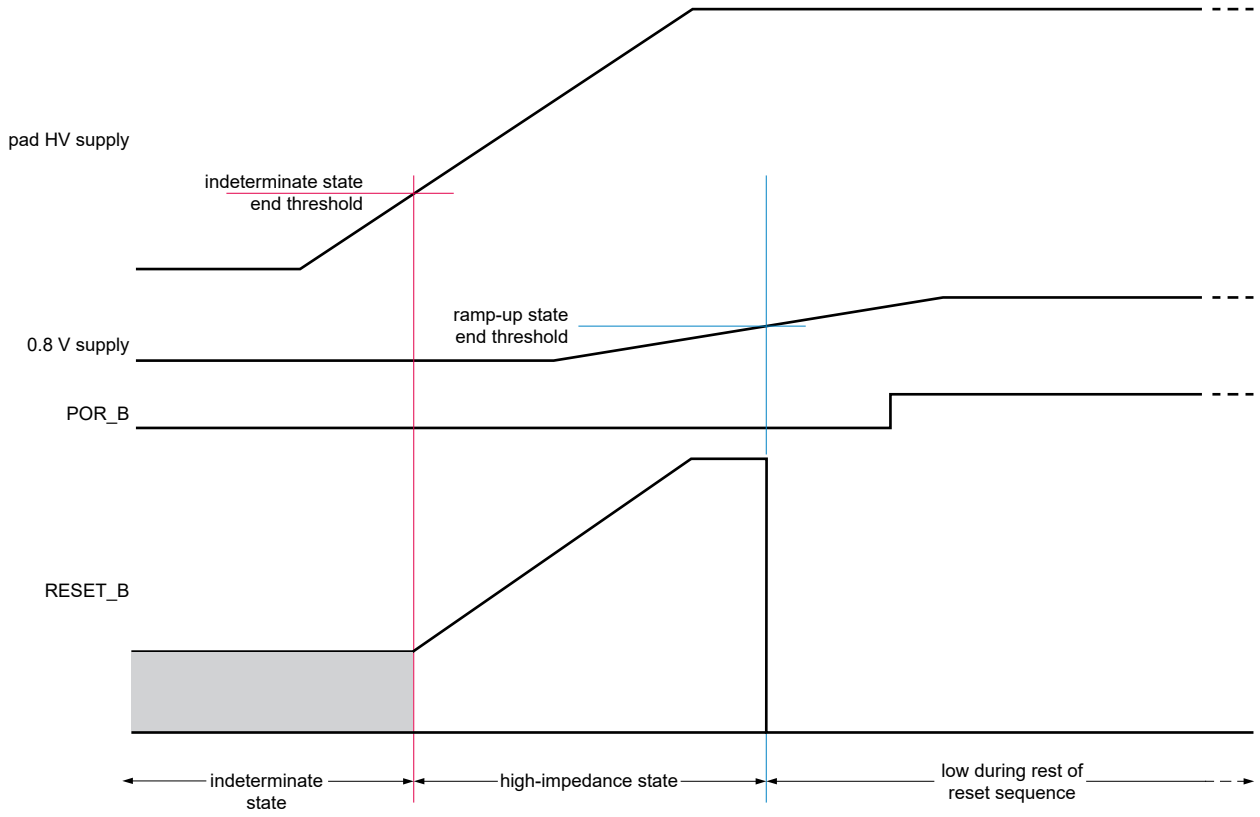


Figure 18. RESET_B pad detailed behavior

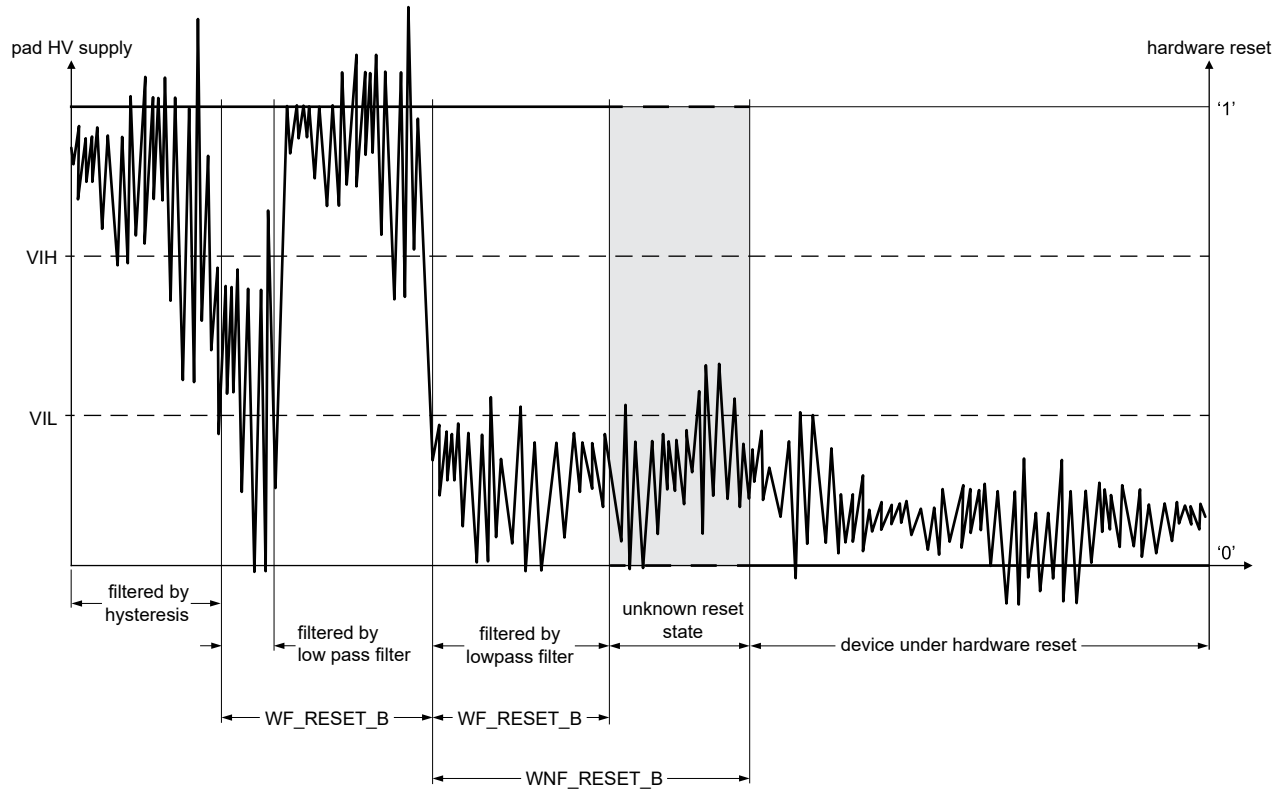


Figure 19. Noise filtering on RESET_B pad

During SoC power-up, the PMIC asserts the POR_B input before the SoC supplies are turned on and kept asserted until all SoC supplies have reached their operational levels (i.e., all the corresponding voltage monitors in the PMIC have been satisfied) and any required PMIC BIST has completed. See the 'Power Sequencing' section for details.

The PMIC asserts the POR_B input whenever one of its voltage detectors detects an SoC supply's voltage is outside its operational range (i.e., a corresponding PMIC LVD or HVD event occurs).

15.2.1 PMIC Standby Mode Entry / Exit Protocol

The PMIC_STBY_MODE_B output is:

1. asserted by the SoC when the power domains that are not needed during Standby mode are to be turned off

2. deasserted by the SoC when the power domains that are not needed during Standby mode are to be turned on

The PMIC_VDD_OK input is:

1. deasserted by the PMIC when the power domains that are not needed during Standby mode have been turned off

2. asserted by the PMIC when the power domains that are not needed during Standby mode have been turned on and have reached their operational levels (e.g., all the corresponding voltage monitors in the PMIC have been satisfied) and any required PMIC BIST has completed. See the "Power Sequencing" section for any exceptions.

This implies that the PMIC_VDD_OK input is asserted and deasserted together with the POR_B input during non-Standby modes. Asserting PMIC_VDD_OK during non-Standby modes while not also asserting POR_B will cause the SoC to start a power-on reset sequence.

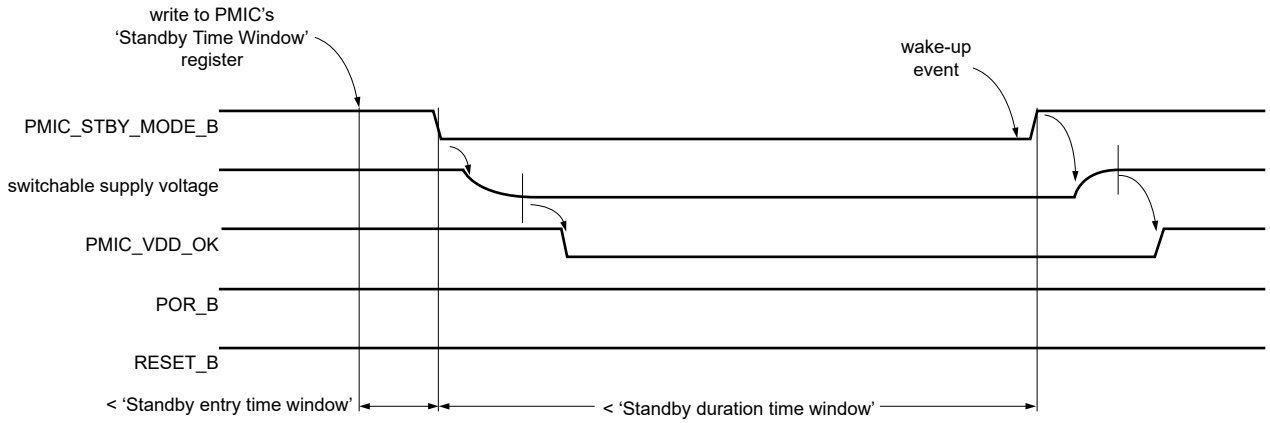


Figure 20. Standby Mode Entry and Exit Sequence

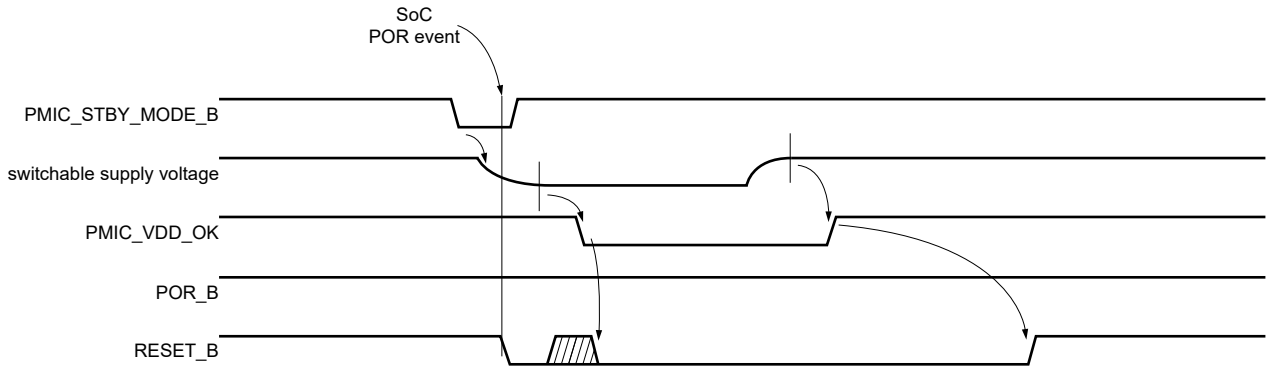


Figure 21. Standby Mode Aborted by SoC POR Event Prior to PMIC_VDD_OK Deassertion

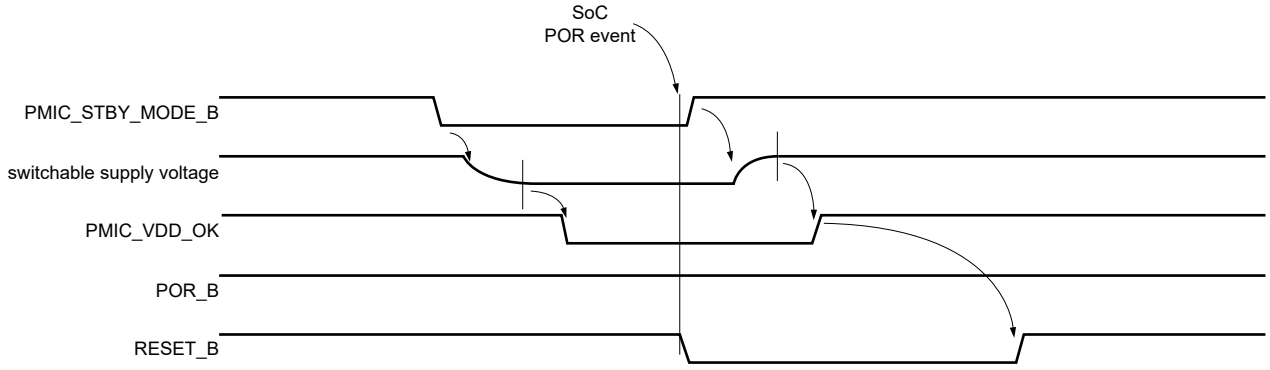


Figure 22. Standby Mode Aborted by SoC POR Event After PMIC_VDD_OK Deassertion

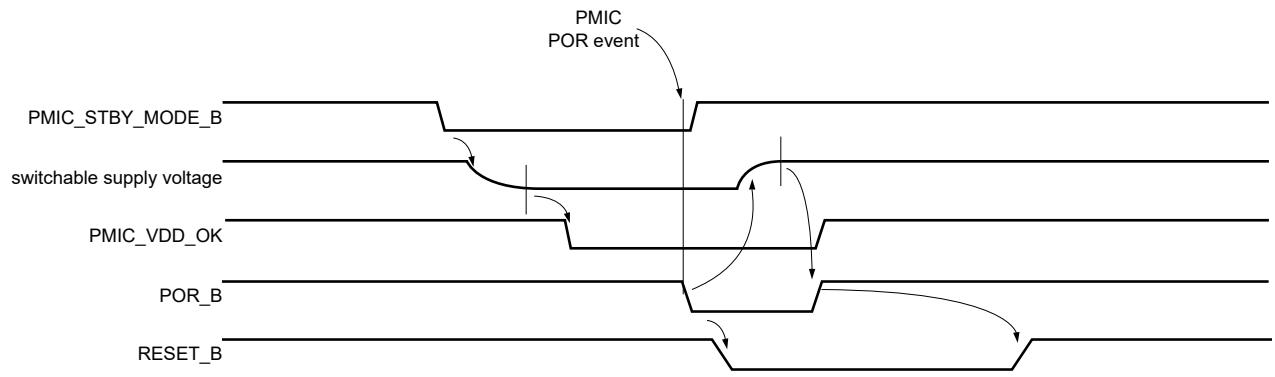


Figure 23. Standby Mode Aborted by PMIC POR Event

16 Peripheral specifications

16.1 Analog Modules

16.1.1 SAR ADC

Table 18. SAR ADC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VAD_INPUT	ADC Input Voltage [1, 2, 3]	VREFL_ADC	—	VREFH_ADC	V	on or off channels	—
fAD_CK	ADC Clock Frequency [1, 2]	20	—	80	MHz	—	—
tSAMPLE	ADC Input Sampling Time [1, 2, 4]	275	—	—	ns	—	—
tCONV	ADC Total Conversion Time [1, 2, 5]	1	—	—	us	—	—
tRECOVERY	ADC Initialization Time from power-down [1, 2]	—	—	1	us	—	—
CAD_INPUT	ADC Input Capacitance [1, 2]	—	—	7	pF	ADC component plus pad capacitance (~2pF)	—
RAD_INPUT	ADC Input Series Resistance [1, 2]	—	—	1.25	kΩ	—	—
OFS	ADC Offset Error [1, 2, 6]	-6	—	6	LSB	after calibration	—
GNE	ADC Gain Error (full scale) [1, 2, 6]	-6	—	6	LSB	after calibration	—

Table continues on the next page...

Table 18. SAR ADC (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
DNL	ADC Differential Non-linearity [1, 2, 6, 7, 8]	-1	—	2	LSB	after calibration	—
INL	ADC Integral Non-linearity [1, 2, 6, 8]	-3	—	3	LSB	after calibration	—
TUE	ADC Total Unadjusted Error [1, 2, 6, 8]	-8	—	8	LSB	after calibration	—
SNR	Signal-to-Noise Ratio [1, 2, 6]	—	65	—	dBFS	input signal frequency <= 50KHz	—
THD	Total Harmonic Distortion [1, 2, 6]	—	72	—	dBFS	Input signal frequency <= 50KHz.	—
IAD_LKG	ADC Input Leakage Current [1, 2, 9]	-1	—	1	uA	TJ = 125C, Dedicated input channel, channel selection switch open	—
IAD_LKG	ADC Input Leakage Current [1, 2, 9]	-2	—	2	uA	TJ = 125C, Shared channel, channel selection switch open	—
CP1	ADC input pin capacitance 1	—	—	4	pF	—	—
CP2	ADC input pin capacitance 2	—	—	0.5	pF	—	—
CS	ADC input sampling capacitance	—	—	4	pF	—	—
RSW1	Internal resistance of analog source	—	—	600	ohm	—	—
RAD	Internal resistance of analog source	—	—	150	ohm	—	—

1. ADC performance specifications are only guaranteed when the injection current limits in the operating conditions table of this electrical specification are met.
2. Although functionally supported on devices with 2 ADCs, ADC performance specifications are not guaranteed for shared channels between the 2 ADCs if the input channel is sampled or converted simultaneously by both ADCs. For best performance in this case, the external capacitance at the input pin should be maximized.
3. The reduced limits for VAD_INPUT in this table are recommended for normal operation.
4. During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within tsample. After the end of the sample time tsample, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock tsample depend on programming.
5. 1Msps is the ADC output rate and includes both sampling and analog to digital conversion.
6. ADC performance specifications are guaranteed when calibration uses maximum averaging i.e. when AVGEN = 1 and NRSMPL = 3.
7. During calibration, the ADC determines its (positive or negative) offset value and stores the result in an internal register. During each conversion, the offset value is subtracted from the raw result to compensate the individual ADC offset.Since the ADC cannot generate negative numbers, a negative calibration offset results in a minimum output code between 0 and

6. A positive calibration offset does not impact the max. code output of 4095. Calibration fails if it determines an offset larger than +/- 6 LSB.
8. This specification is taken with averaging through post process ADC data.
9. The maximum and minimum leakage current values are reached when Vin=VREF and Vin=0, respectively.

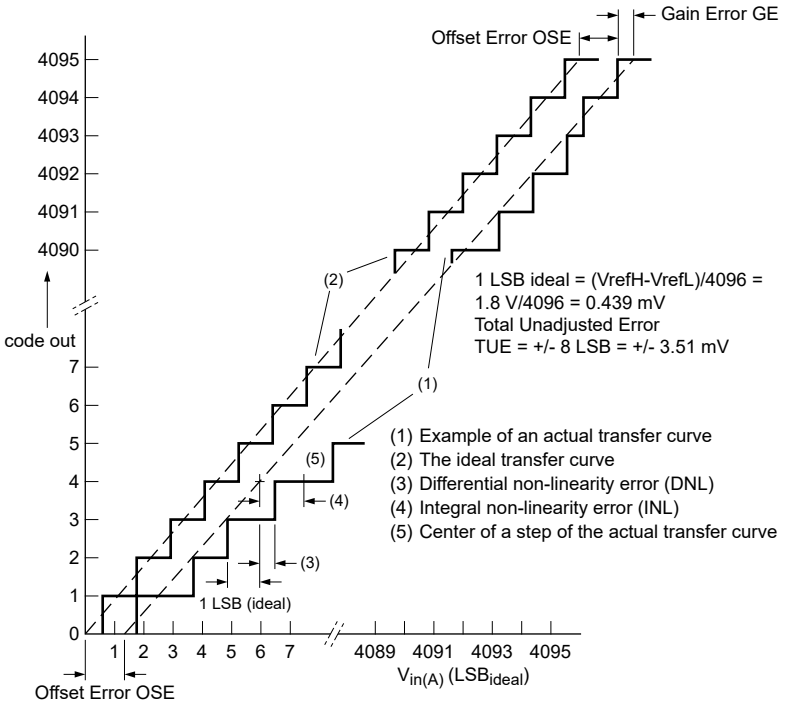


Figure 24. SAR ADC Specification Characteristics

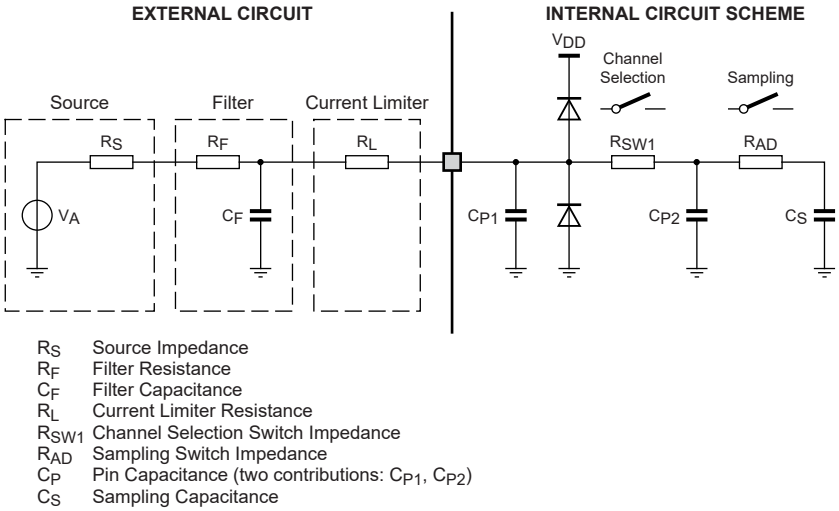


Figure 25. SAR ADC Input Circuit

16.1.2 Temperature Monitoring Unit (TMU)

The table below gives the specification for the Temperature Monitoring Unit (TMU). Specifications apply to all remote temperature sensors connected to the TMU on the device.

Table 19. Temperature Monitoring Unit (TMU)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TRANGE	Temperature monitoring range	-40	—	125	C	—	—
TERR	Temperature sensor error	-8	—	8	C	TRANGE = -40C to 84C	—
TERR	Temperature sensor error	-5	—	5	C	TRANGE = 85C to 110C	—
TERR	Temperature sensor error	-3	—	3	C	TRANGE = 111C to 125C	—

16.1.3 Glitch Filter

Table 20. Glitch Filter

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TFILT	Glitch filter max filtered pulse width [1, 2, 3, 4]	—	—	17	ns	—	—
TUNFILT	Glitch filter min unfiltered pulse width [2, 3, 4, 5]	400	—	—	ns	—	—

1. Pulses shorter than defined by the maximum value are guaranteed to be filtered (not passed).
2. Pulses in between the max filtered and min unfiltered may or may not be passed through.
3. See the device reference manual for which package pins include glitch filters on the pin input.
4. An input signal pulse is defined by the duration between the input signal's crossing of a Vil/Vih threshold voltage level, and the next crossing of the opposite level.
5. Pulses larger than defined by the minimum value are guaranteed to not be filtered (passed).

16.1.4 IRQ

The following table gives the input specifications for the external interrupt pins.

Table 21. IRQ

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tIPWL	IRQ pulse width low [1]	4	—	—	tCYC	MAXCNT = 3	1
tIPWH	IRQ pulse width high [1]	4	—	—	tCYC	MAXCNT = 3	2

1. tCYC is the FIRC_CLK clock period.

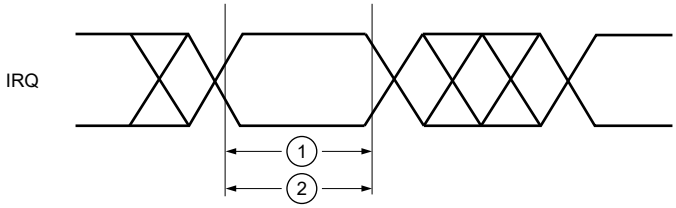


Figure 26. External Interrupt Timing (IRQ)

16.2 Clock and PLL Interfaces

16.2.1 DFS

The following table specifies the output frequency ranges and characteristics of the Digital Frequency Synthesizer (DFS).

Table 22. DFS

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fDFS_CORE_CLK1	Core DFS Output Clock 1 Frequency	40	—	800	MHz	CORE_DFS1	—
fDFS_CORE_CLK2	Core DFS Output Clock 2 Frequency	40	—	800	MHz	CORE_DFS2	—
fDFS_PER_CLK1	Peripheral DFS Output Clock 1 Frequency	532	—	800	MHz	PERIPH_DFS1	—
fDFS_PER_CLK2	Peripheral DFS Output Clock 2 Frequency	40	—	960	MHz	PERIPH_DFS2	—
fDFS_PER_CLK3	Peripheral DFS Output Clock 3 Frequency	416	—	800	MHz	PERIPH_DFS3	—
fDFS_PER_CLK5	Peripheral DFS Output Clock 5 Frequency	2.54	—	80	MHz	PERIPH_DFS5	—
fDFS_CLKIN	DFS Input Clock Frequency	1300	—	2000	MHz	—	—
PER_jitter	DFS Period Jitter [1, 2, 3]	-30	—	30	ps	Even MFN	—
PER_jitter	DFS Period Jitter [1, 2, 3]	-45	—	45	ps	fDFS_CLKIN = 2000 MHz, Odd MFN	—
PER_jitter	DFS Period Jitter [1, 2, 3]	-60	—	60	ps	fDFS_CLKIN = 1300 MHz, Odd MFN	—

1. For SoC clocks that are futher divided down from the DFS output clock, the jitter is multiplied by a factor of SQRT(N), where N is the ratio of the DFS output clock and destination clock periods.
2. Jitter value does not apply when the DFS clock is output on an external pin. In this case, the rise and fall time variations in the I/O pad are orders of magnitude more than the DFS and SoC mux jitter contributions.
3. Min jitter=Min(PER_jitter(PLL))*(sqrt(N))+Min(PER_jitter(DFS)). Max jitter=Max(PER_jitter(PLL))*(sqrt(N)) +Max(PER_jitter(DFS)). Where N is the DFS division factor. All jitter numbers are in ps.

16.2.2 FIRC

Table 23. FIRC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fFIRC	FIRC Target Frequency	—	48	—	MHz	—	—
ðfVAR	FIRC Frequency Variation [1]	-5	—	5	%	Trimmed	—
TSTART	Startup Time	—	10	20	us	After valid supply level reached	—

1. ðfVAR defines how much the output frequency can shift over the specified temperature and voltage ranges of the device after initial factory trim.

16.2.3 SIRC

Table 24. SIRC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSIRC	SIRC Target Frequency Trimmed	—	32	—	KHz	Trimmed	—
PTA	SIRC Post Trim Accuracy [1]	-1	—	1	%	Trimmed 32KHz, 25C, 0.8V Core	—
ðfVAR	SIRC Frequency Variation [2]	-5	—	5	%	Trimmed	—
TSTART	SIRC Startup Time	—	—	50	us	—	—

1. PTA defines how close the output frequency is to target after the initial factory trim.
2. ðfVAR defines how much the output frequency can shift over the specified temperature and voltage ranges of the device.

16.2.4 FXOSC

Table 25. FXOSC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fXTAL	Input Frequency Range [1, 2, 3]	20	—	40	MHz	Crystal mode	—
TCST	Crystal Startup Time	—	—	2	ms	Crystal mode	—
fBYP_SE	FXOSC Bypass Frequency [3]	—	40	—	MHz	single-ended bypass mode	—
VIH_EXTAL	EXTAL Input High Level [4]	Vref + 0.3	—	VDD_FXOSC	V	Vref = VDD_FXOSC / 2, Single-ended bypass mode	—

Table continues on the next page...

Table 25. FXOSC (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIL_EXTAL	EXTAL Input Low Level [4]	0	—	Vref - 0.3	V	Vref = VDD_FXOSC / 2, Single-ended bypass mode	—
CLOAD	XTAL/EXTAL pin load capacitance [5]	—	8	—	pF	Crystal mode	—
CS_XTAL	XTAL/EXTAL pin on-chip stray capacitance [5]	—	—	3	pF	—	—
Leakage_injection	EXTAL injection current	-50	—	100	nA	Mean current flowing into EXTAL in crystal mode	—
Leakage_extal	External Leakage on EXTAL Pin	-20	—	20	nA	Bypass mode, 0.5V	—
EXTAL_AMP	EXTAL_amplitude (p k-pk)	300	—	900	mV	Crystal mode	—
LT_Jitter	Long term jitter	-120	—	120	ps	gm_sel=1111 with 40MHz crystal (NX5032GA)	—

1. Only 20MHz, 24MHz, and 40MHz crystal frequencies are verified in simulation.
2. All specifications only valid for this frequency range if the correct FXOSC transconductance setting is used. Please see the device reference manual for the correct setting per the crystal type.
3. The input clock must be 40 MHz nominal frequency.
4. The input clock signal should be symmetric around common mode voltage. V common_mode= (VDD_FXOSC)/2
5. Account for on-chip stray capacitance (CS_XTAL) and PCB capacitance in the total XTAL/EXTAL pin load capacitance. CS_XTAL don't include miller capacitance.

See Hardware design guide for recommended circuits for each mode.

In crystal mode NX5032GA crystal at 20 MHz has a load cap of 8 pF and configure gm_sel[3:0]=4'b0100 and NX3225GA crystal has a load cap of 8 pF and configure gm_sel[3:0]=4'b100.

In crystal mode NX5032GA crystal at 24 MHz has a load cap of 8 pF and configure gm_sel[3:0]=4'b0101 and NX3225GA has a load cap of 8 pF and configure gm_sel[3:0]=4'b0110.

In crystal mode NX5032GA crystal at 40 MHz (ALC enable) has a load cap of 8 pF and configure gm_sel[3:0]=4'b1111.

RGMII specifications require clock source to have tolerance of +/- 50ppm. When using this mode, the crystal selected for system clock (FXOSC) should adhere to this specification.

16.2.5 PLL

The following table gives the operating frequencies and characteristics of the PLL, and applies to instances on the device. Actual operating frequencies for the device are constrained to the values given below.

Table 26. PLL

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fPLL_CLKIN	PLL Input Clock Frequency [1, 2]	20	—	100	MHz	Before PLL input divider.	—
fPLL_CLKIN_PFD	PLL Phase Detector Clock Frequency [1, 3]	20	—	40	MHz	After PLL input divider.	—
fPLL_CORE_VCO	Core PLL VCO Frequency Range [4, 5]	1300	—	1970	MHz	with center-spread SSCG enabled	—
fPLL_CORE_VCO	Core PLL VCO Frequency Range [4, 5]	1300	—	2000	MHz	without center-spread SSCG enabled	—
fPLL_CORE_PHI0	Core PLL PHI0 Frequency	—	—	985	MHz	CORE_PLL_PHI0, with center-spread SSCG enabled	—
fPLL_CORE_PHI0	Core PLL PHI0 Frequency	—	—	1000	MHz	CORE_PLL_PHI0, without center-spread SSCG enabled	—
fPLL_PER_VCO	Peripheral PLL VCO Frequency Range	1300	—	2000	MHz	—	—
fPLL_PER_PHI0	Peripheral PLL PHI0 Frequency	100	—	125	MHz	PERIPH_PLL_PHI0	—
fPLL_PER_PHI1	Peripheral PLL PHI1 Frequency	—	—	80	MHz	PERIPH_PLL_PHI1	—
fPLL_PER_PHI2	Peripheral PLL PHI2 Frequency	40	—	80	MHz	PERIPH_PLL_PHI2	—
fPLL_PER_PHI3	Peripheral PLL PHI3 Frequency	—	—	133	MHz	PERIPH_PLL_PHI3	—
fPLL_PER_PHI4	Peripheral PLL PHI4 Frequency	—	—	200	MHz	PERIPH_PLL_PHI4	—
fPLL_PER_PHI5	Peripheral PLL PHI5 Frequency	—	—	500	MHz	PERIPH_PLL_PHI5	—
fPLL_PER_PHI7	Peripheral PLL PHI7 Frequency	—	—	100	MHz	PERIPH_PLL_PHI7	—
fPLL_ACCEL_VCO	Accelerator PLL VCO Frequency Range	1300	—	2364	MHz	with center-spread SSCG enabled	—
fPLL_ACCEL_VCO	Accelerator PLL VCO Frequency Range	1300	—	2400	MHz	without center-spread SSCG enabled	—

Table continues on the next page...

Table 26. PLL (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fPLL_ACCEL_PHI1	Accelerator PLL PHI1 Frequency	—	—	591	MHz	ACCEL_PHI1, with center-spread SSCG enabled	—
fPLL_ACCEL_PHI1	Accelerator PLL PHI1 Frequency	—	—	600	MHz	ACCEL_PHI1, without center-spread SSCG enabled	—
fPLL_DDR_VCO	DDR PLL VCO Frequency Range	1300	—	1576	MHz	with center-spread SSCG enabled	—
fPLL_DDR_VCO	DDR PLL VCO Frequency Range	1300	—	1600	MHz	without center-spread SSCG enabled	—
fPLL_DDR_PHI0	DDR PLL PHI0 Frequency [6]	788	—	788	MHz	DDR_CLK (3200 MT/s), with center-spread SSCG enabled	—
fPLL_DDR_PHI0	DDR PLL PHI0 Frequency [6]	800	—	800	MHz	DDR_CLK (3200 MT/s), without center-spread SSCG enabled	—
fPLL_DDR_PHI0	DDR PLL PHI0 Frequency [6]	533.3	—	533.3	MHz	DDR_CLK (2133 MT/s)	—
fPLL_DDR_PHI0	DDR PLL PHI0 Frequency [6]	466.6	—	466.6	MHz	DDR_CLK (1866 MT/s)	—
fPLL_DDR_PHI0	DDR PLL PHI0 Frequency [6]	400	—	400	MHz	DDR_CLK (1600 MT/s)	—
fPLL_DDR_PHI0	DDR PLL PHI0 Frequency [6]	666.5	—	666.5	MHz	DDR_CLK (2666 MT/s)	—
tLOCK	System PLL Lock Time [1]	—	—	100	us	—	—
PER_jitter	System PLL Period Jitter [1, 7, 8, 9]	-23	—	23	ps	fPLL_CLKIN = 40MHz, fVCO = 2GHz, 6-sigma, SSCG & Frac mode disabled	—
LT_jitter	System PLL Long Term Jitter [1, 9, 10]	-120	—	120	ps	Saturated, 6-sigma	—
ΔfPLL_MOD	Spread Spectrum Clock Modulation Depth [11]	+/- 0.25	—	+/- 1.5	%	SSCG enabled, center spread	—
fPLL_MOD	Spread Spectrum Clock Modulation Frequency [11]	30	—	64	KHz	—	—

1. PLL refers to the Core, Peripheral, Accelerator, and DDR reference PLLs on the device.
2. This refers to spec number 1 which is shown in the figure in Aurora port specifications
3. This specification is PLL input reference clock frequency after pre-divider.
4. Duty cycle of the system PLL clock when output on an external pin is given in the I/O pad specifications.
5. The frequencies are the nominal frequencies (i.e., what the PLL's VCO is configured to).

6. The DDR PHY internally multiplies the PLL_DDR_PHI0 by factor of two.
7. For chip clocks that are futher divided down from the PLL output clock, the jitter is multiplied by a factor of SQRT(N), where N is the ratio of the PLL output clock and destination clock periods.
8. Jitter is dependent on supply noise, the period of the PLL output clock, and the division ratio of the clock at the destination module. Specified jitter values are valid for the FXOSC reference clock input only - not valid for FIRC reference clock input.
9. Jitter value does not apply when a PLL clock is output on an external pin. In this case, the rise and fall time variations in the I/O pad are orders of magnitude more than the PLL and SoC mux jitter contributions.
10. This specification is valid when all clock sources are stable.
11. Spread spectrum clock modulation is only available on the Core, Accelerator and DDR reference PLLs.

NOTE

fPLL_DDR_PHI0 frequencies and data rate mentioned in this table are for LPDDR4. DDR3L frequencies and data rates are half of the LPDDR4.

16.3 Communication modules

16.3.1 SPI

Table 27. SPI

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tSCK	SPI cycle time [1, 2]	40	—	10000	ns	Master, MTFE=0	1
tSCK	SPI cycle time [1]	25	—	10000	ns	Master, MTFE=1	1
tSCK	SPI cycle time [1, 3]	16.67	—	10000	ns	Slave Receive Mode	1
tSCK	SPI cycle time [1]	40	—	10000	ns	Slave Transmit Mode	1
tCSC	PCS to SCK delay [4]	20	—	10000	ns	—	2
tASC	After SCK delay [5]	20	—	10000	ns	—	3
tSDC	SCK duty cycle	40	—	60	%	—	4
tA	Slave access time	—	—	40	ns	SS active to SOUT valid	5
tDIS	Slave SOUT disable time	—	—	15	ns	SS inactive to SOUT hi-z or invalid	6
tPCSC	PCSx to PCSS time	13	—	—	ns	—	7
tPASC	PCSS to PCSx time	13	—	—	ns	—	8
tSUI	Input data setup time [6, 7]	15	—	—	ns	Master, MTFE=0	9
tSUI	Input data setup time [6]	15 - N * ipg_clk_dspi_period	—	—	ns	Master, MTFE=1, CPHA=0, SMPL_PTR = 1	9
tSUI	Input data setup time [6]	15	—	—	ns	Master, MTFE=1, CPHA=1, SMPL_PTR = 1	9
tSUI	Input data setup time [6]	2	—	—	ns	Slave Receive Mode	9

Table continues on the next page...

Table 27. SPI (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tHI	Input data hold time [6]	0	—	—	ns	Master, MTFE=0	10
tHI	Input data hold time [6]	0 + N * ipg_clk_dspi_period	—	—	ns	Master, MTFE=1, CPHA=0, SMPL_PTR = 1	10
tHI	Input data hold time [6]	0	—	—	ns	Master, MTFE=1, CPHA=1, SMPL_PTR = 1	10
tHI	Input data hold time [6]	4	—	—	ns	Slave Receive Mode	10
tSUO	Output data valid time (after SCK edge) [8]	—	—	5	ns	Master, MTFE=0 max CLOAD=25pF, max pad drive setting, SRE[2:0] = 101	11
tSUO	Output data valid time (after SCK edge) [8]	—	—	5 + ipg_clk_dspi_period	ns	Master, MTFE=1, CPHA=0 max CLOAD=25pF, max pad drive setting, SRE[2:0] = 101	11
tSUO	Output data valid time (after SCK edge) [8]	—	—	5	ns	Master, MTFE=1, CPHA=1 max CLOAD=25pF, max pad drive setting, SRE[2:0] = 101	11
tSUO	Output data valid time (after SCK edge) [7, 8]	—	—	16	ns	Slave Transmit Mode, SRE[2:0] = 101	11
tHO	Output data hold time [8]	-2	—	—	ns	Master, MTFE=0 max CLOAD=25pF, max pad drive setting, SRE[2:0] = 101	12
tHO	Output data hold time [8]	-2 + ipg_clk_dspi_period	—	—	ns	Master, MTFE=1, CPHA=0 max CLOAD=25pF, max pad drive setting, SRE[2:0] = 101	12
tHO	Output data hold time [8]	-2	—	—	ns	Master, MTFE=1, CPHA=1 max CLOAD=25pF, max pad drive setting, SRE[2:0] = 101	12

Table continues on the next page...

Table 27. SPI (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tHO	Output data hold time [8]	3	—	—	ns	Slave Transmit Mode, SRE[2:0] = 101	—

1. The maximum SPI baud rate that is achievable in a dedicated master-slave connection depends on several parameters that are independent of the SPI module clocking capabilities (e.g. capacitive load of the signal lines, SPI slave clock-to-datadelay, pad slew rate, etc.). The maximum achievable SPI baud rate needs to be evaluated in a corresponding SPI master-slave setup.
2. SMPL_PTR should be set to 1. For SPI_CTARn[BR] - 'Baud Rate Scaler' configuration is >= 3
3. Slave Receive Mode can operate at a maximum frequency of 60 MHz. In this mode, the DSPI can receive data on SIN, but no valid data is transmitted on SOUT.
4. This value of 20 ns is with the configuration prescaler values: SPI_CTARn[PCSSCK] - "PCS to SCK Delay Prescaler" configuration is "3" (01h) and SPI_CTARn[CSSCK] - "PCS to SCK Delay Scaler" configuration is "2" (0000h)
5. This value of 20 ns is with the configuration prescaler values: SPI_CTARn[PASC] - "After SCK Delay Prescaler" configuration is "3" (01h) and SPI_CTARn[ASC] - "After SCK Delay Scaler" configuration is "2" (0000h)
6. Input timing assumes an input signal slew rate of 2ns (20%/80%).
7. For the case of both master and slave being NXP S32x devices, frequency of operation will be reduced to [1000 /2* {tSUI_master + tSUO_slave + PCB delay}] in ns.
8. Output timing valid for maximum external load CL = 25pF, which is assumed to be a 10pF load at the end of a 50Ohm, un-terminated, 5 inch microstrip trace on standard FR4 (1.5pF/inch), (25pF total with margin). For best signal integrity, the series resistance of the transmission line should be matched closely to the RDSON of the I/O pad output driver.

Slave mode timing values given below are applicable when device is in MTFE=0.

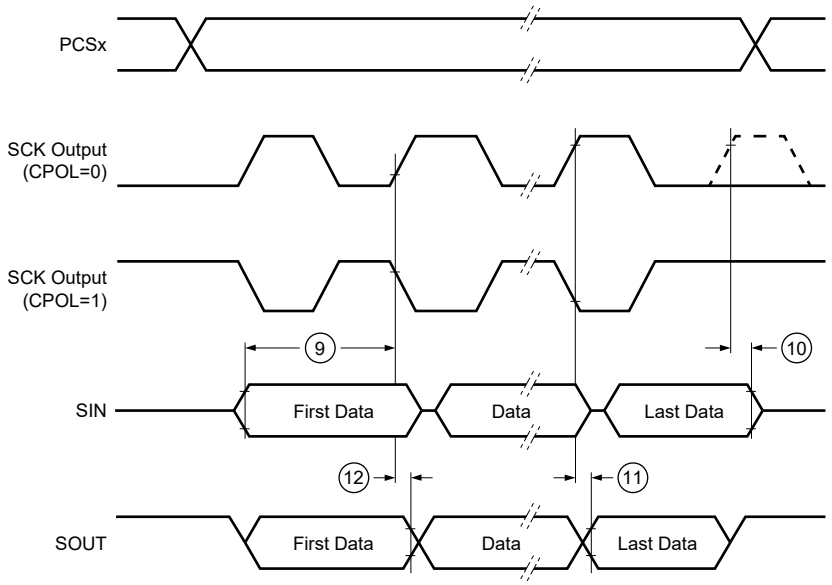


Figure 27. SPI Modified Transfer Format Timing - Master, CPHA = 1, MTFE=1

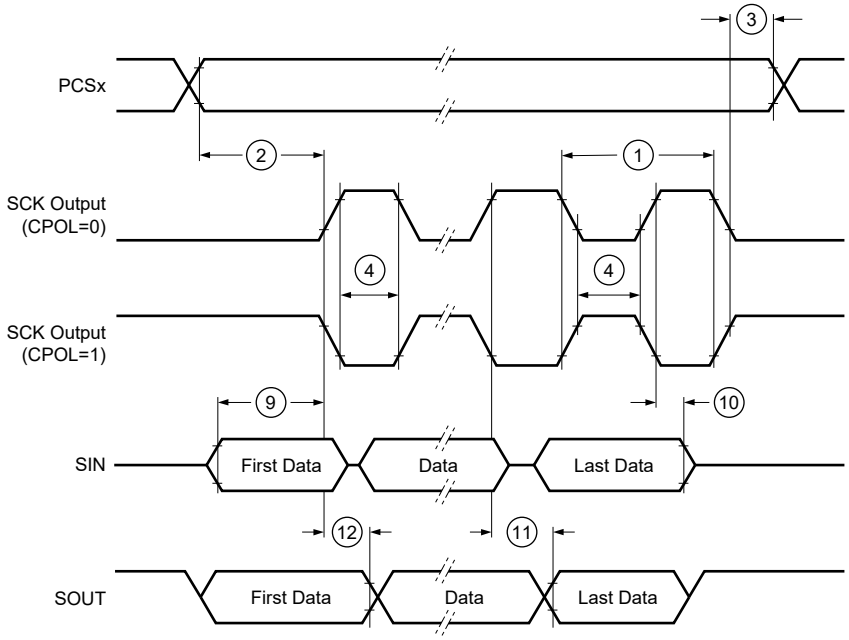


Figure 28. SPI Modified Transfer Format Timing - Master, CPHA = 0, MTFE=1

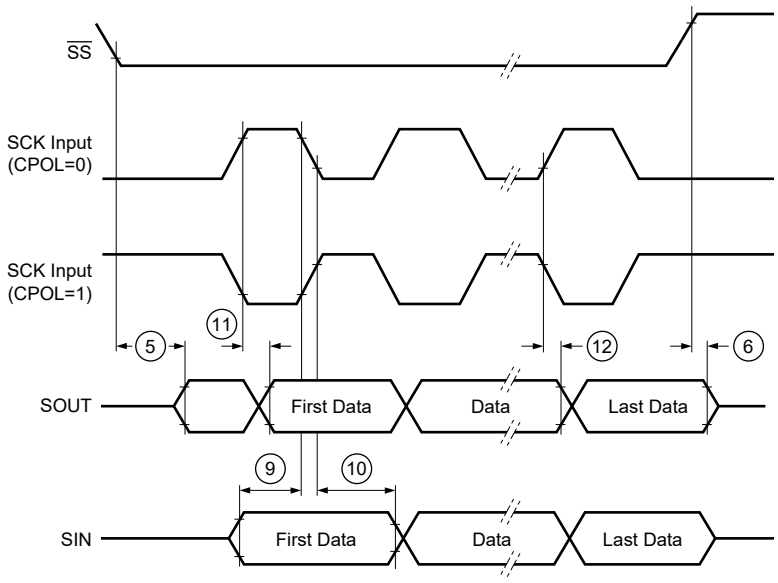


Figure 29. SPI Classic Timing - Slave CPHA = 1, MTFE=0

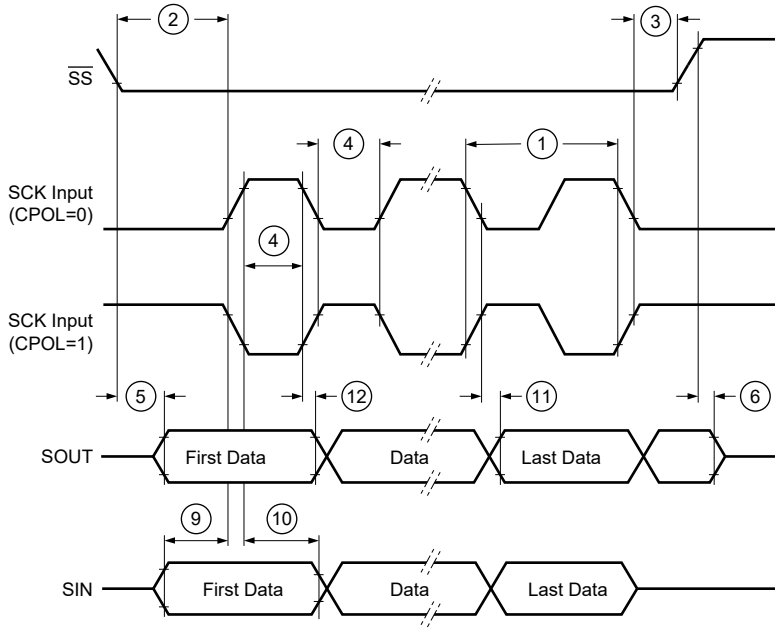


Figure 30. SPI Classic Timing - Slave CPHA = 0, MTFE=0

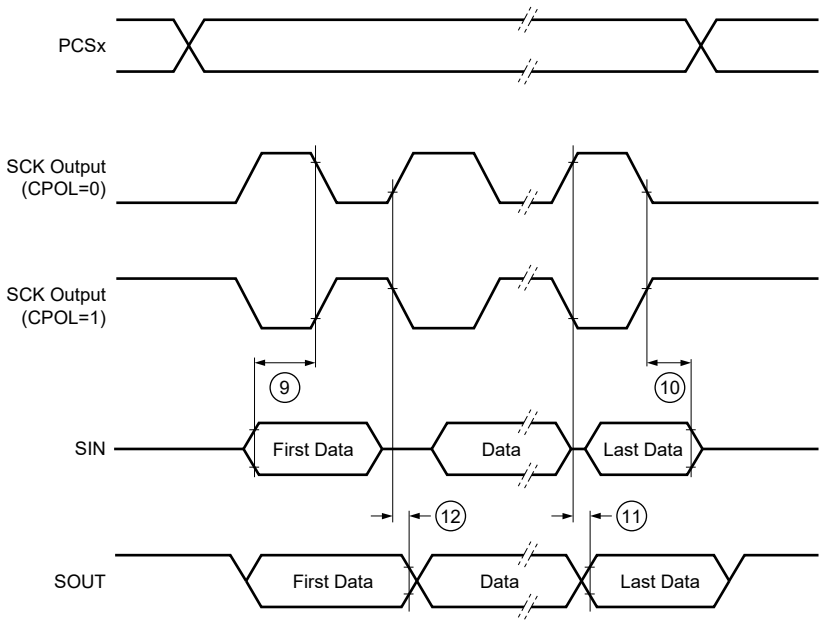


Figure 31. SPI Classic Timing - Master, CPHA = 1, MTFE=0

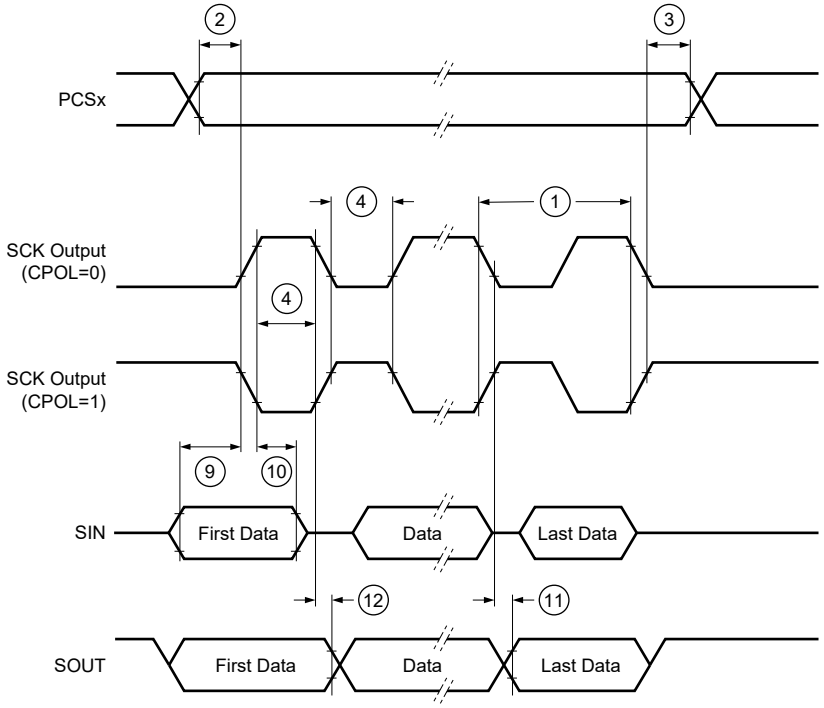


Figure 32. SPI Classic Timing - Master, CPHA = 0, MTFE=0

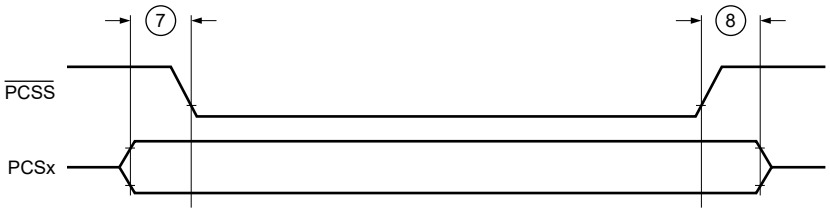


Figure 33. SPI PCS Strobe (PCSS) Timing

16.3.2 I2C

16.3.2.1 I2C Input

Table 28. I2C Input

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tIH_SC	Input Start condition hold time [1, 2]	2	—	—	PER_CLK cycle	—	1
tCL	Input Clock low time [1, 2]	8	—	—	PER_CLK cycle	—	2
tIH	Input Data hold time [1, 2]	0	—	—	ns	SDA transitions after SCL falling edge	4
tCH	Input Clock high time [1, 2]	4	—	—	PER_CLK cycle	—	6

Table continues on the next page...

Table 28. I2C Input (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tISU	Input Data setup time (standard mode) [1, 2, 3]	250	—	—	ns	SDA transitions before SCL rising edge	7
tISU_F	Input Data setup time (fast mode) [1, 2, 3]	100	—	—	ns	SDA transitions before SCL rising edge	7
tISU_RSC	Input Start condition setup time (repeated start condition) [1, 2]	2	—	—	PER_CLK cycle	—	8
tISU_SC	Input Start condition setup time [1, 2]	2	—	—	PER_CLK cycle	—	9

1. PER_CLK from the MC_CGM is the clock driving the I2C block.
2. Input timing assumes an input signal slew rate of 3ns (20%/80%).
3. PER_CLK frequency should be greater than 5 MHz for standard mode and 20 MHz for fast mode.

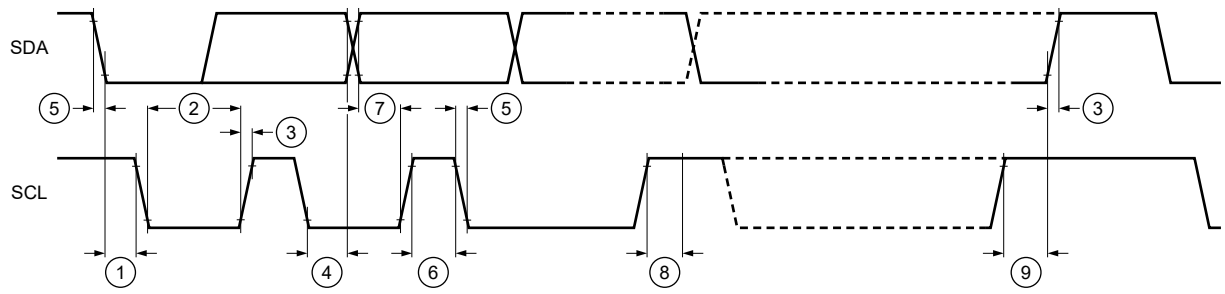


Figure 34. I2C Input/Output Timing

16.3.2.2 I2C Output

Table 29. I2C Output

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tOH_SC	Output Start condition hold time [1, 2, 3]	6	—	—	PER_CLK cycle	—	1
tCL	Output Clock low time [1, 2, 3]	10	—	—	PER_CLK cycle	—	2
tRISE	SDA/SCL rise time [1, 2, 3, 4]	—	—	100	ns	SRE[2:0] = 110	3
tOH	Output Data hold time [1, 2, 3]	7	—	—	PER_CLK cycle	SRE[2:0] = 110	4
tFALL	SDA/SCL fall time [1, 2, 3, 4]	—	—	100	ns	SRE[2:0] = 110	5

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Table 29. I2C Output (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tCH	Output Clock high time [1, 2, 3]	10	—	—	PER_CLK cycle	SRE[2:0] = 110	6
tOSU	Output Data setup time [1, 2, 3]	2	—	—	PER_CLK cycle	SRE[2:0] = 110	7
tOSU_RSC	Output repeated start condition setup time [1, 2, 3]	20	—	—	PER_CLK cycle	SRE[2:0] = 110	8
tOSU_SC	Output start condition setup time [1, 2, 3]	11	—	—	PER_CLK cycle	SRE[2:0] = 110	9

1. Timing valid for maximum external load CL = 400pF, at the maximum clock frequency defined by the I2C clock high and low time specifications.
2. PER_CLK from the MC_CGM is the clock driving the I2C block.
3. Programming IBFD (I2C bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I2C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IBFD.
4. Because SCL and SDA are open-drain outputs, which the processor can only actively drive low, the time SCL or SDA takes to reach a high level depends on external signal capacitance and pullup resistor values

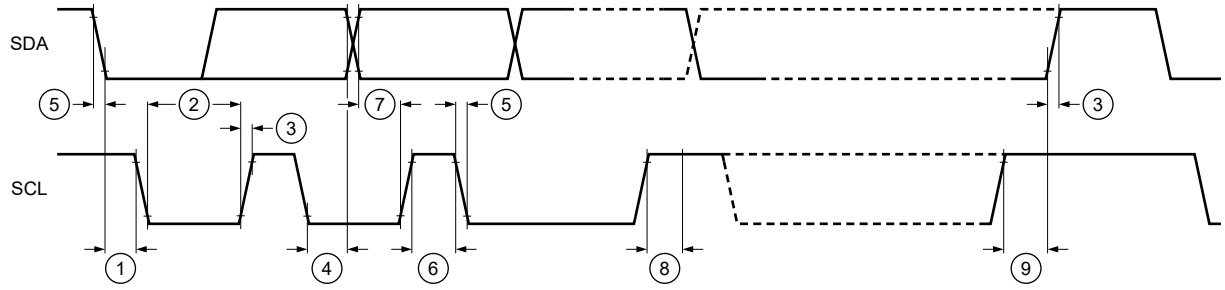


Figure 35. I2C Input/Output Timing

16.3.3 LIN

Table 30. LIN

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
RATE	Bit Rate	—	—	2.0	Mbps	UART mode SRE[2:0] = 110	—
RATE	Bit Rate	4.8	—	20	Kbps	LIN mode SRE[2:0] = 110	—

16.3.4 LPSPI

Table 31. LPSPI

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fOP	LPSPI operating frequency [1, 2, 3, 4]	fPER_CLK / 2048	—	40	MHz	Master	—
fOP	LPSPI operating frequency [3, 4, 5]	—	—	20	MHz	Slave	—
tSPSCK	SPSCK period [1, 2, 3, 4]	25	—	1 (fPER_CLK / 2048)	ns	Master	—
tSPSCK	SPSCK period [3, 4, 5]	50	—	—	ns	Slave	—
tLEAD	Enable lead time (PCS to SPSCK delay) [4, 6, 7]	tSPSCK - 3.5	—	—	ns	Master	—
tLEAD	Enable lead time (PCS to SPSCK delay) [4, 6]	25	—	—	ns	Slave	—
tLAG	Enable lag time (after SPSCK delay) [4, 8, 9]	tSPSCK - 2.5	—	—	ns	Master	—
tLAG	Enable lag time (after SPSCK delay) [4, 8]	25	—	—	ns	Slave	—
tSW	Clock (SPSCK) high or low time (duty cycle)	(tSPSCK / 2) - 3	—	(tSPSCK / 2) + 3	ns	Master	—
tSW	Clock (SPSCK) high or low time (duty cycle)	(tSPSCK / 2) - 3	—	(tSPSCK / 2) + 3	ns	Slave	—
tSU	Data setup time (inputs)	12	—	—	ns	Master	—
tSU	Data setup time (inputs)	4	—	—	ns	Slave	—
tHO	Data hold time (inputs)	0	—	—	ns	Master	—
tHO	Data hold time (inputs)	3	—	—	ns	Slave	—
tA	Slave access time	—	—	12.5	ns	Slave	—
tDIS	Slave MISO disable time	—	—	12.5	ns	Slave	—

Table continues on the next page...

Table 31. LPSPI (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tV	Data valid (after SPSCK edge) [4, 10, 11]	—	—	6	ns	Master, SRE[2:0] = 101	—
tV	Data valid (after SPSCK edge) [4, 10, 11]	—	—	20	ns	Slave, SRE[2:0] = 101	—
tHO	Data hold time (outputs) [4, 10, 11]	0	—	—	ns	Master, SRE[2:0] = 101	—
tHO	Data hold time (outputs) [4, 10, 11]	0	—	—	ns	Slave, SRE[2:0] = 101	—
tRI_FI	Rise / Fall time (input) [12]	—	—	1	ns	Master + Slave	—

1. The maximum master mode LPSPI clock frequency can be no more than the peripheral clock frequency divided by 2.
2. fPER_CLK is the frequency of the device peripheral clock (PER_CLK).
3. The maximum LPSPI baud rate that is achievable in a dedicated master-slave connection depends on several parameters that are independent of the LPSPI module clocking capabilities (e.g. capacitive load of the signal lines, SPI slave clock-to-datadelay, pad slew rate, etc.). The maximum achievable LPSPI baud rate needs to be evaluated in a corresponding SPI master-slave setup.
4. All timing valid to 20% and 80% levels of the LPSPI I/O voltage supply on the device.
5. The maximum slave mode LPSPI clock frequency can be no more than the peripheral clock frequency divided by 4.
6. Set the PCSSCK configuration bit as 0, for a minimum of 1 delay cycle of LPSPI baud rate clock, where PCSSCK ranges from 0 to 255.
7. tPCSSCK = (PCSSCK+1) * (2**PRESCALE) * (1 / fPER_CLK)
8. Set the SCKPCS configuration bit as 0, for a minimum of 1 delay cycle of LPSPI baud rate clock, where SCKPCS ranges from 0 to 255.
9. tSCKPCS = (SCKPCS+1) * (2**PRESCALE) * (1 / fPER_CLK)
10. Timing valid for maximum external load CL = 25pF, which is assumed to be a 10pF load at the end of a 50ohm, un-terminated, 5 inch microstrip trace on standard FR4 (1.5pF/inch), (25pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output.
11. Output rise/fall time is determined by the output load and GPIO pad drive strength setting. See the GPIO specifications for detail.
12. The input rise/fall time specification applies to both clock and data, and is required to guarantee related timing parameters.

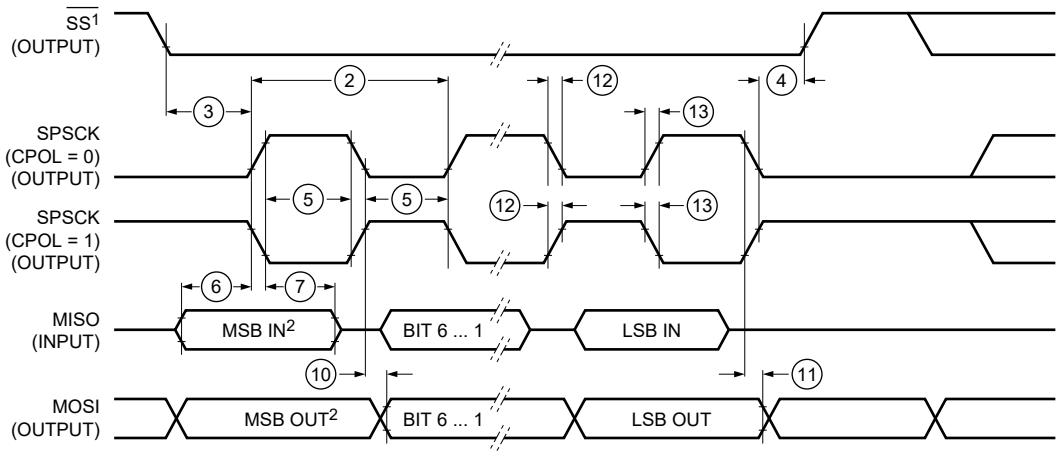


Figure 36. LPSPI Master Mode Timing (CPHA=0)

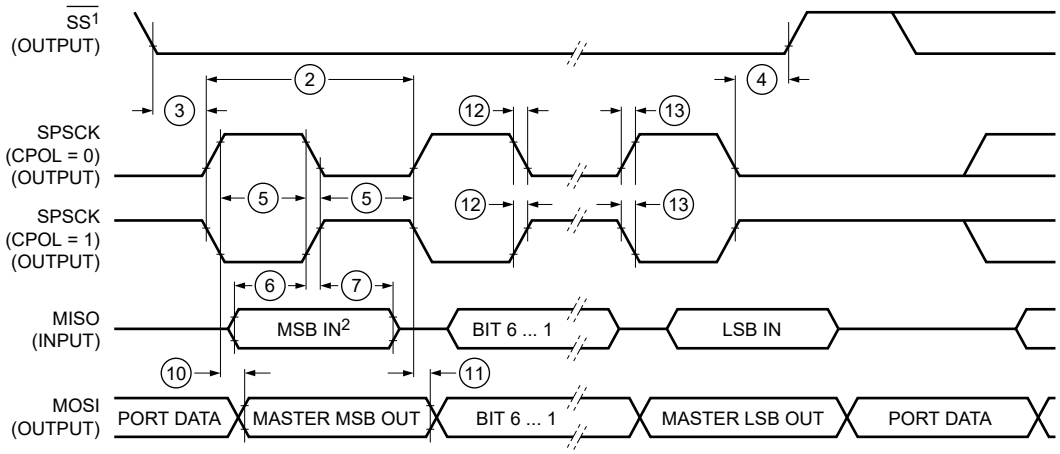


Figure 37. LPSPI Master Mode Timing (CPHA=1)

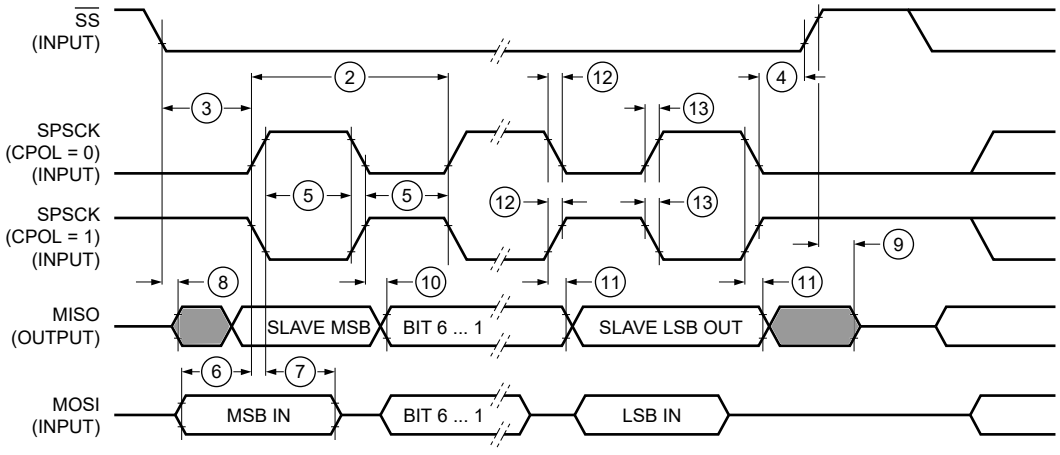


Figure 38. LPSPI Slave Mode Timing (CPHA=0)

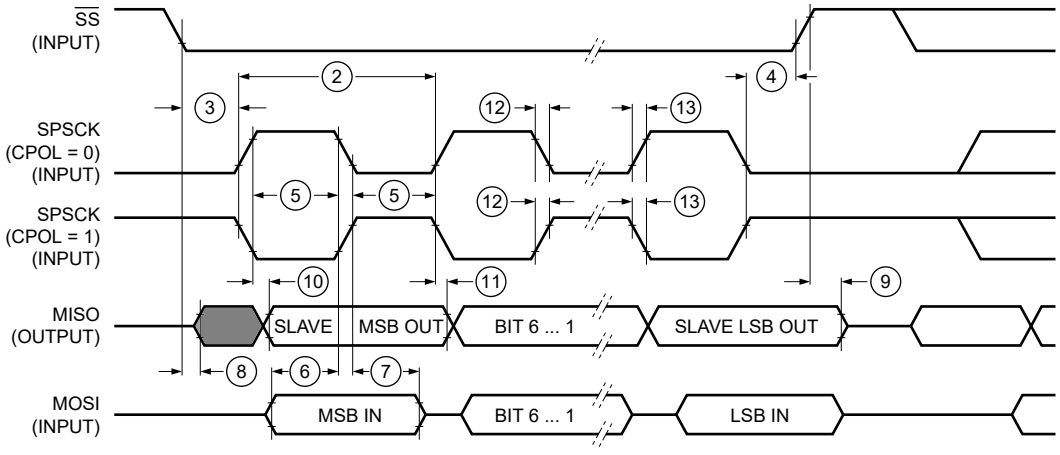


Figure 39. LPSPI Slave Mode Timing (CPHA=1)

16.3.5 FlexRay

16.3.5.1 FlexRay - RxD

Table 32. FlexRay - RxD

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
C_CCRxD	Input capacitance on RxD pin	—	—	8	pF	—	—
uCCLogic_1	Threshold for detecting logic high	35	—	70	%	—	—
uCCLogic_0	Threshold for detecting logic low	30	—	65	%	—	—
dCCRxD01	Sum of delay from actual input to the D input of the first FF, rising edge [1]	—	—	10	ns	—	—
dCCRxD10	Sum of delay from actual input to the D input of the first FF, falling edge [1]	—	—	10	ns	—	—
dCCRxAsymAccept15	Acceptance of asymmetry at receiving CC with 15pF load [1]	-31.5	—	44	ns	—	—
dCCRxAsymAccept25	Acceptance of asymmetry at receiving CC with 25pF load [1]	-30.5	—	43	ns	—	—

1. FlexRay RxD timing assumes an input signal slew rate of 2ns (20%/80%).

16.3.5.2 FlexRay - TxD

Table 33. FlexRay - TxD

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
dCCTxAsym	Asymmetry of sending CC, dCCTxD50% - N x gdBit [1]	-2.45	—	2.45	ns	N=1, gdBit = 100ns, TxD load = 25pF max, SRE[2:0] = 110 (3.3V GPIO)	—
dCCTxDRISE25 + dCCTxDFALL25	Sum of rise and fall time of TxD signal at the ouptut pin [1]	—	—	9	ns	TxD load = 25pF max, Z = 50ohms, delay = 0.6ns, SRE[2:0] = 110 (3.3V GPIO)	—

Table continues on the next page...

Table 33. FlexRay - TxD (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
dCCTxD01	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge [1]	—	—	25	ns	TxD load = 25pF max, SRE[2:0] = 110 (3.3V GPIO)	—

1. Timing valid for maximum external load CL = 25pF, which is assumed to be a 8pF load at the end of a 50Ohm, un-terminated, 5 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the RDSON of the I/O pad output driver.

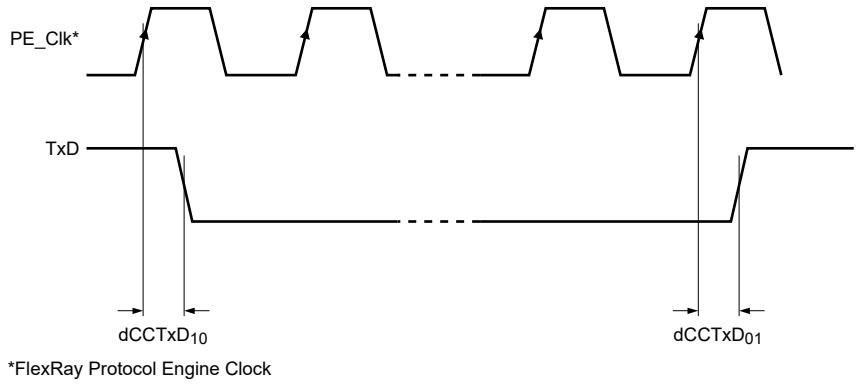


Figure 40. TxD Signal Propogation Delay

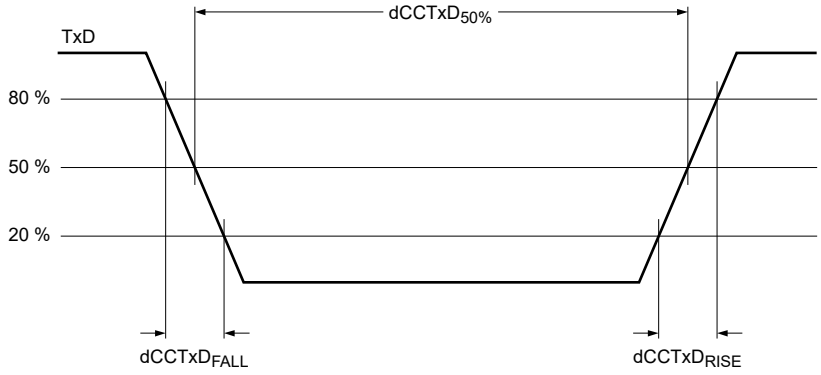


Figure 41. TxD Signal

16.3.5.3 FlexRay - TxEN

Table 34. FlexRay - TxEN

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
dCCTxENRISE25	Rise time of TxEN signal at CC [1]	—	—	9	ns	TxEN load = 25pF max, SRE[2:0] = 110 (3.3V GPIO)	—

Table continues on the next page...

Table 34. FlexRay - TxEN (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
dCCTxENFALL25	Fall time of TxEN signal at CC [1]	—	—	9	ns	TxEN load = 25pF max, SRE[2:0] = 110 (3.3V GPIO)	—
dCCTxEN01	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge [1]	—	—	25	ns	TxEN load = 25pF max, SRE[2:0] = 110 (3.3V GPIO)	—
dCCTxEN10	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge [1]	—	—	25	ns	TxEN load = 25pF max, SRE[2:0] = 110 (3.3V GPIO)	—

1. Timing valid for maximum external load CL = 25pF, which is assumed to be a 8pF load at the end of a 50Ohm, un-terminated 5 inch microstrip trace on standard FR4 (1.5pF/inch), (25pF total with margin). For best signal integrity, the series resistance of the transmission line should be matched closely to the RDSON of the I/O pad output driver.

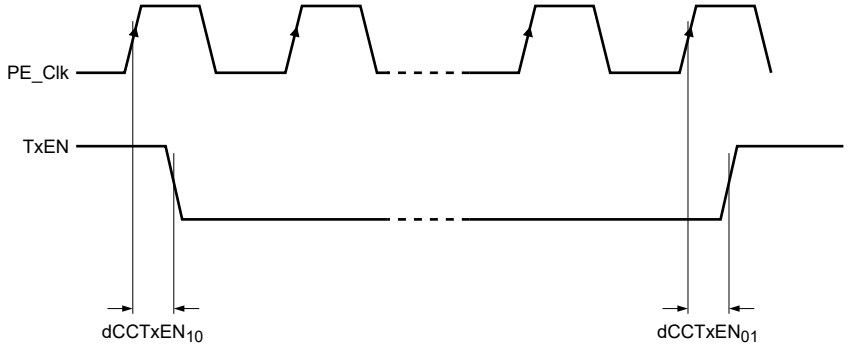


Figure 42. TxEN Signal Propogation Delay

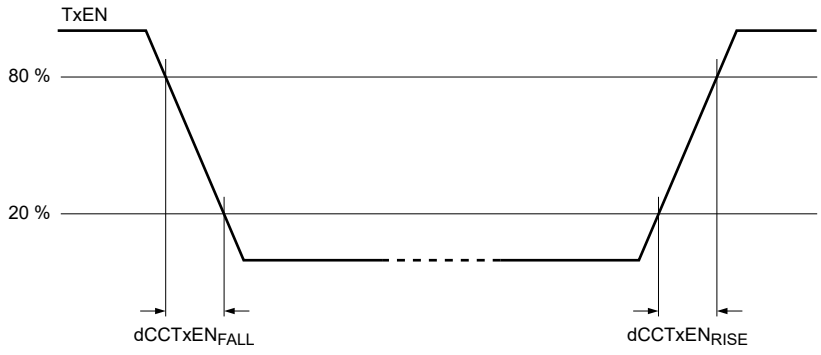


Figure 43. TxEN Signal

16.3.6 PCIe

Table 35. PCIe

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
UI	Unit Interval [1]	399.88	—	400.12	ps	2.5GT/s	—
UI	Unit Interval [1]	199.94	—	200.06	ps	5.0GT/s	—
UI	Unit Interval [1]	124.9625	—	125.0375	ps	8.0GT/s	—
VTX-DIFF-PP	Differential p-p Tx voltage swing [1]	0.8	—	1.2	Vp-p	2.5GT/s, 5.0GT/s	—
VTX-DE-RATIO-3.5dB	Tx de-emphasis level ratio [1]	2.5	—	4.5	dB	2.5GT/s, 5.0GT/s	—
VTX-DE-RATIO-6dB	Tx de-emphasis level ratio [1]	5	—	7	dB	5.0GT/s	—
TMIN-PULSE	Instantaneous lone pulse width [1]	0.9	—	—	UI	5.0GT/s	—
TTX-EYE	Transmitter Eye including all jitter sources [1]	0.75	—	—	UI	2.5GT/s, 5.0GT/s	—
TTX-HF-DJ-DD	Tx deterministic jitter > 1.5 MHz [1]	—	—	0.15	UI	5.0GT/s	—
TTX-LF-RMS	Tx RMS jitter < 1.5 MHz [1]	—	3	—	ps RMS	5.0GT/s	—
BWTX-PKG-PLL1	Tx PLL BW corresponding to PKGTX-PLL1 [1]	8	—	16	MHz	5.0GT/s	—
BWTX-PKG-PLL1	Tx PLL BW corresponding to PKGTX-PLL1 [1]	2	—	4	MHz	8.0GT/s	—
BWTX-PKG-PLL2	Tx PLL BW corresponding to PKGTX-PLL2 [1]	5	—	16	MHz	5.0GT/s	—
BWTX-PKG-PLL2	Tx PLL BW corresponding to PKGTX-PLL2 [1]	2	—	5	MHz	8.0GT/s	—
PKGTX-PLL1	Tx PLL peaking [1]	—	—	3	dB	5.0GT/s	—
PKGTX-PLL1	Tx PLL peaking [1]	—	—	2	dB	8.0GT/s	—
PKGTX-PLL2	Tx PLL peaking [1]	—	—	1	dB	5.0GT/s	—
PKGTX-PLL2	Tx PLL peaking [1]	—	—	1	dB	8.0GT/s	—
BWTX-PLL	Maximum Tx PLL bandwidth [1]	1.5	—	22	MHz	2.5GT/s	—

Table continues on the next page...

Table 35. PCIe (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TTX-EYE-MEDIAN-to-MAXJITTER	Maximum time between the jitter median and max deviation from the median [1]	—	—	0.125	UI	2.5GT/s	—
VTX-FS-NO-EQ	Full Swing Tx voltage with no TxEq [1]	800	—	1300	mVPP	8.0GT/s	—
VTX-EIEOS-FS	Min Swing during EIEOS for full swing [1]	250	—	—	mVPP	8.0GT/s	—
TTX-UTJ	Tx uncorrelated total jitter [1]	—	—	31.25	ps PP @ 10e-12	8.0GT/s	—
TTX-UDJDD	Tx uncorrelated deterministic jitter [1]	—	—	12	ps PP	8.0GT/s	—
VTX-BOOST-FS	Tx boost ratio for full swing [1]	8	—	—	dB	8.0GT/s	—
VRX-DIFF-PP-CC	Differential Rx peak-peak voltage for common Refclk Rx architecture [1]	0.175	—	1.2	V	2.5GT/s	—
VRX-DIFF-PP-CC	Differential Rx peak-peak voltage for common Refclk Rx architecture [1]	0.12	—	1.2	V	5.0GT/s	—
TRX-EYE	Receiver eye time opening [1]	0.4	—	—	UI	2.5GT/s	—
TRX-TJ-CC	Max Rx inherent timing error [1]	—	—	0.4	UI	5.0GT/s	—
TRX-DJ-DD_CC	Max Rx deterministic timing error [1]	—	—	0.3	UI	5.0GT/s	—
VRX-EYE	Receive eye voltage opening [1]	—	120	—	mVPP diff	5.0GT/s	—
VRX-SV-8G	Eye height at TP2P [1]	—	25	—	mVPP	8.0GT/s, -20dB Ch	—
VRX-SV-8G	Eye height at TP2P [1]	—	50	—	mVPP	8.0GT/s, -12dB Ch	—
VRX-SV-8G	Eye height at TP2P [1]	—	200	—	mVPP	8.0GT/s, -3dB Ch	—
TRX-SV-8G	Eye width at TP2P [1]	0.3	—	0.35	UI	8.0GT/s	—
TRX-SV-SJ-8G	Sinusoidal Jitter at 100MHz [1]	—	0.1	—	UI PP	8.0GT/s	—

Table continues on the next page...

Table 35. PCIe (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TRX-SV-RJ-8G	Random Jitter [1]	—	2	—	ps RMS	8.0GT/s	—
REXTPCIe	External pin calibration resistance	198	200	202	Ω	—	—

1. The PCI Express link conforms to the PCI Express Base Specification, Revision 3.1. The summary of Transmitter and Receiver specifications are copied directly from the Base Specification. Consult the Base Specification for additional details.

NXP completed PCI-SIG compliance testing with the following PHY registers modified from default settings as described below. PHY register and programming details are provided in S32SERDESSUBSYSRM. PHY TX settings optimized for NXP validation board for SUP_ANA_TERM_CTRL = 4 and TX_VBOOST_LVL = 4. PHY PLL bandwidth updated for MPLLB_BW_OVRD_VAL = 218 and MPLLA_BW_OVRD_VAL = 197. PHY RX equalization tuned for PCIe Gen3 long and short channel cases for RX_EQ_DELTA_IQ_OVRD_VAL = 3.

NXP completed PCI-SIG TX compliance testing using external reference clock source.

16.3.7 GMAC and PFE

16.3.7.1 GMAC and PFE MII

Table 36. GMAC and PFE MII

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tCYC_RX	RX_CLK period	—	40 / 400	—	ns	10/100 Mbps	—
ΔtCYC_RX	RX_CLK duty cycle (tPWH / tCYC)	45	—	55	%	—	—
tS	Input setup time to RX_CLK [1]	5	—	—	ns	10/100 Mbps	—
tH	Input hold time to RX_CLK [1]	5	—	—	ns	10/100 Mbps	—
tCYC_TX	TX_CLK period [2]	—	40 / 400	—	ns	10/100 Mbps, SRE[2:0] = 100	—
ΔtCYC_TX	TX_CLK duty cycle (tPWH / tCYC) [2]	45	—	55	%	SRE[2:0] = 100	—
tD	Output delay from TX_CLK [2]	2	—	25	ns	10/100 Mbps, SRE[2:0] = 100	—

1. Input timing assumes an input signal slew rate of 3ns (20%/80%).
2. Output timing valid for maximum external load CL = 25pF, which is assumed to be a 10pF load at the end of a 50Ohm, un-terminated, 5 inch microstrip trace on standard FR4 (1.5pF/inch), (25pF total with margin). For best signal integrity, the series resistance of the transmission line should be matched closely to the RDSON of the I/O pad output driver.

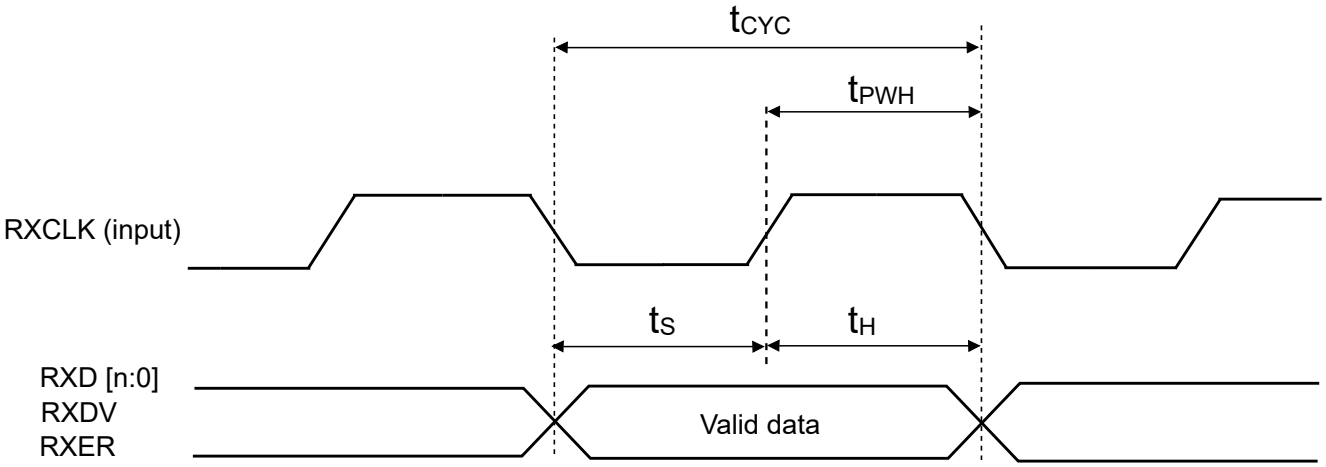


Figure 44. MII Receive Timing

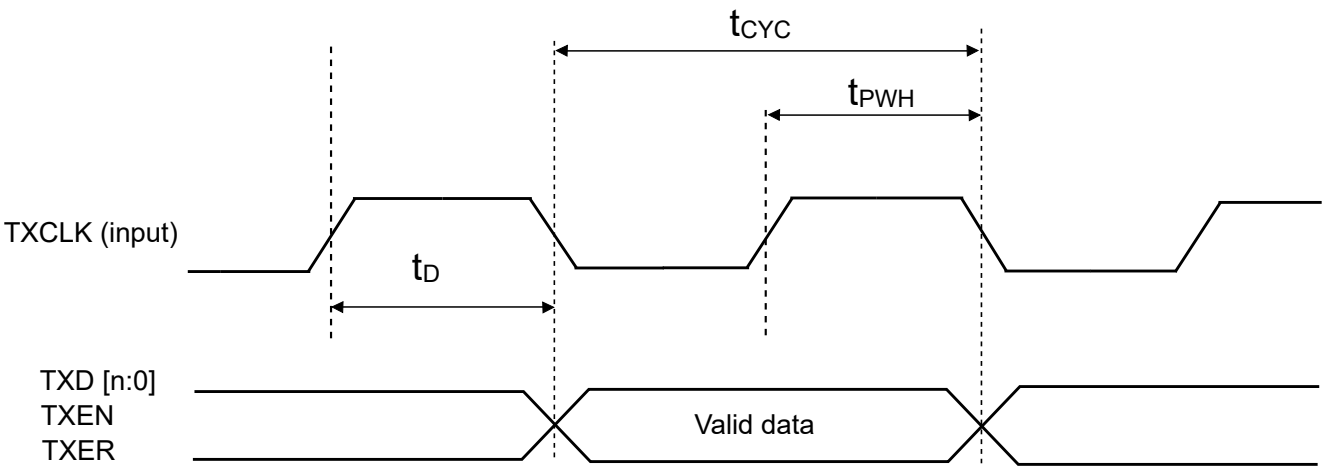


Figure 45. MII Transmit Timing

16.3.7.2 GMAC MII 50MHz

NOTE

GMAC MII 50MHz spec apply to GMAC only.

Table 37. GMAC MII 50MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fRXCLK	RXCLK frequency [1]	—	—	50	MHz	—	—
dtRXCLK	RXCLK pulse width high [1]	35	—	65	% RXCLK period	—	E3
dtRXCLK	RXCLK pulse width low [1]	35	—	65	% RXCLK period	—	E4

Table continues on the next page...

Table 37. GMAC MII 50MHz (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tSETUP	RXD[3:0], RXDV, RXER to RXCLK setup time [1]	4	—	—	ns	—	—
tHOLD	RXCLK to RXD[3:0], RXDV, RXER hold time [1]	2	—	—	ns	—	—
fTXCLK	TXCLK frequency [2]	—	—	50	MHz	—	—
dtTXCLK	TXCLK pulse width high [2]	35	—	65	% TXCLK period	—	E7
dtTXCLK	TXCLK pulse width low [2]	35	—	65	% TXCLK period	—	E8
tDATA_VALID	TXCLK to TXD[3:0], TXDV, TXER valid [2]	—	—	15	ns	—	E6
tDATA_INVALID	TXCLK to TXD[3:0], TXDV, TXER invalid [2]	2	—	—	ns	—	E5

1. Input timing assumes an input signal slew rate of 3ns (20%/80%).
2. Output timing valid for maximum external load CL = 25pF, which is assumed to be a 10pF load at the end of a 50Ohm, un-terminated, 5 inch microstrip trace on standard FR4 (1.5pF/inch, (25pF total with margin). For best signal integrity, the series resistance in the transmission line should be matched closely to the selected RDSON of the I/O pad output driver.

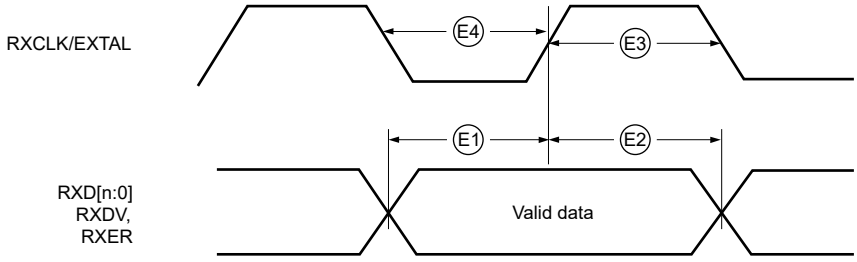


Figure 46. MII 50MHz Receive Timing

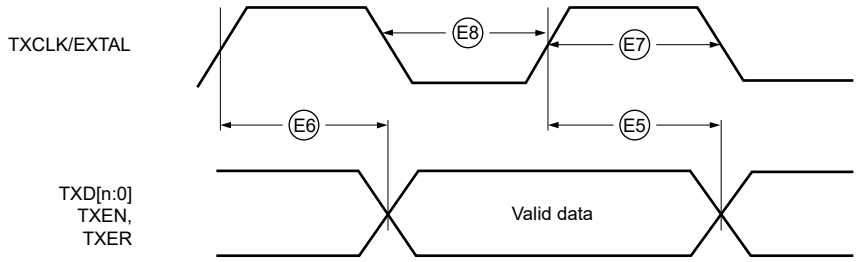


Figure 47. MII 50MHz Transmit Timing

16.3.7.3 GMAC and PFE RMII

Table 38. GMAC and PFE RMII

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fRMII_CLK	RMII input clock frequency (RMII_CLK)	—	—	50	MHz	—	—
ΔtRMII_CLK	RMII_CLK duty cycle (tPWH / tCYC)	35	—	65	%	—	E3, E4, E7, E8
tS	RXD[1:0], CRS_DV, RXER to RMII_CLK setup time [1]	4	—	—	ns	—	E1
tH	RMII_CLK to RXD[1:0], CRS_DV, RXER hold time [1]	2	—	—	ns	—	E2
tDATA_VALID	RMII_CLK to TXD[1:0], TXEN data valid [2]	—	—	14	ns	CLOAD = 25pF, SRE[2:0] = 100	E6
tDATA_INVALID	RMII_CLK to TXD[1:0], TXEN data invalid [2]	2	—	—	ns	CLOAD = 25pF, SRE[2:0] = 100	E5

1. Input timing assumes an input signal slew rate of 3ns (20%/80%).
2. Output timing valid for maximum external load CL = 25pF, which is assumed to be a 10pF load at the end of a 50Ohm, un-terminated, 5 inch microstrip trace on standard FR4 (1.5pF/inch), (25pF total with margin). For best signal integrity, the series resistance of the transmission line should be matched closely to the RDSON of the I/O pad output driver.

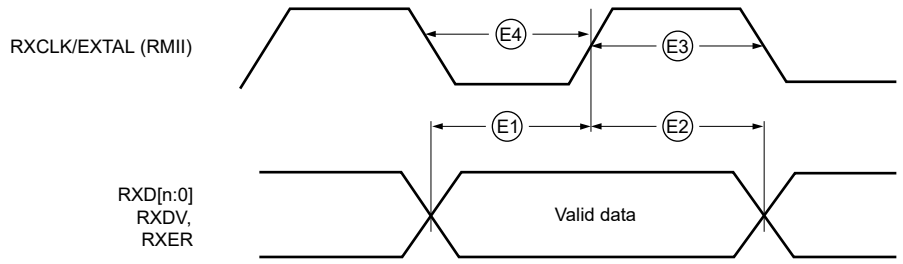


Figure 48. RMII Receive Timing

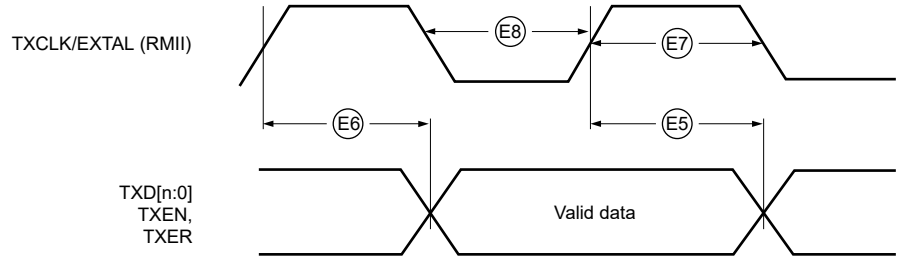


Figure 49. RMII Transmit Timing

16.3.7.4 GMAC and PFE Management Interface

Table 39. GMAC and PFE Management Interface

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fMDC	MDC clock frequency	—	—	2.5	MHz	—	MDC00
MDIO_CH	MDC pulse width high time	40	—	60	%	—	MDC14
MDIO_CL	MDC pulse width low time	40	—	60	%	—	MDC15
MDIO_DOI	MDC falling edge to MDIO output invalid (minimum propagation delay)	-0.45	—	—	ns	SRE[2:0] = 100	MDC10
MDIO_DOV	MDC falling edge to MDIO output valid (maximum propagation delay)	—	—	15	ns	SRE[2:0] = 100	MDC11
MDIO_ISU	MDIO (input) to MDC rising edge setup time [1]	13	—	—	ns	—	MDC12
MDIO_IH	MDIO (input) to MDC rising edge hold time	0	—	—	ns	—	MDC13

1. MDIO_ISU spec is for GMAC, for PFE it is 17ns (min)

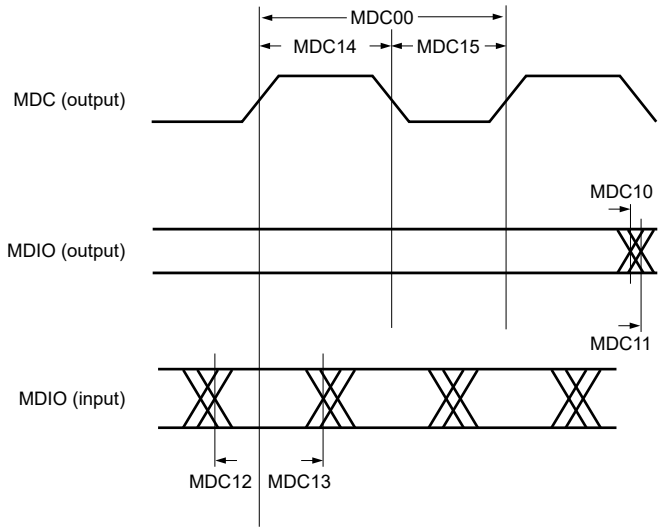


Figure 50. MDC / MDIO Timing

16.3.7.5 GMAC and PFE RGMII

Table 40. GMAC and PFE RGMII

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Tcyc	Clock cycle duration [1, 2, 3, 4]	7.2	—	8.8	ns	SRE[2:0] = 100	—
TskewT	Data to clock output skew (at transmitter) [2, 3, 4, 5]	-500	—	500	ps	SRE[2:0] = 100	—
TskewR	Data to clock input skew (at receiver) [2, 4, 5]	1	—	2.6	ns	SRE[2:0] = 100	—
Duty_G	Clock duty cycle for Gigabit [2, 4, 6]	45	—	55	%	SRE[2:0] = 100	—
Duty_T	Clock duty cycle for 10/100T [2, 4, 6]	40	—	60	%	SRE[2:0] = 100	—

1. For 10 Mbps and 100 Mbps, Tcyc will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.
2. Measured as defined in EIA/JESD 8-6 1995 with a timing threshold voltage of VDDQ/2
3. Output timing valid for maximum external load CL = 15pF, which is assumed to be a 8pF load at the end of a 50ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the selected RDSON of the I/O pad output driver.
4. RGMII timing specifications are valid for both 1.8V and 3.3V nominal I/O pad supply voltage.
5. For all versions prior to RGMII v2.0 specifications; This implies that PC board design will require clocks to be routed such that an additional delay of greater than 1.5 ns and less than 2 ns will be added to the associated clock signal. For 10/100, the max value is unspecified.
6. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

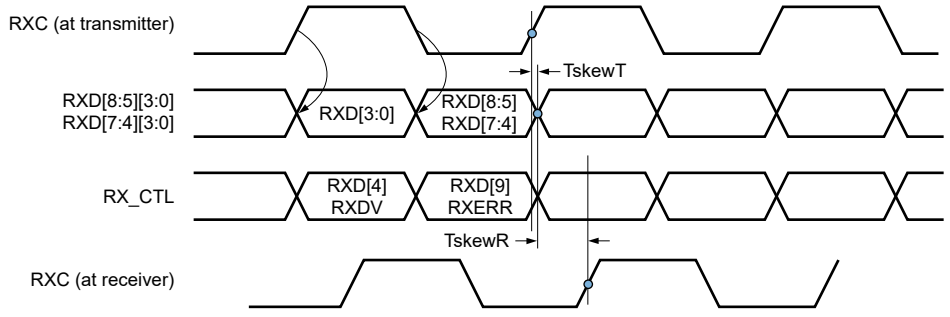


Figure 51. RGMII Receive Timing

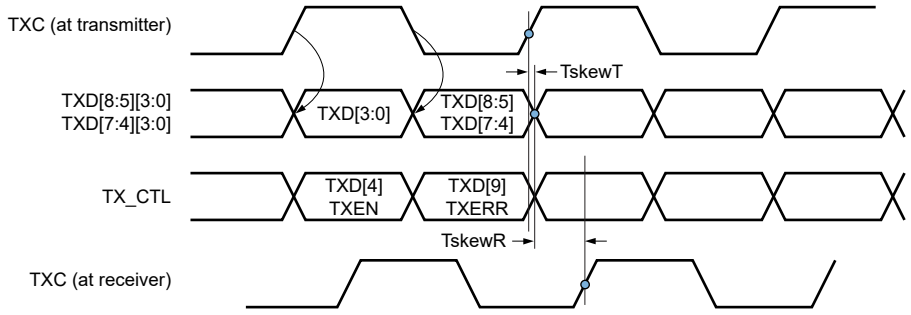


Figure 52. RGMII Transmit Timing

16.3.7.6 GMAC and PFE SGMII

Table 41. GMAC and PFE SGMII

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
UI	Unit Interval	799.92	800	800.08	ps	1.25Gbps, applies to both transmitter and receiver	—
UI	Unit Interval	319.968	320	320.032	ps	3.125Gbps, applies to both transmitter and recdeiver	—
trise	Transmit Vod rise time (20-80%)	—	—	100	ps	—	—
tfall	Transmit Vod fall time (20-80%)	—	—	100	ps	—	—
|VOD|	Transmit Output Differential Voltage	400	—	600	mV	1.25Gbps	—
|VOD|	Transmit Output Differential Voltage [1]	400	—	600	mV	3.125Gbps	—
RDOUT	Transmit Differential Output Impedance	80	100	120	Ohm	—	—
Dj	Transmit Deterministic Jitter	—	—	0.17	UI	—	—
Tj	Transmit Total Jitter	—	—	0.35	UI	—	—
RDIN	Receiver Differential Input Impedance	80	—	120	Ohm	—	—
VIN	Receiver Differential Input Voltage	200	—	1200	mV	—	—
LOS	Loss-of-signal threshold	75	—	200	mV	—	—
Sjt	Receiver deterministic jitter	—	—	0.37	UI	—	—

Table continues on the next page...

Table 41. GMAC and PFE SGMII (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	tolerance with sinusoidal noise [2]						
DRjt	Receiver combined random and deterministic jitter tolerance with sinusoidal noise [2]	—	—	0.55	UI	—	—
Tjt	Receiver total jitter tolerance	—	—	0.65	UI	—	—
BER	Bit Error Rate	—	—	10^-12	—	—	—

1. VOD at 3.125Gbps is only applicable for PFE_MAC0.
2. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the un-shaded region of the figure below.

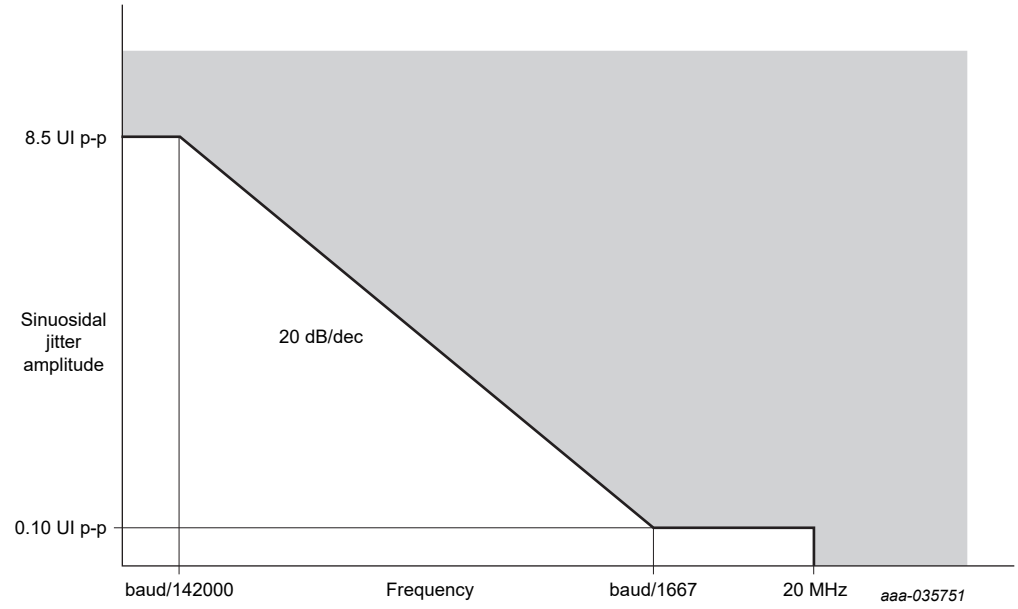


Figure 53. SGMII Timing

16.3.8 USB

16.3.8.1 USB-ULPI

Table 42. USB-ULPI

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TCLK	USB_CLKIN period	—	16.67	—	ns	—	U1

Table continues on the next page...

Table 42. USB-ULPI (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
DFCLK	USB_CLKIN duty cycle	—	50	—	%	—	—
tISU	Input setup time (control and data) [1]	5	—	—	ns	—	U2
tIH	Input hold time (control and data) [1]	1	—	—	ns	—	U3
tOV	Output valid time (control and data) [2]	—	—	9.5	ns	—	U4
tOH	Output hold time (control and data) [2]	1	—	—	ns	—	U5

1. Input timing assumes an input signal slew rate of 3ns (20%/80%).
2. Output timing valid for maximum external load CL = 25pF, which is assumed to be a 10pF load at the end of a 50Ohm, un-terminated, 5 inch microstrip trace on standard FR4 with 1.5pF/inch (25pF total with margin). For best signal integrity, the series resistance of the transmission line should match closely to the RDSON of the I/O pad output driver.

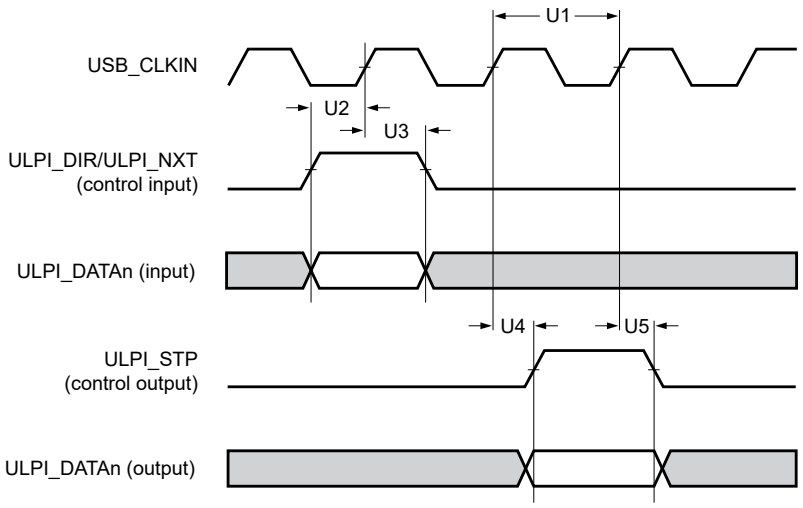


Figure 54. ULPI Mode Interface Timing

16.4 Memory interfaces

16.4.1 QuadSPI

16.4.1.1 QuadSPI

An external resistor is needed to pull up a QuadSPI chip select signal.

16.4.1.2 QuadSPI Quad 1.8V DDR 66MHz

The SRE[2:0]=110 is the required drive setting to meet the timing.

FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 3.

Table 43. QuadSPI Quad 1.8V DDR 66MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK	SCK clock frequency [1, 2]	—	—	66	MHz	DLL mode enabled	—
tCL_SCK	SCK clock low time [1, 2, 3]	6.818	—	—	ns	—	—
tCH_SCK	SCK clock high time [1, 2, 3]	6.818	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK) [1]	2.316	—	4.802	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK) [1, 4]	5.016 - n/fSCK	—	1.802 + m/fSCK	ns	—	—
tDVW	Input data valid window [2]	5.14	—	—	ns	—	—
tLSKEW	Skew target for Auto-learning mode [5]	1.89	—	—	ns	—	—

1. Output timing valid for maximum external load CL = 20pF, which is assumed to be a 10pF-15pF load at the end of a 50ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance in the transmission line should be matched closely to the selected RDSON of the I/O pad output.
2. Input timing assumes maximum input signal transition of 1ns (20%/80%).
3. Clock measurements done with respect to VDD_IO_QSPI/2 level.
4. Where m=TCSS and n=TCSH-1.
5. Data valid window includes DLL Margin, and determines LEARNING skew targets which can be more pessimistic than tISU_SCK and tIH_SCK.

16.4.1.3 QuadSPI Quad 1.8V SDR 133MHz

The SRE[2:0]=110 is the required drive setting to meet the timing.

FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 3.

Table 44. QuadSPI Quad 1.8V SDR 133MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK	SCK clock frequency [1, 2]	—	—	133	MHz	DLL mode enabled	—
tCL_SCK	SCK low time [1, 2, 3]	3.383	—	—	ns	—	—
tCH_SCK	SCK high time [1, 2, 3]	3.383	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK) [1]	-0.594	—	1.594	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK) [1, 4]	4.016 - n/fSCK	—	4.204 + m/fSCK	ns	—	—
tDVW	Input data valid window [2]	4.624	—	—	ns	—	—

Table continues on the next page...

Table 44. QuadSPI Quad 1.8V SDR 133MHz (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tISU_SCK	Input setup time (w.r.t. SCK) [2]	0.580	—	—	ns	—	—
tIH_SCK	Input hold time (w.r.t. SCK) [2]	1.000	—	—	ns	—	—

1. Output timing valid for maximum external load CL = 20pF, which is assumed to be a 10pF-15pF load at the end of a 50ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance in the transmission line should be matched closely to the selected RDSON of the I/O pad output.
2. Input timing assumes maximum input signal transition of 1ns (20%/80%).
3. Clock measurements done with respect to VDD_IO_QSPI/2 level.
4. Where m=TCSS and n=TCSH-1.

16.4.1.4 QuadSPI Octal 1.8V DDR 100MHz

The SRE[2:0]=110 is the required drive setting to meet the timing.

FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 3.

Table 45. QuadSPI Octal 1.8V DDR 100MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK_DQS	SCK / DQS frequency [1, 2]	—	—	100	MHz	—	—
tCL_SCK_DQS	SCK / DQS low time [1, 2, 3]	4.500	—	—	ns	—	—
tCH_SCK_DQS	SCK / DQS high time [1, 2, 3]	4.500	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK) [2]	1.016	—	3.484	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK) [2, 4]	3.016 - n/fSCK	—	-0.016 + m/fSCK	ns	—	—
tDVW	Input data valid window [1]	3.284	—	—	ns	—	—
tISU_DQS	Input setup time (w.r.t. DQS) [1]	-0.816	—	—	ns	—	—
tIH_DQS	Input hold time (w.r.t. DQS) [1]	3.684	—	—	ns	—	—

1. Input timing assumes maximum input signal transition of 1 ns (20%/80%). DQS denotes external strobe provided by the Flash.
2. Output timing valid for maximum external load CL = 20pF, which is assumed to be a 10pF-15pF load at the end of a 50ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance in the transmission line should be matched closely to the selected RDSON of the I/O pad output.
3. Clock measurements done with respect to VDD_IO_QSPI/2 level.
4. Where m=TCSS and n=TCSH-1.

16.4.1.5 QuadSPI Octal 1.8V DDR 133MHz

The SRE[2:0]=110 is the required drive setting to meet the timing.

FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 3.

Table 46. QuadSPI Octal 1.8V DDR 133MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK_DQS	SCK / DQS frequency [1, 2]	—	—	133	MHz	DLL mode enabled	—
tCL_SCK_DQS	SCK / DQS low time [1, 2, 3]	3.383	—	—	ns	—	—
tCH_SCK_DQS	SCK / DQS high time [1, 2, 3]	3.383	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK) [2]	0.816	—	2.567	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK) [2, 4]	3.015 - n/fSCK	—	-1.33 + m/fSCK	ns	—	—
tDVW	Input data valid window [1]	2.314	—	—	ns	—	—
tISU_DQS	Input setup time (w.r.t. DQS) [1]	-0.616	—	—	ns	—	—
tIH_DQS	Input hold time (w.r.t. DQS) [1]	2.767	—	—	ns	—	—

1. Input timing assumes maximum input signal transition of 1 ns (20%/80%). DQS denotes external strobe provided by the Flash.
2. Output timing valid for maximum external load CL = 20pF, which is assumed to be a 12pF-15pF load at the end of a 50ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance in the transmission line should be matched closely to the selected RDSON of the I/O pad output.
3. Clock measurements done with respect to VDD_IO_QSPI/2 level.
4. Where m=TCSS and n=TCSH-1.

16.4.1.6 QuadSPI Octal 1.8V DDR 166MHz

The SRE[2:0]=000 is the required drive setting to meet the timing.

FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 3.

Table 47. QuadSPI Octal 1.8V DDR 166MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK-DQS	SCK/DQS frequency [1, 2]	—	—	166	MHz	—	—
tCL_SCK-DQS	SCK/DQS low time [1, 2, 3]	2.711	—	—	ns	—	—
tCH_SCK-DQS	SCK/DQS high time [1, 2, 3]	2.711	—	—	ns	—	—

Table continues on the next page...

Table 47. QuadSPI Octal 1.8V DDR 166MHz (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tOD_DATA	Data output delay (w.r.t. SCK) [1]	0.616	—	2.095	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK) [1, 4]	3.016 - n/fSCK	—	-1.805 + m/fSCK	ns	—	—
tIH_DQS	Input hold time (w.r.t. DQS) [2]	2.145	—	—	ns	—	—
tISU_DQS	Input setup time (w.r.t. DQS) [2]	-0.496	—	—	ns	—	—
tDVW	Input data valid window [2]	1.694	—	—	ns	—	—

1. Output timing valid for maximum external load CL = 20pF, which is assumed to be a 12pF-15pF load at the end of a 50ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance in the transmission line should be matched closely to the selected RDSON of the I/O pad output.
2. Input timing assumes maximum input signal transition of 1 ns (20%/80%). DQS denotes external strobe provided by the Flash.
3. Clock measurements done with respect to VDD_IO_QSPI/2 level.
4. Where m=TCSS and n=TCSH-1. Both TCSS and TCSH should be set to 2.

16.4.1.7 QuadSPI Octal 1.8V DDR 200MHz

The SRE[2:0]=000 is the required drive setting to meet the timing.

FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 3.

Table 48. QuadSPI Octal 1.8V DDR 200MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK-DQS	SCK/DQS frequency [1, 2]	—	—	200	MHz	—	—
tCL_SCK-DQS	SCK/DQS low time [1, 2, 3]	2.25	—	—	ns	—	—
tCH_SCK-DQS	SCK/DQS high time [1, 2, 3]	2.25	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK) [1]	0.616	—	1.634	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK) [1, 4]	3.016 - n/fSCK	—	-2.266 + m/fSCK	ns	—	—
tIH_DQS	Input hold time (w.r.t. DQS) [2]	1.684	—	—	ns	—	—
tISU_DQS	Input setup time (w.r.t. DQS) [2]	-0.466	—	—	ns	—	—
tDVW	Input data valid window [2]	1.284	—	—	ns	—	—

1. Output timing valid for maximum external load CL = 20pF, which is assumed to be a 12pF-15pF load at the end of a 50ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance in the transmission line should be matched closely to the selected RDSON of the I/O pad output.
2. Input timing assumes maximum input signal transition of 1 ns (20%/80%). DQS denotes external strobe provided by the Flash.
3. Clock measurements done with respect to VDD_IO_QSPI/2 level.
4. Where m=TCSS and n=TCSH-1.

16.4.1.8 QuadSPI Octal 1.8V SDR 100MHz

The SRE[2:0]=110 is the required drive setting to meet the timing.

FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 3.

Table 49. QuadSPI Octal 1.8V SDR 100MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK	SCK clock frequency [1, 2]	—	—	100	MHz	—	—
tCL_SCK	SCK clock low time [1, 2, 3]	4.5	—	—	ns	—	—
tCH_SCK	SCK clock high time [1, 2, 3]	4.5	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK) [2]	-2.822	—	2.822	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK) [2, 4]	3.016 - n/fSCK	—	5.160 + m/fSCK	ns	—	—
tDVW	Input data valid window [1]	6.884	—	—	ns	—	—
tISU_SCK	Input setup time (w.r.t. SCK) [1]	3.036	—	—	ns	—	—
tIH_SCK	Input hold time (w.r.t. SCK) [1]	0.9	—	—	ns	—	—

1. Input timing assumes an input signal transition of 1ns (20%/80%).
2. Output timing valid for maximum external load CL = 20pF, which is assumed to be a 10pF-15pF load at the end of a 50ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the selected RDSON of the I/O pad output driver.
3. Clock measurements done with respect to VDD_IO_QSPI/2 level.
4. Where m=TCSS and n=TCSH-1.

16.4.1.9 QuadSPI Octal 1.8V SDR 133MHz

The SRE[2:0]=110 is the required drive setting to meet the timing.

FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 3.

Table 50. QuadSPI Octal 1.8V SDR 133MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK	SCK clock frequency [1, 2]	—	—	133	MHz	DLL mode enabled	—
tCL_SCK	SCK clock low time [1, 2, 3]	3.383	—	—	ns	—	—
tCH_SCK	SCK clock high time [1, 2, 3]	3.383	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK) [1]	-1.594	—	1.594	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK) [1, 4]	3.016 - n/fSCK	—	2.704 + m/fSCK	ns	—	—
tDVW	Input data valid window [2]	4.609	—	—	ns	—	—
tISU_SCK	Input setup time (w.r.t. SCK) [2]	0.580	—	—	ns	—	—
tIH_SCK	Input hold time (w.r.t. SCK) [2]	0.9	—	—	ns	—	—

1. Output timing valid for maximum external load CL = 20pF, which is assumed to be a 10pF-15pF load at the end of a 50ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance in the transmission line should be matched closely to the selected RDSON of the I/O pad output.
2. Input timing assumes maximum input signal transition of 1ns (20%/80%).
3. Clock measurements done with respect to VDD_IO_QSPI/2 level.
4. Where m=TCSS and n=TCSH-1.

16.4.1.10 QuadSPI Quad 3.3V DDR 66MHz

The SRE[2:0]=110 is the required drive setting to meet the timing.

FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 3.

Table 51. QuadSPI Quad 3.3V DDR 66MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK	SCK clock frequency [1, 2]	—	—	66	MHz	DLL mode enabled	—
tCL_SCK	SCK clock low time [1, 2, 3]	6.818	—	—	ns	—	—
tCH_SCK	SCK clock high time [1, 2, 3]	6.818	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK) [1]	2.316	—	4.802	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK) [1, 4]	5.016 - n/fSCK	—	1.802 + m/fSCK	ns	—	—

Table continues on the next page...

Table 51. QuadSPI Quad 3.3V DDR 66MHz (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tDVW	Input data valid window [2]	5.14	—	—	ns	—	—
tLSKEW	Skew target for Auto-learning mode [5]	1.89	—	—	ns	—	—

1. Output timing valid for maximum external load CL = 20pF, which is assumed to be a 10pF-15pF load at the end of a 50ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance in the transmission line should be matched closely to the selected RDSON of the I/O pad output.
2. Input timing assumes maximum input signal transition of 1ns (20%/80%).
3. Clock measurements done with respect to VDD_IO_QSPI/2 level.
4. Where m=TCSS and n=TCSH-1.
5. Data valid window includes DLL Margin, and determines LEARNING skew targets which can be more pessimistic than tISU_SCK and tIH_SCK..

16.4.1.11 QuadSPI Quad 3.3V SDR 104MHz

The SRE[2:0]=110 is the required drive setting to meet the timing.

FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 3.

Table 52. QuadSPI Quad 3.3V SDR 104MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK	SCK clock frequency [1, 2]	—	—	104	MHz	—	—
tCL_SCK	SCK clock low time [1, 2, 3]	4.327	—	—	ns	—	—
tCH_SCK	SCK clock high time [1, 2, 3]	4.327	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK) [1]	-2.330	—	2.880	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK) [1, 4]	3.391 - n/fSCK	—	5.901 + m/fSCK	ns	—	—
tDVW	Input data valid window [2]	4,624	—	—	ns	—	—
tISU_SCK	Input setup time (w.r.t. SCK) [2]	2.152	—	—	ns	—	—
tIH_SCK	Input hold time (w.r.t. SCK) [2]	2.0	—	—	ns	—	—

1. Timing valid for maximum external load CL = 20pF, which is assumed to be a 10pF-15pF load at the end of a 50ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the selected RDSON of the I/O pad output driver.
2. Input timing assumes maximum input signal transition of 1ns (20%/80%).
3. Clock measurements done with respect to VDD_IO_QSPI/2 level.
4. Where m=TCSS and n=TCSH-1.

16.4.1.12 QuadSPI interfaces

The QuadSPI module supports 2 interfaces; QSPI A & QSPI B. These interfaces are not independent & the QSPI chapter of the reference manual should be consulted for their usage. The table below summarizes which specifications are supported on each interface.

Table 53. QuadSPI interfaces

Specification / Interface	3.3V Quad	1.8V Quad	1.8V Octal	1.8V Hyperflash
QSPI A	n/a	SDR 100/133MHz DDR 66MHz	SDR 100/133MHz DDR 100/133/166/200 MHz	DDR 100/133/166 MHz
QSPI B	SDR 104MHz DDR 66MHz	SDR 100/133MHz DDR 66MHz	SDR 100/133MHz DDR 100/133MHz	DDR 100/133MHz

16.4.1.13 QuadSPI configurations

Table 54. QuadSPI configurations

-	DDR-200MHz	DDR-133MHz	SDR-133MHz	SDR-104MHz	DDR-66MHz
DQS mode	External DQS Edge Aligned	External DQS Edge Aligned	Internal pad loopback	Internal pad loopback	Internal pad loopback
Sampling mode	DDR	DDR	SDR	SDR	DDR
DLL Mode	DLL Enable	DLL Enable	DLL Bypass	DLL Bypass	DLL Enable
Data Learning	No	No	No	No	Yes
IO Voltage	1.8V	1.8V	1.8V	3.3V	1.8V/3.3V
Frequency	166/200 MHz	100/133 MHz	100/133 MHz	104 MHz	66 MHz
FLSHCR[TDH]	1	1	0	0	1
FLSHCR[TCSH]	3	3	3	3	3
FLSHCR[TCSS]	3	3	3	3	3
MCR[DLPEN]	0	0	0	0	1
DLLCR[DLLEN]	1	1	0	0	1
DLLCR[FREQEN]	1	0	0	0	0
DLLCR[DLL_REFCNTR]	2	2	NA	NA	2
DLLCR[DLLRES]	8	8	NA	NA	8
DLLCR[SLV_FINE_OFFSET]	0	0	0	0	0
DLLCR[SLV_DLY_OFFSET]	0	0	0	0	3

Table continues on the next page...

Table 54. QuadSPI configurations (continued)

-	DDR-200MHz	DDR-133MHz	SDR-133MHz	SDR-104MHz	DDR-66MHz
DLLCR[SLV_DLY_COARSE]	NA	NA	0	0	0
DLLCR[SLAVE_AUTO_UPDT]	1	1	0	0	1
DLLCR[SLV_EN]	1	1	1	1	1
DLLCR[SLV_DLL_BYPASS]	0	0	1	1	0
DLLCR[SLV_UPD]	1	1	1	1	1
SMPR[DLLFSMPF]	4	4	0	0	NA
SMPR[FSDLY]	0	0	0	0	1
SMPR[FSPHS]	NA	NA	1	1	NA

16.4.1.14 QuadSPI timing diagrams

The sections shows the QuadSPI timing diagrams for all modes supported by the device. All data is based on a negative edge data launch from the device.

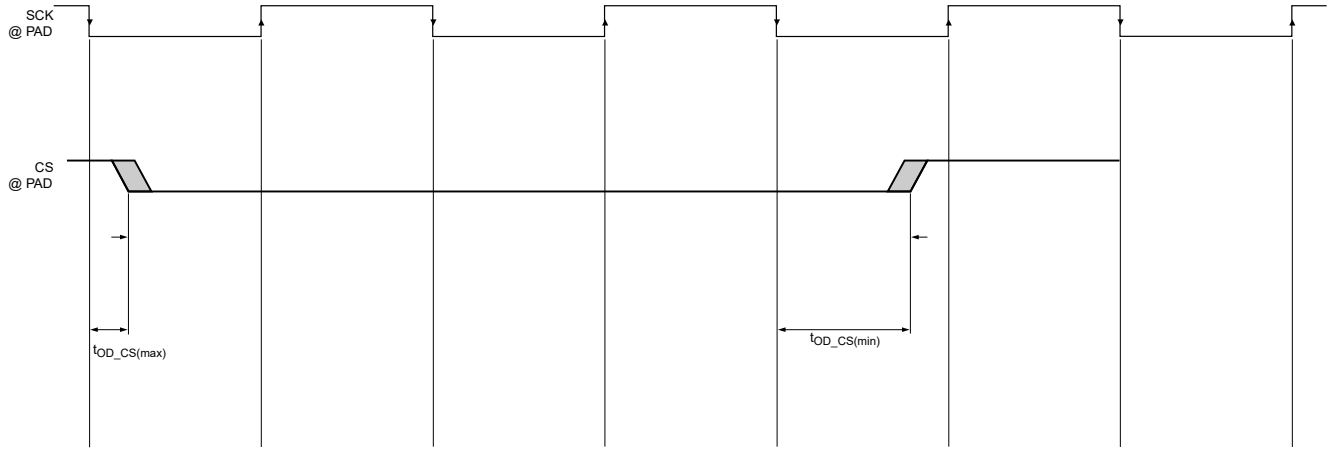


Figure 55. CS output timing

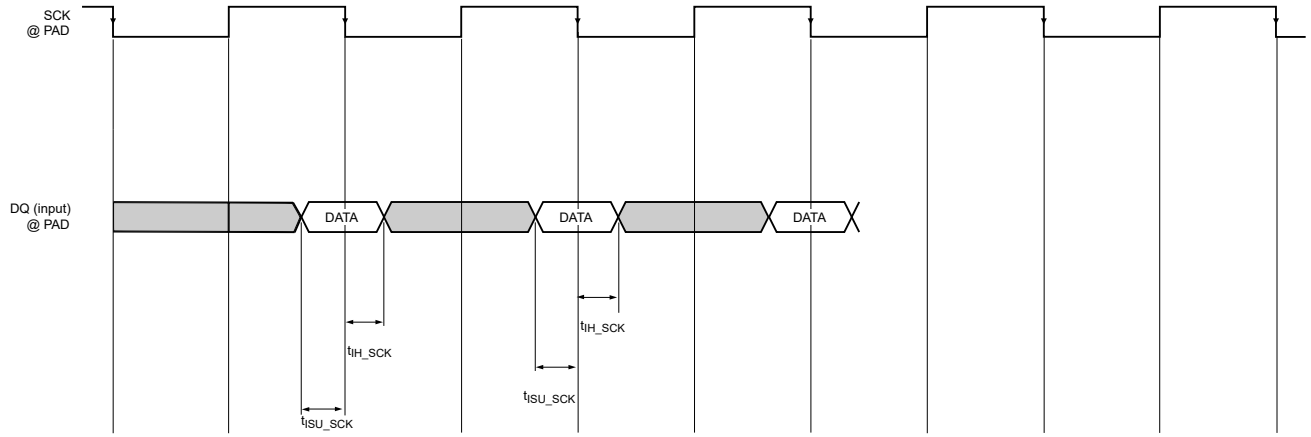


Figure 56. SDR input timing

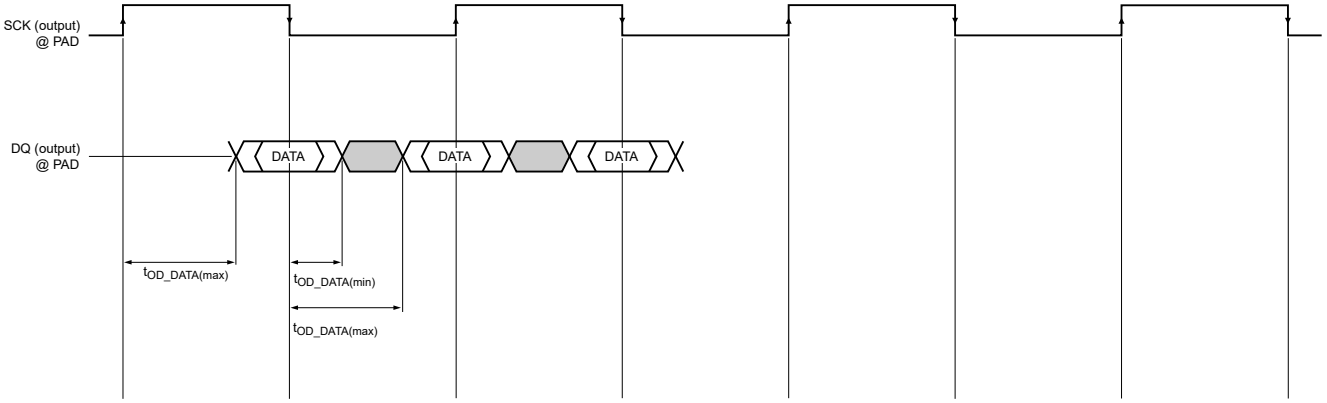


Figure 57. DDR output timing

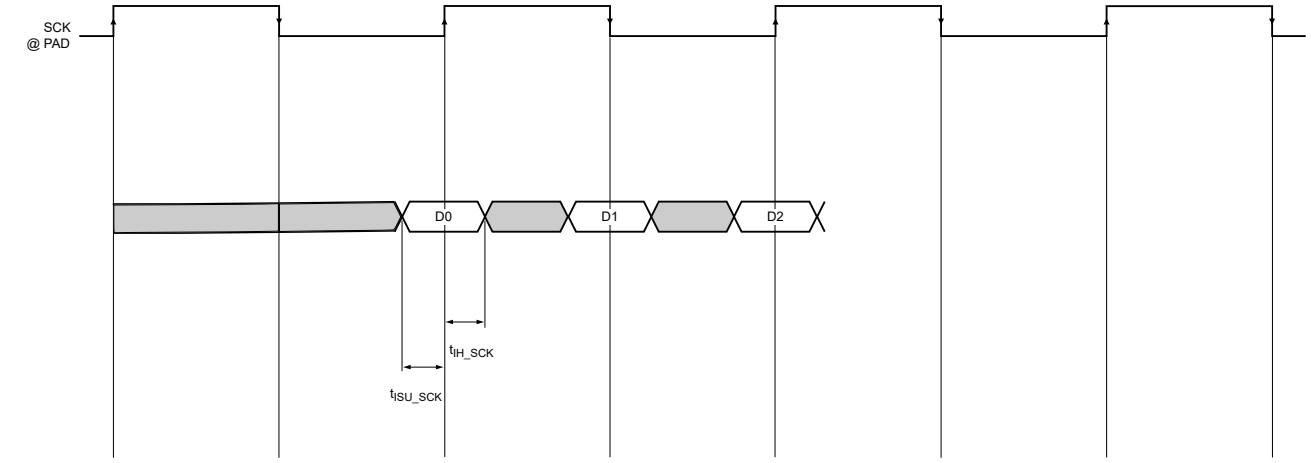


Figure 58. DDR with internal pad loopback input timing

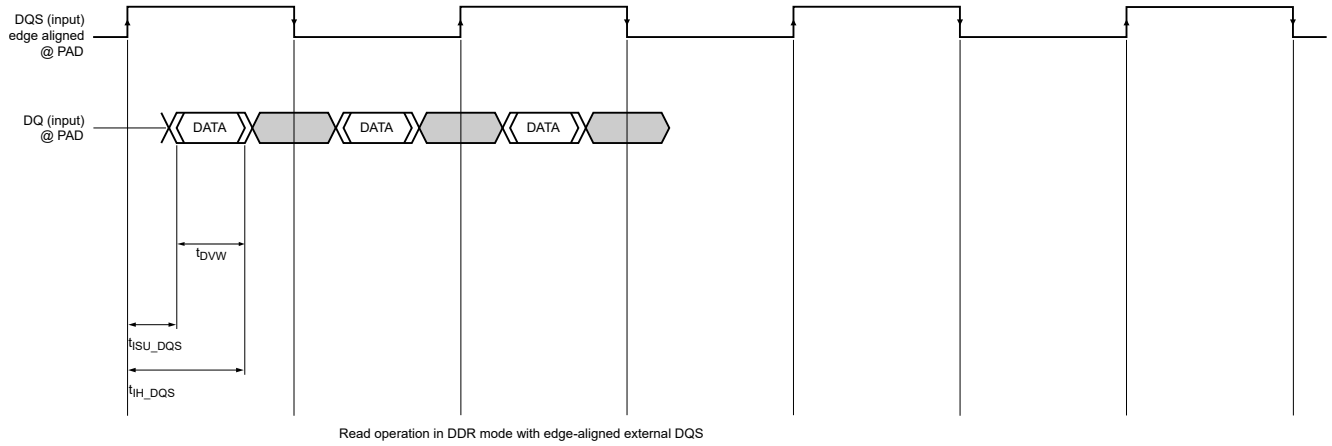


Figure 59. DDR edge-aligned DQS input timing

16.4.2 DDR

16.4.2.1 DDR

The chip supports the following memory types:

1. LPDDR4 SDRAM compliant to JEDEC209-4A LPDDR4 JEDEC standard release November, 2015

2. DDR3L SDRAM compliant to JESD79-3-1A DDR3L JEDEC standard release July, 2010.

DDR operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the chip's Hardware Design Guide Document.

LPDDR4 routing constraints are documented in the chip's Hardware Design Guidelines Document.

16.4.2.2 DDR Common DC Input

The specifications given in the table below represent the common DC input conditions for all DDR interface modes. Unless otherwise specified, all input specifications (both common and DDR standard specific) are measured at the host PHY input pins. Subsequent sections list input parameters for the specific memory interface standards.

Table 55. DDR Common DC Input

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IIZ-VREF	VREF input leakage current [1]	-50	—	50	uA	—	—
IIZ-BP	Input leakage current [2, 3, 4]	-50	—	50	uA	—	—
VIH-DC_BPDAT	Input high voltage threshold	VREF+0.085	—	—	V	—	—
VIL-DC_BPDAT	Input low voltage threshold	—	—	vref - 0.085	V	—	—

1. Leakage is valid for Vref over the range 0 <= VIN <= VDD_IO_DDR0, with Vref input function enabled. All pins not under test = VDD_IO_DDR0.
2. Leakage current is measured when the pin is configured to a high-impedance state with all on-die termination disabled. Leakage is valid for any input except for Vref over the range:0 <= VIN <= VDD_IO_DDR0. All pins not under test = VSS or VDD_IO_DDR0.

3. In DQS, PAD leakage would be twice the maximum DDR0_D_n leakage, as that have two attenuators.
4. Receiver attenuator leakage path can be disabled during test in certain configurations to reduce PAD leakage to maximum of 10uA. Note: The customer must keep the DDR0_D_n within VDD level in that case.

16.4.2.3 DDR Common DC Output

Table 56. DDR Common DC Output

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
ROnPu	Output driver pull-up impedance: DQ, DQS outputs [1]	—	120,60,40	—	Ohm	—	—
ROnPd	Output driver pull-down impedance: DQ, DQS outputs [1]	—	120,60,40	—	Ohm	—	—
ROnPu	Output driver pull-up impedance: address, command [1]	—	120,60,40	—	Ohm	—	—
ROnPd	Output driver pull-down impedance: address, command [1]	—	120,60,40	—	Ohm	—	—
ROnPu	Output driver pull-up impedance: DDR0_RESET_B, CLK outputs [2]	—	18-28	—	Ohm	—	—
ROnPd	Output driver pull-down impedance: DDR0_RESET_B, CLK outputs [2]	—	18-28	—	Ohm	—	—

1. Calibrated at VDD_IO_DDR0 / 2.
2. For the DDR0_RESET_B pin, the driver is in maximum strength and impedance value is process dependent.

NOTE: Refer to IBIS model for the complete IV curve characteristics.

16.4.2.4 DDR3L Output Timing

Table 57. DDR3L Output Timing

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tCK(avg)	Average clock period [1, 2]	—	1.25	—	ns	—	—
tOS(Vref)	Command and address setup time to CK (to Vref levels) [1, 2]	350	—	—	ps	—	—
tOH(Vref)	Command and address hold time	350	—	—	ps	—	—

Table continues on the next page...

Table 57. DDR3L Output Timing (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	to CK (to Vref levels) [1, 2]						
tDOeye	Output data eye [1, 2]	0.6	—	—	UI	—	—

1. All measurements are in refernce to the Vref level.
2. Measurements were done with signals terminated with a 50ohm resistor terminated to VDD_IO_DDR0/2, Phy output is calibrated to a drive strength of 40ohms. Slew rate AtxSlewRate was set to 0x3FF (PreDrvMode=3, PreN=F,PreP=F); TxSlewRate was set 0x3FF (PreDrvMode=3, PreN=F,PreP=F).

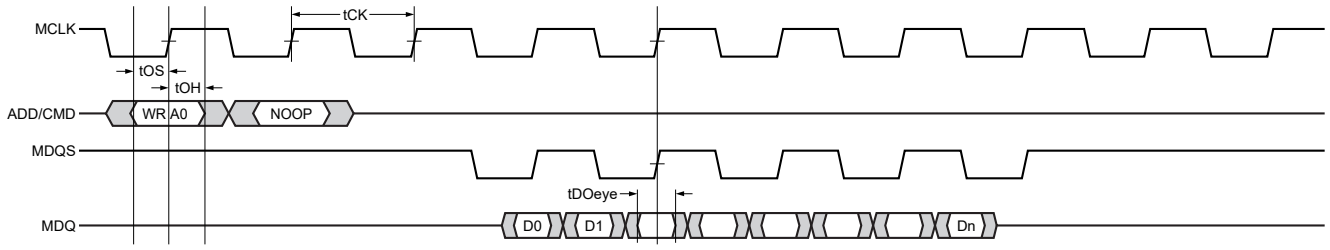


Figure 60. DDR3L Output Timing

16.4.2.5 LPDDR4 DC Input

Table 58. LPDDR4 DC Input

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Vref	Internal reference voltage [1, 2]	—	Variable	—	V	—	—

1. Because termination at the DRAMs is configurable, there is no fixed setting. The Vref value is dependent on driver impedance Ron and system effective ODT impedance Rtt.
2. Externally supplied Vref is not recommended. Internal Vref generation through local Vref generation at each receiver is preferred.

16.4.2.6 LPDDR4 Output

Table 59. LPDDR4 Output

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tCK(avg)	Average clock period [1]	—	0.625	—	ns	—	—
tDOeye	Output data eye [1, 2, 3]	0.55	—	—	UI	—	—
tCAOeye	CA output data eye [1, 4]	0.62	—	—	UI	UI=625ps	—

1. Measurements were done with signals terminated with a 50ohm resistor terminated to VSS, Phy output is calibrated to a drive strength of 40ohms. Slew rate AtxSlewRate was set to 0x1FF (PreDrvMode=1, PreN=F,PreP=F); TxSlewRate was set 0x1FF (PreDrvMode=1, PreN=F, PreP=F).

2. tDOeye is trained to be shifted min 200 ps from DQS edge (tDQS2DQ learning).
3. Tx DQS to MCLK edges are trained to be aligned.
4. Addr/Cmd is centered aligned by training.

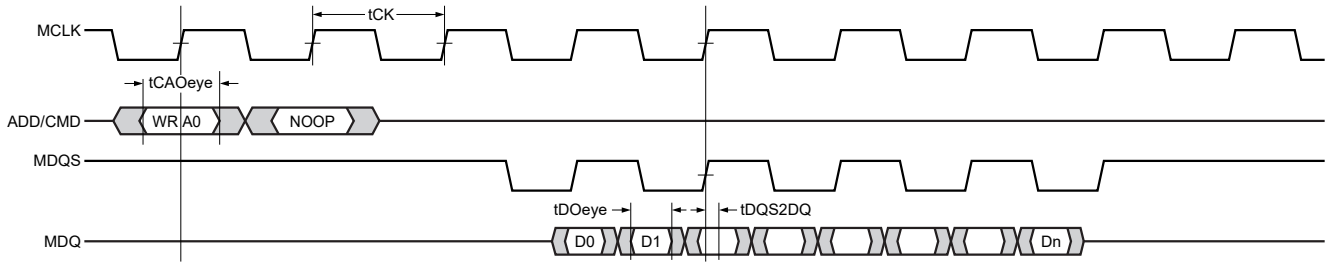


Figure 61. LPDDR4 Output Timing

16.4.3 uSDHC

16.4.3.1 uSDHC DDR-52MHz

The SRE[2:0]=101 is required drive setting to meet the timing.

Table 60. uSDHC DDR-52MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fpp	Clock frequency (eMMC4.4/4.41 DDR) [1]	—	—	52	MHz	—	SD1
fpp	Clock frequency (SD3.0 DDR) [1]	—	—	50	MHz	—	SD1
tWL	Clock low time	8.8	—	—	ns	—	—
tWH	Clock high time	8.8	—	—	ns	—	—
tTLH	Clock rise time [1, 2]	—	—	0.8	ns	—	—
tTHL	Clock fall time [1, 2]	—	—	0.8	ns	—	—
tOD	SHDC output delay (output valid) [1]	2.7	—	5.6	ns	SDHC_CLK to SDHC_DAT	SD2
tOD	SDHC output delay (output valid) [1]	-5.6	—	2.6	ns	SDHC_CLK to SDHC_CMD	SD6 (See SDR-52 MHz figure)
tISU	SDHC Input setup time [3]	1.6	—	—	ns	SDHC_DAT to SDHC_CLK	SD3
tISU	SDHC Input setup time [3]	4.8	—	—	ns	SDHC_CMD to SDHC_CLK	SD7 (See SDR-52 MHz figure)

Table continues on the next page...

Table 60. uSDHC DDR-52MHz (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tIH	SDHC Input hold time [3]	1.5	—	—	ns	SDHC_CLK to SDHC_DAT	SD4
tIH	SDHC Input hold time [3]	1.5	—	—	ns	SDHC_CLK to SDHC_CMD	SD8 (See SDR-52 MHz figure)

1. Output timing valid for maximum external load CL = 25pF, which is assumed to be a 10pF load at the end of a 50Ohm, un-terminated, 5 inch microstrip trace on standard FR4 (1.5pF/inch), (25pF total with margin).
2. The SDHC_CLK rise/fall time specification applies to the input clock transition required in order to meet the output delay specifications. SDHC_CLK output transition time is dependent on output load and GPIO pad drive strength. See the GPIO pad specifications for detail.
3. Input timing assumes an input signal slew rate of 3ns (20%/80%).

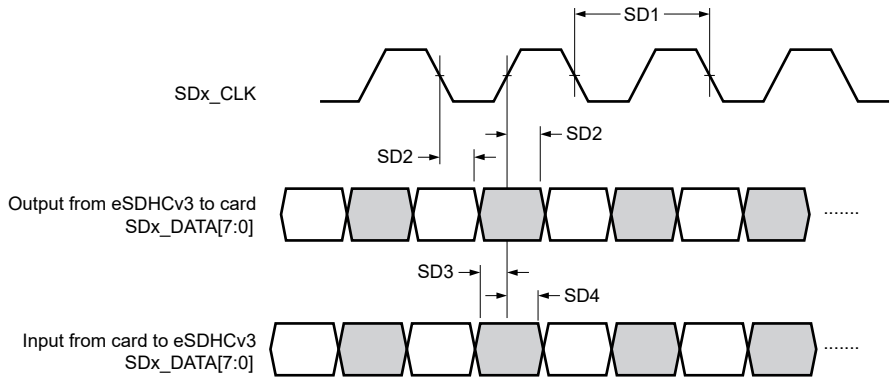


Figure 62. SD/eMMC4.4/4.41 DDR50 Mode Interface Timing

16.4.3.2 uSDHC SDR-52MHz

The SRE[2:0]=101 is required drive setting to meet the timing.

Table 61. uSDHC SDR-52MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fpp	Clock frequency (low speed) [1, 2]	—	—	400	kHz	—	SD1
fpp	Clock frequency (SD/SDIO full speed/ high speed [2, 3]	—	—	25/50	MHz	—	SD1
fpp	Clock frequency (mmc full speed/high speed [2, 4]	—	—	20/52	MHz	—	SD1

Table continues on the next page...

Table 61. uSDHC SDR-52MHz (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fOD	Clock frequency (identification mode) [2]	100	—	400	kHz	—	SD1
tWL	Clock low time	8.8	—	—	ns	—	SD2
tWH	Clock high time	8.8	—	—	ns	—	SD3
tTLH	Clock rise time [2, 5]	—	—	0.8	ns	—	SD4
tTHL	Clock fall time [2, 5]	—	—	0.8	ns	—	SD5
tOD	SHDC output delay (output valid) [2]	-5.6	—	2.6	ns	SDHC_CLK to SDHC_CMD / SDHC_DAT	SD6
tISU	SDHC Input setup time [6]	4.8	—	—	ns	SDHC_CMD / SDHC_DAT to SDHC_CLK	SD7
tIH	SDHC Input hold time [6]	1.5	—	—	ns	SDHC_CLK to SDHC_CMD / SDHC_DAT	SD8

1. In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7V to 3.6V.
2. Output timing valid for maximum external load CL = 25pF, which is assumed to be a 10pF load at the end of a 50Ohm, un-terminated, 5 inch microstrip trace on standard FR4 (1.5pF/inch), (25pF total with margin).
3. In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.
4. In normal (full) speed mode for MMC card, clock frequency can be any value between 0–20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.
5. The SDHC_CLK rise/fall time specification applies to the input clock transition required in order to meet the output delay specifications. SDHC_CLK output transition time is dependent on output load and GPIO pad drive strength. See the GPIO pad specifications for detail.
6. Input timing assumes an input signal slew rate of 3ns (20%/80%).

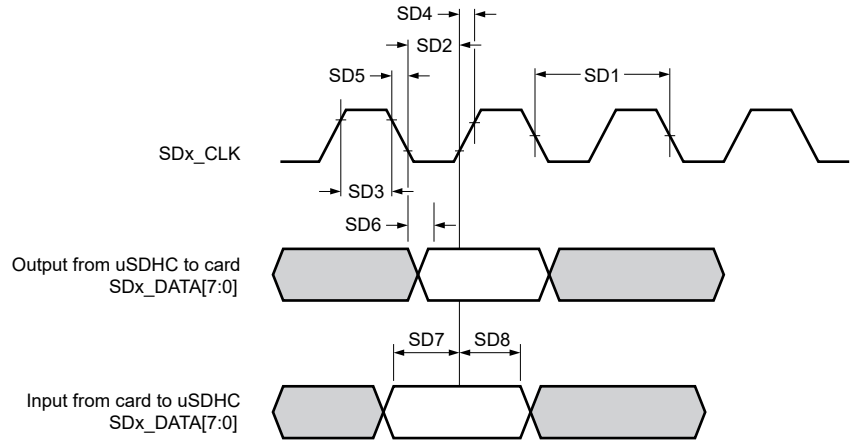


Figure 63. SD/eMMC4.3 High Speed Mode Interface Timing

16.4.3.3 uSDHC SDR-100MHz

The SRE[2:0]=101 is required drive setting to meet the timing.

Table 62. uSDHC SDR-100MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tCLK	Clock frequency [1]	—	—	100	MHz	—	SD1
tCL	Clock low time	4.5	—	—	ns	—	SD2
tCH	Clock high time	4.5	—	—	ns	—	SD3
tTLH	Clock rise time [1, 2]	—	—	0.8	ns	—	—
tTHL	Clock fall time [1, 2]	—	—	0.8	ns	—	—
tOD	uSDHC output delay [1]	-3.5	—	1.3	ns	SDHC_CLK to SDHC_CMD / SDHC_DAT	SD4
tISU	uSDHC input setup time [3]	1.6	—	—	ns	SDHC_CMD / SDHC_DAT to SDHC_CLK	SD6
tIH	uSDHC input hold time [3]	1.5	—	—	ns	SDHC_CLK to SDHC_CMD / SDHC_DAT	SD7

1. Output timing valid for maximum external load CL = 15pF, which is assumed to be a 10pF load at the end of a 50Ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the RDSON of the I/O pad output driver.
2. The SDHC_CLK rise/fall time specification applies to the input clock transition required in order to meet the output delay specifications. SDHC_CLK output transition time is dependent on output load and GPIO pad drive strength. See the GPIO pad specifications for detail.
3. Input timing assumes an input signal slew rate of 1ns (20%/80%).

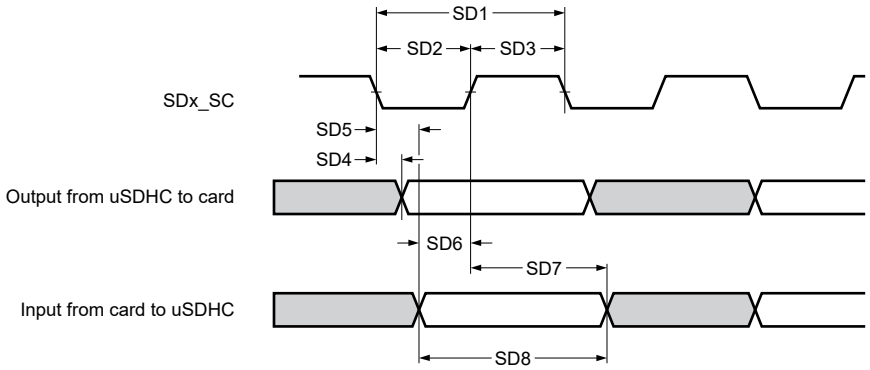


Figure 64. SDR100 Mode Interface Timing

16.4.3.4 uSDHC SDR-HS200

The SRE[2:0]=000 is required drive setting to meet the timing.

Table 63. uSDHC SDR-HS200

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tCLK	Clock frequency [1]	—	—	200	MHz	—	SD1
tCL	Clock low time	2.2	—	—	ns	—	SD2

Table continues on the next page...

Table 63. uSDHC SDR-HS200 (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tCH	Clock high time	2.2	—	—	ns	—	SD3
tTLH	Clock rise time [1, 2]	—	—	0.8	ns	—	—
tTHL	Clock fall time [1, 2]	—	—	0.8	ns	—	—
tOD	uSDHC output delay [1]	-1.2	—	0.6	ns	SDHC_CLK to SDHC_CMD / SDHC_DAT	SD4
tODW	Input data window [3]	2.6	—	—	ns	—	SD8

1. Output timing valid for maximum external load CL = 15pF, which is assumed to be a 10pF load at the end of a 50Ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the RDSON of the the I/O pad output driver.
2. The SDHC_CLK rise/fall time specification applies to the input clock transition required in order to meet the output delay specifications. SDHC_CLK output transition time is dependent on output load and GPIO pad drive strength. See the GPIO pad specifications for detail.
3. Input timing assumes an input signal slew rate of 1ns (20%/80%).

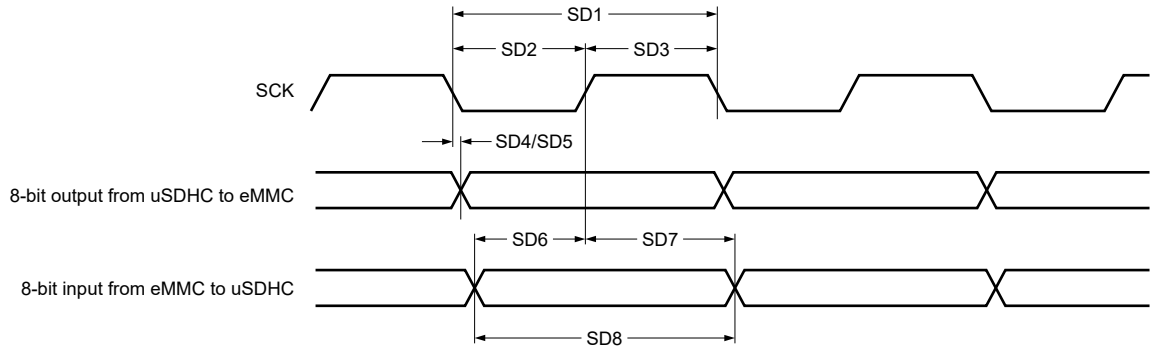


Figure 65. HS200 Mode Interface Timing

16.4.3.5 uSDHC DDR-HS400

The SRE[2:0]=000 is required drive setting to meet the timing.

Table 64. uSDHC DDR-HS400

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tPP	Clock frequency [1]	133	—	200	MHz	—	SD1
tCL	Clock low time	2.2	—	—	ns	—	SD2
tCH	Clock high time	2.2	—	—	ns	—	SD3
tTLH	Clock rise time [1, 2]	—	—	0.8	ns	—	—
tTHL	Clock fall time [1, 2]	—	—	0.8	ns	—	—
tOD	Output delay [1, 3, 4]	0.45	—	1.75	ns	SDHC_CLK to SDHC_DAT	—

Table continues on the next page...

Table 64. uSDHC DDR-HS400 (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tISU	uSDHC input setup time [3, 5]	-0.15	—	—	ns	SDHC_CMD / SDHC_DAT to SDHC_CLK	—
tIH	uSDHC input hold time [3, 5]	1.75	—	—	ns	SDHC_CLK to SDHC_CMD / SDHC_DAT	—

1. Output timing valid for maximum external load CL = 15pF, which is assumed to be a 10pF load at the end of a 50Ohm, un-terminated, 2 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the RDSON of the I/O pad output driver.
2. The SDHC_CLK rise/fall time specification applies to the input clock transition required in order to meet the output delay specifications. SDHC_CLK output transition time is dependent on output load and GPIO pad drive strength. See the GPIO pad specifications for detail.
3. Board skew margin between CLK and DATA/CMD is considered as +/-50 ps in calculations
4. The CMD output timing for HS400 mode is the same as CMD output timing for HS200 mode.
5. Input timing assumes an input signal slew rate of 1ns (20%/80%).

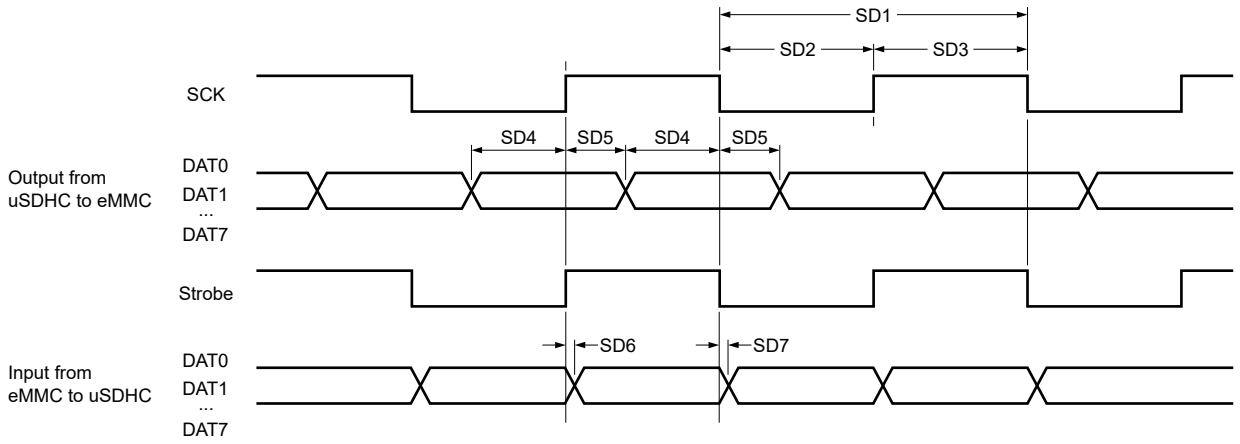


Figure 66. HS400 Mode Interface Timing

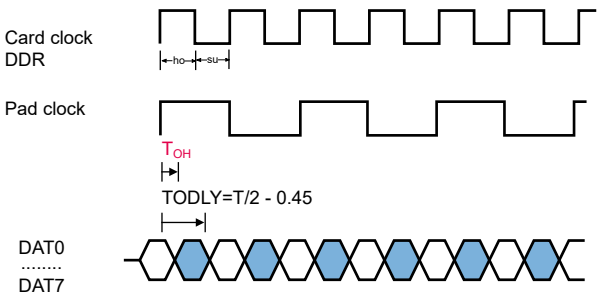


Figure 67. HS400 mode uSDHC output timing

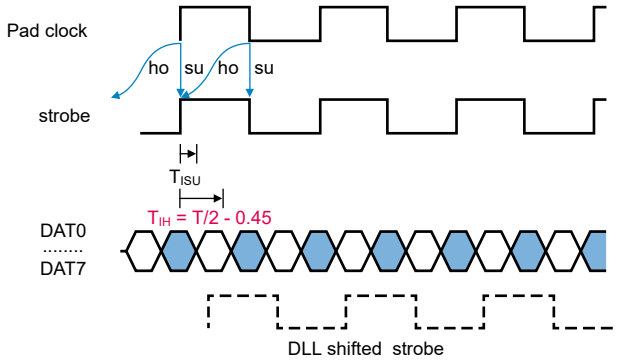


Figure 68. HS400 mode uSDHC input timing

16.5 Debug modules

16.5.1 JTAG Boundary Scan

The following table gives the JTAG specifications in boundary scan mode.

Table 65. JTAG Boundary Scan

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tJCYC	TCK cycle time [1, 2, 3]	100	—	—	ns	—	1
tJDC	TCK clock pulse width [2, 3]	45	—	55	%	—	2
tTCKRISE	TCK rise/fall time [2, 4]	—	—	3	ns	—	3
tTMSS, tTDIS	TMS, TDI data setup time [2, 5]	5	—	—	ns	—	4
tTMSH, tTDIH	TMS, TDI data hold time [2, 5]	5	—	—	ns	—	5
tTDOV	TCK low to TDO data valid [2, 6, 7]	—	—	17.5	ns	SRE[2:0] = 101	6
tTDOI	TCK low to TDO data invalid [2, 6]	0	—	—	ns	SRE[2:0] = 101	7
tTDOHZ	TCK low to TDO high impedance [2, 6]	—	—	17.5	ns	SRE[2:0] = 101	8
tJCMPPW	JCOMP assertion time [2]	100	—	—	ns	—	9
tJCMPS	JCOMP setup time to TCK high [2]	40	—	—	ns	—	10
tBSDV	TCK falling edge to output valid [2, 6, 8]	—	—	600	ns	SRE[2:0] = 101	11
tBSDVZ	TCK falling edge to output valid out of high impedance [2, 6]	—	—	600	ns	SRE[2:0] = 101	12

Table continues on the next page...

Table 65. JTAG Boundary Scan (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tBSDVHZ	TCK falling edge to output high impedance [2, 6]	—	—	600	ns	SRE[2:0] = 101	13
tBSDST	Boundary scan input valid to TCK rising edge [2]	15	—	—	ns	—	14
tBSDHT	TCK rising edge to boundary scan input invalid [2]	15	—	—	ns	—	15

1. JTAG port interface speed only. Does not apply to boundary scan timing.
2. These specifications apply to JTAG boundary scan mode only.
3. TCK pin must have external pull down.
4. The TCK rise/fall time specification applies to the input clock transition required in order to meet the TDO output specifications that are relative to TCK.
5. Input timing assumes an input signal slew rate of 3ns (20%/80%).
6. Output timing valid for maximum external load CL = 25pF, which is assumed to be a 10pF load at the end of a 50Ohm, un-terminated, 5 inch microstrip trace on standard FR4 (1.5pF/inch), (25pF total with margin). For best signal integrity, the series resistance of the transmission line should be matched closely to the selected RDSON of the I/O pad output driver.
7. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
8. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

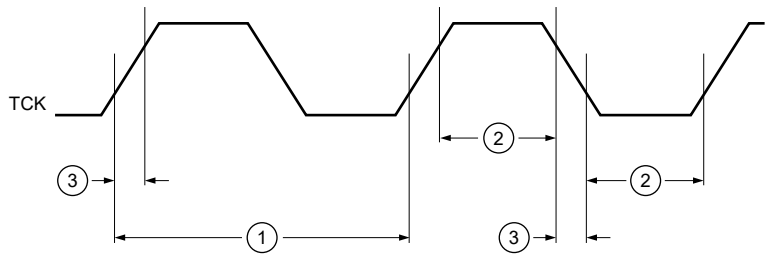


Figure 69. JTAG TCK Input Timing

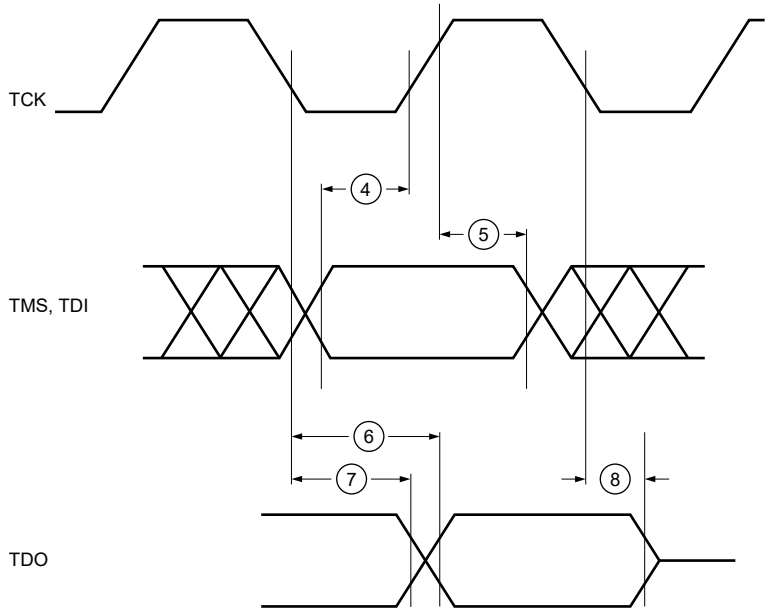


Figure 70. JTAG Test Access Port Timing

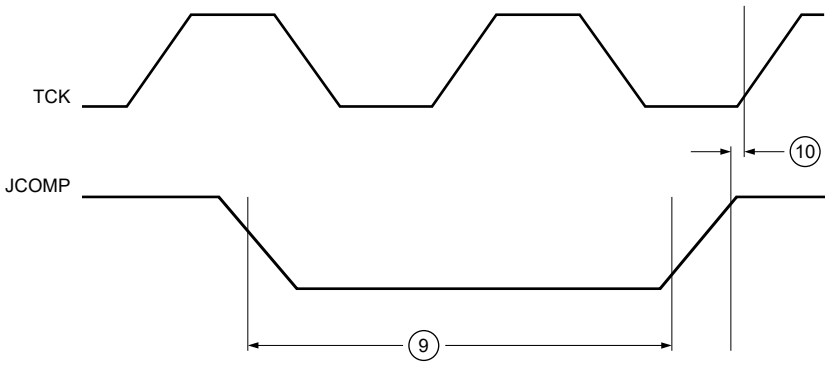


Figure 71. JCOMP Timing

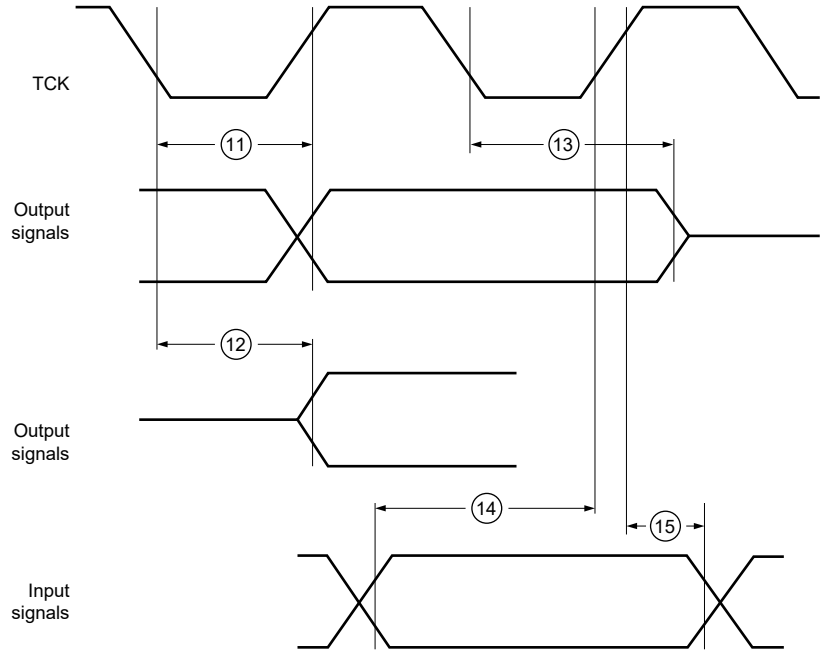


Figure 72. Boundary Scan Timing

16.5.2 JTAG Debug Interface Timing

The following table gives the JTAG specifications in debug interface mode.

Table 66. JTAG Debug Interface Timing

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tTCYC	Absolute minimum TCK cycle time (TDO sampled on posedge of TCK) [1, 2]	50	—	—	ns	—	—
tTCYC	Absolute minimum TCK cycle time (TDO sampled on negedge of TCK) [1, 2]	25	—	—	ns	—	—
tJDC	TCK clock pulse width	45	—	55	%	—	—
tNTDIS	TDI data setup time [3]	5	—	—	ns	—	11
tNTDIH	TDI data hold time [3]	5	—	—	ns	—	12
tNTMSS	TMS data setup time	5	—	—	ns	—	13
tNTMSH	TMS data hold time	5	—	—	ns	—	14

Table continues on the next page...

Table 66. JTAG Debug Interface Timing (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tNTDOD	TDO propagation delay from falling edge of TCK [4, 5]	—	—	17.5	ns	—	15
tNTDOH	TDO hold time with respect to falling edge of TCK [4]	1	—	—	ns	—	16
tTDOHZ	TCK low to TDO high impedance [4]	—	—	17.5	ns	—	—

1. Maximum frequency for TCK is limited to 6MHz during BOOTROM startup of the device, when the system clock is the trimmed 48MHz FIRC.
2. TCK pin must have external pull down.
3. Input timing assumes an input signal slew rate of 3ns (20%/80%).
4. Output timing valid for maximum external load CL = 25pF, which is assumed to be a 10pF load at the end of a 50Ohm, un-terminated, 5 inch microstrip trace on standard FR4 (1.5pF/inch), (25pF total with margin). For best signal integrity, the series resistance of the transmission line should be matched closely to the RDSON of the I/O pad output driver.
5. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.

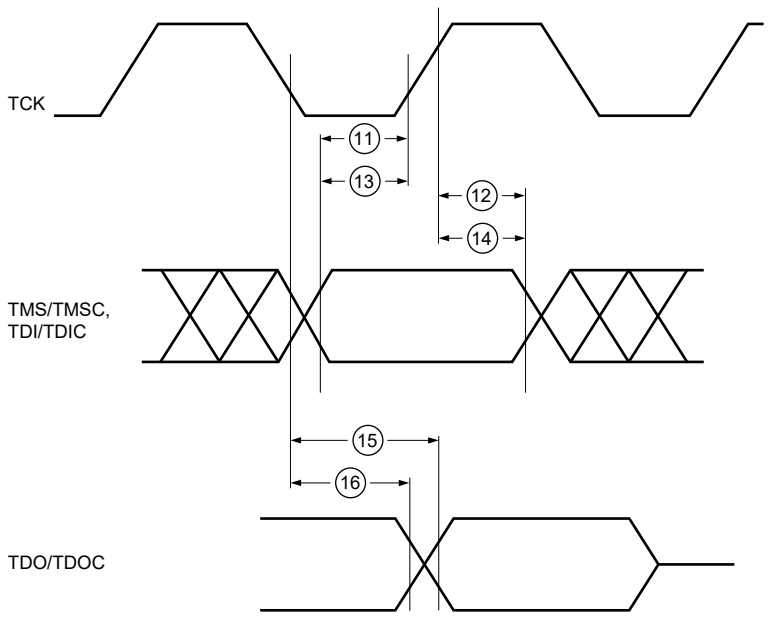


Figure 73. JTAG debug Interface Timing

17 Pinouts

For package pinouts and signal descriptions, refer to the Reference Manual.

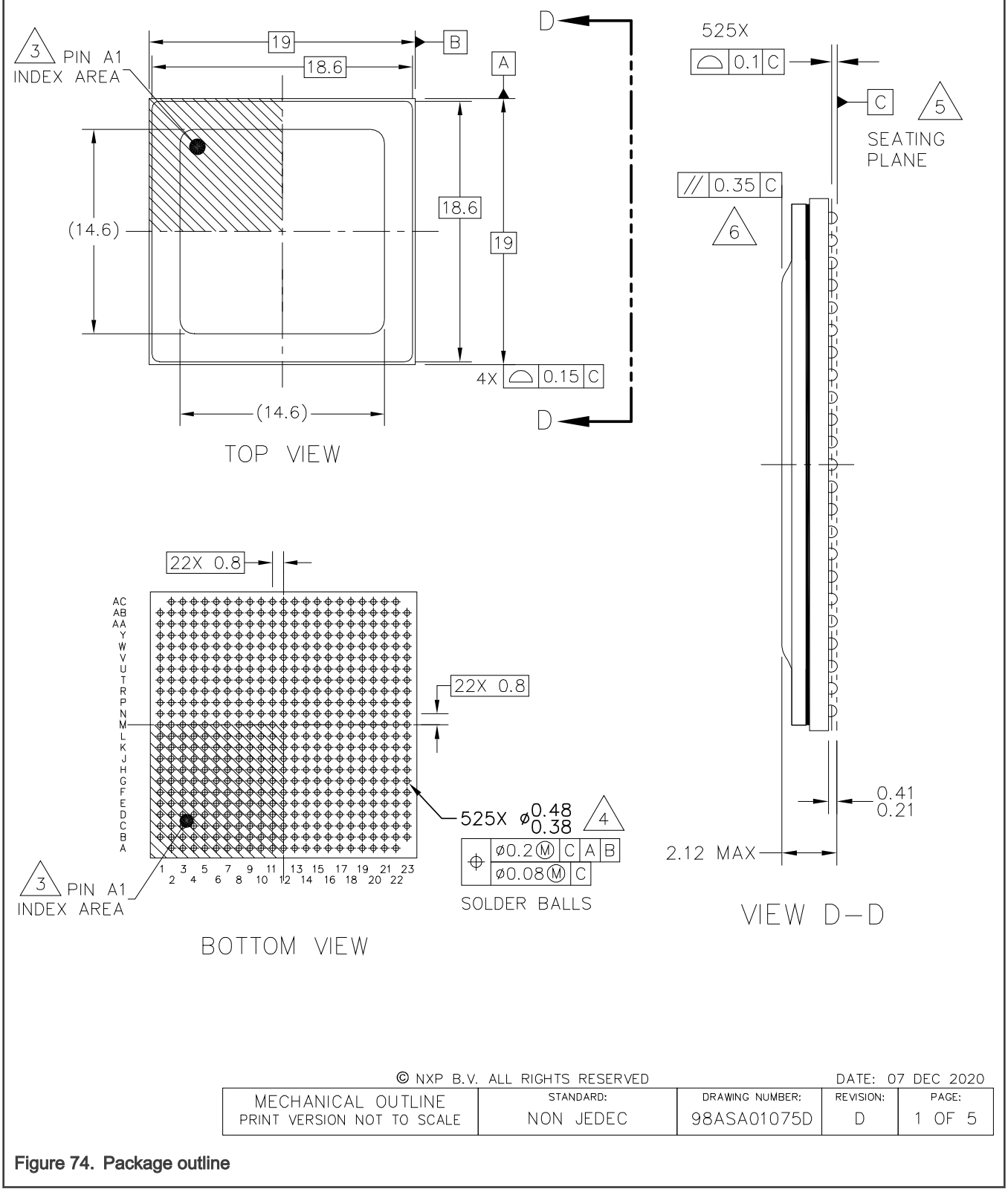
18 Packaging

The S32G2 is offered in the following package types.

If you want the drawing for this package	Then use this document number
525-ball FCBGA	98ASA01075D

NOTE

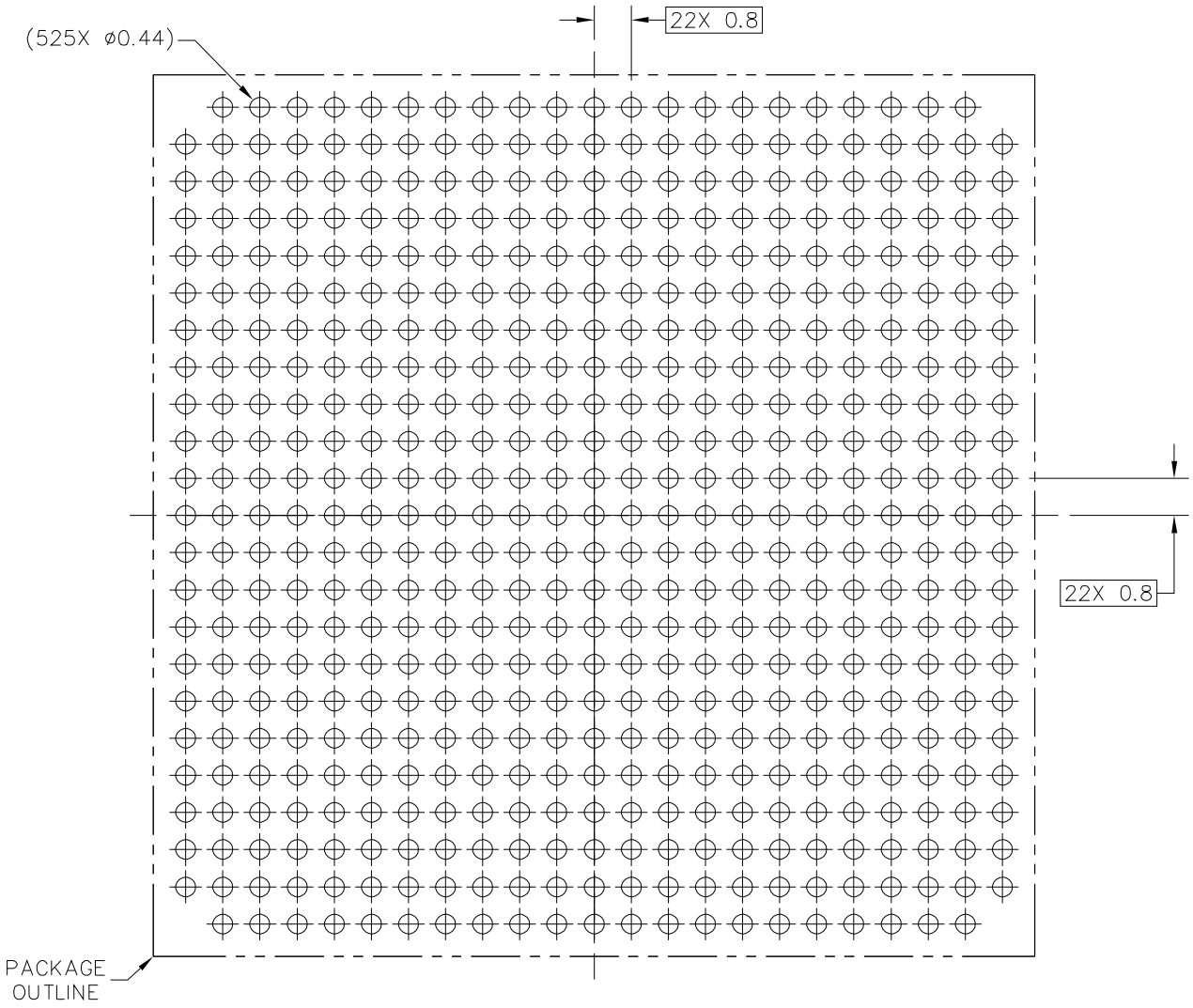
To find a package drawing, go to http://www.nxp.com and perform a keyword search for the drawing's document number or see below figures.



DATE: 07 DEC 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01075D	REVISION: D	PAGE: 1 OF 5

Figure 74. Package outline



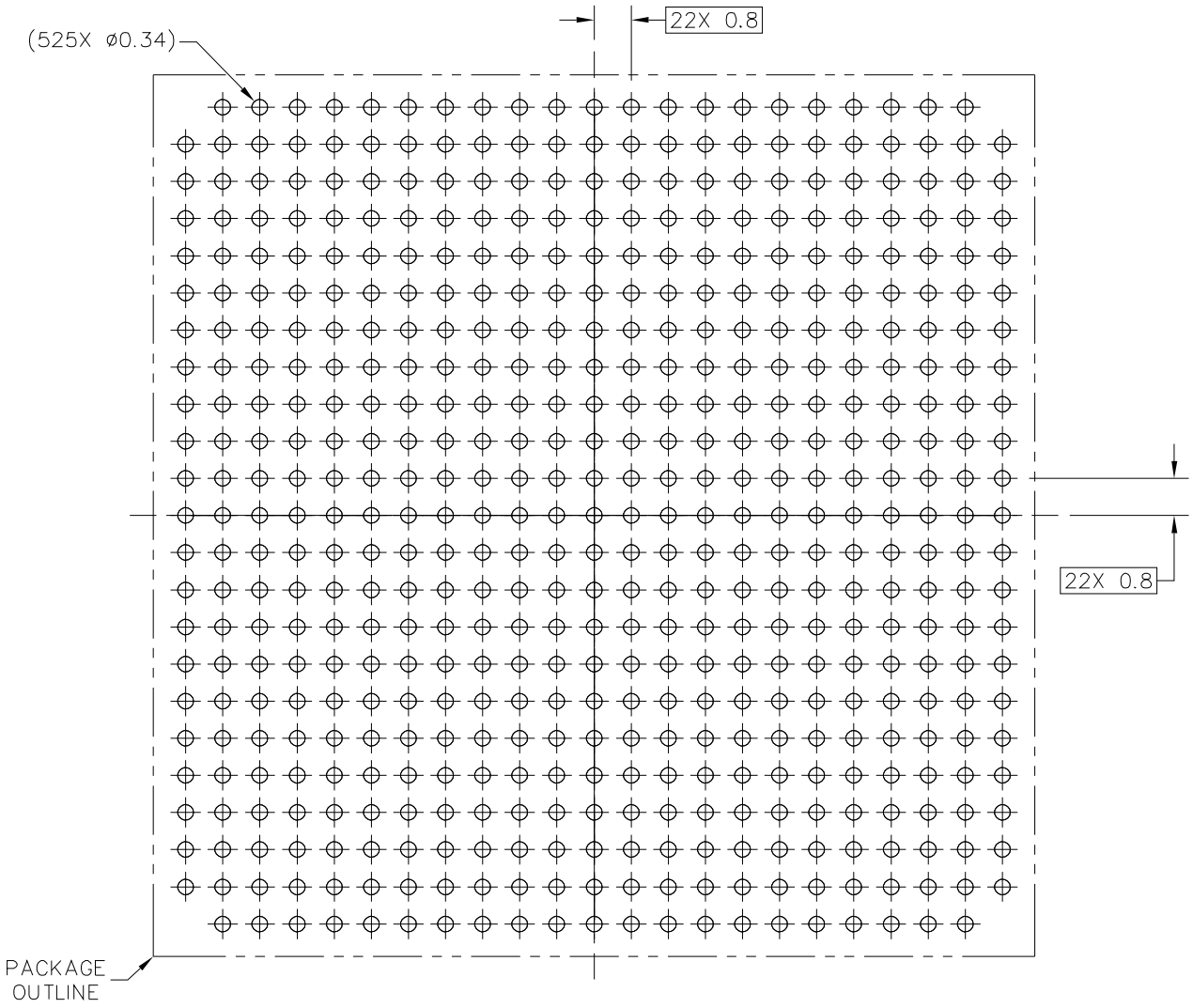
PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 07 DEC 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01075D	REVISION: D	PAGE: 2

Figure 75. Soldering footprint part 1 of 3



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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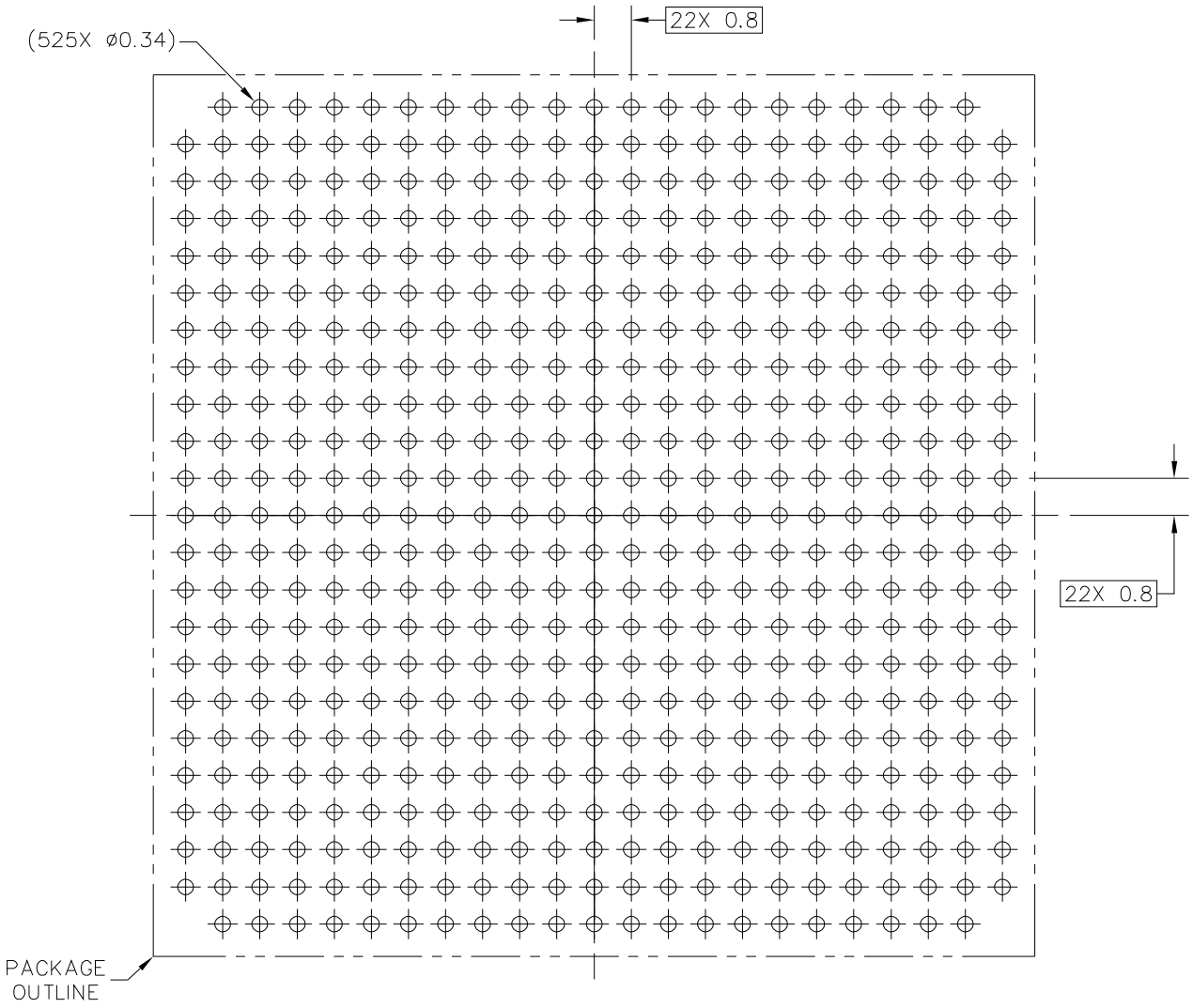
DATE: 07 DEC 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01075D	REVISION: D	PAGE: 3

Figure 76. Soldering footprint part 2 of 3



RECOMMENDED STENCIL THICKNESS 0.125MM

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 07 DEC 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01075D	REVISION: D	PAGE: 4

Figure 77. Soldering footprint part 3 of 3

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
7. LID OVERHANG ON SUBSTRATE NOT ALLOWED.

DATE: 07 DEC 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01075D	REVISION: D	PAGE: 5

Figure 78. Package outline notes

19 Revision history

The following table lists the changes in this document.

Rev 3, Apr 2021
• In section "Absolute Max Ratings", Symbol "IINJ_A" clarified footnote "Non-disturb of ADC channels during current injection...." for -40 Tj. • In section "Operating conditions", added a footnote to clarify voltage differential "The "voltage differential" refers to the difference between the lowest and highest voltages...". • In section "Total power specifications for 0.8V and 1.8V Analog Domains", for S32G254A Thermal Usecase is updated to 4.22 W to correct a typography error as it was in previous versions. • In section "Power Sequencing", figure "1.8V supply timing with respect to PMIC_VDD_OK during Standby Mode Exit" is updated to mention correct supply name "PMIC_VDD_OK". • In section "DFS", fDFS_CORE_CLK3 is deleted as this is used for BIST. • In section "PLL", fPLL_PER_PHI6 is deleted as this is used for BIST. • In section "PLL", updated this note "fPLL_DDR_PHI0 frequencies and data rate mentioned in this table are for LPDDR4. DDR3L frequencies and data rates are half of the LPDDR4." • In all QuadSPI sections added pharase "FLSHCR[TCSS] and FLSHCR[TCSH]should be set to 3" and moved the information to top of the table to be consistent with "QuadSPI configurations" section. • In section "QuadSPI interfaces" — Added 100 MHz to "1.8V Quad" column. — Added support for Hyperflash. • In section "QuadSPI Configurations" — Frequency row updated to include 100 MHz

Rev 3, Apr 2021
— A reserved bit is deleted. • In section "DDR Common DC Input", updated the description of "IIZ-BP" specification to make it applicable to all DDR pins. • In section "DDR3L Output Timing", updated the footnote to mention slew rate. • In section "DDR3L Output Timing" and "LPDDR4 Output", updated figures to remove symbols not in the corresponding tables.

Rev 2.1, Apr 2021
• In section "Operating Conditions", for Symbol "VDD_IO_STBY" condition updated to "Min 2.91V supported in low-power standby mode". • In section "Operating Conditions", for Symbol "VDD_STBY" and "VDD_IO_STBY" footnote updated to replace 3.0V to 2.91V, "A minimum of 2.91V is supported on the VDD_IO_STBY supply ....".

Rev 2, Apr 2021
• Updated section "Applications", "block diagram", "feature comparision" and ordering information figure. • In section "Absolute Max Ratings", Symbol "VDD_LV_PLL_DDR" is deleted as this redundant. • In section "Absolute Max Ratings", Symbol "VDD_DDR0" updated condition. • In section "Absolute Max Ratings", added specification "VDD_HV_PLL_DDR0". • In section "Absolute Max Ratings", specification "VXTAL" and "EXTAL" is added. • In section "Absolute Max Ratings", specification "VAD_INPUT" is added. • In section "Absolute Max Ratings", for Symbol "VIN" footnotes updated. • In section "Absolute Max Ratings", for Symbol "IINJ_D added a footnote "IINJ_D specifications are per pin for an...". • In section "Absolute Max Ratings", for Symbol "IINJ_A" Min changed from "-2" to "-1". • In section "Absolute Max Ratings", for Symbol "IINJ_A" Max changed from "2" to "1". • In section "Absolute Max Ratings", for Symbol "IINJ_A" footnote updated "Non-disturb of adjacent ADC channels dur..." and added footnote "Allowed for a cumulative duration of 50 hours operation....". • In section "Absolute Max Ratings", added overshoot/undershoot voltage specs and related figure. • In section "Absolute Max Ratings", footnotes updated to change min voltage for reliability. — Allowed 1.92V - 2.16V for 60 seconds cumulative over lifetime.... — Allowed 3.52V - 4.0V for 60 seconds cumulative over lifetime.... • In section "Operating Conditions", for Symbol "fSYS_A53" footnote updated "The stated maximum operating frequency m..." top remove down spread reference. • In section "Operating Conditions", specification "Ta" is added. • In section "Operating Conditions", DDR4 removed and DDR3L added. • In section "Operating Conditions", Symbol "VDD_HV_PLL_DDR" is updated to "VDD_HV_PLL_DDR0". • In section "Operating Conditions", Symbol "ðVDD_HV_PLL_DDR" is updated to "ðVDD_HV_PLL_DDR0".

Rev 2, Apr 2021
• In section "Operating conditions", for specification "VIN_18" min updated to "VSS - 0.3" and max updated to "VDD_IO* +0.3" • In section "Operating conditions", for specification "VIN_33" min updated to "VSS - 0.3" and max updated to "VDD_IO* +0.3 • In section "Operating Conditions", updated paragraph "The device hardware design guide summarizes..." • In section "Operating conditions", for specification "VIN_33" and "VIN_18" added these two footnotes: — Absolute minimum level for VIN signal is -0.3V. — Additional +0.3V are supported for DC signal. • In section "Operating Conditions", for Symbol "VRAMP_LV" with condition "Applies to 0.8V supplies" Max changed from "10" to "24". • In section "Operating Conditions", Symbol "VRAMP_HV" is splitted into two rows: — For 1.8V supplies and DDR I/O supplies Max changed from "10" to "24". — For 3.3V I/O supplies Max changed from "10" to "50".. • In section "Operating Conditions", for Symbol "IINJ_D" deleted footnote "GPIO electrical specifications and AC timing interface..." and added footnote "IINJ_D specifications are per pin for an unpowered condition...". • In section "Operating Conditions", for Symbol "IINJ_A" Min changed from "-1mA" to "-20uA". • In section "Operating Conditions", for Symbol "IINJ_A" Max changed from "1mA" to "20uA". • In section "Operating Conditions", for Symbol "IINJ_A" updated footnote "The SAR ADC electrical specifications are..." and deleted footnote "The specified injection current is allowed...". • In section "Clock frequency ranges", Symbol "fSDHC_CLK" condition updated from "SDHC_CLK - DDR HS200" to "SDHC_CLK - SDR HS200". • In section "Clock frequency ranges", for Symbol "fSDHC_CLK" with condition "SDHC_CLK - DDR HS400" Min value changed to "133". • In section "Clock frequency ranges", for Symbol "fSDHC_CLK" with condition "SDHC_CLK - DDR HS400" Max changed from "400" to "200". • In section "Thermal Characteristics" JESD51-9, 2s2p value updated to 15.5 C/W. • In Section "Device Power and Operating Current Specifications" PVDD_STBY typ updated to 48 and PVDD_IO_STBY typ updated to 120 uW. This causes total typical power consumption in standby to drop from 174uW to 168uW". • Section "Device Power and Operating Current Specifications" is updated thouroghly. • Section "Total current specifications" is renamed as "Total power specifications for 0.8V and 1.8V Analog Domains" and the updates are: — Added paragraph "The following table contains ...." — Updated condition of 0.8V supply rails to adde VDD_STBY — Updated condition of 1.8V supply rails to delete VDD_EFUSE (Read) — Updated footnote "Thermal usecase: This is provided...." — Added footnote "Note that during Self Test execution, the power consumption...". • Added section "Static power specifications for I/O Domains". • In section "Power Sequencing", updated paragraph "The following sequence has been validated by NXP ....".

Rev 2, Apr 2021
• In section "Power Sequencing", updated sequence to power 3.3V supplies first. • In section "Power Sequencing", for Symbol "Vpwrdwn" footnotes deleted. • In section "Power Sequencing" added note "It is acceptable for the 1.8V supplies to not yet be within..." and added a figure "1.8V supply timing with respect to PMIC_VDD_OK during Standby Mode Exit". • In section "GPIO Pads", paragraph updated "The high-impedance state level is shown based ....". • In section "GPIO Pads", for Symbol "VIH" with condition "1.8V / 3.3V" Max value deleted. • In section "GPIO Pads", for Symbol "VIL" with condition "1.8V / 3.3V" Min value deleted. • In section "GPIO Pads", for Symbol "FMAX_18" with condition "SRE[2:0] = 101" Max changed from "100" to "133". • In section "GPIO Pads", for Symbol "FMAX_18" with condition "SRE[2:0] = 110" Max changed from "50" to "100". • In section "GPIO Pads", for Symbol "FMAX_18" with condition "SRE[2:0] = 111" Max changed from "1" to "50". • In section "GPIO Pads", for Symbol "FMAX_33" with condition "SRE[2:0] = 110" Max changed from "20" to "50". • In section "GPIO Pads", fig with title "Reference Load Diagram" is updated. • In section "GPIO Pads", fig with title "1.8V/3.3V GPIO pad detailed behavior during power up" is updated. • In section "GPIO Pads", fig with title "1.8V and 3.3V GPIO pad detailed behavior during power up" is updated. • In section "Aurora Pads", for Symbol "VSLEW_AURORA" with condition "max fAURORA" Min value deleted. • In section "Aurora Pads", for Symbol "IDD_HV_AUR" with condition "max fAURORA per active transmit lane" max updated from "30" to "31". • In section "Reset and Standby related pad electrical characteristics", fig with title "RESET_B pad detailed behavior" is updated. • In section "PMIC Standby Mode Entry / Exit Protocol" added reference to "Power sequencing" section to look for exceptions. • In section "SAR ADC", for Symbol "VAD_INPUT" footnote added "The reduced limits for VAD_INPUT in this...". • In section "SAR ADC", Symbol "IAD_LKG" with condition "TJ = 125C, Shared channel, channel OFF" is deleted. • In section "SAR ADC", Symbol "IAD_LKG" condition updated, changed "channel OFF" to "channel selection switch open" • In section "SAR ADC", Symbol "IAD_LKG" added footnote "The maximum and minimum leakage current...". • In section "SAR ADC", for multiple Symbol footnote updated "This specification is taken with averagi...". • In section "Temperature Monitoring Unit (TMU)", redundant paragraph removed "For High/Low temperature immediate threshold ....." • In section "FXOSC", updated crystal name to add suffix "GA". • In section "FXOSC" removed reference to "Contact NXP semiconductors....". • In section "FXOSC" added paragraph "RGMII specifications require clock source to have tolerance of +/- 50ppm. When using this mode, the crystal selected for system clock (FXOSC) should adhere to this specification." • In section "PLL", Symbol "fPLL_DDR_PHI0" min values added and a note added as "fPLL_DDR_PHI0 frequencies mentioned in this table....". • In section "PLL", Symbol "fPLL_MOD" with condition "SSCG enabled, down spread" is deleted. • In section "PLL", Symbol "PER_jitter" updated footnote to remove reference tom RM for jitter formula. • In section "LPSPI", for Symbol "tLEAD" with condition "Master" Min changed from "tSPSCK - 2.5" to "tSPSCK - 3.5".

Rev 2, Apr 2021
• In section "PCIe", Symbol "EQTX-COEFF-RES" with condition "8.0GT/s" is deleted. • GMAC sections are remamed as GMAC and PFE as these are applicable to PFE aslo. Differences are noted in notes and footnotes. • In section "GMAC and PFE RGMII", for Symbol "TskewT" footnote changed from "For all versions of RGMII prior to 2.0; ..." to "For all versions prior to RGMII v2.0 spec..." • In section "GMAC and PFE Management Interface", for symbol "MDIO_DOI" updated min to "-0.45". • In section "QuadSPI Octal 1.8V DDR 100MHz" updated "tCL_SCK_DQS" and "tCH_SCK_DQS" symbols. • In section "QuadSPI Quad 1.8V SDR 133MHz" added missing specs "tCL_SCK_DQS" and "tCH_SCK_DQS". • In all QuadSPI section: — Moved SRE to the top of the table in form of paragraph. — For Symbol "tOD_CS" min is update as "existing data - n/fSCK" and max updated as "existing data - m/fSCK" and added related footnote "Where m=TCSS and n=TCSH-1. Both...". — For Symbol "tCL_SCK" and "tCH_SCK" added a footnote "Clock measurements done with respect to VDD_IO_QSPI/2 level". — Footnote updated to mention maximun "Input timing assumes an maximum input...". • In section "QuadSPI configurations" updated header of the table. • In section "DDR", removed references to DDR4 and and added DDR3L standards. • In section "DDR Common DC Input", for Symbol "IIZ-BP" Min changed from "10" to "-50". • In section "DDR Common DC Output", for Symbol "ROnPu" from description removed "CLK outputs" from row 3 and row 4 and added them to description of row 5 and row 6. • Deleted section "DDR Common Input", "DDR4 DC Input" and "DDR4 Output" • Added section "DDR3L Output Timing". • In section "LPDDR4 DC Input", deleted a figure "Equation for Vref Footnote" and related reference. • In section "LPDDR4 Output", Symbol "tCAOeye" min updated to 0.62 and added condition as "UI=625ps". • In all sections of "uSDHC", added SRE to the top of table. • In section "uSDHC DDR-52MHz", added dedicated specifications for SDHC_CMD" and updated footnotes accordingly. • In section "uSDHC SDR-100MHz", updated tISU min 1.6ns. • In section "uSDHC DDR-HS400", updated tISU min -0.15ns. • In section "uSDHC DDR-HS400", for Symbol "tPP" Min changed from "200" to "133". • In section "uSDHC DDR-HS400", figures updated. • In section "JTAG Boundary Scan", for Symbol "tJCYC" footnote added as "TCK pin must have external pull down.". • In section "JTAG Boundary Scan", for Symbol "tJCYC" and "tJDC" footnote added as "TCK pin must have external pull down.". • In section "JTAG Debug Interface Timing", for Symbol "tJCYC" footnote added as "TCK pin must have external pull down.".

Rev 2 Draft E, Nov 2020
• In section "Total current specifications", for S32G254A power the max is updated to 4.37 W and thermal is updated to 4.22 W.

Rev 2 Draft D, Nov 2020
• Added information on the first page as DDR3L is supported and DDR4 is not. • Block diagram updated. • Updated “feature comparison” • Updated “Ordering information” figure. • In "Operating conditions" for LPDDR4 I/O voltage supply updated min value to 1.06 V. • Unsupported modes removed from “Clock frequency ranges”. • In DC electricals added specifications for “PVDD_IO_AUR” and removed "IDD_HV_AUR_LKG". • “Power sequencing” updated. • Added a note in “Aurora pads” as “Direct 100 ohm board termination not allowed …” • In section “Reset and Standby related pad electrical characteristics” updated WF_RESET_B max value from 20 to 17 ns. • In section “DFS” added minimum frequencies for fDFS_CORE_CLK1/2/2/3 and fDFS_PER_CLK2/5. • In section “FIRC” for PTA spec updated footnote starting from “fVAR defines how much the output frequency…” • In section “FXOSC” updated a footnote for CS_XTAL that it does not include miller capacitance and removed ALC enable mode from EXTAL_AMP spec. • In section “PCIe” updated a note containing term “TX_VBOOST_LVL = 5” to “TX_VBOOST_LVL = 4” • In “QuadSPI” updated SRE as: — b000 for 166 and 200 MHz — b110 for other modes. — Added section “QuadSPI configurations”

Rev 2 Draft C, Sept 2020
• Updated "should be equal to" to "should be matched closely to" in respect of transmission line resistance throughout the document. • S32G274A is replaced with S32G2 throughout the document. • Revised section “Overview” • In the "Feature comparison" table: — Revised the PCI express (PCIe) and SERDES rows for S32G234M. — Number of STM updated to 8. — PLL updated to 5. — For package added phrase "525 FC-PBGA" • In section "Absolute Max Ratings", for Symbol "VDD_LV_PLL" footnote added "VDD_LV_PLL must be connected to VDD..."

Rev 2 Draft C, Sept 2020

- In section "Operating Conditions", for Symbol "VIN_33" and "VIN_18" Typ value deleted.
- In section "Operating Conditions", removed references to Fast/Typical silicon, updated with DIE_PROCESS and updated missing values.
- In section "clock frequency ranges", removed some unused rows.
- Revised section "Device Power and Operating Current Specifications".
- Added section "Total current specifications".
- From section "GPIO Pads", moved ISLEW_POR_B and ISLEW_RESET_B to a new section "Reset and Standby related pad electrical characteristics".
- In section "GPIO Pads",added paragraphs "The weak pull-down is ...." and "The ramp-up state level ..."
- In section "GPIO Pads", updated figures.
- In section "GPIO Pads",
  - for Symbol "IOH_3318" with condition "SRE[2:0] = 110, 80% * VDD_IO_*" Min changed from "-27.7" to "-32"
  - for Symbol "IOH_3318" with condition "SRE[2:0] = 110, 80% * VDD_IO_*" Max changed from "-9.5" to "-10"
  - for Symbol "IOL_3318" with condition "SRE[2:0] = 000, 20% * VDD_IO_*" Min changed from "13.3" to "15"
  - for Symbol "IOL_3318" with condition "SRE[2:0] = 000, 20% * VDD_IO_*" Max changed from "34.0" to "40"
  - for Symbol "IOL_3318" with condition "SRE[2:0] = 101, 20% * VDD_IO_*" Min changed from "12.0" to "13"
  - for Symbol "IOL_3318" with condition "SRE[2:0] = 101, 20% * VDD_IO_*" Max changed from "31.4" to "36"
  - for Symbol "IOL_3318" with condition "SRE[2:0] = 100, 20% * VDD_IO_*" Min changed from "13.3" to "15"
  - for Symbol "IOL_3318" with condition "SRE[2:0] = 100, 20% * VDD_IO_*" Max changed from "34.0" to "40"
  - for Symbol "RDSON_3318" with condition "SRE[2:0] = 000, 50% * VDD_IO_*" Min changed from "20.0" to "18.0"
  - for Symbol "RDSON_3318" with condition "SRE[2:0] = 000, 50% * VDD_IO_*" Max changed from "45.0" to "43.0"
  - for Symbol "RDSON_3318" with condition "SRE[2:0] = 101, 50% * VDD_IO_*" Min changed from "22.0" to "21.0"
  - for Symbol "RDSON_3318" with condition "SRE[2:0] = 101, 50% * VDD_IO_*" Max changed from "51.5" to "50.0"
  - for Symbol "IOH_3318" with condition "SRE[2:0] = 000, 80% * VDD_IO_*" Min changed from "-33.7" to "-40"
  - for Symbol "IOH_3318" with condition "SRE[2:0] = 000, 80% * VDD_IO_*" Max changed from "-13" to "-14"
  - for Symbol "RDSON_3318" with condition "SRE[2:0] = 100, 50% * VDD_IO_*" Min changed from "20.0" to "19.0"
  - for Symbol "RDSON_3318" with condition "SRE[2:0] = 100, 50% * VDD_IO_*" Max changed from "45.0" to "44.0"
  - for Symbol "IOH_3318" with condition "SRE[2:0] = 111, 80% * VDD_IO_*" Min changed from "-27.7" to "-32"
  - for Symbol "IOH_3318" with condition "SRE[2:0] = 111, 80% * VDD_IO_*" Max changed from "-9.5" to "-10"
  - for Symbol "RDSON_3318" with condition "SRE[2:0] = 110, 50% * VDD_IO_*" Min changed from "25.0" to "23.0"
  - for Symbol "RDSON_3318" with condition "SRE[2:0] = 110, 50% * VDD_IO_*" Max changed from "61.5" to "61.0"
  - for Symbol "IOH_3318" with condition "SRE[2:0] = 101, 80% * VDD_IO_*" Min changed from "-31.0" to "-35"
  - for Symbol "IOH_3318" with condition "SRE[2:0] = 101, 80% * VDD_IO_*" Max changed from "-11" to "-10"
  - for Symbol "IOH_3318" with condition "SRE[2:0] = 100, 80% * VDD_IO_*" Min changed from "-33.7" to "-40"
  - for Symbol "IOH_3318" with condition "SRE[2:0] = 100, 80% * VDD_IO_*" Max changed from "-13" to "-14"

Rev 2 Draft C, Sept 2020
— for Symbol "IOL_3318" with condition "SRE[2:0] = 111, 20% * VDD_IO_*" Min changed from "10.0" to "11" — for Symbol "IOL_3318" with condition "SRE[2:0] = 111, 20% * VDD_IO_*" Max changed from "27.7" to "32" — for Symbol "IOL_3318" with condition "SRE[2:0] = 110, 20% * VDD_IO_*" Min changed from "10.5" to "12" — for Symbol "IOL_3318" with condition "SRE[2:0] = 110, 20% * VDD_IO_*" Max changed from "28.6" to "33" — for Symbol "RDSON_3318" with condition "SRE[2:0] = 111, 50% * VDD_IO_*" Min changed from "26.5" to "26.0" — for Symbol "RDSON_3318" with condition "SRE[2:0] = 111, 50% * VDD_IO_*" Max changed from "61.5" to "61.0" • Removed section "LVDS pads" as the receiver specs are already part of Aurora pads. • In section "Aurora Pads", for Symbol "IDD_HV_AUR" Max changed from "28" to "30". • In section "Aurora Pads", for Symbol "VOH_AURORA" with condition "100 termination at receiver end" Min changed from "VDD_IO_AUR/2 + 0.2" to "VDD_IO/2 + 0.2" • In section "Aurora Pads", for Symbol "VOL_AURORA" with condition "100 termination at receiver end" Max changed from "VDD_IO_AUR/2 - 0.2" to "VDD_IO/2 - 0.2" and a added footnote "VDD_IO maps to corresponding supply...". • In section "Aurora port timing", added JD spec for between 3.0Gbps to 5.0Gbp with 0.25 OUI. • Added section "Reset and Standby related pad electrical characteristics" and its subsection "PMIC Standby Mode Entry / Exit Protocol". • In section "SAR ADC", for Symbol "DNL" with condition "after calibration" footnote added "This specification is taken with averaging." • In section "FIRC", PTA specification and related footnote deleted. • In section "FXOSC", added specs for EXTAL_AMP, LT_Jitter. • In section "FXOSC", paragraph updated "In crystal mode NX5032 crystal ..." • In section "PLL", for Symbol "fPLL_MOD" Max changed from "32" to "64". • In section "LPSPI", fig with title "LPSPI Slave Mode Timing (CPHA=1)" and "LPSPI Slave Mode Timing (CPHA=0)" is updated. • In Flexray section, removed references to 1.8V/3.3V GPIO and related SRE. • In section "PCIe", for Symbol "VTX-DE-RATIO-6dB" with condition "5.0GT/s" Min changed from "5.5" to "5" and Max changed from "6.5" to "7" • In section "PCIe", for Symbol "UI" with condition "5.0GT/s" Min changed from "199.4" to "199.94" • In section "PCIe", for Symbol "VTX-DE-RATIO-3.5dB" with condition "2.5GT/s, 5.0GT/s" Min changed from "3" to "2.5" and Max changed from "4" to "4.5". • In section "GMAC Management Interface" , fig with title "MDC / MDIO Timing" is changed • In section "GMAC Management Interface", for Symbol "MDIO_DOI" and "MDIO_DOV" description updated to mention falling edge. • In section "GMAC RGMII", SRE updated to b100. • In section "QuadSPI", added paragraph as "An external resistor is needed to pull up a QuadSPI chip select signal." • In section "DDR" added information on related JEDEC standards and other information. • In section "DDR4 Output" and "LPDDR4 Output", for Symbol "tCK(avg)" footnote updated to mention updated slew rate "Measurements were done with signals ...." • In section "DDR4 Output", for Symbol "tCK(avg)" value "0.625" moved from min to typ.

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- In section "JTAG Boundary Scan" removed spec "TJCMPH" and figure "JCOMP Timing" is updated to reflect the spec update.

Rev 2 Draft B, June 2020

- In uSDHC DDR-HS400, for tPP, added min value as 200 MHz
- In SAR ADC, updated a footnote “ADC performance specifications are only guaranteed…”
- In QuadSPI, added Octal 1.8V DDR 166/200 MHz modes.
- In QuadSPI, updated 1.8V Quad SDR 133 MHz
- In SAR_ADC, updated the conditon of TUE as "after calibration, no current injection on an adjacent pin" to "after calibration"
- In TMU, removed a non-applicable footnote.

Rev 2 Draft A, May 2020

- In section "Feature comparison", changed from "Arm CoreSight JTAG (IEEE 1149.1/1149.7)" to "Arm CoreSight JTAG (IEEE 1149.1)" as cJTAG is defeatured.
- In section "Operating conditions" deleted "fCLKOUT_LVDS".
- In section "Operating Conditions", LPDDR4 I/O voltage supply updated to 1.078 (min)
- In section "Operating Conditions", a footnote deleted "VDD_IO_* I/O supplies require +/- 5% DC tolerance at 3.3V. Tolerance up to +/- 10% is allowed when including AC noise on the supply."
- In section "Operating Conditions", for Symbol "IINJ_A" footnote updated "The specified injection current is allowed ....."
- In section "Operating Conditions", for Symbol "IINJ_A" Min value changed to "-1"
- In section "Operating Conditions", for Symbol "IINJ_A" Max changed from "0" to "1"
- In section "Operating Conditions", for Symbol "VDD_VP_PCIEn" with condition "Fast silicon (fuse setting = b01)" footnote value changed to "Both PCIe supplies must ramp for the SerDes PHY to safely power up into its reset state. Until both supplies are ramped, the SerDes PHY will be in an undefined state."
- In section "Operating Conditions", for Symbol "VRAMP_LV" with condition "Applies to 0.8V supplies" footnote added as "On slow ramps, the RESET_B pin may be observed to be asserted multiple times during the supply ramping if the RESET_B pin is not being driven low by the PMIC during this time as recommended."
- In section "Operating Conditions", for Symbol "VDD_EFUSE" footnote changed from "VDD_EFUSE may be grounded in order to save power when not actively programming the fuses. This supply is not required to be powered for fuse reads." to "VDD_EFUSE must be grounded when not actively programming the fuses. This supply is not required to be powered for fuse reads."
- In section "Operating Conditions", added sentence "The “fuse setting” values/conditions in above table correspond with the DIE_PROCESS[1:0] fuses which NXP programs during manufacturing. See Reference Manual and it’s Fuse Map for further details about the purpose. Example: Value “b01” represents DIE_PROCESS[1]=0 and DIE_PROCESS[0]=1”."
- In section "Operating Conditions", added sentence "The chip hardware design guidelines document summarizes mandatory board design rules in table “Decoupling caps values” and section “PDN impedance calculations”."
- In section "Operating Conditions", for Symbol "VDD_LV_PLL" with condition "Fast silicon (fuse setting = b01)" footnote changed from "The minimum operating voltage applies when SVS is enabled, FAST silicon. SVS guidelines apply to all LV supplies on the device." to "The minimum operating voltage applies when SVS is enabled, FAST silicon. SVS

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guidelines apply to all LV supplies on the device. Refer power management chapter of device reference manual for details on SVS." • In section "Operating Conditions", added figure "TDISCHARGE STDBY definition" • In section "Power Sequencing", update a note "Note that while powering up the device or exiting from Standby mode, ..." • In section "GPIO Pads", for Symbol "VHYS_33" with condition "Always enabled." description changed from "GPIO33 input hysteresis voltage" to "3.3V GPIO input hysteresis voltage" • In section "GPIO Pads", added specifications for "ISLEW_POR_B" and "ISLEW_RESET_B". • In section "GPIO Pads", added specifications for "VISE_33", "VISE_18" and "VISE_3318" and corresponding figures at the end of section. • In section "GPIO Pads", for Symbol "FMAX_18" with condition "SRE[2:0] = 000" footnote updated "I/O timing specifications are valid for the un-terminated 50ohm ..." • In section "GPIO Pads", added a note "In the Standby mode exit case, the rising edge of the PMIC_VDD_OK ..." • In section "GPIO Pads", for Symbol "FMAX_33" with condition "SRE[2:0] = 110" Max changed from "10" to "20" • In section "LVDS Pads", description of Symbol "F_RX_PAD_CORE" updated. • In section "LVDS Pads", for Symbol "VCM_LVDS_RX" with condition "high gain setting" changed specs to 0.6V (min) to 1 V (max). • In section "LVDS Pads", for Symbol "VDIFF_LVDS_RX" with condition "high gain setting" changed specs 400mV (min). • In section "LVDS Pads", deleted IDD_HV_LVDS_RX. • In section "Aurora Pads", for Symbol "fAURORA" with condition "100 external termination (Not on board but inside receiver after AC coupling)" Min value changed to "0.05" • In section "Aurora Pads", deleted ISTDBY_AURORA. • In section "Aurora Pads", for Symbol "VCM_AURORA" Min changed from "775" to "0.775" • In section "Aurora Pads", for Symbol "RTERM_AURORA" with condition "enabled" Max changed from "125" to "130" • In section "Aurora Pads", for Symbol "VOD_AURORA_DC" with condition "ipp_obe=1 DC condition" Min changed from "900" to "800" • In section "Aurora Pads", for Symbol "VOD_AURORA_DC" with condition "ipp_obe=1 DC condition" Max deleted. • In section "Aurora Pads", updated a footnote "Termination scheme as shown in “End Termination Circuit” applies to debug tool hardware and is not recommended to be placed on the PC." • In section "Aurora Pads", added note "Source termination Circuit – Transmitter side 100 ohm termination is present inside the Tx pad and should not be placed on the PCB." • In section "Aurora Pads", for Symbol "VOD_AURORA_DC" with condition "ipp_obe=1 DC condition" footnote deleted. • In section "Aurora Pads", other footnotes also updated thoroughly. • In section "Aurora PLL", for Symbol "fPLL_CLKIN_PFD" footnote added as "It is Aurora PLL Input Reference Clock Frequency after pre-divider." • In section "Aurora PLL", removed mod sign and pk-pk from description. • In section "PMC Bandgap", for Symbol "VBG_SCALED" with condition "Both bandgap and buffer are trimmed" description changed from "Scaled version of bandgap referencevoltage" to "Scaled version of bandgap referencevoltage measured by SAR ADC"

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• In section "PMC Bandgap", for Symbol "VBG_SCALED" with condition "Both bandgap and buffer are trimmed" footnote value updated to "ADC conversion error must be included when reading the bandgap reference voltage via the chip ADC." • In section "PMC Bandgap", deleted specification for VBG_REF_T. • In section "Reset Duration", for Symbol "POR" with condition "FIRC_CLK, trimmed during destructive reset phase" Max changed from "600.3" to "1500" • In section "Reset Duration", for Symbol "TFR" with condition "FIRC_CLK, trimmed" Max changed from "333.3" to "545" • In section "Reset Duration", for Symbol "TDR" with condition "FIRC_CLK, trimmed during destructive reset phase" Max changed from "583.1" to "1370" • In section "Reset Duration", added figures. • In section "SAR ADC", updated condition of "IAD_LKG" to show full range specifications and deleted corresponding note. • In section "SAR ADC", for Symbol "DNL" min updated to "-1" and max updated to "2" LSB. • In section "SAR ADC", for Symbol "THD" condition updated as "Input signal frequency >= 50KHz." • In section "SAR ADC", added specifications for CP1, CP2, CS, RSW1 and RAD. • In section "SAR ADC", figure "SAR ADC Specification Characteristics" updated • In section "SAR ADC", added note "ADC performance specifications are guaranteed when calibration uses maximum averaging i.e. when AVGEN = 1 and NRSMPL = 3." • In section "Temperature Monitoring Unit (TMU)", removed overlaping of TRANGE as per TERR and removed THTF_MAX and TLTF_MIN. • In section "Temperature Monitoring Unit (TMU)", added note "For High/Low temperature immediate threshold value flag setting procedures, see TMHTITR[TEMP] and TMLTITR[TEMP] register fields in device reference manual." • In section "Temperature Monitoring Unit (TMU)", deleted redundant notes. • In section "Glitch Filter", for Symbol "TFILT" Max changed from "20" to "17" • In section "IRQ", deleted specification for tICYC and the related footnote. • In section "DFS", added frequencies for fDFS_CORE_CLK3, fDFS_PER_CLK2 and fDFS_PER_CLK5. • In section "DFS", added PER_jitter at odd and even mfn with different fDFS_CLKIN and removed pk-pk from description. • In section "DFS", revised footnote "Min jitter=Min(PER_jitter(PLL))*(sqrt(N))+Min(PER_jitter(DFS)). Max jitter=Max(PER_jitter(PLL))*(sqrt(N))+Max(PER_jitter(DFS)). Where N is the DFS division factor. All jitter numbers are in ps." • In section "FXOSC", added note "See Hardware design guide for recommended circuits for each bypass mode." • In section "FXOSC", added note "In crystal mode, 20 MHz, NX5032 crystal has 8 pF load cap and gm_sel[3:0]=4'b0100 and NX3225 has 8pF load cap and gm_sel[3:0]=4'b100." • In section "FXOSC", added note "In crystal mode 24 MHz, NX5032 crystal has 8 pF load cap and gm_sel[3:0]=4'b0101 and NX3225 has 8pF load cap and gm_sel[3:0]=4'b0110." • In section "FXOSC", added note "In crystal mode 40 MHz, NX5032 crystal has 8 pF load cap and gm_sel[3:0]=4'b0101 and NX3225 has 8pF load cap and gm_sel[3:0]=4'b1100." • In section "FXOSC", added new specification for Leakage_injection. • In section "FXOSC", updated Leakage_extal specs as -20 (min) and 20 (max) nA with condition "Bypass mode, 0.5V"

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- In section "FXOSC", deleted "FXOSC Bypass Frequency"
- In section "PLL", updated thoroughly to show frequencies with/without centre spread and other updates.
- In section "SPI", changed note from "SPI timing specifications are valid only with a slave device in classic mode (MTFE=0)" to "Slave mode timing values given below are applicable when device is in MTFE=0."
- In section "SPI", updated footnotes for clarity.
- In section "I2C Output", for Symbol "tOH_SC" footnote changed IFDR to IBFD.
- In section "LPSPI", for Symbol "tSU" with condition "Slave" Min changed from "2.5" to "4"
- In section "LPSPI", for Symbol "tLAG" with condition "Master" Min changed from "tSPSCK / 2" to "tSPSCK - 2.5"
- In section "LPSPI", for Symbol "tLAG" with condition "Slave" Min changed from "-" to "25"
- In section "LPSPI", for Symbol "tSU" with condition "Master" Min changed from "10" to "12"
- In section "LPSPI", for Symbol "tV" with condition "Master, SRE[2:0] = 101" Max changed from "4" to "6"
- In section "LPSPI", for Symbol "tLEAD" with condition "Master" Min changed from "tSPSCK / 2" to "tSPSCK - 2.5"
- In section "LPSPI", for Symbol "tLEAD" with condition "Slave" Min changed from "-" to "25"
- In section "LPSPI", for Symbol "tLAG" with condition "Master" footnote added "tSCKPCS = (SCKPCS+1) * (2**PRESCALE) * (1 / fPER_CLK)"
- In section "LPSPI", for Symbol "tLEAD" with condition "Master" footnote added "tPCSSCK = (PCSSCK+1) * (2**PRESCALE) * (1 / fPER_CLK)"
- In section "FlexRay - TxD", for Symbol "dCCTxAsym" updated description and added min/max as -2.5/+2.5 ns.
- In section "PCIe", added a paragraph "NXP completed PCI-SIG compliance ...".
- In section "PCIe", added a paragraph "NXP completed PCI-SIG TX compliance testing ..."
- In section "PCIe", for Symbol "UI" with condition "8.0GT/s" Min changed from "125.0375" to "124.9625"
- In section "PCIe", for Symbol "UI" with condition "8.0GT/s" Max changed from "129.9625" to "125.0375"
- In section "PCIe", for Symbol "TTX-UTJ" with condition "8.0GT/s" Unit changed from "ps PP @ 10-12" to "ps PP @ 10e-12"
- In section "GMAC Management Interface", "ENET_MSCR [HOLDTIME] should be set to 001 when Module Clock = 125 MHz. MDIO pin must have external pull up." removed
- In section "GMAC Management Interface", for Symbol "MDIO_DOI" with condition "SRE[2:0] = 100" Min changed from "(-0.8 + (ENET_MSCR[HOLDTIME] +1)*(PBRIDGE_n_CLK period in ns))" to "0"
- In section "GMAC Management Interface", for Symbol "MDIO_DOV" with condition "SRE[2:0] = 100" Max changed from "(13 + (ENET_MSCR[HOLDTIME] +1)*(PBRIDGE_n_CLK period in ns))" to "15"
- In section "GMAC RGMII", SRE updated to 110 for all specs.
- In section "GMAC SGMII" , figure with title "SGMII Timing" is changed.
- In section "GMAC SGMII" , Transmit Random Jitter (RJ) is deleted.
- In section "QuadSPI" ,deleted tISU_SCK Auto-learning, tCK2CKmin, tCK2CKmax and deleted some redundant figures.
- In section "QuadSPI" ,added tLSKEW for 66MHz.
- In section "DDR Common DC Output", added "NOTE: Refer to IBIS model for the complete IV curve characteristics."
- In section "DDR Common DC Output", for Symbol "ROnPu" moved value from Max to Typ.

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• In section "DDR Common Input", footnotes revised. • In section "DDR4 Output", for Symbol "tOS(Vref)" with condition "dskew = +/- 30ps" Min changed from "225" to "210" • In section "DDR4 Output", for Symbol "tOH(Vref)" with condition "dskew = +/- 30ps" Min changed from "225" to "210" • In section "DDR4 DC Input", footnotes revised. • In section "LPDDR4 Output", for Symbol "tCK(avg)" value "0.625" moved from typ to min. • In section "LPDDR4 Output", footnote 2 updated • In section "uSDHC DDR-52MHz", symbol tOD, SDHC_CMD deleted from condition and added a footnote "CMD signal operates synchroounously ...." • In section "uSDHC DDR-HS400", symbol tOD, SDHC_CMD deleted from condition and added a footnote "The CMD output timing for HS400 mode ...." • Deleted section "Serial Wire Debug (SWD) Timing" • In section "JTAG Boundary Scan", for Symbol "tJCYC" footnote addedm "JTAG port interface speed only. Does not apply to boundary scan timing." to "These specifications apply to JTAG boundary scan mode only." • In section "JTAG Boundary Scan", for Symbol "tJCMPS" description changed from "JCOMP setup time to TCK low" to "JCOMP setup time to TCK high" • In section "JTAG Boundary Scan", added spec "TJCMPH" - JCOMP hold time to TCK low • In section "JTAG Debug Interface Timing", for Symbol "tNTDOD" description changed from "TDO/TDOC propagation delay from falling edge of TCK" to "TDOpropagation delay from falling edge of TCK" • In section "JTAG Debug Interface Timing", for Symbol "tNTDOD" deleted footnote "Timing includes TCK pad delay, clock tree delay, logic delay and TDO/TDOC output pad delay." to "Timing includes TCK pad delay, clock tree delay, logic delay and TDOoutput pad delay." • In section "JTAG Debug Interface Timing", for Symbol "tTCYC" description changed from "Absolute minimum TCK cycle time (TDO/TDOC sampled on negedge of TCK)" to "Absolute minimum TCK cycle time (TDO sampled on negedge of TCK)" • In section "JTAG Debug Interface Timing", for Symbol "tNTMSS" description changed from "TMS/TMSC data setup time" to "TMS data setup time" • In section "JTAG Debug Interface Timing", for Symbol "tNTMSS" deleted footnote "TMSC represents the TMS bit frame of the scan packet in compact JTAG 2-wire mode." • In section "JTAG Debug Interface Timing", for Symbol "tNTDIH" description changed from "TDI/TDIC data hold time" to "TDI data hold time" • In section "JTAG Debug Interface Timing", for Symbol "tNTDOH" description changed from "TDO/TDOC hold time with respect to falling edge of TCK" to "TDO hold time with respect to falling edge of TCK" • In section "JTAG Debug Interface Timing", for Symbol "tNTDIS" description changed from "TDI/TDIC data setup time" to "TDI data setup time" • In section "JTAG Debug Interface Timing", for Symbol "tNTMSH" description changed from "TMS/TMSC data hold time" to "TMSdata hold time" • In section "JTAG Debug Interface Timing", deleted tTCYC for cJTAG.

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