AN1832

Application Note

MSCSICSP6/REF3 SiC SP6LI Module Driver Reference Design

Final

October 2018

Microsemi

a Microchip company

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision B

Revision B was published in October 2018. In Revision B of this document, the following changes were made:

- Updated the Quickstart (see page 15)subsection.
- Added the Full Setup with a Module and DC Bus Power (see page 15) subsection.
- Updated the Block Diagram (see page 2) in the Introduction (see page 2) section.

1.2 Revision A

Revision A was published in May 2018. It was the first publication of this document.

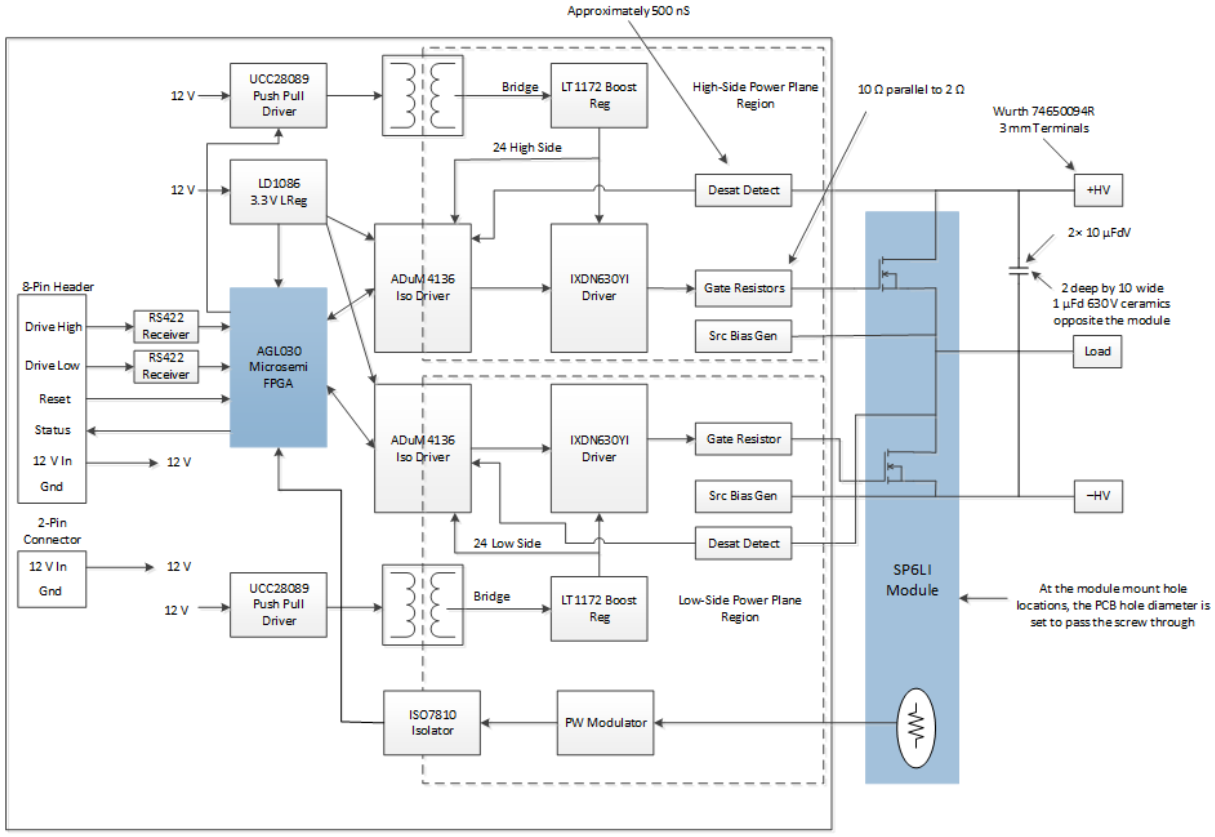
2 Introduction

This reference design provides an example of a highly isolated SiC MOSFET dual-gate driver for the SP6LI SiC phase leg modules. It can be configured by switches to drive in a half-bridge configuration with only one side on at any time and with dead time protection. It can also be configured to provide concurrent drive, if necessary. This design is intended for use with Microsemi SiC SP6LI modules. The dead time and gate drive resistance are adjusted by the user to match the requirements of the application. Optional dead time protection and optional desaturation protection makes device evaluation easier while lowering the risk of damaging parts.

In this document, you will find a quick start guide in addition to useful reference information, including the bill of materials and schematics. Contact your local sales office to request Gerber files, Verilog code, and the Libero project.

This design is offered as an engineering tool for the evaluation of Microsemi SP6LI SiC modules in a laboratory environment. It has not been tested at voltage across the insulation boundaries. It is the responsibility of the engineer to use the proper safety equipment and procedures. Refer to the appropriate UL or IEC standards for guidance on insulation and creepage requirements.

Figure 1 • Block Diagram with Half Bridge



When comparing the drive of Si devices against SiC devices, there are two important differences to consider:

- The slew rate at the output of a SiC half bridge can be much higher than with silicon. SiC power stages can easily achieve a dV/dt of 50 kV/µs or more. This affects the design of the gate drive signal isolation and EMI mitigation. It creates potential issues with the method of implementation of parts of the system such as the gate power DC–DC function. The intention of this board is to provide an off-the-shelf test solution which addresses these issues.
- SiC MOSFETs are normally driven at higher asymmetrical gate voltages compared to silicon MOSFETs. Typical drive levels are –5 V to 20 V. The driver can be configured to a lower drive level of –5 V to 18 V if the resulting higher R_{ON} is acceptable. Reference Microsemi Application Note 1826 for additional gate drive recommendations.

3 Reference Design Description

This reference design is optimized to drive SP6LI SiC MOSFET devices at high speeds with desaturation protection. It is a base design that can be simplified depending upon the individual system requirements. The following is a list of features:

- Requires only a 12 V power input
- –5 V, 20 V output gate drive, jumper selectable to –5 V, 18 V
- Includes an example of temperature monitoring
- Galvanic isolation of more than 2000 V on both gate drivers[1]
- Capable of 16 W of gate drive power/side
- Peak gate current of up to 30 A
- Maximum output current of approximately 150 A due to limitations of the trace
- Maximum switching frequency greater than 400 kHz[2]
- Single-ended or RS485/RS422 differential input gate control
- Shoot through (short-circuit) protection
- ±100 kV/µs capability
- Programmable dead time protection
- Fault signaling
- Under voltage lockout protection

Notes:

1. The ICs and transformer are rated to greater than 2000 V. The trace clearance rating is dependent upon the allowable contamination level and is the responsibility of the user. Note that the board clearance around the gate transformers is low for a 2 kV design. An epoxy coating should be added to adjacent trace if additional protection is desired.
2. The board has been tested to 400 kHz. Any calculation of gate-power drive must include the frequency dependent portion of the driver IXDN630 and the ADuM4136.

3.1 Gate Drive

This design uses Analog Devices ADuM4136 to pass signals across the isolation boundary. An IXDN630 driver is then used to increase the output drive current to 30 A, something more in line with the current associated with a module. A Zener diode is added in the positive leg of the ADuM4136 to increase the UVLO trip point to approximately 18 V.

There is a need to transfer energy across the isolation interface to drive the gates. Most standard isolation supplies are not designed with adequate insulation, a low capacitance interface and tolerance to the high dV/dt associated with SiC MOSFETs in a half bridge. Consider that 10 pF of capacitance across the barrier translates to a 350 mA current spike back into the gate supply and its associated grounding at 35 V/ns. It is desirable to keep the capacitance across the gate supply transformer to a minimum.

The transformer used in this design has a few pF capacitances. Other designs can be considered and higher capacitance can be tolerated. However, it is important to keep in mind that the displacement current across the transformer winding must be absorbed by the drive FETs into the source sense resistors and from the low voltage ground into the system environment.

This driver has capacitors from the low voltage (SELV) side ground to the screw holes. This provides a means by which the currents can be directed to a chassis or other ground reference. Without this grounding, the displacement currents are directed into the RS422 pairs, possibly resulting in excessive common-current mode or failure of the signal interface.

Power is transferred across the isolation boundary with a UCC28089 push-pull driver and FDS3512 MOSFETs, followed by a custom transformer. Power is transferred unregulated over the boundary and then regulated on the gate side. This decouples the isolation transformer design from the regulator design.

A Microsemi FPGA controls power sequencing. If at any time a fault is flagged by one of the ADuM4136 drivers, then switching is cut off to both drivers. This may help the power stage survive output device failures or at least lead to less damage.

The gate power transformer is constructed from an RM10 core (Epcsos B65813J0000R041) and split bobbin (Epcsos B65814N1012D002). The wire is by Belden (part number 8051; double insulated magnet wire). The primary is 12 turns center tapped, 22 gauge. The secondary is 12 turns, 22 gauge. The pins on the bobbin are not used. Instead, the pins are pulled. The resulting hole is then drilled to pass the 22 gauge wire. This results in a cleaner construction than what would occur by wrapping the wire on the pins, as is normally done.

3.2 Gate Resistor Selection

Gate resistor selection is driven by a number of factors, including the following:

- Lower resistance results in lower switching loss.
- Gate resistance that is too low results in excessive ringing.
- The gate OFF drive should be roughly 2:1 greater than the ON drive to avoid excessive Miller Effect conduction from the bump on the opposing transistors.
- Modules that drive at a high frequency have a relatively high gate resistor power dissipation. Heat sinking of the resistors may be necessary.
- If desaturation protection is being considered, there may be a need to turn OFF slowly. This is more applicable to product development where it may be acceptable to take the additional switching loss.

This board is provided with three parallel 10 Ω resistors that provide ON and OFF drive, 3.3 Ω, and two parallel 10 Ω resistors that provide only OFF drive through a diode resulting in 2 Ω.

3.3 Desaturation Protection

In a general sense, desaturation protection is provided as an attempt to protect the power module in the event of an over-current condition normally due to a loss of control or failure of the opposing device. If an over-current condition results in a device going out of saturation when the gate is commanded ON, then the device is commanded permanently OFF. Sometimes it is desirable to have this function during product development even if it will not be used in the final product.

Setting up desaturation protection is tricky. Desaturation events generally result from excessive drain current. In an over-current event, the inductive kick on the drain is higher than normal. A technique around this is to shut off the transistor slowly. Note that this does not protect in the event the command to turn OFF happened to occur just below the desaturation point. In addition, at the higher currents of modules, it becomes more difficult to provide a bus structure with a proportionally lower inductance. For this reason, the function is not used in many cases.

The gate resistors on this driver should be set such that the turn-ON drive current is less than the turn-OFF drive current. The ratio of the currents normally is about 2:1 to avoid Miller Effect conduction. This is not a precise number and closer to 1:1 is fine in many applications. If testing shows there is a sufficient margin on the breakdown voltage during an over-current event, then the desaturation circuitry can be considered.

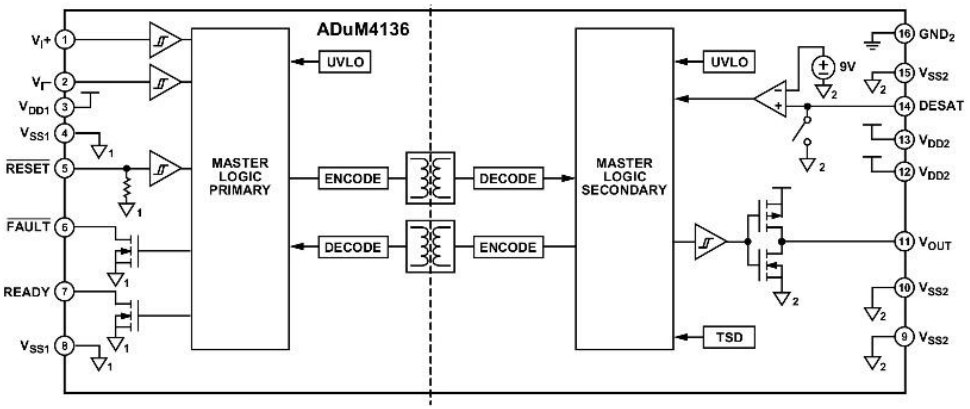
The top-side and bottom-side drivers are identical. The top-side driver desaturation circuit is described here. The artwork is setup such that two series high-voltage diodes can be considered (D12 and D22). The printed circuit board (PCB) is assembled with one RP1HV1 fast recovery diode. During switching, the diode capacitance (about 2 pF) drives current into the SBD clamp diodes (D9 and D10). R31 sets the forward current in the D12 and D22 diodes. Reference the ADuM4136 specification for information on setting up the circuit. It is important to consider the following:

- If desaturation detection is not used, D31 should be shorted.
- If desaturation detection is used, then D31 is recommended. If D31 is not installed, then R32 should not be less than the 220 Ω in the circuit. This is to avoid latching U7 due to excessive current in a diode internal to U7 that parallels D31.
- If D31 is installed, it is important to be sure that the average switching current carried by D31 does not rise to a level high enough that it collapses the Zener negative gate-voltage supply.

When a gate high is asserted, it is expected that within a few hundred ns the source-to-drain voltage across the power FET will be low. If this is not the case, then circuitry both internal and external to the ADuM4136 verifies this and shuts off the FET.

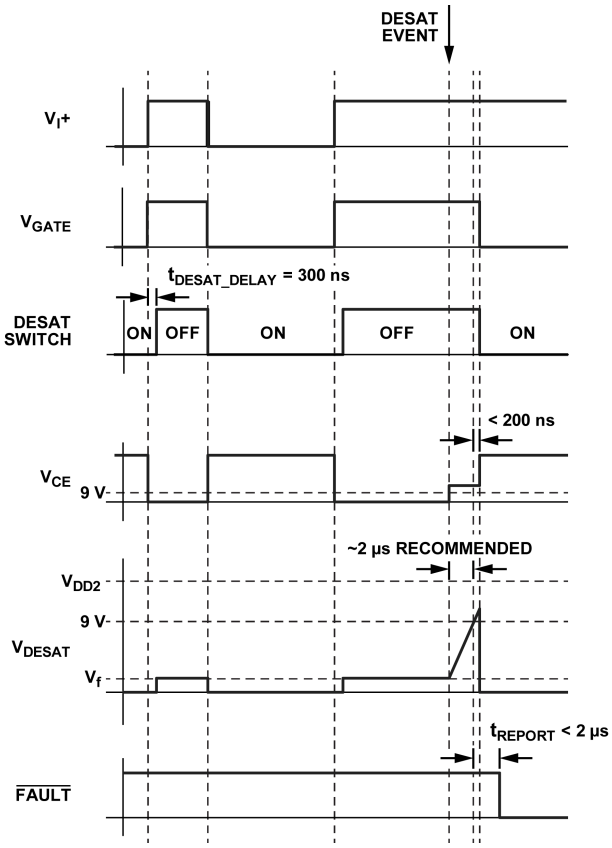
At approximately 300 ns after asserting the high-FET gate voltage, a FET internal to the ADuM4136 releases the DESAT pin. The pin is then free to float up. A 500 µA current source pulls it up internal to the ADuM4136. In addition, a 10K resistor pulls it up externally. If it crosses 9 V, the ADuM4136 interprets the condition as a fault and shuts off FET drive. The FET gating the DESAT pin is at the switch in the upper right of the following block diagram (note that the grounds on the primary and secondary sides are isolated from each other).

Figure 2 • ADuM4136 Block Diagram



SiC MOSFETs have a much smaller die than their silicon counterpart. As a result they have lower thermal mass and heat faster in a short circuit condition. The following figure is from the ADuM4136 spec showing timing typical of an IGBT. With SiC MOSFETs, a delay of 200 ns–300 ns would be more appropriate than 2 µs delay.

Figure 3 • ADuM4136 Spec



The delay time is controlled by R31 and C17. ADuM4136 has a blanking time of 300 ns, which should be enough for a SiC power stage in most cases. The additional delay past blanking can be increased by adding C17 or decreased slightly by reducing R31. If a scope is used to observe the desat signal at the input to the ADuM4135, the low-side driver should be observed and a very low capacitance probe should be used.

3.4 Thermistor Support

This board demonstrates a method by which the module thermistor can be brought back to a processor in a safe and relatively simple manner. In the event of a catastrophic failure of the module, there is the possibility a plasma within the device could touch the thermistor. If the thermistor directly interfaces with the control structure, this would result in power from the DC bus feeding back into the low-voltage control structure. To prevent this, the thermistor information is captured in the environment of the low-side driver. U17 then passes back a pulse width modulation (PWM) signal across the insulation boundary.

The thermistor resistance is converted to a PWM signal by U12. U12A is an oscillator that generates a triangular-like wave between 1/3 and 2/3 V_{CC}. In this case, V_{CC} is 3.3 V from PS2. U12B then compares the oscillator with the level from the thermistor, resulting in a PWM input to U17.

The PWM output normally would be linearized by a remote processor. The current implementation of the FPGA does not process the signal. However, the signal can be observed at the feed through next to C59. See Figure 5 (see page 13) for the location.

It is common practice to map the response of a thermistor to the temperature through a look-up table. The interface circuit provided adds another layer of non-linearity. This adds another calculation in the generation of the look-up table. With the ramp limits at 1/3 and 2/3 V_{CC}, the circuit captures over a 4:1 range of thermistor resistance. This can be extended as described below.

3.5 Thermistor Transfer Function

This section describes the transfer function of the voltage at the thermistor to the duty factor observed by the FPGA/processor. These equations are provided without proof. Define the following variables:

- D = duty factor. It ranges from 0 to 1.
- Vx = thermistor voltage. This is expressed as a ratio of V_{CC}. In the circuit provided, Vx can be measured between values of 1/3 (0.333) and 2/3 (0.666)
- Variables A, B, C are temporary variables to simplify expressions.

At the high-temperature measure limit, Vx = 1/3 and D = 1. Likewise at the low-temperature measure limit, Vx = 2/3 and D = 0.

The equation that maps Vx to D is as follows:

A = ln((1 – Vx)/Vx);

B = 2 * ln(2);

D = ½ + A/B;

The inverse equation mapping D to Vx is as follows:

C = (2 * D – 1) * ln(2);

Vx = 1/(1 + exp(C));

The resistor R67 sets the resistance at which the thermistor resistance maps to Vx = 0.5, which defines the center of the measure range. Resistors R47, R64, and R65 set the oscillator ramp limits at 1/3 V_{CC} and 2/3 V_{CC}.

It may be desired to increase the measure range of the circuit beyond the 4:1 range provided. Again provided without proof, if R47 and R64 are increased such that the oscillator limits are (k – 1)/k * V_{CC} and (1/k) * V_{CC}, then substitute ln(2) with ln(k – 1) in the above equations.

As the circuit is provided, k = 3. This assumes R47 = R64. Lowering R65 instead is okay as long as the output impedance of U11 is not significant and the additional current demand is not significant. As an example, if R47, R64 = 50K and R65 = 10K, then the oscillator ranges from 0.142 V_{CC} to (1 – 0.142) V_{CC}. Then k = 1/0.142 = 7. Substitute ln(6) in the above equations.

3.6 High-Current Connections and Structure

The SP6LI Driver Reference Board comes with ceramic capacitors installed opposite the module. It also comes with two 10 µF four-lead film capacitors installed on the side opposite the module. It does not include bus snubbing. Bus snubbing along with the gate drive resistors are left for the customer to define.

Normally with an SP6 module, the DC connection is made from the side opposite the output terminal—J7 and J8 in this case. The gate driver would be built on a fine geometry PCB with a separate high-current PCB for the power circuitry. This PCB is a compromise to demonstrate the module but is not capable of carrying the module's full current.

All five power connectors can carry 150 A RMS with approximately a 20 °C rise in temperature of the PCB. Connectors J7 and J8 are preferred over J4 and J6 because they have a slightly better connection to the module. Testing of the board was done using 2 mm thick copper terminal connected to 4 gauge flat braid wire. The PCB in the area around J5 tends to be the hottest.

The current artwork SP6LI footprint is not an ideal layout for a design that would utilize the full current and voltage capability of the SP6LI module. The gate and source connections should have tape on the PCB to be sure the module gate lead does not short to the PCB source trace. In addition, copper pads should have been placed on the bottom side of the PCB to make a better contact to the module.

In the current design, the Wurth connectors (J4–J8) limit the current more than the module connections. Brass screws with brass washers are supplied with the module for the high-current connections.

The PCB is constructed with 3 oz. outside layers and 4 oz. inside layers. It has a large thermal mass. When reworking the PCB, it is recommended that a PCB pre-heater is used like the AOYUE 866 station.

3.7 Reduced Gate Voltage Operation

In some applications, it may be desirable to reduce the gate drive voltages. The gate drive voltages are controlled by two circuits. The following table describes this relationship.

Table 1 • Reduced Gate Voltage Operation

Parameter	High-side Driver	Low-side Driver
Total voltage 25 V typical	R37, R38, R39	R82, R83, R84
Negative gate drive voltage	D13	D23

Note that resistors set the total voltage (25 V typical). Also, note that the total voltage is set by a boost regulator and the negative gate drive is set by Zener diode regulators.

Example: assume a –3 V/18 V drive is desired. The Zener diodes should be replaced with 3 V Zeners (SZBZ84C3VOLT1G would be a good candidate). In addition, the total drive voltage should be reduced from 25 V to 21 V. This is outside of the adjustment range using R37 and R82, so R39 and R84 should be replaced with a value roughly 4K lower (around 16.5K).

There are two things to be aware of when doing this. The first is that the LT1171 boost regulator input voltage must be below the output voltage in order to maintain regulation. With this change, the nominal input voltage should be considered 11 V instead of 12 V without a change to the transformer. The second thing is that the Zener diode used to set the negative gate drive, like any Zener regulator, can be loaded down by excessive loading. The most common cause of excessive loading is an improperly configured desaturation circuit and a module with gate loading due to a damaged gate structure.

4 Firmware

The default firmware is configured by switches for two modes:

1. The upper and lower drivers act independently. This function allows the drive signal to propagate through immediately. There is no dead time protection.
2. Only one ON (half-bridge mode). With this mode, there is a switch-programmable dead time. Dead time is programmable in 100 ns steps up to 3.1 µs.

A switch selects between a "one-input mode" and a "two-input mode." "One-input mode" makes it unnecessary to program dead time into a source-pulse generator. The use of the FPGA to generate dead time makes it unnecessary to program the dead time into an external generator.

Internal logic is all driven by a 10 MHz clock. Inputs are quantized to the 10 MHz clock in half-bridge mode. The quantization to the clock makes the hold-off logic immune to input noise. However, it means that there will be timing jitter in the signal propagated through the FPGA.

Table 2 • Configuration Switch Settings

Switch	Function
1	Switch On, signal low—2 input mode: pins 1,2 to low side; pins 6,7 to high side Switch Off, signal high—1 input mode (pins 1,2)
2	Switch On, signal low—80 kHz mode Switch Off, signal high—external input mode
3	Switch Off, signal high—one drive only, synchronous mode with dead time Switch On, signal low—independent drive, asynchronous mode
4	Dead time select Switch On, signal low = no delay Switch Off, signal high = 1600 ns
5	Dead time select Switch On, signal low = no delay Switch Off, signal high = 800 ns
6	Dead time select Switch On, signal low = no delay Switch Off, signal high = 400 ns
7	Dead time select Switch On, signal low = no delay Switch Off, signal high = 200 ns
8	Dead time select Switch On, signal low = no delay Switch Off, signal high = 100 ns

The FPGA is a Microsemi Igloo AGL030V2-VQ100. A Microsemi Flashpro 5 or Flashpro 4 programmer can be used to program the device. Other devices have not been tested. The project is in Verilog using Libro SoC. Information on IGLOO FPGAs can be found at http://www.microsemi.com/product-directory/fpgas/1689-igloo.

Switch 1 is closest to the FPGA. Common switch settings are as follows:

Table 3 • Common Switch Settings

Mode	Sw1	Sw2	Sw3	Dead Time
80 kHz demo	Don't care	ON	ON	Yes
2 input	ON	OFF	ON	Yes
1 input on high-side input only	OFF	OFF	ON	Yes
Independent	ON	OFF	OFF	Not App

SiC MOSFETs require very little dead time. Generally, dead time corrects for the delays associated with output switching of gate driver skew (the time it takes to drive the gate) and the recovery of the power device. With SiC MOSFETs, there is no recovery time. In addition, the ADuM4136 is a very low skew driver. A minimum dead time of 100 ns is possible in most applications. This is programmed with SW4 through SW7 ON, SW8 OFF.

4.1 Layout Considerations

This design was done in KiCad. KiCad is not a preferred tool for high-voltage layouts due primarily to limitations with the design rules. This design was done with the following general guidelines.

The gate power supply cores are conductors. Appropriate creepage should be observed around the core on the component side.

The placement of the IXDN630 gate driver and all trace are designed to minimize drive inductance. This includes trace width, multiple feed-throughs, and the placement of all components involved with the nets that carry the high-gate current pulses.

The thermistor is sensed within the environment of the low-side driver. This is to provide isolation from the low-voltage (SELV) environment, but at the same time not place it in the environment of the high-side driver and its associated dV/dt.

The thermistor trace passes over nets that are not subject to the high dV/dt of the high-side driver.

The desaturation detection diodes bridge the plane environments of the two sides of the diodes. This allows the use of series-connected diodes. UIS capable diodes are preferred with series-connected diodes.

The output nets must carry the rated current and have the proper creepage.

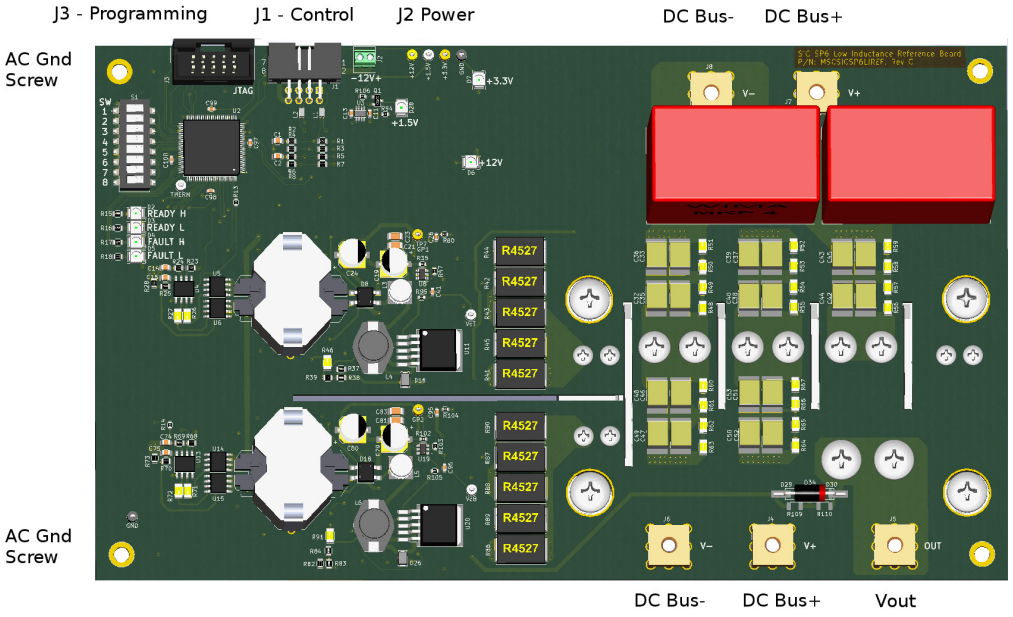
5 IO and Settings

This section describes the IO and settings for the SP6LI driver reference design.

5.1 Connectors

The following image shows the placement of important connectors on the board.

Figure 4 • Connectors



Connector J1 is an eight-pin male header with the following pinout:

Table 4 • J1, Control Connector Pinout

Pin	Signal	Condition
1	Drive high +	True will turn ON the high-side FET. Depending upon switch SW0 it can also control the low side.
2	Drive high –	
3	Reset	A high (3.3 V logic) input asserts reset to the ADuM4135. Pulled down through 10K on the board.
4	Ground	Signal ground. Optionally power ground.
5	Drive low +	Depending upon switch SW0 turns ON the low-side FET
6	Drive low –	
7	Status	Fault output (3.3 V logic with 1K source resistance)
8	Power	12 V input

Connector J2 is an alternate power connector.

Table 5 • J2, Alternate Power Connector Pinout

Pin	Signal
1	12
2	Gnd

Connector J3 is the programming connector. The connector pinout follows that of the Microsemi Flashpro programmers.

5.2 LEDs and Gate-Voltage Adjustments

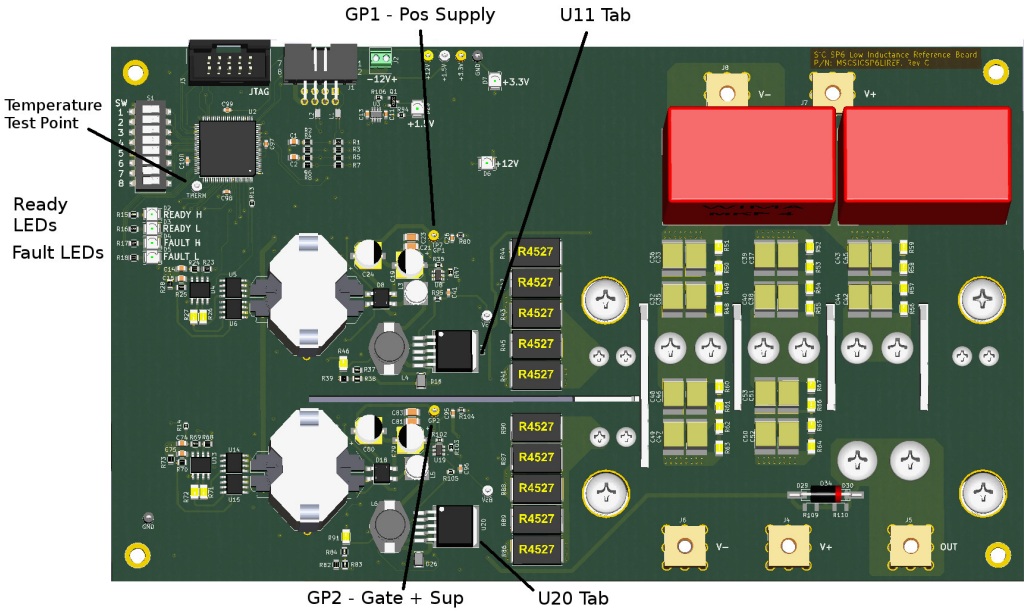
Three power LEDs indicate the presence of 12 V, 3.3 V, and 1.5 V core voltage. Two LEDs labeled “RDY H” and “RDY L” indicate the current status of the ready signal from the two ADuM4136 drivers. Two LEDs labeled "FLT H" and "FLT L" indicate the current status of the fault signal from the ADuM4136 drivers.

The following table shows how the LEDs respond. The status of the high-side interface and low-side interface display separately.

Table 6 • J1, Control Connector Pinout

Ready	Fault	Condition
Off	Off	The secondary side is under voltage.
On	Off	Normal operating state.
On	On	Faulted due to a desaturation condition.

Figure 5 • LEDs and Test Points



The PCB is shipped configured for –5 V, 20 V gate drive. R82 and R37 should be shorted to yield –5 V, 18 V gate drive. Four test points are shown in the above diagram GP1 to U11 tab should measure 25 V when configured for 20 V gate drive and 23 V with 18 V gate drive. U11 tab to the corresponding module source lead should measure 5 V. On the low side test point GP2 and U20 tab have the same role.

It should be noted that the board input voltage should be kept under 13 V. Otherwise, the boost regulators will conduct through and start raising the gate voltage.

5.3 Electrical Characteristics

In the following tables, all voltages are referenced to ground.

Table 7 • Electrical Limits

Description	Min	Typ	Max	Units
Supply voltage, full power	11	12	13	V
Supply current, idle		0.16	0.2	A
Supply current maximum[1]			3.0	A
Maximum slew rate			100	V/ns
Maximum current output			150	A

Note:

1. The driver input power is primarily dissipated in the gate resistors internal and external to the module. In most cases, the power limitations of the gate resistors will limit the module power.

Table 8 • Status Output

Description	Min	Typ	Max	Units
Status output high, status is faulted	3.15	3.3	3.45	V
Status output low, status is OK	0.8			V
Status output impedance high or low	950	1000	1100	Ω

Table 9 • Reset Input

Description	Min	Typ	Max	Units
Reset input low—dis-assert reset	–0.5	0	1.0	V
Reset input high—assert reset	2.5	3.3	3.45	V
Input pull-down resistance	1000	1100	1200	Ω

Table 10 • Digital RS422 Inputs

Description	Min	Typ	Max	Units
Common mode input range	–0.5		5.5	V
Differential voltage threshold		0.050	0.200	V
Differential impedance	84	92	100	Ω
Common mode impedance	240	255	270	Ω
Common mode Thevenin voltage	1.5	1.65	1.8	V

5.4 Board Mounting

The board has two #6 mounting screws. These provide mounting and AC grounding for the controls. The screws are optional but **AC ground should always be used to limit the common mode voltage on the RS422 control interface**. They direct switching currents from the isolation interface to the chassis. Without the screws, the currents are directed through the signal input and power cable. This results in much higher emissions and may interfere with control.

5.5 Quickstart

The basic functionality of the board can be tested without a module or DC bus power. To do this the desaturation protection circuitry must first be disabled using jumpers.

To test the board without a module proceed as follows:

- Set switch 2 and switch 3 ON. This selects 80 kHz self-clocking mode. The dead time switches (4–8) will be in effect.
- Connect the source-to-drain at the high and low side gate drive pins. See Desat Jumper Locations (see page 16) for the location of these jumpers. This is to prevent triggering the desaturation circuitry.
- Apply 11 V–13 V power at J2. The loading should be approximately 0.18 A without FETs. With FETs there is the additional power required for the gates.

The gate drive can then be observed at the module input. The procedure is the same if a module is installed except the jumpers are not needed.

5.5.1 Full Setup with a Module and DC Bus Power

When switching with a module and with DC bus power switching currents are driven from the output devices back into the low voltage signaling environment by capacitive coupling from the high side switch. C8 and C9 are intended to direct these currents back to the DC switching environment and bypass the signal input cable. The following is recommended:

- Mount the board with metal screws on the control side. Their use is highly recommended if control through J1 is used.
- Select the gate resistors as required.
- Set the configuration switches as desired. See Configuration Switch Settings (see page 10).
- Reference section 3.6 (see page 4) for recommendations on connecting power.

It will be assumed as an example here that testing of the low side switch will be done with the high side OFF. The following input connection figures show the recommended setup. By grounding pin 1, the voltage margin on the upper receiver is doubled. This is recommended if a cable is attached on pins 1 and 2 but should not be necessary if there is no connection at J1. Pin 6 is open. The input at pin 5 should cross the threshold at about 3.3 V.

If noise problems are encountered placing capacitors between pins 1 and 2 and between pins 5 to 6 should help. Also placing a common mode choke on the cable will help direct currents through C8 and C9. If a differential pulse generator is used it is still recommended that pin 4 connect to the pulse generator ground in order to control the common mode input voltage range.

Figure 6 • Desat Jumper Locations

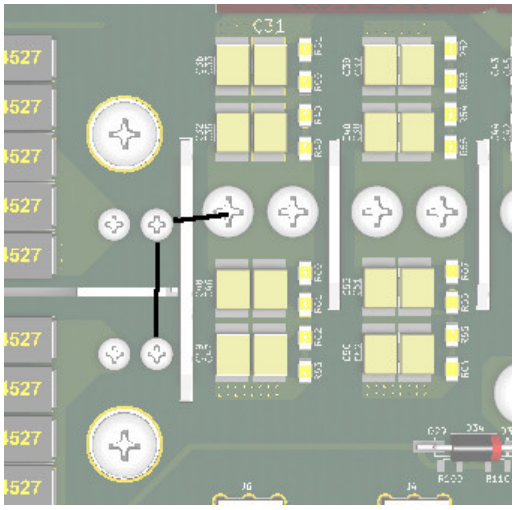


Figure 7 • Singled-ended Input Connection

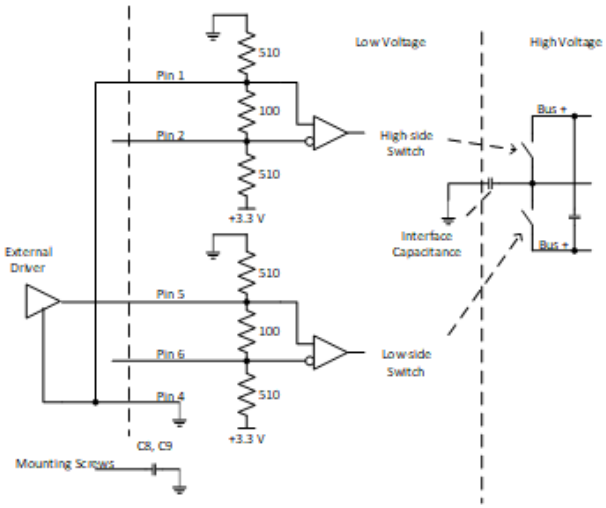
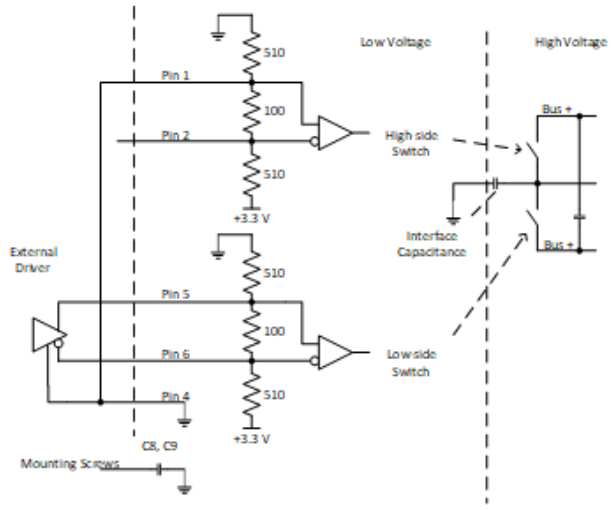


Figure 8 • Differential Input Connection



6 Bill of Materials

The following table shows the bill of materials for the SP6LI driver reference designs.

Table 11 • Bill of Materials

Reference	Man µFacturer	Part number	Description	QTY per board
C10	Wurth Electronics Inc.	865060445005	CAP 100 µF 20% 25 V	1
C11 C86 C93–C94	Samsung Electro-Mechanics America, Inc.	CL10B105KA8NNNC	CAP CER 1 µF 25 V X7R 0603	4
C13	Murata Electronics North America	GRM188R61E225MA12D	CAP CER 2.2 µF 25 V X5R 0603	1
C14 C74	Samsung Electro-Mechanics	CL21C241JBANNNC	CAP CER 240 pF 50 V C0G/NP0 0805	2
C15 C75	TDK Corporation	C2012C0G1E103J060AA	CAP CER 10000 pF 25 V C0G 0805	2
C19 C24 C79–C80	Nichicon	UCM1H101MCL1GS	CAP ALUM 100 µF 20% 50 V SMD	4
C1-C2	Kemet	C0805C101K3GACTU	CAP CER 100 pF 25 V 10% NP0 0805	2
C21 C23 C81 C83	Taiyo Yuden	UMK316BBJ106ML-T	CAP CER 10 µF 50 V X5R 1206	4
C22 C25 C27 C82 C85 C87	Taiyo Yuden	C3225X7S1H106M250AB	CAP CER 10 µF 50 V X7R 1210	6
C29 C31	WIMA	DCP4R251007HD4KYSD	Film Capacitors 10 µF 1300 V 10% 4 LD 24x45.5x41.5PCM 37.5	2
C3	Taiyo Yuden	TMK212BBJ106KG-T	CAP CER 10 µF 25 V X5R 0805	1
C30 C34	Murata Electronics North America	CGA3E2X7R1E104K080AA	CAP CER 0.1 µF 25 V X7R 0603	2
C32–C33 C35–C40 C42–C53	TDK Corporation	CKG57NX7T2J105M500JH	CAP CER 1 µF 630 V X7T SMD	20
C4 C97-C100	Murata Electronics North America	GRM21BR71E104KA01L	CAP CER 0.1 µF 25 V X7R 0805	5
C5	TDK Corporation	CGA3E3X5R1H334K080AB	CAP CER 0.33 µF 50 V X7R 0603	1
C6 C26 C41 C95–C96	KEMET	CL10B103MB8NNNC	CAP CER 10000 pF 50 V X7R 0603	5
C7 C12 C89 C91	Nichicon	UUD1H100MCL1GS	CAP ALUM 10 µF 20% 50 V SMD	4
C8 C9 C18 C20 C28 C78 C84 C88	KEMET	CL21B104KBC5PNL	CAP CER 0.1 µF 50 V X7R 0805	8
C90 C92	Wurth Electronics Inc.	885012209019	CAP CER 0.1 µF 25 V X7R 1210	2
D1	ON Semiconductor	MMBD7000LT1G	DIODE ARRAY GP 100 V 200 mA SOT23	1
D11 D21	Diodes Incorporated	DDZ4V7ASF-7	DIODE ZENER 4.56 V 500 mW SOD323F	2
D12 D22 D29–D30	SMC Diode Solutions	UA1MTR	DIODE SCHOTTKY 1 kV 1 A SMA	4
D13 D23	ON Semiconductor	BZX84C4V7LT1G	DIODE ZENER 4.7 V 225 mW SOT23-3	2
D14–D17 D24–D27	Vishay Semiconductor Diodes Division	SS3P4-M3/84A	DIODE SCHOTTKY 40 V 3 A DO220AA	8
D28	OSRAM Opto Semiconductors Inc.	LY T67K-K2M1-26-Z	LED YELLOW CLEAR 2PLCC SMD	1

Reference	Man µFacturer	Part number	Description	QTY per board
D2–D5	OSRAM Opto Semiconductors Inc.	LG T67K-H2K1-24-Z	LED GREEN CLEAR 2PLCC SMD	4
D6	OSRAM Opto Semiconductors Inc.	LS T67F-T2V2-1-1-Z	LED RED CLEAR 2PLCC SMD	1
D7	OSRAM Opto Semiconductors Inc.	LO T67K-K1L2-24-Z	LED ORANGE CLEAR 2PLCC SMD	1
D8 D18	Comchip Technology	CDBHD240-G	DIODE BRIDGE 2 A 40 V TO-269AA	2
D9–D10 D19–D20 D31–D32	RΩ Semiconductor	RB520CM-60T2R	DIODE SCHOTTKY 60 V 100 mA VMN2M	6
J1	Wurth Electronics Inc.	61200821721	CONN HEADER 8 POS RA 2.54	1
J2	On Shore Technology Inc.	OSTVN02 A150	CONN TERM BLOCK 2.54 mm 2POS PCB	1
J3	On Shore Technology Inc.	302-S101	CONN HEADER VERT 10POS GOLD	1
J4–J8	Wurth Electronics Inc.	74650094R	BUSH, THR OPENM4, THR 3.0 mm	5
L1–L2	TDK Corporation	ACM2012-201-2P-T002	CMC 350 mA 2LN 200 Ω SMD	2
L3 L5	J.W. Miller	PM54-220M-RC	Fixed Inductors 22uH 20%	2
L4 L6	Bourns Inc.	SDR1005-101KL	FIXED IND 100 µH 1 A 330 MΩ SMD	2
PS1	STMicroelectronics	LD1086DT33TR	IC REG LDO 3.3 V 1.5 A DPAK	1
PS2	Texas Instruments	LM3480IM3-3.3/NOPB	IC REG LINEAR 3.3 V 100 mA SOT23-3	1
Q1	ON Semiconductor	BSS138L	MOSFET N-CH 50 V 0.2 A SOT-23	1
R1 R3 R5 R7	Stackpole Electronics Inc.	RMCF0805FT510R	RES SMD 510 Ω 1% 1/8 W 0805	4
R100	Stackpole Electronics Inc.	RNCP0603FTD4K99	RES SMD 4.99 Ω 1% 1/8 W 0603	1
R106	Panasonic Electronic Components	ERJ-3EKF10R0 V	RES SMD 10 Ω 1% 1/10 W 0603	1
R107–R110	RΩ Semiconductor	KTR18EZ pF7874	RES SMD 7.87M Ω 1% 1/4 W 1206	4
R11	Stackpole Electronics Inc.	RMCF0805FT10R0	RES SMD 10 Ω 1% 1/8 W 0805	1
R12	Stackpole Electronics Inc.	RMCF0805JT10K0	RES SMD 10K Ω 5% 1/8 W 0805	1
R13–R14	Stackpole Electronics Inc.	RNCP0603FTD20K0	RES SMD 20K Ω 1% 1/8 W 0603	2
R15–R18	Panasonic Electronic Components	ERJ-6ENF1500 V	RES SMD 150 Ω 1% 1/8 W 0805	4
R19–R20	Stackpole Electronics Inc.	RMCF0603JT1K00	RES SMD 1K Ω 5% 1/10 W 0603	2
R2 R4 R6 R8	Stackpole Electronics Inc.	RMCF0805FT51R0	RES SMD 51 Ω 1% 1/8 W 0805	4
R21	Yageo	RC0603FR-0714K3L	RES SMD 14.3K Ω 1% 1/10 W 0603	1
R22	Panasonic Electronic Components	ERJ-PA3F1500 V	RES SMD 150 Ω 1% 1/4 W 0603	1
R23 R68	Yageo	RC0805JR-07110KL	RES SMD 110K Ω 5% 1/8 W 0805	2
R24 R69	Stackpole Electronics Inc.	RNCP0805FTD180R	RES SMD 180 Ω 1% 1/4 W 080	2
R25 R70	Yageo	RC0805FR-07100RL	RES SMD 100 Ω 1% 1/8 W 0805	2
R26–R27 R30 R71–R72 R75	Stackpole Electronics Inc.	RNCP1206FTD10R0	RES SMD 10 Ω 1% 1/2 W 1206	6

Reference	Man µFacturer	Part number	Description	QTY per board
R28 R73	RΩ Semiconductor	UCR10EVHFLR100	RES 0.1 Ω 1% 1/3W 0805	2
R31 R76	Stackpole Electronics Inc.	RMCF1206FT10K0	RES SMD 10K Ω 1% 1/4 W 1206	2
R32 R77	Stackpole Electronics Inc.	RMCF0805JT220R	RES SMD 220 Ω 5% 1/8 W 0805	2
R33 R78	Stackpole Electronics Inc.	RMCP2010FT47R0	RES SMD 47 Ω 1% 1 W 2010	2
R35 R102	Vishay Dale	RCS0603100KFKEA	RES SMD 100K Ω 1% 1/4 W 0603	2
R36 R81	Stackpole Electronics Inc.	RMCF1206FT4K70	RES SMD 4.7K Ω 1% 1/4 W 1206	2
R38 R83	Yageo	RC0805FR-072KL	RES SMD 2K Ω 1% 1/8 W 0805	2
R39 R84	Panasonic Electronic Components	ERJ-6ENF2152V	RES SMD 21.5K Ω 1% 1/8 W 0805	2
R40-R45 R85-R90	Bourns Inc.	CRM2512-FX-10R0ELF	RES SMD 10 Ω 1% 2 W 2512	12
R46 R91	Stackpole Electronics Inc.	RMCF1206FT1K24	RES SMD 1.24K Ω 1% 1/4 W 1206	2
R47 R103	Panasonic Electronic Components	ERJ-PA3J302V	RES SMD 3K Ω 5% 1/4 W 0603	2
R48–R67	Yageo	RV1206FR-071ML	RES SMD 1M Ω 1% 1/4 W 1206	20
R80 R104	Stackpole Electronics Inc.	RNCP0603FTD100R	RES SMD 100 Ω 1% 1/8 W 0603	2
R94	Panasonic Electronic Components	ERJ-PA3F7500 V	RES SMD 750 Ω 1% 1/4 W 0603	1
R95 R105	Stackpole Electronics Inc.	RNCP0603FTD2K00	RES SMD 2K Ω 1% 1/8 W 0603	2
R96–R98	Stackpole Electronics Inc.	RMCF0603FT10K0	RES SMD 10K Ω 1% 1/10 W 0603	3
R99 R101	Stackpole Electronics Inc.	RMCF0603FT100K	RES SMD 100K Ω 1% 1/10 W 0603	2
R9–R10	Stackpole Electronics Inc.	RMCF0805JT1K00	RES SMD 1K Ω 5% 1/8 W 0805	2
S1	TE Connectivity ALCOSWITCH Switches	4-1825059-1	Dip Switch SPST 8 Position Surface Mount Slide (Standard) Actuator 100 mA 24 VDC	1
TP1 TP5	Keystone Electronics	5001	TEST POINT PC MINI .040D	2
TP2	Keystone Electronics	5004	TEST POINT PC MINI .040D	1
TP3 TP7 TP9	Keystone Electronics	5003	TEST POINT PC MINI .040D	3
TP4 TP6 TP8 TP10	Keystone Electronics	5002	TEST POINT PC MINI .040D	4
U1	Texas Instruments	AM26LV32CDR	IC QUAD DIFF LINE RCVR 16-SOIC	1
U11	Linear Technology	LT1171HVCQ#PBF	IC REG MULT CONFG INV ADJ 5DDPAK	1
U12	Maxim Integrated	MAX9019EKA+T	IC COMPARATOR DUAL SOT23-8	1
U13 U4	Texas Instruments	UCC28089DR	IC REG CTRLR PUSH-PULL 8SOIC	2
U17	Texas Instruments	ISO7810FDW	DGTL ISO 5.7 kV GEN PURP 16SOIC	1
U3	Linear Technology	LT3007ITS8-1.5#TRMPBF	IC REG LDO 1.5 V 20 mA TSOT23-8	1
U5–U6 U14 U15	Fairchild/ON Semiconductor	FDS3512	MOSFET N-CH 80 V 4A 8SOIC	4
U7 U16	Analog Devices Inc.	ADUM4136BRWZ	DGTL ISO 5 kV 1CH GATE DVR 16SOIC	2
U8 U19 U20	Texas Instruments	TPS3710DDCT	SUPERVISORY CIRCUITS WIDE VIN	3
U9 U18	IXYS Integrated Circuits Division	IXDD630MYI	IC GATE DRIVER LOW SIDE TO-263-5	2

Reference	Man µFacturer	Part number	Description	QTY per board
Y1	Epson	SG-636PCE	OSC XO 10.000 MHz CMOS SMD	1
T1 T2	Epcos	B65814N1012D002	Coil Form	2
T1 T2	Epcos	B65813J0000R041	5.5 µH, N41 RM10 Core	2
T1 T2	Epcos	B65814B2203X000	RM10 Core Clip	4
T1 T2	Belden	8077	Approx 4 ft. 22 ga wire	
D29/30 D12/22	Sanken	RP 1HV1	2 kV Fast Recovery Diode	2

7 Schematics

The following illustrations show the schematics of the MSCSICSP6/REF3 device.

Figure 9 • SELV/Control Schematic

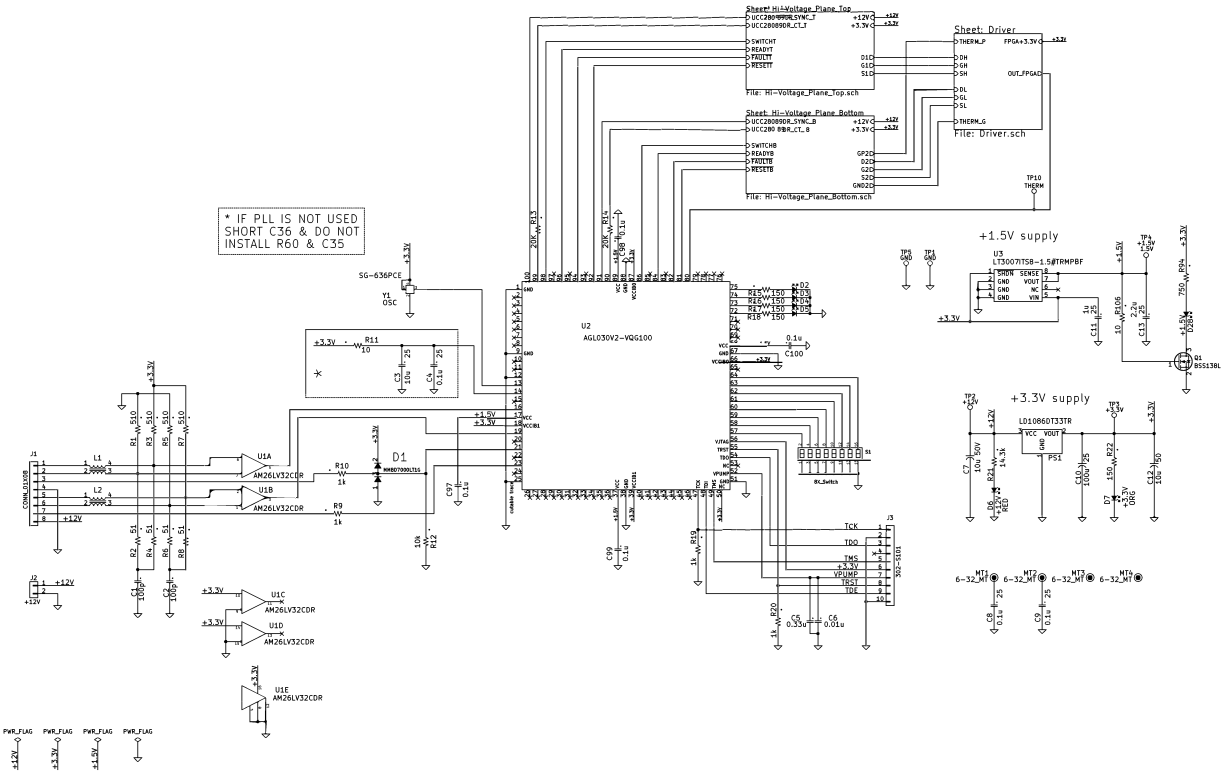


Figure 10 • Bottom-side Driver Schematic

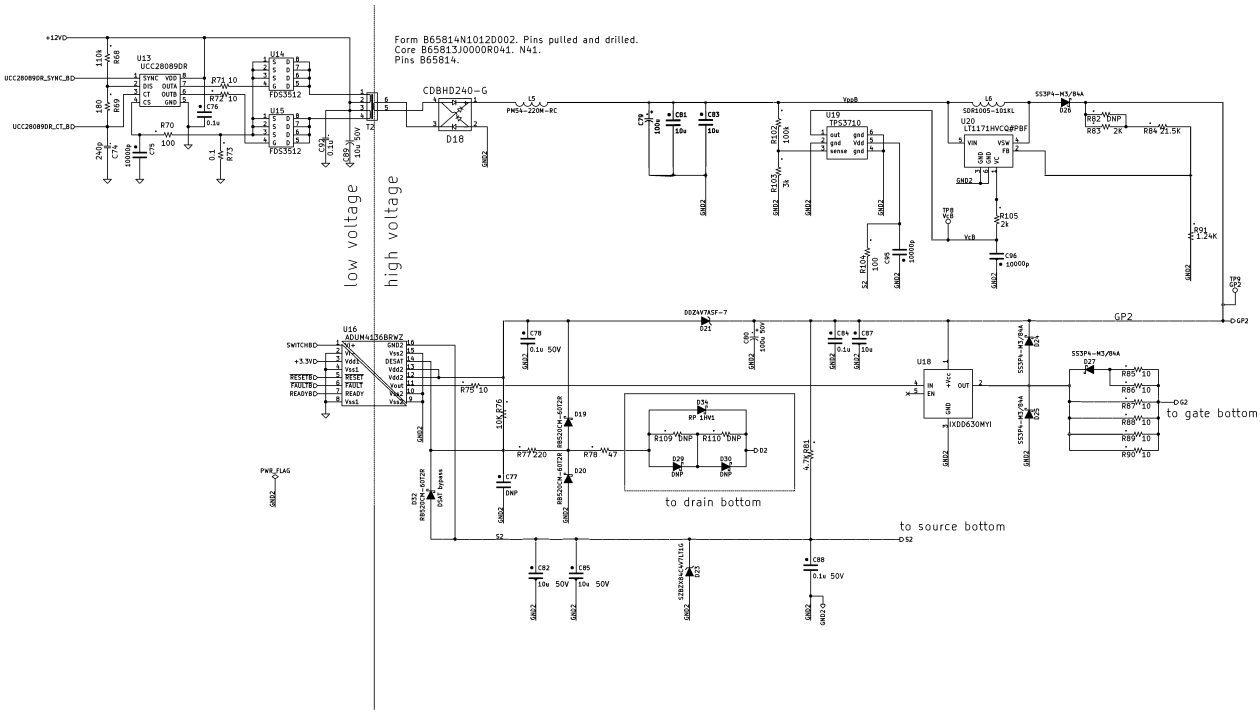


Figure 11 • Power-side and Low-side Thermistor Schematic

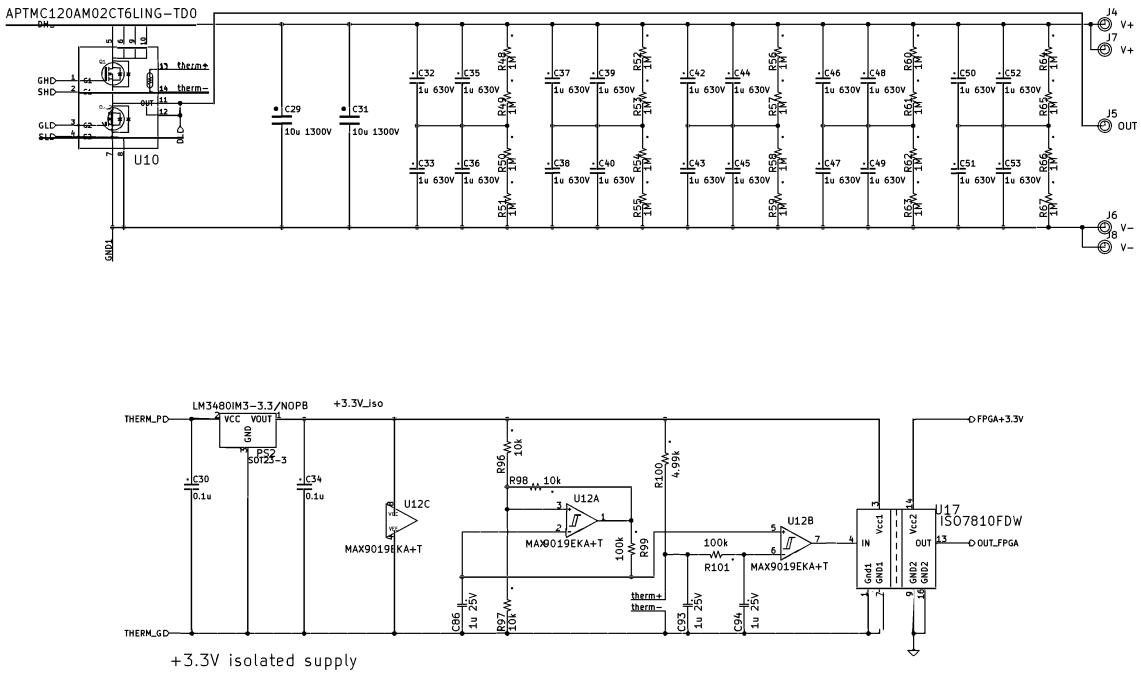
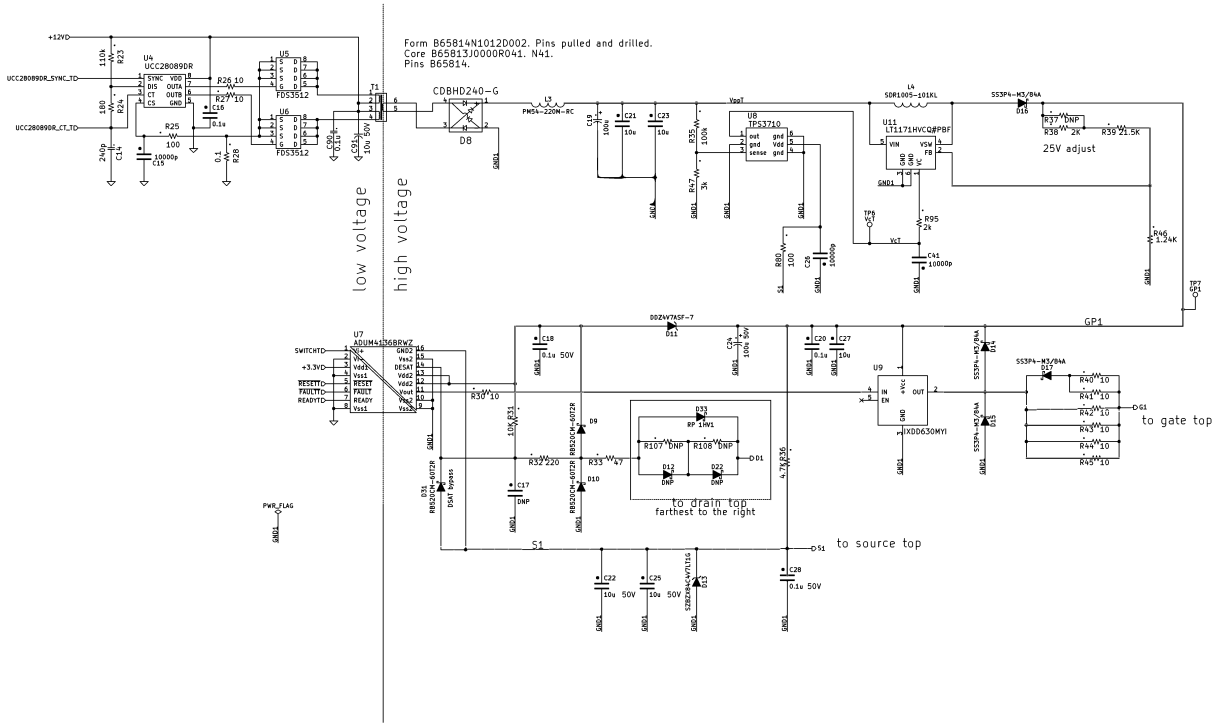


Figure 12 • Top-side Driver Schematic



Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

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