MIC2129

100V, DC-DC Step-Down Controller with Selectable Gate Drive Voltage and Remote Sense

Features

- 4.5V to 100V Wide Input Range
- Adjustable Output Voltage from 0.6V to $D_{MAX} \times V_{IN}$
- 100 kHz to 800 kHz Adjustable Switching Frequency
- Selectable Gate Driver Voltage (5.2V/7.5V/10.5V)
- Output Voltage Remote Sensing
- Precision Enable
- Internal Bootstrap Diode
- Internal Bootstrap LDO
- Selectable Light Load Operating Mode
- Adjustable Soft Start Time
- Adjustable Positive and Negative Current Limit Threshold
- Selectable Current Limit Mode (Hiccup, Latched, Cycle-by-Cycle)
- Output Overvoltage Protection
- Internal Compensation
- ±1% Internal Reference Accuracy from -40°C to +125°C
- Power Good (PG) Output
- -40°C to +125°C Junction Temperature Range
- Available in 24-Lead, VQFN and TSSOP Packages
- AEC-Q100 Qualified (VAO suffix)

Applications

- 48V Telecom and Base Station Power Supplies
- Automotive and Industrial Power Supplies
- Motor Driver Power Supplies
- Battery-Operated Handheld Tools

General Description

The MIC2129 is a wide input voltage range, 4.5V to 100V, Step-down synchronous DC-to-DC controller with Adaptive On-time control architecture. The output voltage is adjustable from 0.6V to $D_{MAX} \times V_{IN}$ with ±1% reference accuracy. The selectable gate driver voltage feature allows customers to use either logic level MOSFETs or standard MOSFETs. The precision enable feature allows the user to turn on the MIC2129 at desired input voltage. Internal bootstrap diode eliminates the need for an external bootstrap diode. Output voltage remote sensing feature improves output voltage regulation by compensating for the voltage drop in ground returns in high current applications.

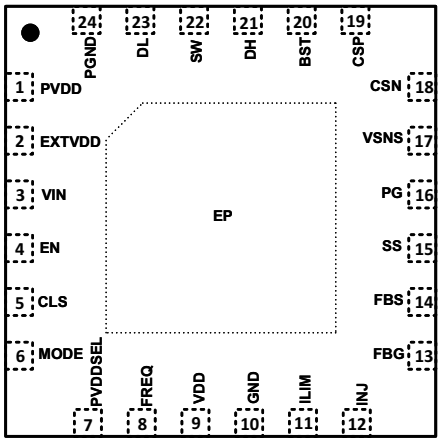
The MIC2129 features adjustable positive and negative current limit thresholds. The MIC2129 senses load current by sensing the voltage across the external low side MOSFET. In applications where a precise current limit is required, customers can use an external precise current sense resistor in series with the external low side MOSFET. The MIC2129 features selectable current limit operation which allows the user to select Hiccup mode, cycle-by-cycle current limit, or Latch-off mode.

The MIC2129 features a bootstrap LDO which supplies the gate driver power from the output of the converter. This improves light load efficiency of the system and reduces the power dissipation in the MIC2129 and hence its temperature rise. The selectable light load operation feature allows the user to select either Continuous Conduction Mode (CCM) or HyperLight Load (HLL) mode. CCM results in almost constant frequency over the entire load current range and HLL mode provides higher efficiency at light loads by reducing the operating switching frequency. The MIC2129 also features adjustable switching frequency from 100 kHz to 800 kHz, adjustable soft start time, and power good output.

Package Type

MIC2129

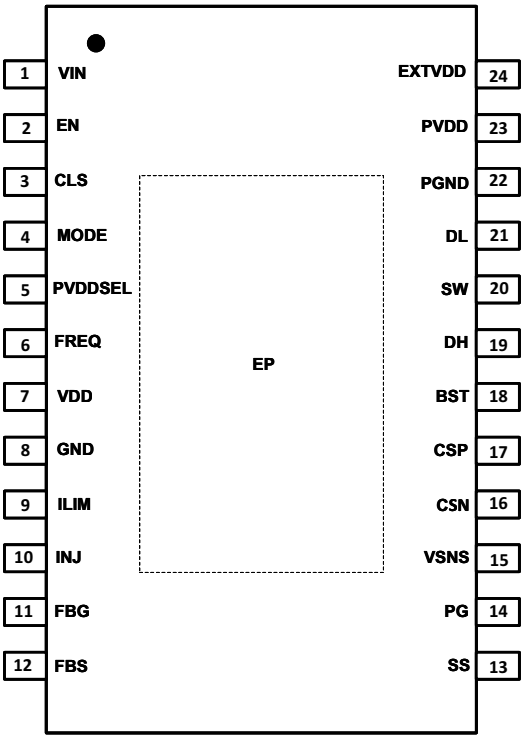
24-Lead 4 mm x 4 mm VQFN*



*Includes Exposed Thermal Pad (EP); see Table 3-1.

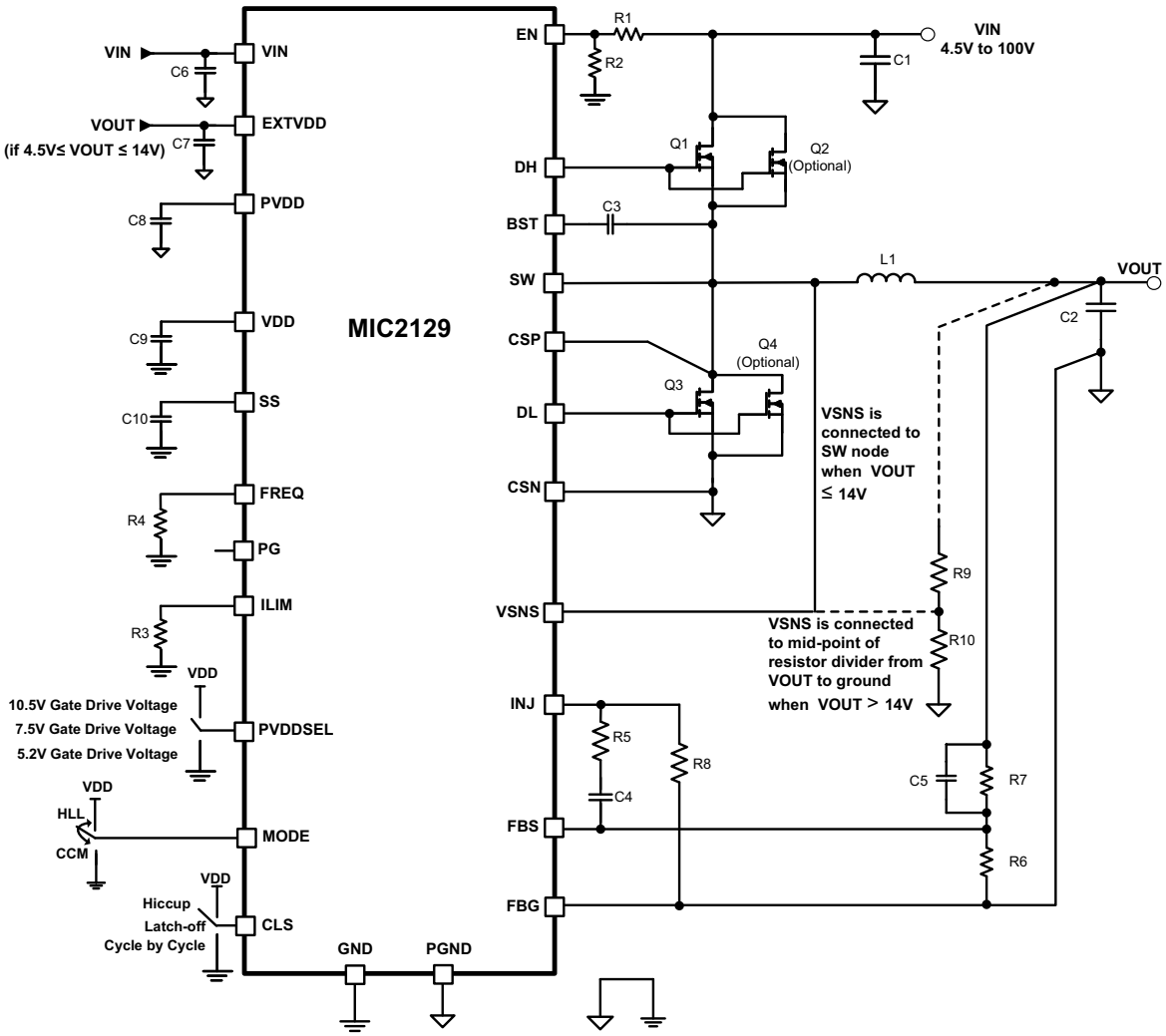
MIC2129

24-Lead 7.8 mm x 6.4 mm, 4.4 Body TSSOP*

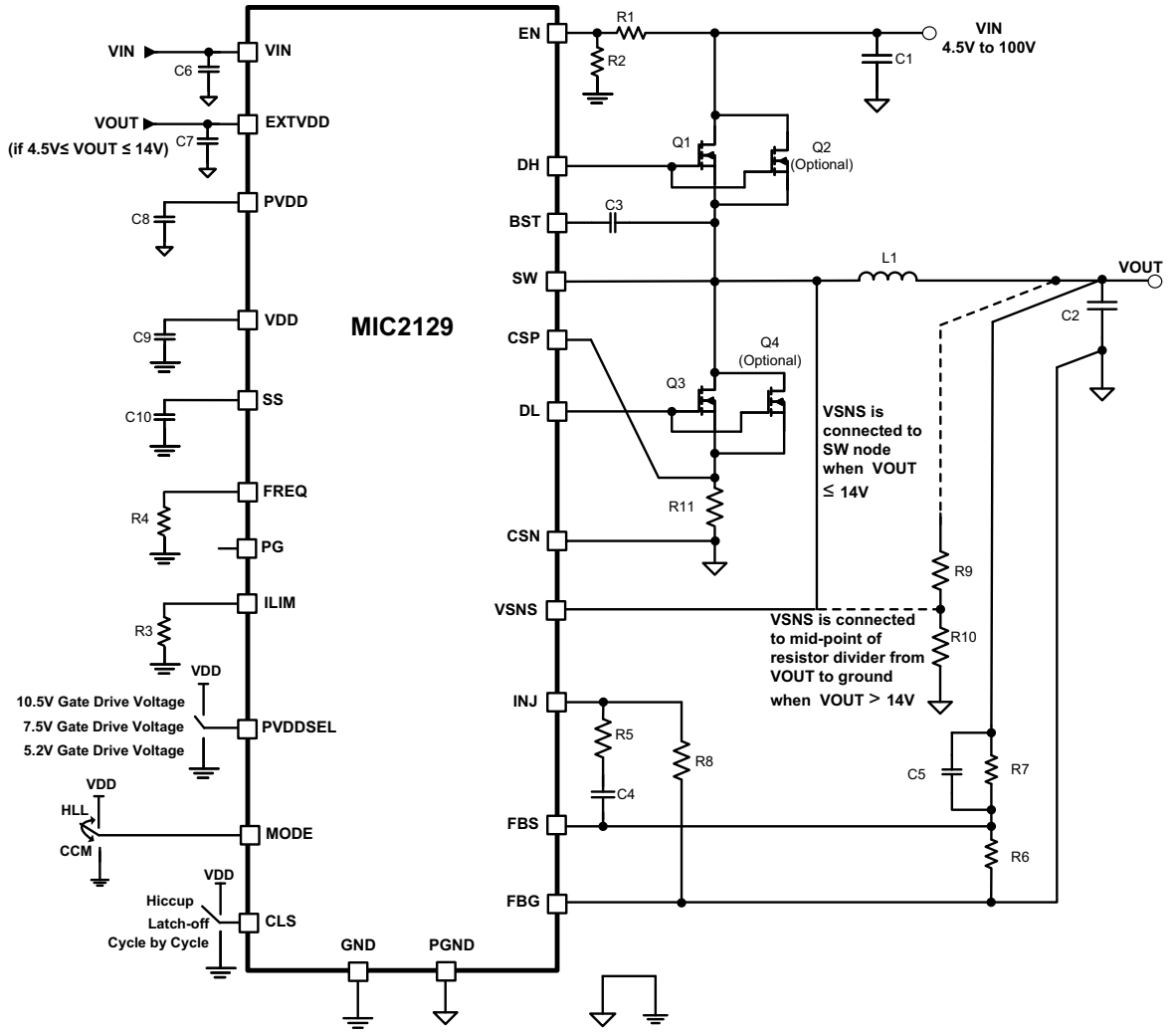


*Includes Exposed Thermal Pad (EP); see Table 3-1.

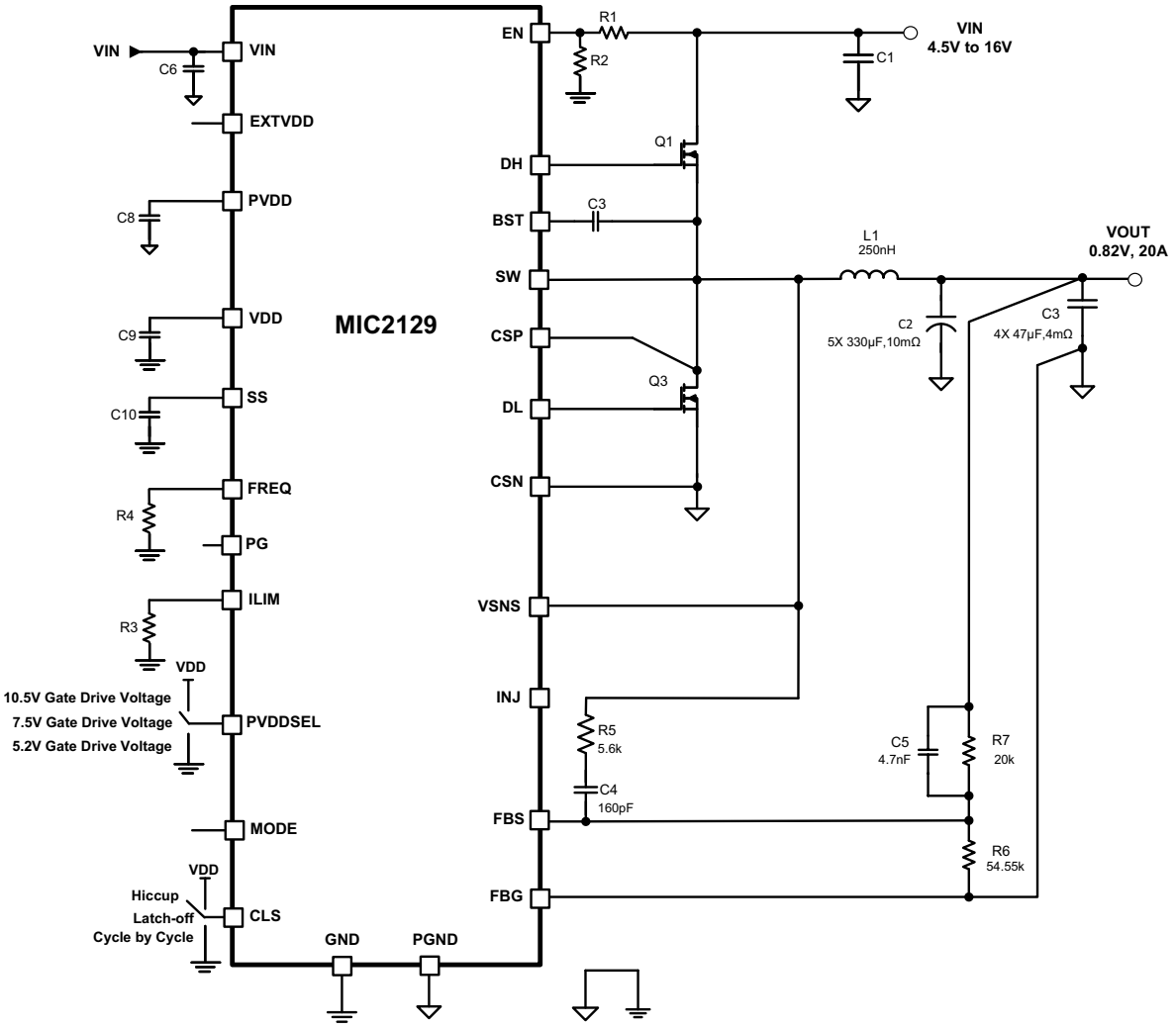
Typical Application Circuits



Typical Application Circuit with FET Sense

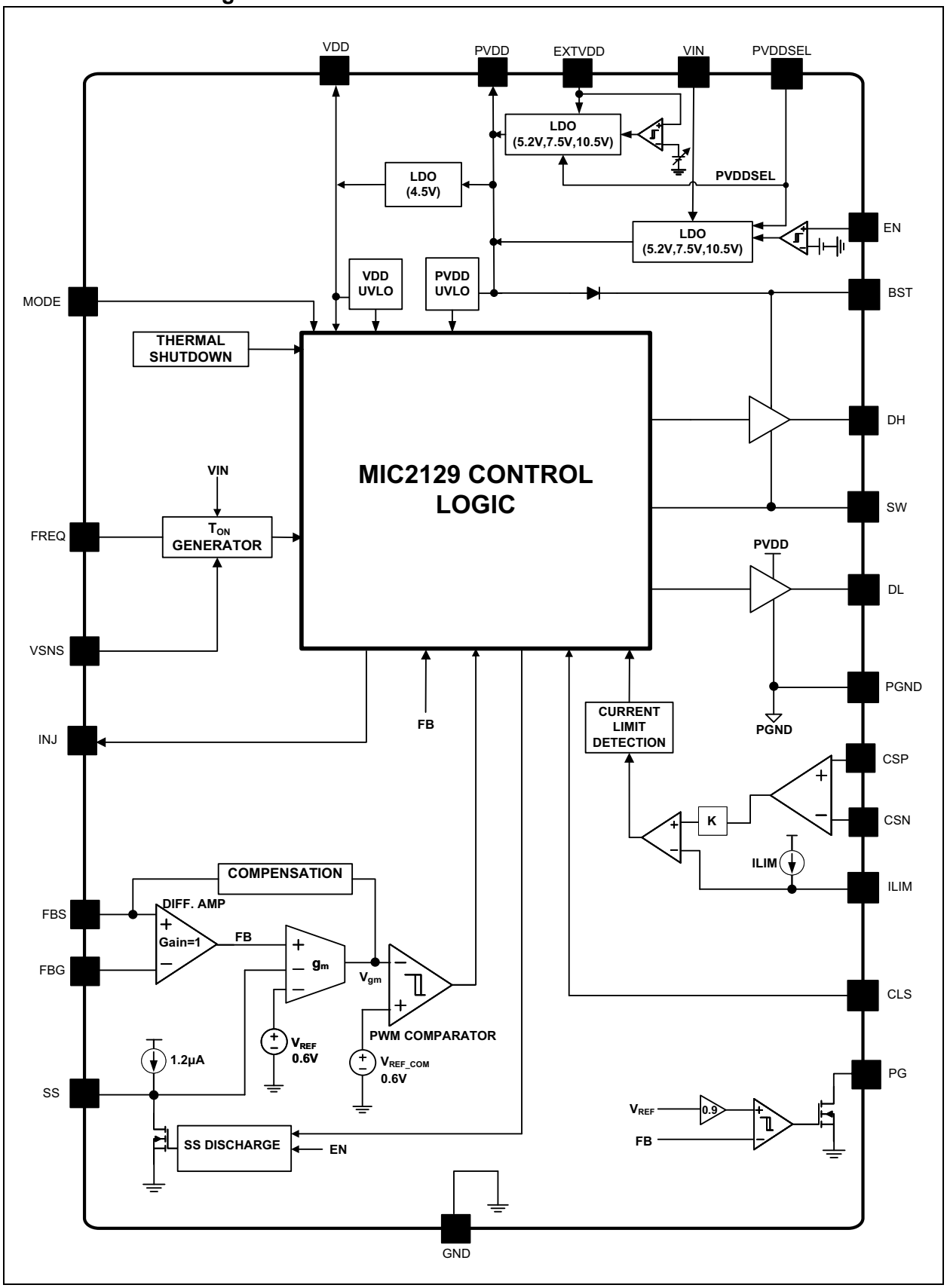


Typical Application Circuit with External Current Sense Resistor



Typical Application Circuit with Ripple Injection Using SW Node

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

V_{IN}, EN to PGND ..... -0.3V to +110V
PV_{DD} to PGND ..... -0.3V to +12V
DH to SW ..... -0.3V to +12V
BST to PVDD ..... -0.3V to +110V
DL to PGND ..... -0.3V to +12V
VDD to GND ..... -0.3V to +6V
BST to SW ..... -0.3V to +12V
SW, CSP, VSNS to PGND ..... -0.3V to (V_{IN} + 0.3V)
FBS, INJ, CLS, PVDDSEL, MODE, FREQ, ILIM, SS, PG to GND ..... -0.3V to (V_{DD} + 0.3V)
EXTVDD to PGND ..... -0.3V to +16V
CSN, FBG, PGND to GND ..... -0.3V to +0.3V
Maximum Junction Temperature (T_J) ..... +150°C
Storage Temperature (T_S) ..... -65°C to +150°C
Lead Temperature (T_{LEAD}) ..... +300°C
ESD Rating(1) (HBM) 1000V
ESD Rating(1) (CDM) 500V

Operating Ratings‡

VIN, EN, VSNS Voltage ..... 4.5V to 100V
EXTVDD Voltage ..... 0V to 14V
Junction Temperature(2) (T_J) ..... -40°C to +125°C

† **Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not guaranteed to function outside its operating ratings.

Note 1: Specification for packaged product only.

2: $P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$, where θ_{JA} depends upon the printed circuit layout.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{IN} = 48V, $V_{BST} - V_{SW} = PV_{DD}$; C_{PVDD} = 4.7 µF, C_{VDD} = 4.7 µF, C_{BST-SW} = 0.1 µF; T_A = +25°C, unless noted. **Bold** values indicate -40°C ≤ T_J ≤ +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Input						
Input Voltage Range	V_{IN}	**4.5**	—	**100**	V	
Quiescent Supply Current in HLL	I_{QVIN_HLL}	—	700	**1000**	µA	MODE = VDD (HLL mode), V_{FBS} = +0.63V, V_{IN} = 48V, No switching
Quiescent Supply Current in CCM	I_{QVIN_CCM}	—	1.5	**2**	mA	MODE = GND (CCM), V_{FBS} = +0.63V, V_{IN} = 48V, No switching
Shutdown Current	I_{SD}	—	15	**25**	µA	V_{IN} = 12V, V_{EN} = 0V
		—	35	**70**	µA	V_{IN} = 100V, V_{EN} = 0V
		—	250	**400**	µA	$V_{IN} = V_{PVDD} = V_{DD}$ = 4.5V, V_{EN} = 0V
PV_{DD} Low Drop-out Regulator (PVDDSEL = GND)						
PV_{DD} Voltage	PV_{DD}	**4.8**	5.2	**5.5**	V	7V ≤ V_{IN} ≤ 60V, V_{EXTVDD} = 0V, PVDDSEL = GND, I_{PVDD} = 25 mA. (**Note 2**), (**Note 3**)
		4.8	5.2	**5.5**	V	60V < V_{IN} ≤ 100V, V_{EXTVDD} = 0V, PVDDSEL = GND, I_{PVDD} = 10 mA. (**Note 2**), (**Note 3**)
		4.8	5.2	**5.5**	V	7V ≤ V_{EXTVDD} ≤ 14V, PVDDSEL = GND, I_{PVDD} = 25 mA.
PV_{DD} Load Regulation	ΔPV_{DD_LD}	**-3**	-2	—	%	V_{IN} = 12V, V_{EXTVDD} = 0V, PVDDSEL = GND, 0 mA ≤ I_{PVDD} ≤ 50 mA
		-1.5	-0.7	—	%	V_{EXTVDD} = 7V, PVDDSEL = GND, 0 mA ≤ I_{PVDD} ≤ 50 mA
PV_{DD} Drop-Out Voltage	V_{DO_PVDD}	—	0.8	**1.3**	V	V_{IN} = 4.8V, V_{EXTVDD} = 0V, PVDDSEL = GND, I_{PVDD} = 25 mA.
		—	0.15	**0.3**	V	V_{EXTVDD} = 4.8V, PVDDSEL = GND, I_{PVDD} = 25 mA.
PV_{DD} UVLO Rising Threshold	V_{PVDDUV_R}	**3.6**	4.1	**4.55**	V	PV_{DD} rising, PVDDSEL = GND
PV_{DD} UVLO Falling Threshold	V_{PVDDUV_F}	**3.4**	3.7	**4.05**	V	PV_{DD} falling, PVDDSEL = GND
EXTVDD Rising Threshold	V_{THR_EVDD}	**4.4**	4.6	**4.85**	V	V_{EXTVDD} rising, PVDDSEL = GND
EXTVDD Falling Threshold	V_{THF_EVDD}	**4.2**	4.4	**4.6**	V	V_{EXTVDD} falling, PVDDSEL = GND

Note 1: Guaranteed by design and characterization. Not production tested.

2: Tested in pulse test mode because of higher power dissipation in the device at higher input voltage.

3: Limited by maximum junction temperature T_J = +125°C.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{IN} = 48V, $V_{BST} - V_{SW} = PV_{DD}$; C_{PVDD} = 4.7 µF, C_{VDD} = 4.7 µF, C_{BST-SW} = 0.1 µF; T_A = +25°C, unless noted. **Bold** values indicate -40°C ≤ T_J ≤ +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
PV_{DD} Low Drop-out Regulator (PVDDSEL = FLOAT)						
PV_{DD} Voltage	PV_{DD}	**7.0**	7.5	**8.0**	V	10V ≤ V_{IN} ≤ 60V, V_{EXTVDD} = 0V, PVDDSEL = Float, I_{PVDD} = 25 mA. (**Note 2**), (**Note 3**)
		7.0	7.5	**8.0**	V	60V < V_{IN} ≤ 100V, V_{EXTVDD} = 0V, PVDDSEL = Float, I_{PVDD} = 10 mA. (**Note 2**), (**Note 3**)
		7.0	7.5	**8.0**	V	10V ≤ V_{EXTVDD} ≤ 14V, PVDDSEL = Float, I_{PVDD} = 25 mA.
PV_{DD} Load Regulation	ΔPV_{DD_LD}	**-2.35**	-1.6	—	%	V_{IN} = 12V, V_{EXTVDD} = 0V, PVDDSEL = Float, 0 mA ≤ I_{PVDD} ≤ 50 mA
		-1.15	-0.7	—	%	V_{EXTVDD} = 10V, PVDDSEL = Float, 0 mA ≤ I_{PVDD} ≤ 50 mA
PV_{DD} Drop-Out Voltage	V_{DO_PVDD}	—	0.7	**1.2**	V	V_{IN} = 7V, V_{EXTVDD} = 0V, PVDDSEL = Float, I_{PVDD} = 25 mA.
		—	0.2	**0.35**	V	V_{EXTVDD} = 7V, PVDDSEL = Float, I_{PVDD} = 25 mA.
PV_{DD} UVLO Rising Threshold	V_{PVDDUV_R}	**5.6**	6.3	**6.95**	V	PV_{DD} rising, PVDDSEL = Float
PV_{DD} UVLO Falling Threshold	V_{PVDDUV_F}	**4.8**	5.4	**5.95**	V	PV_{DD} falling, PVDDSEL = Float
EXTVDD Rising Threshold	V_{THR_EVDD}	**6.3**	6.7	**7.2**	V	V_{EXTVDD} rising, PVDDSEL = Float
EXTVDD Falling Threshold	V_{THF_EVDD}	**6**	6.4	**6.8**	V	V_{EXTVDD} falling, PVDDSEL = Float
PV_{DD} Low Drop-out Regulator (PVDDSEL = VDD)						
PV_{DD} Voltage	PV_{DD}	**9.8**	10.6	**11**	V	12V ≤ V_{IN} ≤ 60V, V_{EXTVDD} = 0V, PVDDSEL = VDD, I_{PVDD} = 25 mA. (**Note 2**), (**Note 3**)
		9.8	10.6	**11**	V	60V < V_{IN} ≤ 100V, V_{EXTVDD} = 0V, PVDDSEL = VDD, I_{PVDD} = 10 mA. (**Note 2**), (**Note 3**)
		9.8	10.6	**11**	V	12V ≤ V_{EXTVDD} ≤ 14V, PVDDSEL = VDD, I_{PVDD} = 25 mA.
PV_{DD} Load Regulation	ΔPV_{DD_LD}	—	-2.1	—	%	V_{IN} = 12V, V_{EXTVDD} = 0V, PVDDSEL = VDD, 0 mA ≤ I_{PVDD} ≤ 50 mA
		-1.15	-0.7	**-0.5**	%	V_{EXTVDD} = 12V, PVDDSEL = VDD, 0 mA ≤ I_{PVDD} ≤ 50 mA

Note 1: Guaranteed by design and characterization. Not production tested.

2: Tested in pulse test mode because of higher power dissipation in the device at higher input voltage.

3: Limited by maximum junction temperature T_J = +125°C.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{IN} = 48V, $V_{BST} – V_{SW} = PV_{DD}$; C_{PVDD} = 4.7 µF, C_{VDD} = 4.7 µF, C_{BST-SW} = 0.1 µF; T_A = +25°C, unless noted. **Bold** values indicate -40°C ≤ T_J ≤ +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
PV_{DD} Drop-Out Voltage	V_{DO_PVDD}	—	0.7	**1.2**	V	V_{IN} = 9.8V, V_{EXTVDD} = 0V, PVDDSEL = VDD, I_{PVDD} = 25 mA.
		—	0.2	**0.3**	V	V_{EXTVDD} = 9.8V, PVDDSEL = VDD, I_{PVDD} = 25 mA.
PV_{DD} UVLO Rising Threshold	V_{PVDDUV_R}	**7.2**	7.9	**8.65**	V	PV_{DD} rising, PVDDSEL = VDD
PV_{DD} UVLO Falling Threshold	V_{PVDDUV_F}	**6.15**	6.8	**7.45**	V	PV_{DD} falling, PVDDSEL = VDD
EXTVDD Rising Threshold	V_{THR_EVDD}	**9**	9.2	**9.4**	V	V_{EXTVDD} rising, PVDDSEL = VDD
EXTVDD Falling Threshold	V_{THF_EVDD}	**8.2**	8.8	**9**	V	V_{EXTVDD} falling, PVDDSEL = VDD
V_{DD} Low Drop-out Regulator						
V_{DD} Voltage	V_{DD}	**4.2**	4.5	**4.8**	V	No external load on VDD
V_{DD} UVLO Rising Threshold	V_{VDDUV_R}	**3.55**	3.9	**4.2**	V	V_{DD} rising
V_{DD} UVLO Falling Threshold	V_{VDDUV_F}	**3.35**	3.7	**4.0**	V	V_{DD} falling
Reference and Remote Sense Amplifier						
Feedback Voltage	$V_{FBS-FBG}$	596	600	603	mV	T_J = 25°C
		594	600	**606**	mV	-40°C ≤ T_J ≤ +125°C
FBS Bias Current	I_{FBS}	**-1**	2	**10**	nA	V_{FBS} = 0.6V, V_{FBG} = 0V
FBG Bias Current	I_{FBG}	**7.5**	11	**13.6**	µA	V_{FBG} = 0V
Enable						
Enable Upper Threshold Voltage	V_{EN_THR}	**1.06**	1.2	**1.34**	V	Enable voltage rising
Enable Hysteresis	V_{EN_HYS}	**29**	54	**82**	mV	
Enable Bias Current	I_{EN}	—	100	—	nA	V_{EN} = 12V
		—	700	—	nA	V_{EN} = 100V

Note 1: Guaranteed by design and characterization. Not production tested.

2: Tested in pulse test mode because of higher power dissipation in the device at higher input voltage.

3: Limited by maximum junction temperature T_J = +125°C.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{IN} = 48V, $V_{BST} - V_{SW} = PV_{DD}$; C_{PVDD} = 4.7 µF, C_{VDD} = 4.7 µF, C_{BST-SW} = 0.1 µF; T_A = +25°C, unless noted. **Bold** values indicate -40°C ≤ T_J ≤ +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
On Timer						
On Time	T_{ON1}	**780**	833	**882**	ns	V_{IN} = 48V, R_{FREQ} = 68.1 kΩ, V_{VSNS} = 12V, f_{SW} = 300 kHz
	T_{ON2}	—	380	—	ns	V_{IN} = 48V, R_{FREQ} = 68.1 kΩ, V_{VSNS} = 5V, f_{SW} = 300 kHz
	T_{ON3}	—	2400	—	ns	V_{IN} = 48V, R_{FREQ} = 200 kΩ, V_{VSNS} = 12V, f_{SW} = 100 kHz
	T_{ON4}	—	347	—	ns	V_{IN} = 12V, R_{FREQ} = 25.5 kΩ, V_{VSNS} = 3V, f_{SW} = 800 kHz
Minimum Controllable ON Time	$T_{ON(MIN)}$	—	120	**175**	ns	V_{VSNS} = 0V
Minimum OFF Time	$T_{OFF(MIN)}$	—	366	**440**	ns	$V_{VSNS} = V_{SW}$, $V_{FBS} = V_{FBG}$ = 0V
Break Before Make Time	$t_{BBM(ON)}$	—	50	—	ns	DL OFF to DH ON (time from DL falling below 1V to beginning of DH rise), (**Note 1**)
	$t_{BBM(OFF)}$	—	50	—	ns	DH OFF to DL ON (time from SW falling below 1V to beginning of DL rise), (**Note 1**)
Ripple Injection Driver						
INJ Signal High Period	t_{ON_INJ}	—	100	**118**	ns	
Ripple Injection Pre-position Current Source	I_{BIAS}	**4.35**	4.9	**5.55**	µA	Force V_{INJ} = 0V, V_{SS} = 0V, measure current
Injection Driver ON Resistance	R_{ON_INJ}	—	50	—	Ω	
Soft Start						
Soft Start Current Source	I_{SS}	**1**	1.2	**1.4**	µA	
Current Limit (ILIM)						
ILIM Current Source (ZTC)	I_{ILIM}	**8.7**	9.6	**10.35**	µA	ZTC, Measurement is Limited by ATE
ILIM Current Source (PTC)		15	19.2	24	µA	PTC at T_J = 25°C, Measurement is Limited by ATE
Current Limit Threshold	V_{TH_ILIM}	**65**	73	**79**	mV	R_{ILIM} = 30.9 kΩ, ZTC
		65	73	79	mV	R_{ILIM} = 15.45 kΩ, PTC
ILIM Current Source Tempco (PTC)	PTC_{ILIM}	—	5100	—	ppm/°C	If CSP is high while SW is high, (**Note 1**)
ILIM Current Source Tempco (ZTC)	ZTC_{ILIM}	—	0	—	ppm/°C	If CSP is low while SW is high, (**Note 1**)

Note 1: Guaranteed by design and characterization. Not production tested.

2: Tested in pulse test mode because of higher power dissipation in the device at higher input voltage.

3: Limited by maximum junction temperature T_J = +125°C.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{IN} = 48V, $V_{BST} - V_{SW} = PV_{DD}$; C_{PVDD} = 4.7 µF, C_{VDD} = 4.7 µF, C_{BST-SW} = 0.1 µF; T_A = +25°C, unless noted. **Bold** values indicate -40°C ≤ T_J ≤ +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Negative Current Limit						
Negative Current Limit Threshold	$V_{TH\_ILIMNEG}$	—	34	—	mV	MODE=GND, ZTC, R_{ILIM} = 30.9 kΩ
		—	34	—	mV	MODE=GND, PTC, R_{ILIM} = 15.45 kΩ
Zero Crossing Detection Comparator						
Zero Crossing Detection Comparator Threshold	V_{TH_ZX}	**-8.53**	-3	**2.31**	mV	
MODE, PVDDSEL, CLS						
Logic Low Threshold	$V_{THL\_MODE,PVS,CLS}$	—	—	1	V	
Logic High Threshold	$V_{THH\_MODE,PVS,CLS}$	V_{DD}–1.1	—	—	V	
Bootstrap Diode						
Bootstrap Diode Forward Dynamic On-Resistance	R_{ON_SDBST}	**3**	5.6	**8**	Ω	$\Delta V_F/\Delta I_F$, I_F = 10mA to 20mA
Bootstrap Diode Forward Voltage Drop	V_{F_SDBST}	**0.3**	0.52	**0.66**	V	I_F = 10 mA
		0.36	0.58	**0.7**	V	I_F = 20 mA
GATE Drivers						
DH Pull-high Resistance	$R_{DH(H)\_5.2V}$	**2.5**	4.3	**6.0**	Ω	PVDDSEL = GND, I_{SOURCE} = 20 mA
DH Pull-low Resistance	$R_{DH(L)\_5.2V}$	**0.8**	1.7	**2.3**	Ω	PVDDSEL = GND, I_{SINK} = 20 mA
DL Pull-high Resistance	$R_{DL(H)\_5.2V}$	**2.3**	4	**5.9**	Ω	PVDDSEL = GND, I_{SOURCE} = 20 mA
DL Pull-low Resistance	$R_{DL(L)\_5.2V}$	**0.8**	1.75	**2.25**	Ω	PVDDSEL = GND, I_{SINK} = 20 mA
DH Pull-high Resistance	$R_{DH(H)\_7.5V}$	**2**	3.2	**4.6**	Ω	PVDDSEL = Float, I_{SOURCE} = 20 mA
DH Pull-low Resistance	$R_{DH(L)\_7.5V}$	**0.7**	1.4	**1.85**	Ω	PVDDSEL = Float, I_{SINK} = 20 mA
DL Pull-high Resistance	$R_{DL(H)\_7.5V}$	**1.9**	3.3	**4.6**	Ω	PVDDSEL = Float, I_{SOURCE} = 20 mA
DL Pull-low Resistance	$R_{DL(L)\_7.5V}$	**0.65**	1.4	**1.8**	Ω	PVDDSEL = Float, I_{SINK} = 20 mA
DH Pull-high Resistance	$R_{DH(H)\_10.5V}$	**1.6**	2.6	**3.7**	Ω	PVDDSEL = VDD, I_{SOURCE} = 20 mA
DH Pull-low Resistance	$R_{DH(L)\_10.5V}$	**0.59**	1.1	**1.5**	Ω	PVDDSEL = VDD, I_{SINK} = 20 mA
DL Pull-high Resistance	$R_{DL(H)\_10.5V}$	**1.6**	2.7	**3.75**	Ω	PVDDSEL = VDD, I_{SOURCE} = 20 mA

Note 1: Guaranteed by design and characterization. Not production tested.

2: Tested in pulse test mode because of higher power dissipation in the device at higher input voltage.

3: Limited by maximum junction temperature T_J = +125°C.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{IN} = 48V, $V_{BST} - V_{SW} = PV_{DD}$; C_{PVDD} = 4.7 µF, C_{VDD} = 4.7 µF, C_{BST-SW} = 0.1 µF; T_A = +25°C, unless noted. **Bold** values indicate -40°C ≤ T_J ≤ +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
DL Pull-low Resistance	$R_{DL(L)\_10.5V}$	**0.58**	1.0	**1.5**	Ω	PVDDSEL = VDD, I_{SINK} = 20 mA
DH Rise Time	t_{R_DH}	—	25	—	ns	PVDDSEL = VDD, C_{DH-SW} = 3300 pF, (**Note 1**)
DH Fall Time	t_{F_DH}	—	15	—	ns	
DL Rise Time	t_{R_DL}	—	25	—	ns	PVDDSEL = VDD, C_{DL} = 3300 pF, (**Note 1**)
DL Fall Time	t_{F_DL}	—	15	—	ns	
SW, BST and VIN Leakage Current						
VIN Leakage	I_{LKG_VIN}	—	—	**70**	µA	V_{IN} = 100V
BST Leakage	I_{LKG_BST}	—	—	**35**	µA	V_{BST} = 112V, V_{PVDD} = 12V
SW Leakage	I_{LKG_SW}	—	—	**1**	µA	V_{IN} = 100V
Power Good (PG)						
PG Rising Threshold	$V_{TH\_PG\_RISE}$	**83**	90	**95**	$\%V_{REF}$	Voltage at FBS rising
PG Hysteresis	$V_{TH\_PG\_HYS}$	—	7	—	$\%V_{REF}$	
PG Delay Time	$t_{D\_PG\_RISE}$	**80**	110	**138**	µs	Voltage at FBS rising
	$t_{D\_PG\_FALL}$	**84**	110	**126**	µs	Voltage at FBS falling
PG Low Voltage	$V_{PG(LOW)}$	—	—	**200**	mV	1 mA into PG pin
Output Over Voltage Protection (OVP)						
OVP Rising Threshold	V_{TH_OVP}	**107**	112	**118**	$\%V_{REF}$	
OVP Delay Time	t_{D_OVP}	**11**	18	**24**	µs	
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}	—	155	—	°C	T_J Rising, (**Note 1**)
Thermal Shutdown Hysteresis	T_{SD_HYS}	—	15	—	°C	**Note 1**

Note 1: Guaranteed by design and characterization. Not production tested.

2: Tested in pulse test mode because of higher power dissipation in the device at higher input voltage.

3: Limited by maximum junction temperature T_J = +125°C.

TEMPERATURE SPECIFICATIONS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Junction Temperature Range	T_J	-40	—	+125	°C	**Note 1**
Absolute Maximum Junction Temperature	$T_{J(ABSMAX)}$	—	—	+150	°C	
Storage Temperature Range	T_S	-65	—	+150	°C	
Lead Temperature	T_{LEAD}	—	—	+300	°C	Soldering, 10s
Package Thermal Resistance						
Thermal Resistance, 4 mm x 4 mm, 24-Lead VQFN	θ_{JA}	—	43	—	°C/W	Junction to Ambient
Thermal Resistance, 7.8 mm x 6.4 mm 4.4 mm Body, 24-Lead TSSOP	θ_{JA}	—	35	—	°C/W	Junction to Ambient

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

Note: Unless otherwise indicated, V_{IN} = 48V; $V_{BST} – V_{SW} = PV_{DD}$ = 10.5V; f_{SW} = 200 kHz; T_A = +25°C.

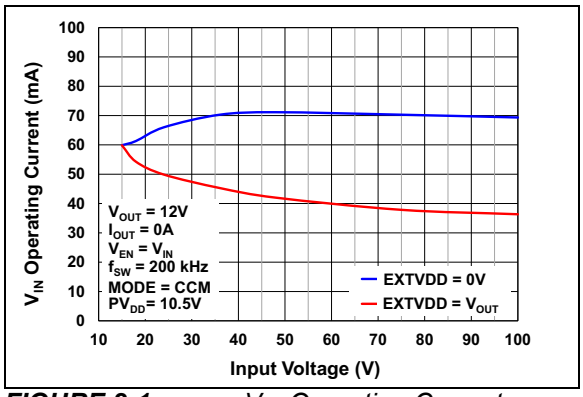


FIGURE 2-1: *V_{IN} Operating Current vs. Input Voltage (CCM).*

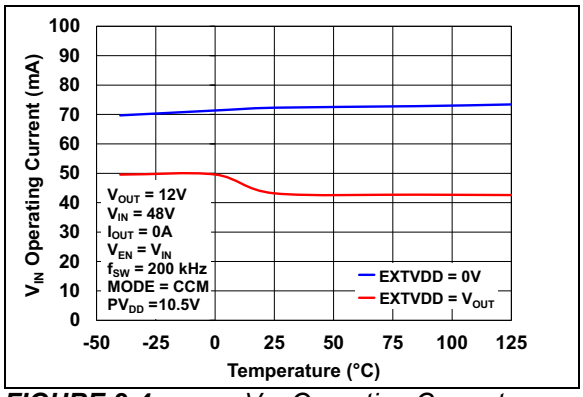


FIGURE 2-4: *V_{IN} Operating Current vs. Temperature (CCM).*

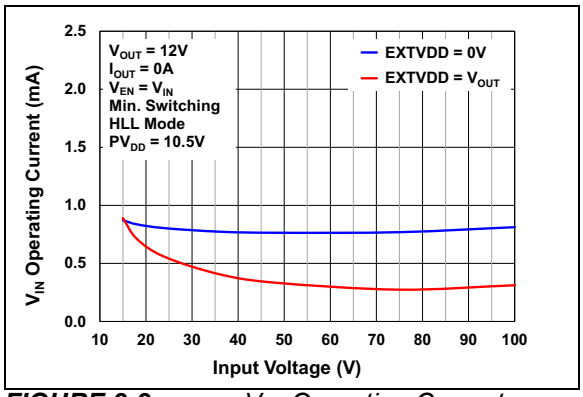


FIGURE 2-2: *V_{IN} Operating Current vs. Input Voltage (HLL Mode).*

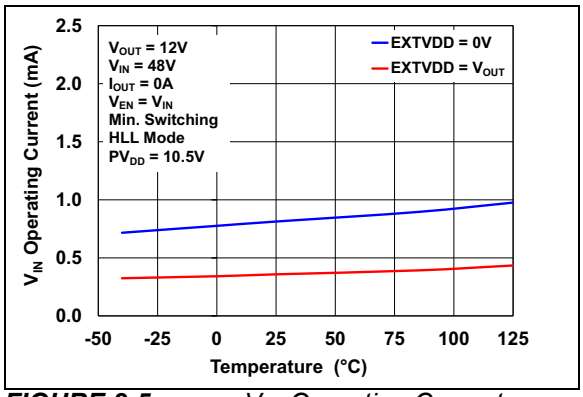


FIGURE 2-5: *V_{IN} Operating Current vs. Temperature (HLL Mode).*

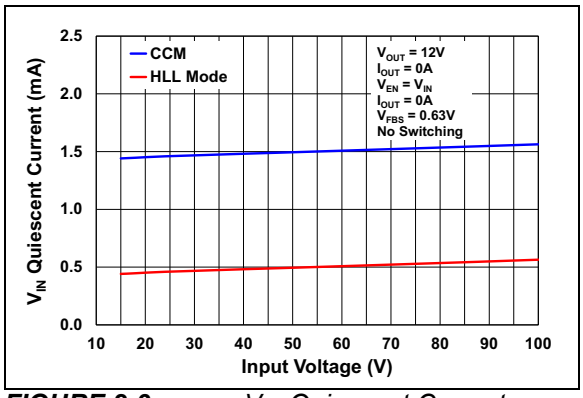


FIGURE 2-3: *V_{IN} Quiescent Current vs. Input Voltage.*

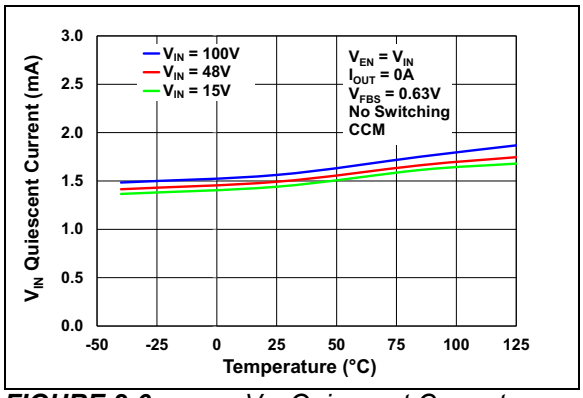


FIGURE 2-6: *V_{IN} Quiescent Current vs. Temperature.*

Note: Unless otherwise indicated, V_{IN} = 48V; $V_{BST} - V_{SW} = PV_{DD}$ = 10.5V; f_{SW} = 200 kHz; T_A = +25°C.

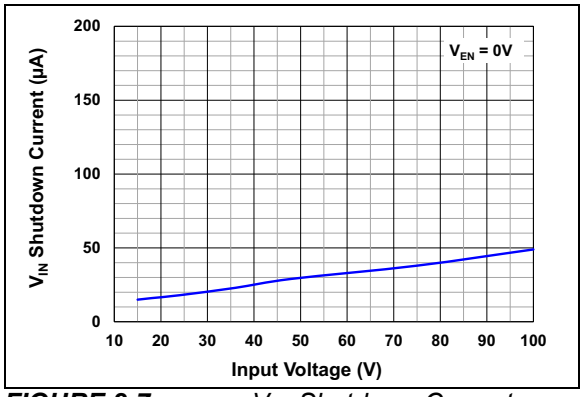


FIGURE 2-7: *V_{IN} Shutdown Current vs. Input Voltage.*

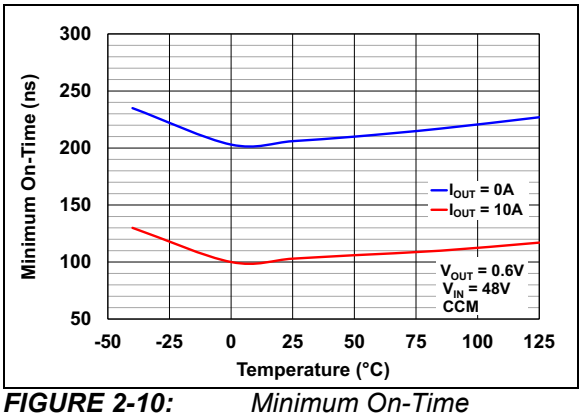


FIGURE 2-10: *Minimum On-Time ($T_{ON(MIN)}$) vs. Temperature.*

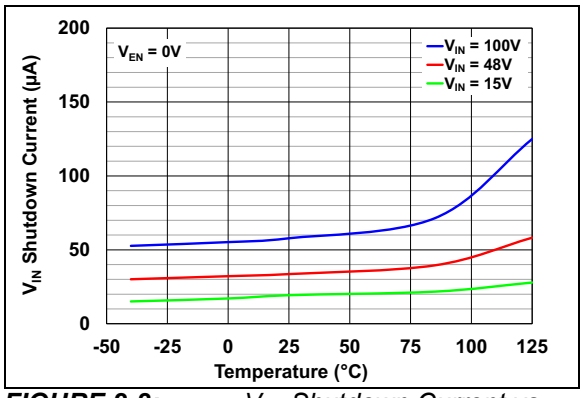


FIGURE 2-8: *V_{IN} Shutdown Current vs. Temperature.*

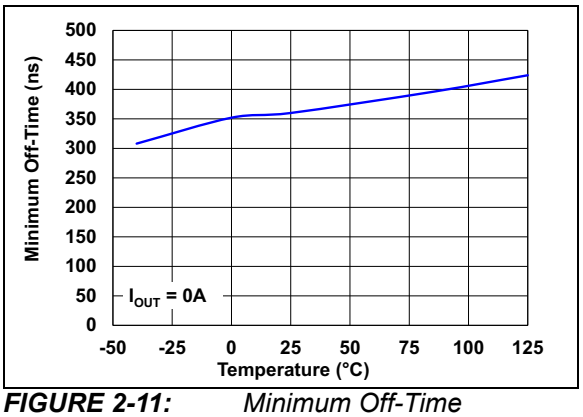


FIGURE 2-11: *Minimum Off-Time ($T_{OFF(MIN)}$) vs. Temperature.*

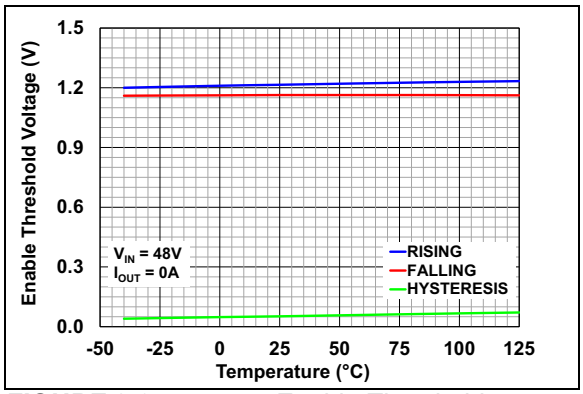


FIGURE 2-9: *Enable Threshold vs. Temperature.*

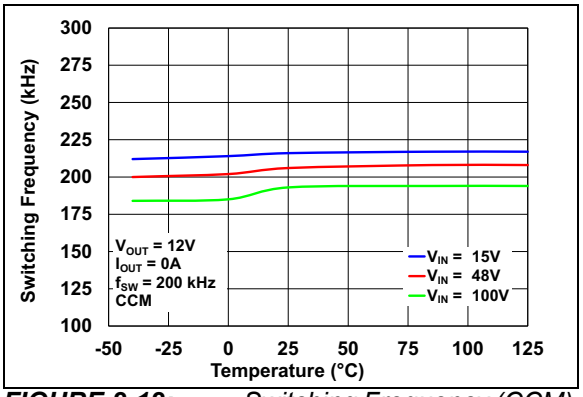


FIGURE 2-12: *Switching Frequency (CCM) vs. Temperature.*

Note: Unless otherwise indicated, V_{IN} = 48V; $V_{BST} – V_{SW} = PV_{DD}$ = 10.5V; f_{SW} = 200 kHz; T_A = +25°C.

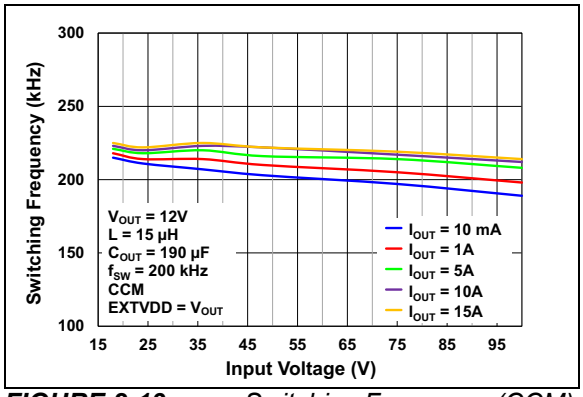


FIGURE 2-13: *Switching Frequency (CCM) vs. Input Voltage.*

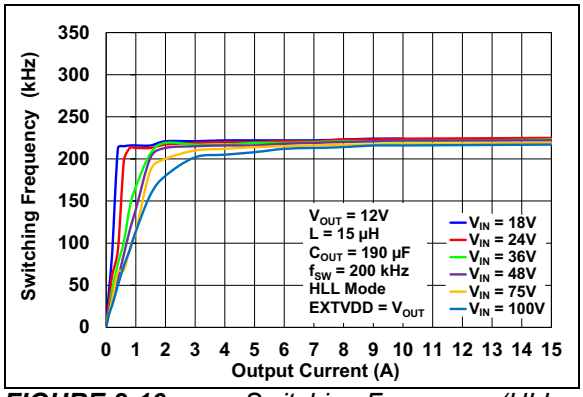


FIGURE 2-16: *Switching Frequency (HLL Mode) vs. Output Current.*

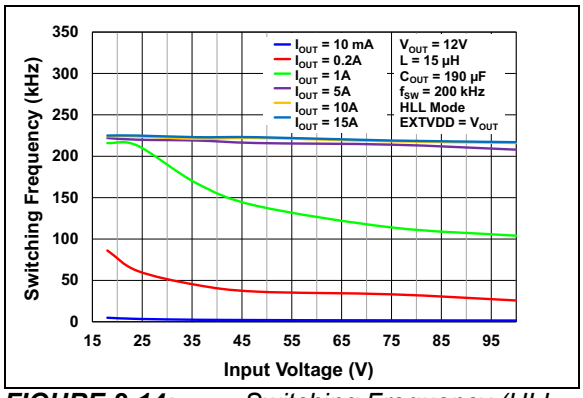


FIGURE 2-14: *Switching Frequency (HLL Mode) vs. Input Voltage.*

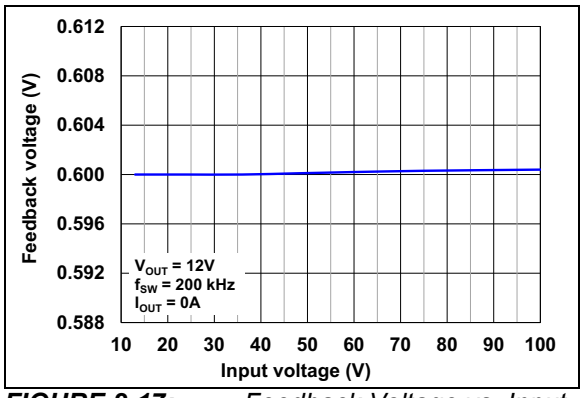


FIGURE 2-17: *Feedback Voltage vs. Input Voltage.*

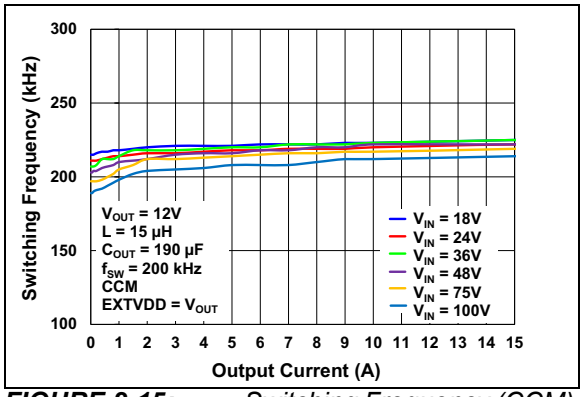


FIGURE 2-15: *Switching Frequency (CCM) vs. Output Current.*

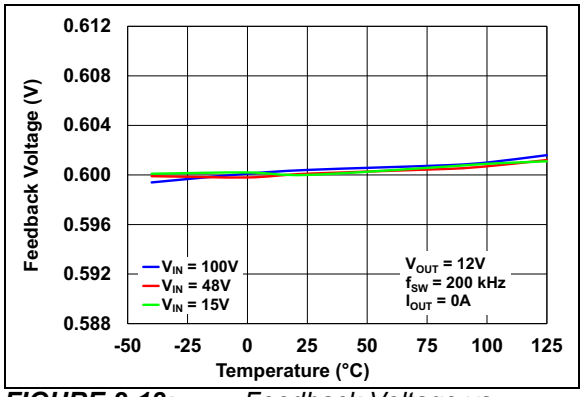


FIGURE 2-18: *Feedback Voltage vs. Temperature.*

Note: Unless otherwise indicated, V_{IN} = 48V; $V_{BST} - V_{SW} = PV_{DD}$ = 10.5V; f_{SW} = 200 kHz; T_A = +25°C.

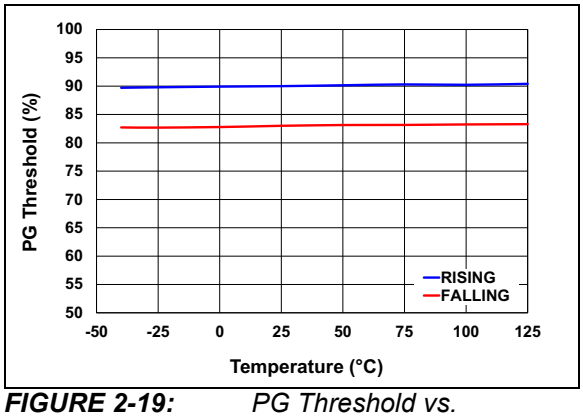


FIGURE 2-19: *PG Threshold vs. Temperature.*

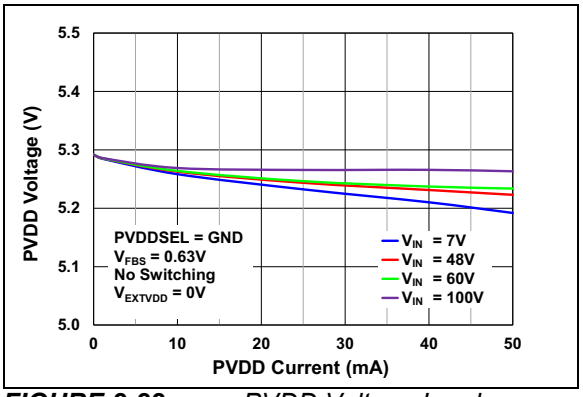


FIGURE 2-22: *PVDD Voltage Load Regulation (HV LDO, PVDDSEL = GND).*

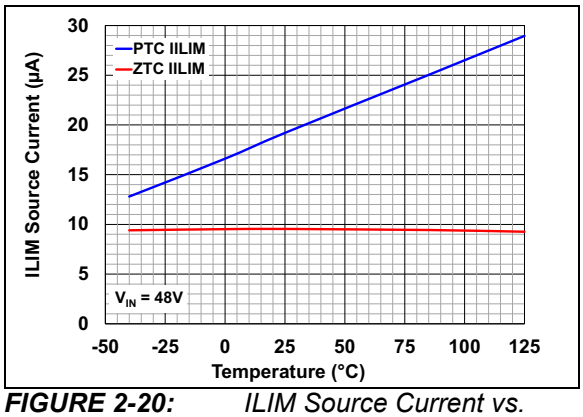


FIGURE 2-20: *ILIM Source Current vs. Temperature.*

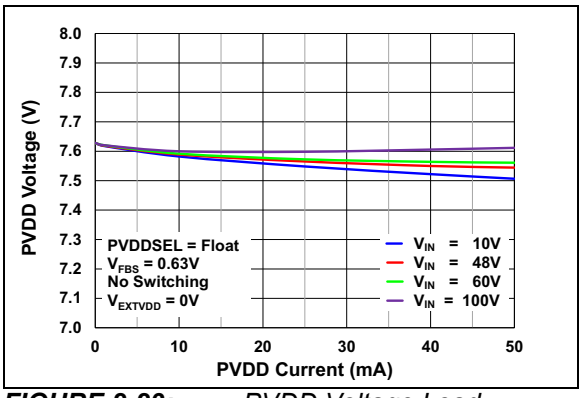


FIGURE 2-23: *PVDD Voltage Load Regulation (HV LDO, PVDDSEL = Float).*

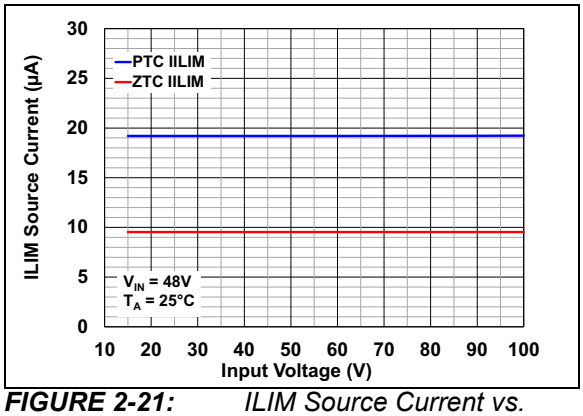


FIGURE 2-21: *ILIM Source Current vs. Input Voltage.*

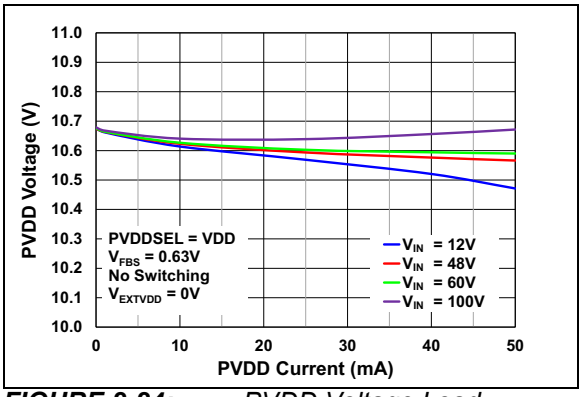


FIGURE 2-24: *PVDD Voltage Load Regulation (HV LDO, PVDDSEL = VDD).*

Note: Unless otherwise indicated, V_{IN} = 48V; $V_{BST} – V_{SW} = PV_{DD}$ = 10.5V; f_{SW} = 200 kHz; T_A = +25°C.

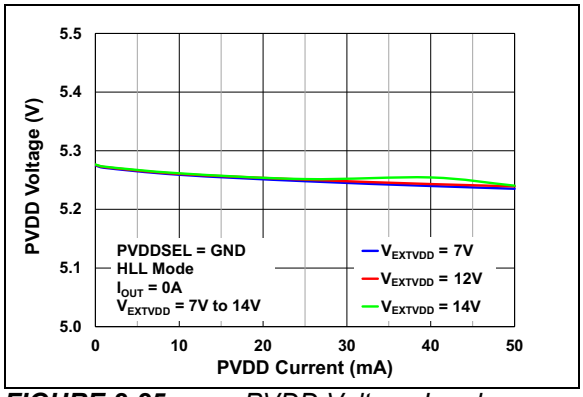


FIGURE 2-25: *PVDD Voltage Load Regulation (EXTVDD LDO, PVDDSEL = GND).*

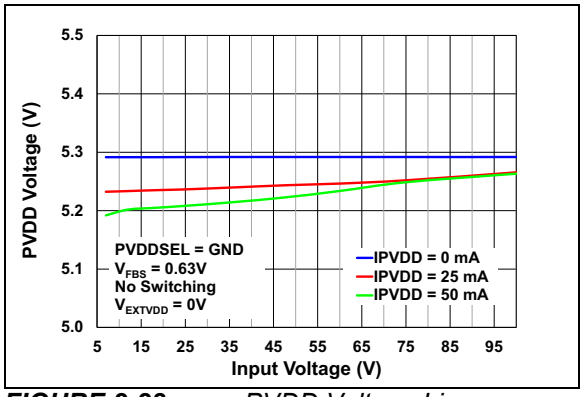


FIGURE 2-28: *PVDD Voltage Line Regulation (HV LDO, PVDDSEL = GND).*

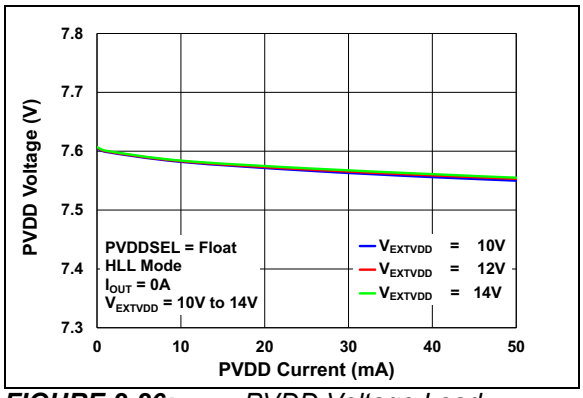


FIGURE 2-26: *PVDD Voltage Load Regulation (EXTVDD LDO, PVDDSEL = Float).*

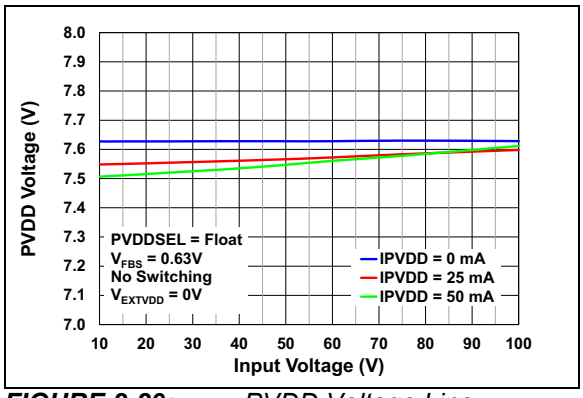


FIGURE 2-29: *PVDD Voltage Line Regulation (HV LDO, PVDDSEL = Float).*

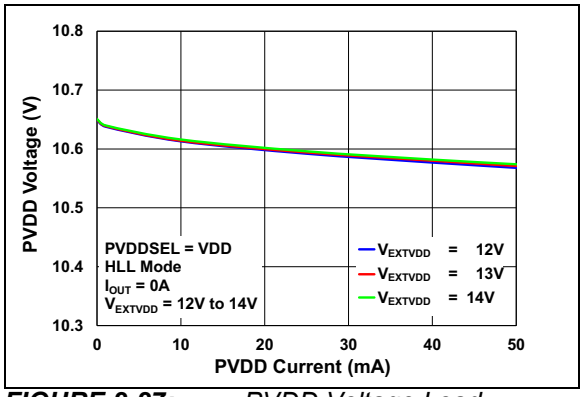


FIGURE 2-27: *PVDD Voltage Load Regulation (EXTVDD LDO, PVDDSEL = VDD).*

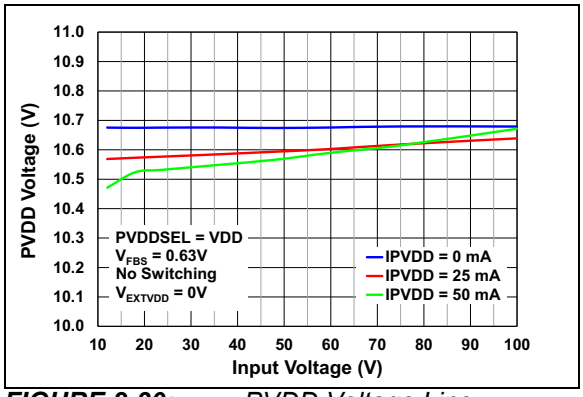


FIGURE 2-30: *PVDD Voltage Line Regulation (HV LDO, PVDDSEL = VDD).*

Note: Unless otherwise indicated, V_{IN} = 48V; $V_{BST} - V_{SW} = PV_{DD}$ = 10.5V; f_{SW} = 200 kHz; T_A = +25°C.

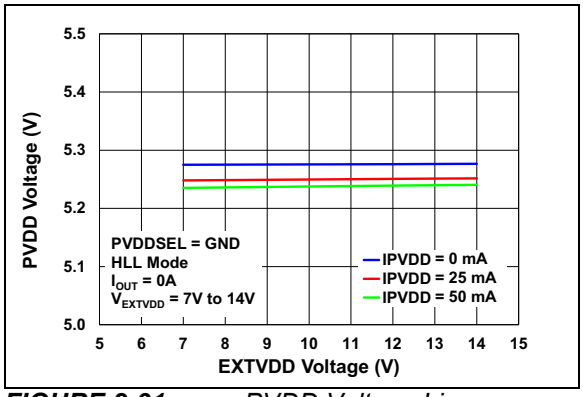


FIGURE 2-31: *PVDD Voltage Line Regulation (EXTVDD LDO, PVDDSEL = GND).*

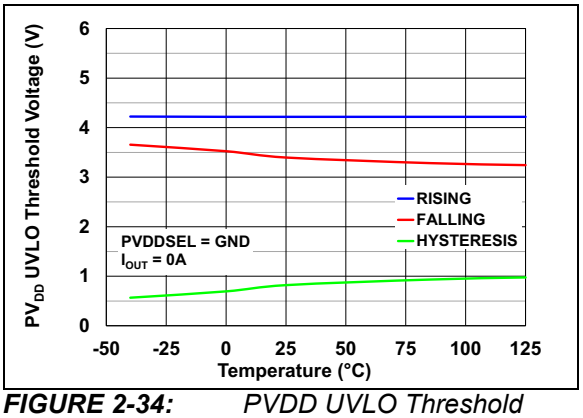


FIGURE 2-34: *PVDD UVLO Threshold (PVDDSEL = GND) vs. Temperature.*

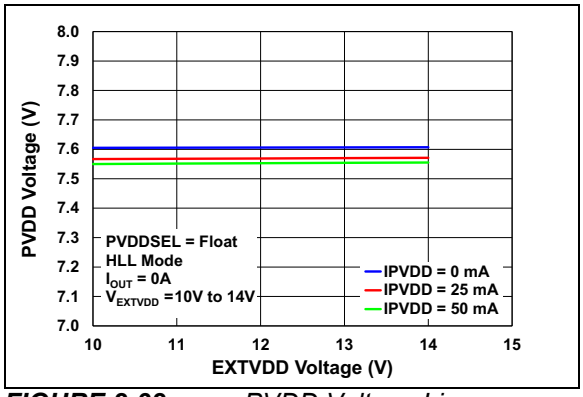


FIGURE 2-32: *PVDD Voltage Line Regulation (EXTVDD LDO, PVDDSEL = Float).*

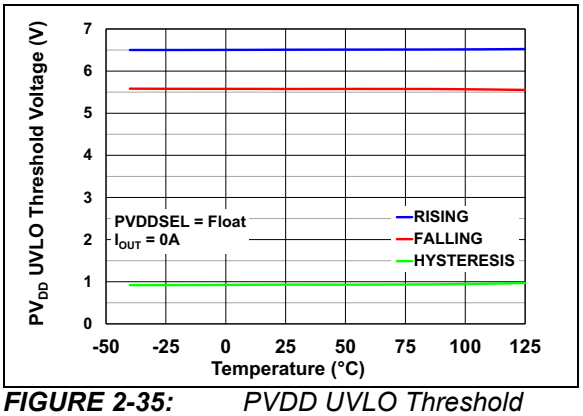


FIGURE 2-35: *PVDD UVLO Threshold (PVDDSEL = Float) vs. Temperature.*

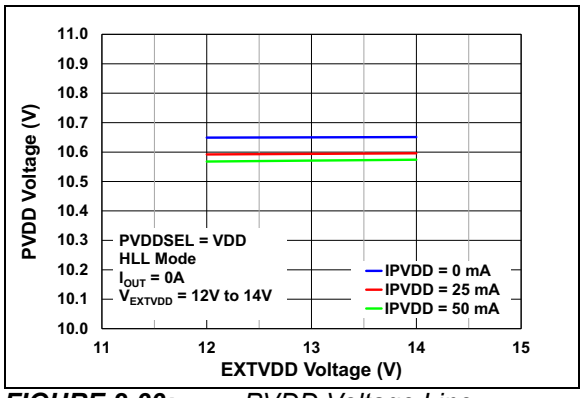


FIGURE 2-33: *PVDD Voltage Line Regulation (EXTVDD LDO, PVDDSEL = VDD).*

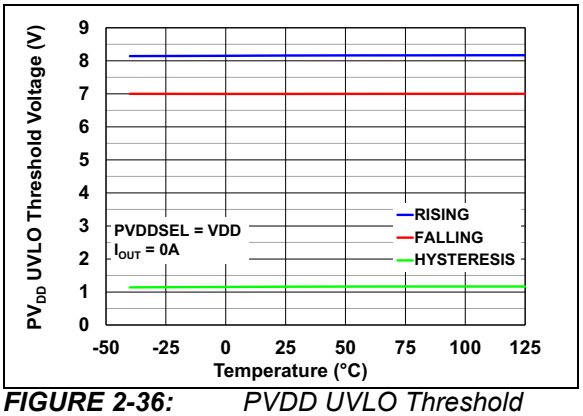


FIGURE 2-36: *PVDD UVLO Threshold (PVDDSEL = VDD) vs. Temperature.*

Note: Unless otherwise indicated, V_{IN} = 48V; $V_{BST} – V_{SW} = PV_{DD}$ = 10.5V; f_{SW} = 200 kHz; T_A = +25°C.

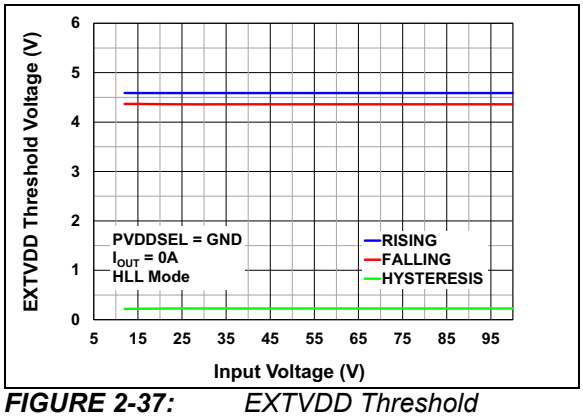


FIGURE 2-37: *EXTVDD Threshold (PVDDSEL = GND) vs. Input Voltage.*

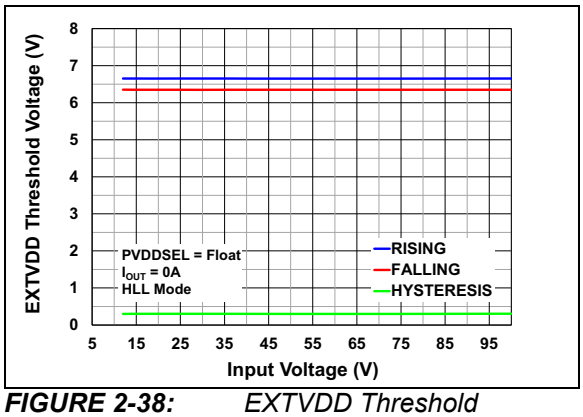


FIGURE 2-38: *EXTVDD Threshold (PVDDSEL = Float) vs. Input Voltage.*

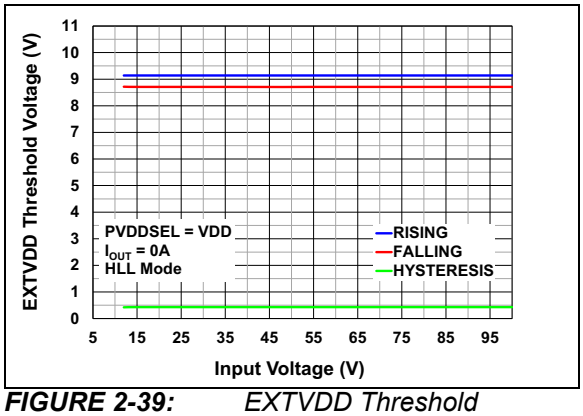


FIGURE 2-39: *EXTVDD Threshold (PVDDSEL = VDD) vs. Input Voltage.*

Note: Unless otherwise indicated, V_{IN} = 48V; $V_{BST} - V_{SW} = PV_{DD}$ = 10.5V; f_{SW} = 200 kHz; T_A = +25°C. L = 15 µH; R_{ILIM} = 15 kΩ; C_{SS} = 10 nF; HSFETs (Q1,Q2) = N-ch, 120V, 49A, 9.6 mΩ; LSFETs (Q3,Q4) = N-ch, 120V, 99A, 6.5 mΩ. Ripple Injection from INJ Pin; C_{FF} = 1 nF; R_{INJ} = 5.1 kΩ; C_{INJ} = 5.6 nF.

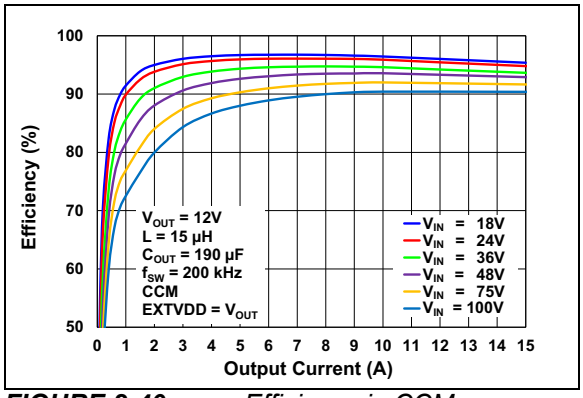


FIGURE 2-40: *Efficiency in CCM vs. Output Current.*

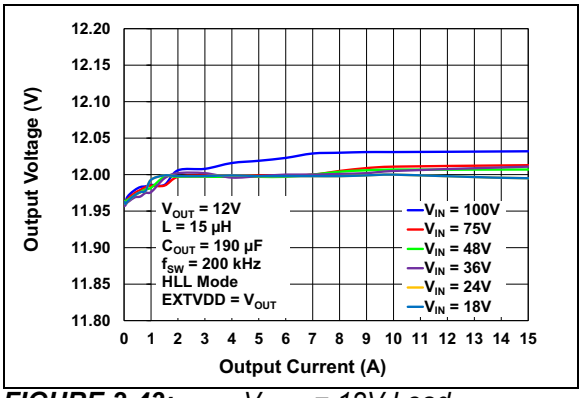


FIGURE 2-43: *V_{OUT} = 12V Load Regulation (HLL Mode).*

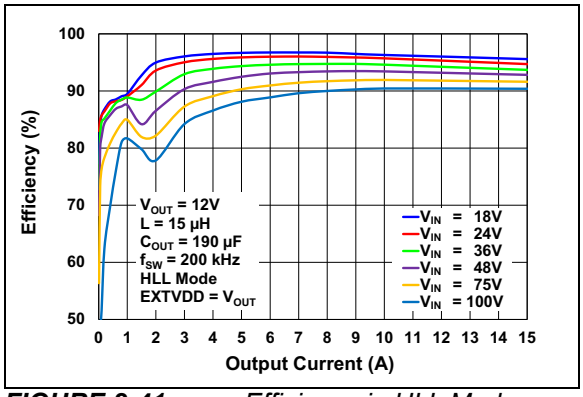


FIGURE 2-41: *Efficiency in HLL Mode vs. Output Current.*

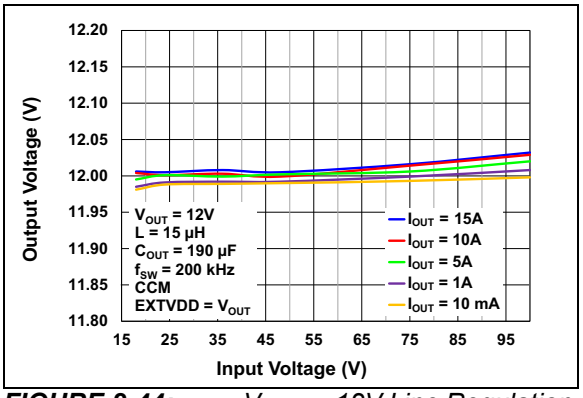


FIGURE 2-44: *V_{OUT} = 12V Line Regulation (CCM).*

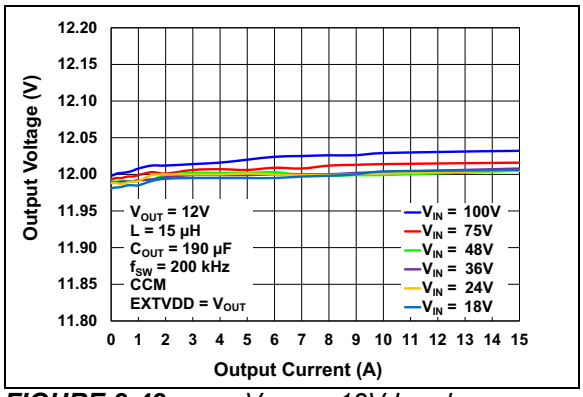


FIGURE 2-42: *V_{OUT} = 12V Load Regulation (CCM).*

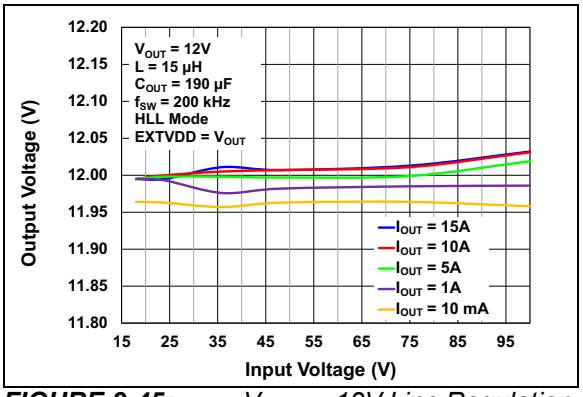


FIGURE 2-45: *V_{OUT} = 12V Line Regulation (HLL Mode).*

Note: Unless otherwise indicated, V_{IN} = 48V; $V_{BST} - V_{SW} = PV_{DD}$ = 10.5V; f_{SW} = 200 kHz; T_A = +25°C.L = 15 µH; R_{ILIM} = 15 kΩ; C_{SS} = 10 nF; HSFETs (Q1,Q2) = N-ch, 120V, 49A, 9.6 mΩ; LSFETs (Q3,Q4) = N-ch, 120V, 99A, 6.5 mΩ. Ripple Injection from INJ Pin; C_{FF} = 1 nF; R_{INJ} = 5.1 kΩ; C_{INJ} = 5.6 nF.

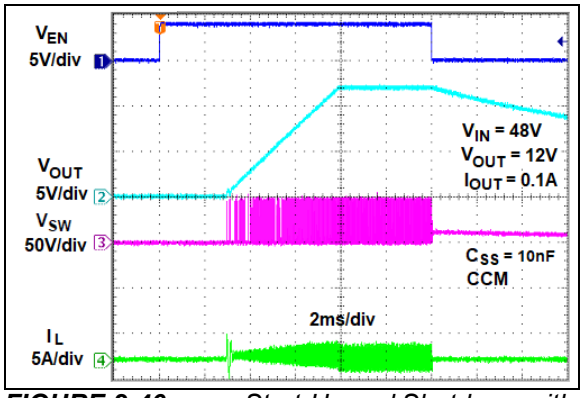


FIGURE 2-46: *Start-Up and Shutdown with Enable in CCM (V_{OUT} = 12V, I_{OUT} = 0.1A).*

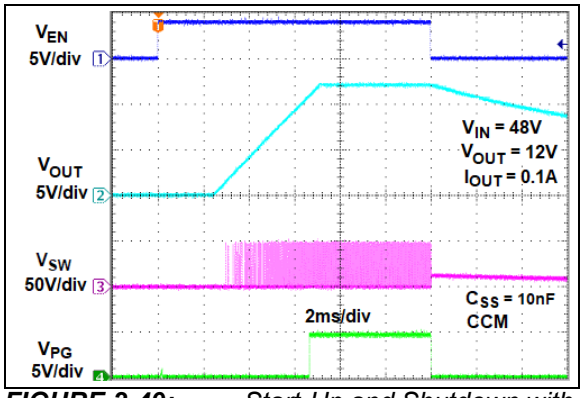


FIGURE 2-49: *Start-Up and Shutdown with PG in CCM (V_{OUT} = 12V, I_{OUT} = 0.1A).*

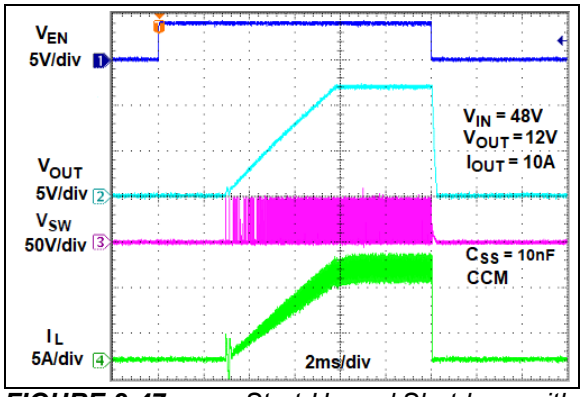


FIGURE 2-47: *Start-Up and Shutdown with Enable in CCM (V_{OUT} = 12V, I_{OUT} = 10A).*

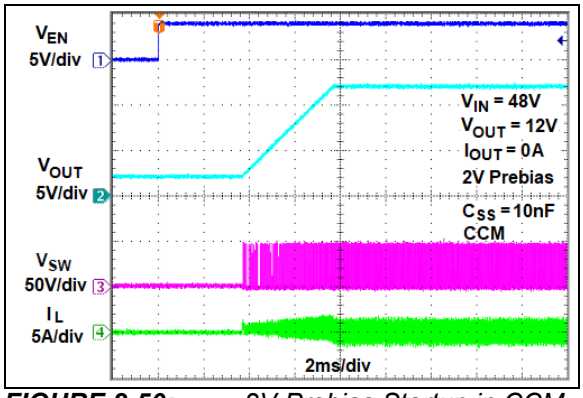


FIGURE 2-50: *2V Prebias Startup in CCM.*

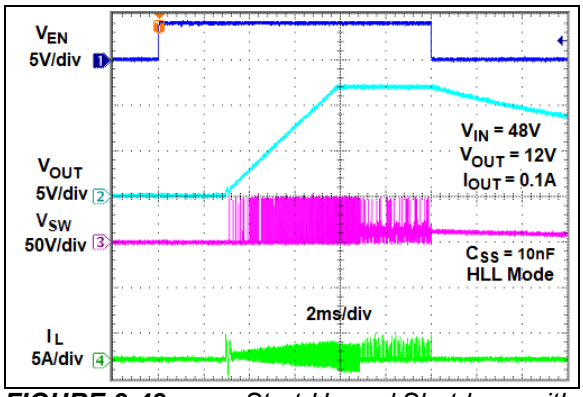


FIGURE 2-48: *Start-Up and Shutdown with Enable in HLL Mode (V_{OUT} = 12V, I_{OUT} = 0.1A).*

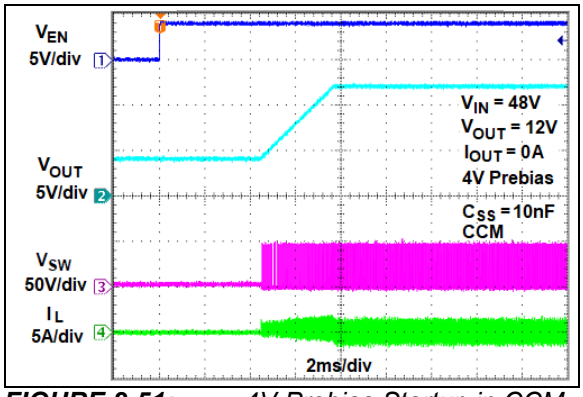


FIGURE 2-51: *4V Prebias Startup in CCM.*

Note: Unless otherwise indicated, V_{IN} = 48V; $V_{BST} - V_{SW} = PV_{DD}$ = 10.5V; f_{SW} = 200 kHz; T_A = +25°C. L = 15 µH; R_{ILIM} = 15 kΩ; C_{SS} = 10 nF; HSFETs (Q1,Q2) = N-ch, 120V, 49A, 9.6 mΩ; LSFETs (Q3,Q4) = N-ch, 120V, 99A, 6.5 mΩ. Ripple Injection from INJ Pin; C_{FF} = 1 nF; R_{INJ} = 5.1 kΩ; C_{INJ} = 5.6 nF.

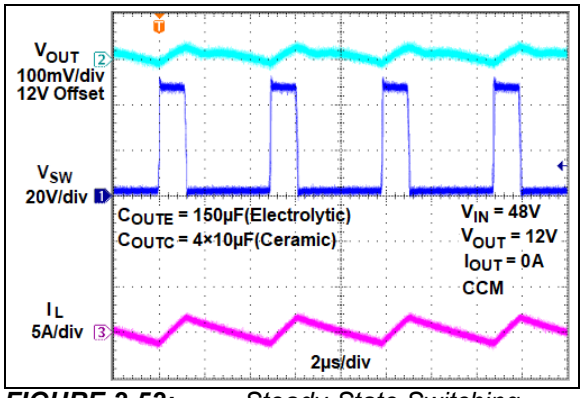


FIGURE 2-52: *Steady-State Switching Operation in CCM at No Load.*

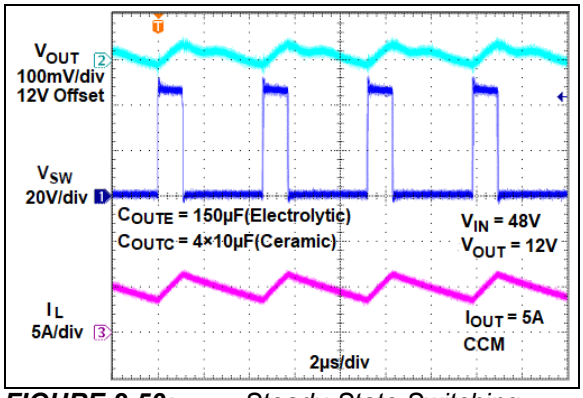


FIGURE 2-53: *Steady-State Switching Operation in CCM at Medium Load.*

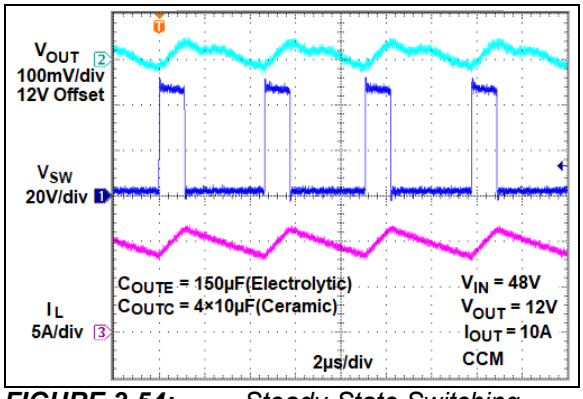


FIGURE 2-54: *Steady-State Switching Operation in CCM at Heavy Load.*

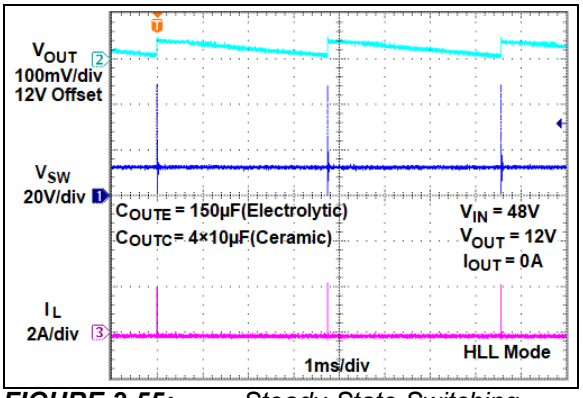


FIGURE 2-55: *Steady-State Switching Operation in HLL Mode at No Load.*

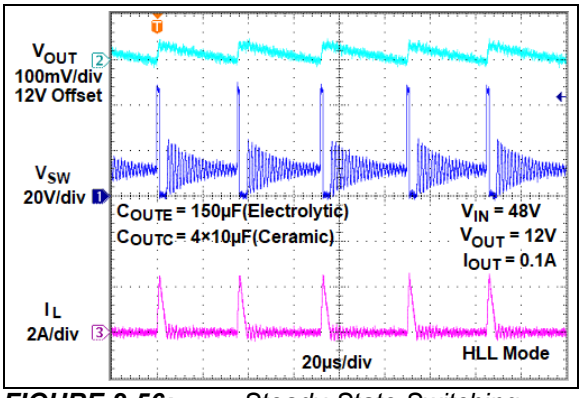


FIGURE 2-56: *Steady-State Switching Operation in HLL Mode at Light Load.*

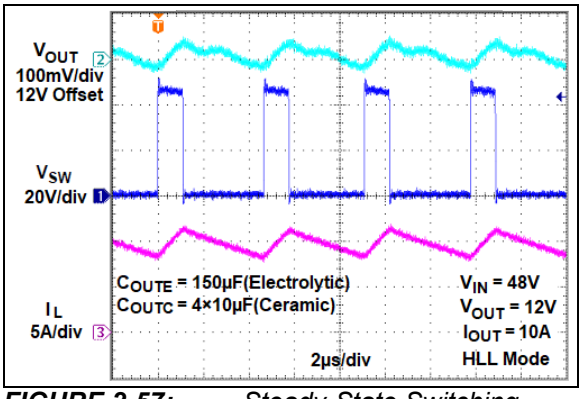


FIGURE 2-57: *Steady-State Switching Operation in HLL Mode at Heavy Load.*

Note: Unless otherwise indicated, V_{IN} = 48V; $V_{BST} - V_{SW} = PV_{DD}$ = 10.5V; f_{SW} = 200 kHz; T_A = +25°C. L = 15 µH; R_{ILIM} = 15 kΩ; C_{SS} = 10 nF; HSFETs (Q1,Q2) = N-ch, 120V, 49A, 9.6 mΩ; LSFETs (Q3,Q4) = N-ch, 120V, 99A, 6.5 mΩ. Ripple Injection from INJ Pin; C_{FF} = 1 nF; R_{INJ} = 5.1 kΩ; C_{INJ} = 5.6 nF.

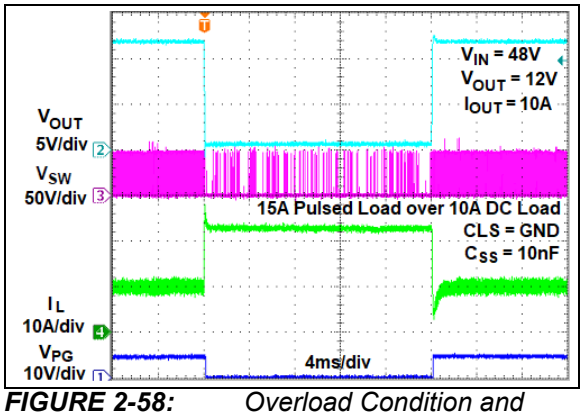


FIGURE 2-58: *Overload Condition and Recovery with CLS = GND.*

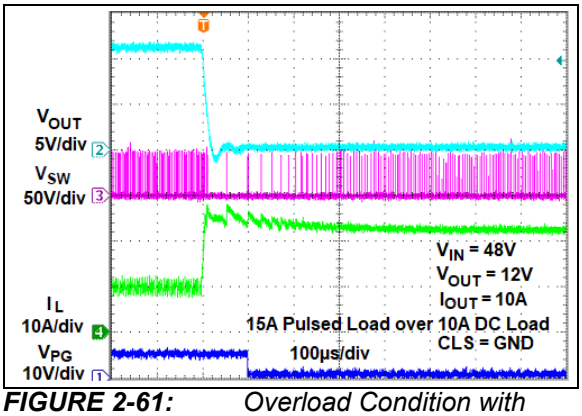


FIGURE 2-61: *Overload Condition with CLS = GND (Zoom-in).*

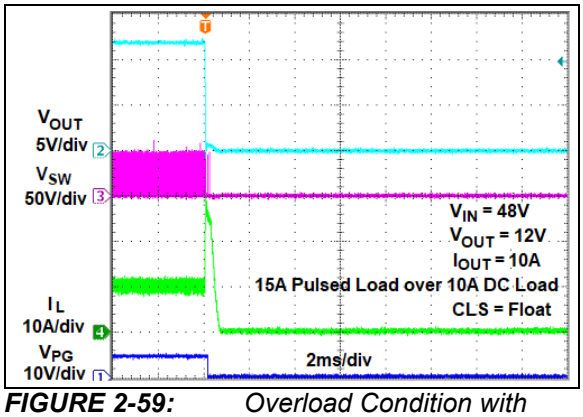


FIGURE 2-59: *Overload Condition with CLS = Float.*

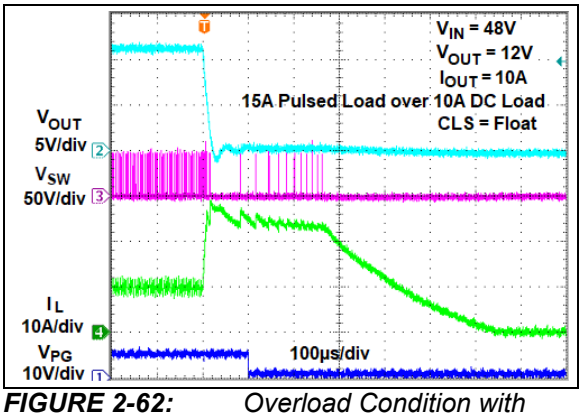


FIGURE 2-62: *Overload Condition with CLS = Float (Zoom-in).*

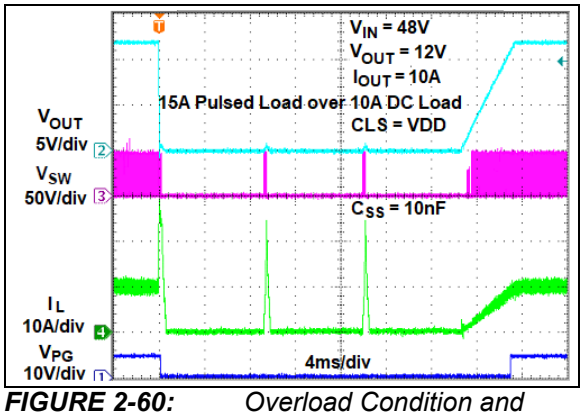


FIGURE 2-60: *Overload Condition and Recovery with CLS = VDD.*

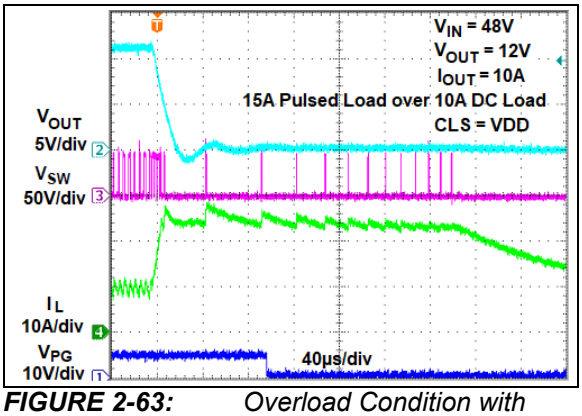


FIGURE 2-63: *Overload Condition with CLS = VDD (Zoom-in).*

Note: Unless otherwise indicated, V_{IN} = 48V; $V_{BST} - V_{SW} = PV_{DD}$ = 10.5V; f_{SW} = 200 kHz; T_A = +25°C. L = 15 µH; R_{ILIM} = 15 kΩ; C_{SS} = 10 nF; HSFETs (Q1,Q2) = N-ch, 120V, 49A, 9.6 mΩ; LSFETs (Q3,Q4) = N-ch, 120V, 99A, 6.5 mΩ. Ripple Injection from INJ Pin; C_{FF} = 1 nF; R_{INJ} = 5.1 kΩ; C_{INJ} = 5.6 nF.

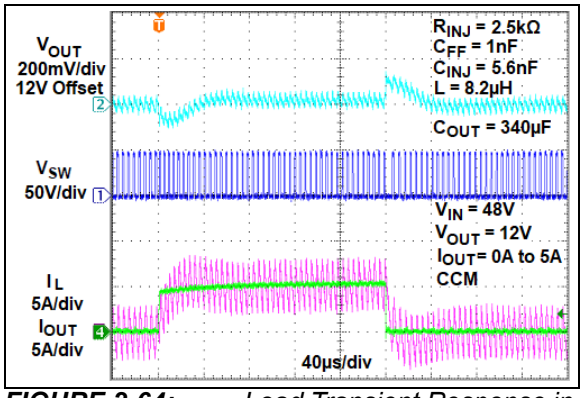


FIGURE 2-64: *Load Transient Response in CCM (I_{OUT} = 0A to 5A).*

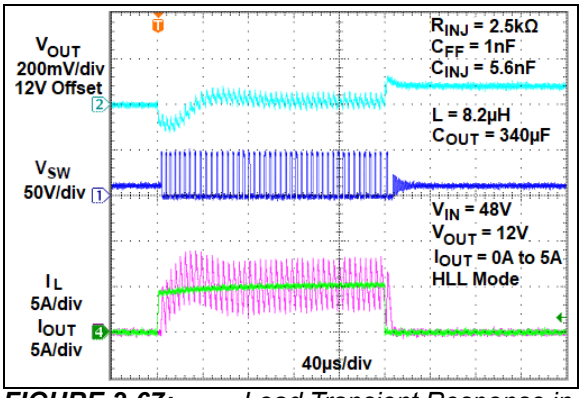


FIGURE 2-67: *Load Transient Response in HLL Mode (I_{OUT} = 0A to 5A).*

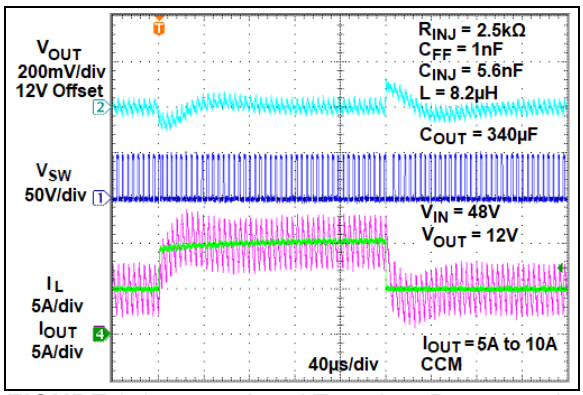


FIGURE 2-65: *Load Transient Response in CCM (I_{OUT} = 5A to 10A).*

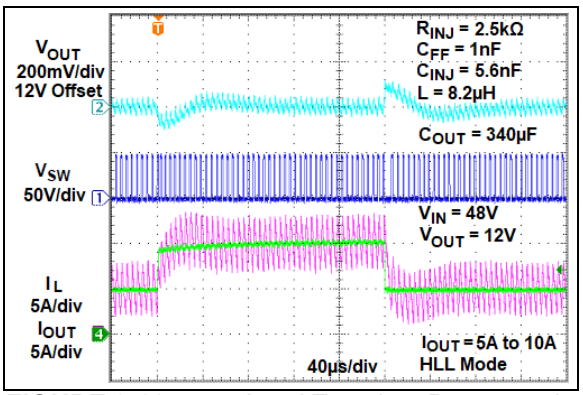


FIGURE 2-68: *Load Transient Response in HLL Mode (I_{OUT} = 5A to 10A).*

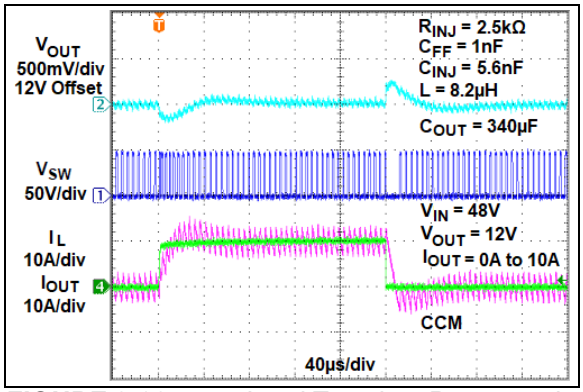


FIGURE 2-66: *Load Transient Response in CCM (I_{OUT} = 0A to 10A).*

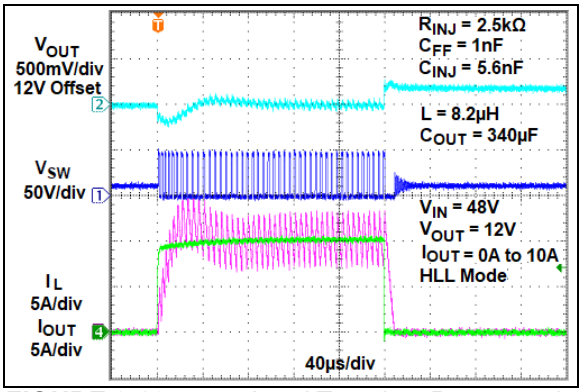


FIGURE 2-69: *Load Transient Response in HLL Mode (I_{OUT} = 0A to 10A).*

Note: Unless otherwise indicated, V_{IN} = 48V; $V_{BST} - V_{SW} = PV_{DD}$ = 10.5V; f_{SW} = 200 kHz; T_A = +25°C. L = 15 µH; R_{ILIM} = 15 kΩ; C_{SS} = 10 nF; HSFETs (Q1,Q2) = N-ch, 120V, 49A, 9.6 mΩ; LSFETs (Q3,Q4) = N-ch, 120V, 99A, 6.5 mΩ. Ripple Injection from INJ Pin; C_{FF} = 1 nF; R_{INJ} = 5.1 kΩ; C_{INJ} = 5.6 nF.

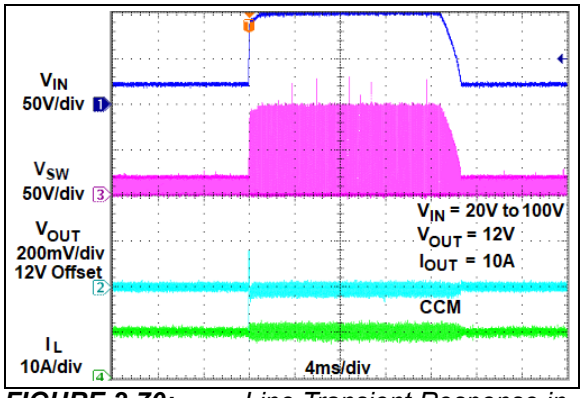


FIGURE 2-70: *Line Transient Response in CCM (V_{IN} = 20V to 100V).*

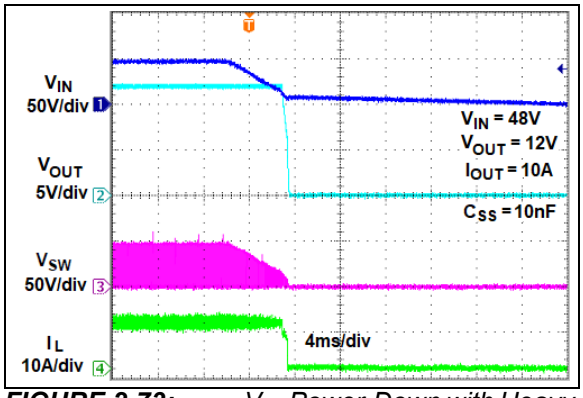


FIGURE 2-73: *V_{IN} Power-Down with Heavy Load.*

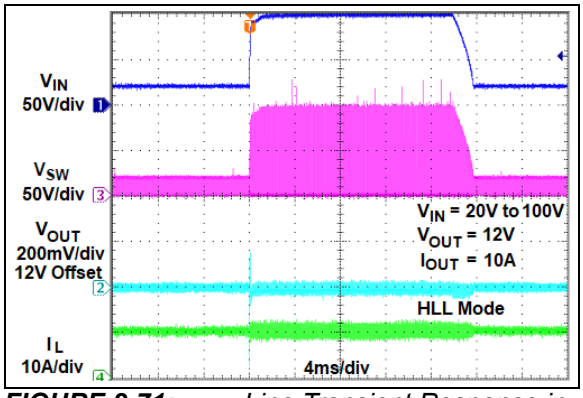


FIGURE 2-71: *Line Transient Response in HLL Mode (V_{IN} = 20V to 100V).*

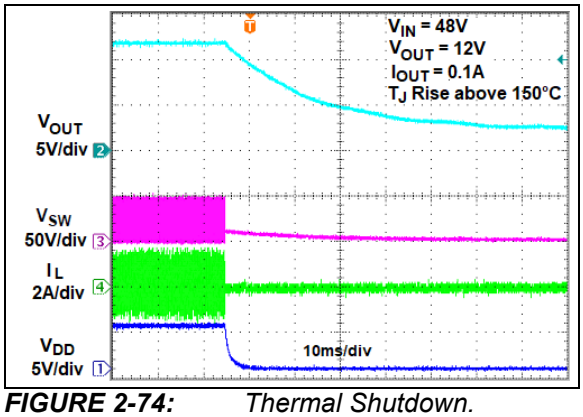


FIGURE 2-74: *Thermal Shutdown.*

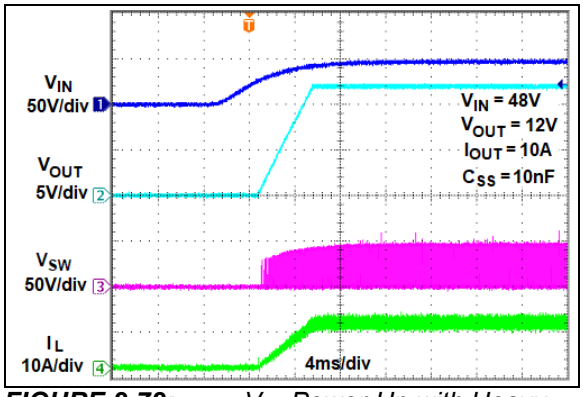


FIGURE 2-72: *V_{IN} Power-Up with Heavy Load.*

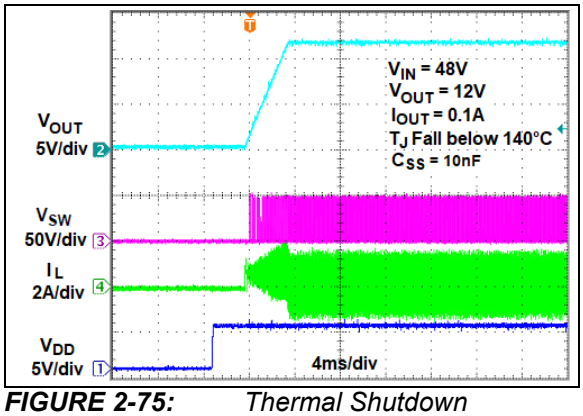


FIGURE 2-75: *Thermal Shutdown Recovery.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number (TSSOP)	Pin Number (VQFN)	Pin Name	Description
1	3	VIN	Input Voltage to the internal high voltage LDO and T_{ON} generator. Connect to supply voltage. Bypass VIN with a minimum of 1 µF low-ESR ceramic capacitor to GND.
2	4	EN	Precision Enable Input. The MIC2129 is enabled when the EN pin voltage is above 1.2V (typ).
3	5	CLS	Current Limit Selection Input. Connect CLS to VDD to set the current limit operating mode to Hiccup. Connect CLS to GND to set the current limit operating mode to cycle-by-cycle current limit. Leave unconnected to set the MIC2129 to latch-off in the event of current limit.
4	6	MODE	Light Load Mode Selection Input. Connect the MODE pin to VDD to select HyperLight Load (HLL) mode at light loads. Connect the MODE pin to GND to select Continuous Conduction Mode (CCM). Leave unconnected to enable soft start in DCM with CCM operation after soft start is done. Refer to Section 4.4.1, Modes of Operation for more details.
5	7	PVDDSEL	PVDD Voltage Selection Input. Connect PVDDSEL to GND to select 5.2V gate drive voltage. Leave PVDDSEL unconnected to select 7.5V gate drive voltage. Connect to VDD to select 10.5V gate drive voltage.
6	8	FREQ	Switching Frequency Programming Input. Connect a resistor between FREQ and GND to program the switching frequency between 100 kHz to 800 kHz.
7	9	VDD	Internal 4.5V Bias LDO output. VDD is the bias supply for MIC2129 internal circuitry. Connect a minimum 2.2 µF low-ESR ceramic capacitor across VDD and GND.
8	10	GND	Analog Ground. GND is the reference to the MIC2129 internal analog circuits. Short to PGND externally at a single point.
9	11	ILIM	Current Limit Threshold Programming Input. Connect a resistor between ILIM and GND to set the current limit threshold. The resistor at the ILIM pin sets both positive and negative current limit thresholds.
10	12	INJ	Ripple Injection Components Connection Node. Connect a resistor and a capacitor in series between INJ and FBS to generate ripple voltage at FBS node. Also connect a resistor to FBG which sets the INJ pin voltage to its steady-state value. Refer to Section 4.2, Start-up Into Prebias Load and Section 4.3, Ripple Injection.
11	13	FBG	Feedback Ground Input. Connect to the remotely sensed load ground.
12	14	FBS	Feedback Sense Input. Connect to the midpoint of the resistor divider between remotely sensed load voltage and load ground.
13	15	SS	Output Voltage Start-up Time Programming Input. Connect a capacitor from SS to GND to program the output voltage ramp-up time.
14	16	PG	Open Drain Power Good Output. PG is low when the FB voltage is <83% of 0.6V internal reference. Connect a pull-up resistor of >10 kΩ from PG to a pull-up source to set the PG voltage when FB voltage is ≥90% of 0.6V internal reference.
15	17	VSNS	Voltage Sense Input for V_{OUT} sense to feed into the T_{ON} generator. Connect to SW if the target output voltage is ≤14V. Connect to the midpoint of the resistor divider between the output of the converter and GND if the target output voltage is greater than 14V.
16	18	CSN	Current Sense Negative Input to the current limit comparator. Connect to LSFET source terminal if LSFET is used for current sensing or connect to current sense resistor PGND terminal if an external sense resistor is used for current sensing.

TABLE 3-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number (TSSOP)	Pin Number (VQFN)	Pin Name	Description
17	19	CSP	Current Sense Positive Input to the current limit comparator. Connect CSP pin to SW node of low-side MOSFET when voltage drop across LSFET is used for current sensing. Connect CSP pin to the junction of LSFET source terminal and external current sense resistor when current sense resistor is used for accurate current limit.
18	20	BST	Bootstrap Capacitor Connection Node. Connect a typical 0.1 µF low-ESR ceramic capacitor between BST pin and SW pin.
19	21	DH	High-Side FET Gate Driver Output. Connect DH to Gate pin of the external N-channel high-side MOSFET.
20	22	SW	Switching Node. SW pin provides return path for the high side gate driver.
21	23	DL	Low-Side FET Gate Driver Output. Connect DL to the gate pin of the external N-channel low-side MOSFET.
22	24	PGND	Power Ground. PGND provides return path for the low-side gate driver. Connect to LSFET source terminal if LSFET is used for current sensing or connect to PGND of current-sense resistor if an external resistor is used for current sensing.
23	1	PVDD	Internal Gate Driver Supply LDO's Output. PVDD is the supply for the low side FET gate driver and is the source which charges the capacitor connected between BST and SW. PVDD voltage is selectable between 5.2V, 7.5V and 10.5V by connecting PVDDSEL to GND, Float or VDD respectively. Connect a minimum 4.7 µF low-ESR ceramic capacitor between PVDD and PGND.
24	2	EXTVDD	Supply for the Internal Bootstrap LDO. Bootstrap LDO is enabled whenever the voltage at EXTVDD pin is above its UVLO rising threshold. The internal high voltage LDO which operates from VIN is disabled once the Bootstrap LDO is enabled. Connect EXTVDD to output of the buck converter if the output voltage is ≥ 4.85V and ≤ 14V (depending on PVDD setting which sets EXTVDD rising threshold).
—	—	EP	Exposed Pad. Connect EP to the GND pin and GND copper layer on the PCB for improved thermal performance.

4.0 FUNCTIONAL DESCRIPTION

4.1 Control Architecture

The MIC2129 is a modified adaptive on-time, synchronous step-down DC/DC controller. It is designed to operate over a wide 4.5V to 100V input voltage range and provides a regulated output voltage. An adaptive on-time control scheme is employed in order to obtain a constant switching frequency and simplify the control compensation.

Unlike true current-mode control, the MIC2129 uses the output voltage ripple to trigger an on-time period. The output voltage ripple is proportional to the inductor current ripple if the ESR of the output capacitor is large enough. In order to meet the stability requirements, the MIC2129 feedback voltage ripple must be in phase with the inductor current ripple and large enough to be sensed by the g_m amplifier and the error comparator. The recommended feedback voltage ripple is 40 mV to 500 mV. If a low-ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the g_m amplifier and the error comparator. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple if the ESR of the output capacitor is very low. In these cases, ripple injection is required to ensure proper operation.

The MIC2129 has a differential remote sense amplifier with unity gain for sensing output voltage. The differential remote sense amplifier helps regulate the output voltage at target level, over the entire load range, by avoiding parasitic voltage drops on the PCB. The output of the differential amplifier will be used as output voltage to the controller. The output voltage is sensed across the MIC2129 device's feedback remote sense FBS pin and the ground feedback remote sense FBG pin via the voltage divider, and compared with a 0.6V reference voltage V_{REF} with a low-gain transconductance (g_m) amplifier. The output of the g_m amplifier, V_{gm}, is then further compared with another 0.6V reference, V_{REF_COM}, at the error comparator. If the feedback voltage decreases and the output of the g_m amplifier is below 0.6V, then the error comparator will trigger the control logic and generate an on-time period. The on-time period length is predetermined by the T_{ON} generation circuitry.

EQUATION 4-1:

$$T_{ON(EST)} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

Where:

V_{OUT} = Output Voltage

V_{IN} = Power Stage Input Voltage

f_{SW} = Switching Frequency

The internal logic starts maintaining the same switching frequency in steady-state as described below.

Figure 4-1 shows the MIC2129 control loop timing during steady-state operation. During steady-state operation, the g_m amplifier senses the feedback voltage ripple, which is proportional to the output voltage ripple and the external ripple from the RIP_INJ pin, injected to the FBS node at the turn-on instant. When the output of the g_m error amplifier falls below the reference voltage, the on-time period is triggered. The on-time is determined by the T_{ON} generator. The high-side driver turns on high-side FET during T_{ON}.

The high-side FET turn-off instant depends on the T_{ON} estimation. At the end of T_{ON}, the internal high-side driver turns off the high-side FET and the low-side driver turns on the low-side FET. The off-time period length depends upon the feedback voltage error in the next cycle. When the output of the g_m error amplifier falls below the reference voltage in the second cycle, new on-time period is triggered.

If the off-time period determined by the feedback voltage is less than the Minimum Off-Time, $T_{OFF(MIN)}$, which is about 400 ns, then the MIC2129 control logic will apply the $T_{OFF(MIN)}$ instead. The $T_{OFF(MIN)}$ period is required to maintain enough energy in the bootstrap capacitor (C_{BST}) to drive the high-side MOSFET.

The maximum duty cycle is obtained from the 400 ns $T_{OFF(MIN)}$:

EQUATION 4-2:

$$D_{MAX} = \frac{T_S - T_{OFF(MIN)}}{T_S} = 1 - \frac{400\ ns}{T_S}$$

Where:

T_S = $1/f_{SW}$

It is not recommended to use the MIC2129 with an off-time close to $T_{OFF(MIN)}$ during steady-state operation. Equation 4-2 should be used to choose the T_S for a lower switching frequency, when the D_{MAX} is reached if V_{IN} is very close to V_{OUT}, knowing that the buck converter duty cycle equals V_{OUT} divided by V_{IN}. The actual on-time and the resulting switching frequency will vary with the part-to-part variation in the rise and fall times of the external MOSFETs, the output load current and the variations in the PV_{DD} voltage. Also, the minimum T_{ON} results in a lower switching frequency in high V_{IN} to V_{OUT} applications, such as 28V to 1.0V.

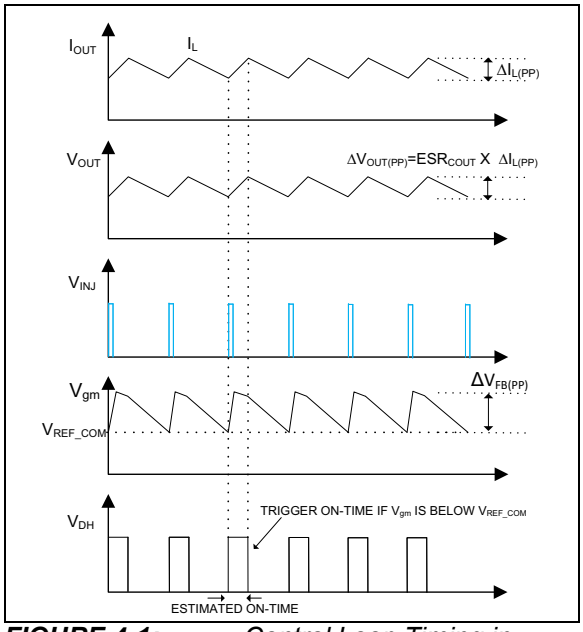


FIGURE 4-1: *Control Loop Timing in Steady-State Operation (FB Ripple Shows Injected and ESR Ripple Only, Reactive Impedances Neglected).*

The MIC2129 uses "modified Adaptive On-Time control" architecture. The modifications are to:

- Allow higher output voltages (>30V)

  This is achieved by having an additional pin (VSNS) which can be connected to either SW (if $V_{OUT} \leq 14V$) or to midpoint of a resistor divider from output if $V_{OUT} > 14V$.

  Connecting VSNS to SW results in the same architecture as in our earlier Adaptive On-time control synchronous DC-DC step-down controllers or converters. Connecting SW to VSNS compensates for the inductor DCR drop and hence the switching frequency variation with respect to load current is low.

  The ON-time generator of preceding Adaptive On-Time control devices impose a limitation on the maximum output voltage. The limitation on the maximum output voltage of 14V is overcome by connecting VSNS to the mid-point of a resistor divider from V_{OUT} to PGND, any output voltage can be achieved (limited by maximum duty cycle) using the MIC2129.
- Reduce the FB ripple variation with input voltage and hence improve line regulation at higher input voltages.

  In the previous Adaptive On-Time control architecture the voltage ripple on FB increases as input voltage increases and vice versa. But there is a limitation on the maximum FB ripple voltage because of the internal clamps. If the FB ripple increases above a certain value based on the internal clamps, the output voltage regulation becomes poor.

  To avoid this problem, the MIC2129 outputs on its INJ pin a pulse of 4.5V magnitude and 100ns fixed on-time duration and in-phase with SW node signal. Connecting the external ripple injection circuit to this pin generates a constant FB ripple voltage independent of the input voltage.

  The MIC2129 can also be configured to use the SW node for injecting feedback ripple. Ripple injection components are connected to SW node like the existing ACOT products. The INJ pin can be left unconnected in this configuration. It is suggested to leave the MODE pin unconnected in this configuration to achieve better prebias startup performance. Refer to Section 4.4.1, Modes of Operation for more details.

Figure 4-2 shows the operation of the MIC2129 during a load transient. The output voltage drops due to the sudden load increase, which causes the V_{FBS} to decrease and the output voltage of the g_m amplifier, V_{gm}, to be less than V_{REF_COM}. This will cause the error comparator to trigger an on-time period. At the end of the on-time period, a Minimum Off-Time, $T_{OFF(MIN)}$, is generated to charge C_{BST}, since the feedback voltage is still below V_{REF}. Then, the next on-time period is triggered and D_{MAX} is achieved due to the low feedback voltage. Therefore, the switching frequency changes during the load transient to deliver maximum duty cycle at high-current step-up load. The opposite occurs at high-current load release, causing a brief zero duty cycle period. The converter returns to the nominal fixed frequency once the output has stabilized at the new load current level.

With the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small in the MIC2129 converter.

The transient response is shown in Figure 4-2.

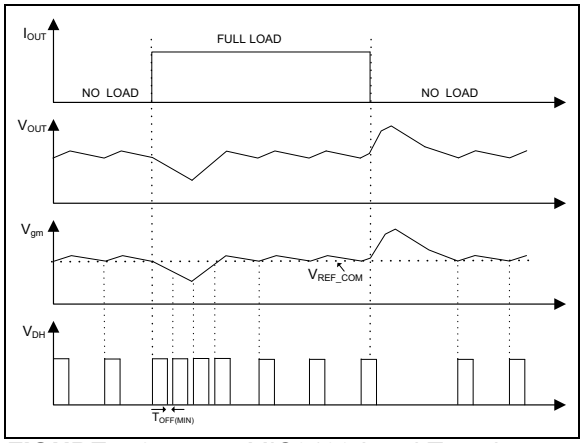


FIGURE 4-2: *MIC2129 Load Transient Response.*

4.2 Start-up Into Prebias Load

For feedback voltage ripple injection using the INJ pin, MIC2129 always starts up in CCM when the MODE pin is connected to either GND or VDD, refer to Section 4.4.2, Continuous Conduction Mode (Mode = GND) and Section 4.4.3, HyperLight Load (HLL) Mode (Mode = VDD) for more details. It is necessary to ensure that the device does not sink current from the pre-biased load. To get proper pre-bias start-up performance, the voltage at the junction of C_{INJ} and R_{INJ} needs to be at its steady-state value when the device starts switching. This is done by biasing the INJ pin voltage using an internal current source (I_{BIAS}) at the INJ pin and an external resistor (R_{BIAS}) at the INJ pin before the device starts switching, see Figure 4-3. The Injection (INJ) driver will be in High-Impedance mode before the device starts switching. This results in a voltage equal to I_{BIAS} x R_{BIAS} at the INJ pin before switching starts. This voltage charges the C_{INJ} capacitor to the value of I_{BIAS} x R_{BIAS}.

As the C_{INJ} takes time to charge to the final voltage, depending on the C_{INJ} x (R_{INJ} + $R_{FB(BOT)}$), the I_{BIAS} is enabled before the switching starts. The MIC2129 has an internal POK signal delay of ≈ 4 ms (i.e., when EN is high, the device starts switching after the internal POK delay of about 4 ms). Therefore, this 4 ms delay is enough to charge C_{INJ} to the final value. The device will not start switching until the V_{SS} voltage ramps above the level of the feedback voltage divided down from the pre-biased output voltage. Once the device starts switching, the I_{BIAS} will no longer have any effect, as the INJ driver will be either high or low (the INJ driver will not be in High-Impedance mode when the device starts switching).

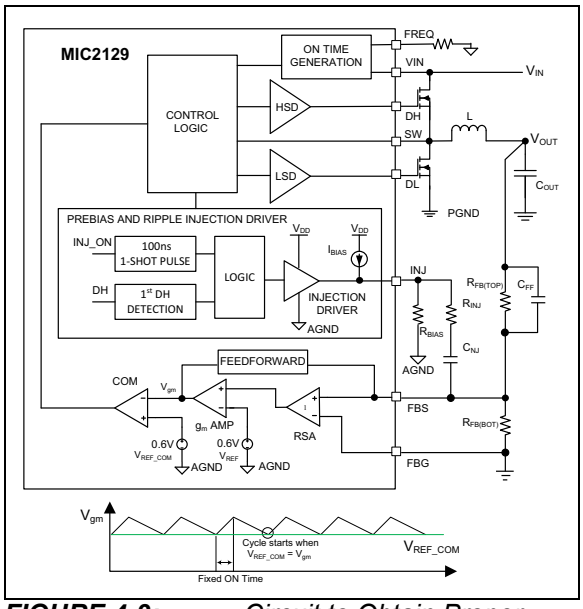


FIGURE 4-3: *Circuit to Obtain Proper Pre-Bias Start-up Performance and Ripple Injection from INJ Node at FBS Pin.*

I_{BIAS} is an internal current source. R_{BIAS} is an external resistor from INJ to GND. RBIAS can be calculated using the formula below:

EQUATION 4-3:

$$R_{BIAS} = \frac{4.5V \times 100\ ns \times f_{SW}}{I_{BIAS}}$$

Where:

$4.5V \times 100\ ns \times f_{SW}$ = Average Voltage on the INJ Pin

I_{BIAS} = Pre-position Bias Current Source 4.9 µA

Note that as R_{BIAS} is always present, it draws an additional current from the injection driver when INJ pin is 4.5V for 100 ns. This adds to the device's I_Q. However, its contribution to the device's I_Q will be low, because this current will be present for 100 ns only.

For feedback ripple voltage injection using the switching node, the MODE pin has to be left floating and the device always starts up in DCM to ensure proper pre-biased start-up performance. Since the device starts up in DCM with the MODE pin unconnected, the device will not sink current from the pre-biased load and the R_{BIAS} resistor is not required to install to set the steady-state voltage at the junction of R_{INJ} and C_{INJ} like the start-up in CCM case.

4.3 Ripple Injection

The MIC2129 uses ripple-based constant on-time architecture to generate switching pulses. The magnitude of feedback ripple voltage needs to be in the range of 40 mV to 500 mV. In order to avoid ripple voltage variation with input voltage, the MIC2129 uses the INJ node instead of the SW node to generate ripple on the FBS node. Doing so keeps the feedback ripple constant independent of the input voltage. Keeping the feedback ripple constant is important for controllers which support wide input voltage range. The SW node still can be used for injecting ripple on feedback node by leaving the MODE pin and the INJ pin unconnected and connecting series R_{INJ} and C_{INJ} across the SW pin and the FBS pin, and this sets the device to start up in DCM. Refer to Section 4.4.4, CCM with DCM Soft Start (Mode = Unconnected).

Figure 4-3 shows the ripple injection from the INJ pin at FBS node with respect to reference voltage. The ripple injection circuit components include R_{INJ}, C_{INJ}, C_{FF}, $R_{FB(TOP)}$ and $R_{FB(BOT)}$.

The output capacitors generally have three components. The capacitive ripple lags the inductor current ripple. The ESR ripple is in phase with the inductor current. The ESL ripple effect is very minimal in low-voltage capacitors. If a low-ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the g_m amplifier and the error comparator. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase

with the inductor current ripple if the ESR of the output capacitor is very low. In these cases, ripple injection must be used to ensure proper operation. The INJ node produces a switching signal with 4.5V magnitude, at a frequency the same as the switching frequency (in CCM), in-phase with the SW node (i.e INJ is high when SW is high) and its ON period is 100 ns.

4.3.1 RIPPLE INJECTION CIRCUIT COMPONENTS SELECTION FOR RIPPLE INJECTION FROM INJ NODE

Follow the below steps for selecting ripple injection circuit components when ripple injection from the INJ node is used. Note that the assumption used for the below guidelines is that the crossover frequency is well over the output filter LC resonant frequency. The below procedures provide a good starting point for selecting the ripple injection components. It is recommended that final values be confirmed by laboratory measurements.

1. Calculate the product of R_{INJ} and C_{FF} for a given injected Feedback Ripple Voltage, ΔV_{FB}, using Equation 4-4. Choose ΔV_{FB} in the range from 40 mV to 500 mV. A good starting point for ΔV_{FB} is 50 mV.

EQUATION 4-4:

$$R_{INJ} \times C_{FF} = \frac{4.5V \times 100ns}{\Delta V_{FB}} \times \left(1 - \frac{100ns}{T_{SW}}\right)$$

Where:

ΔV_{FB}	=	Injected Feedback Ripple Voltage
$4.5V$	=	Magnitude of the INJ Pulse Source
$100\ ns$	=	ON period of the INJ Pulse Source
T_{SW}	=	Switching Period

2. Choose C_{FF} in the range from 0.47 nF to 10 nF.
3. Calculate R_{INJ} using the above equation.
4. Calculate the Top Feedback Resistor, $R_{FB(TOP)}$, value using Equation 4-5.

EQUATION 4-5:

$$R_{FB(TOP)} \geq \frac{1}{2 \times \pi \times C_{FF} \times 0.8 \times f_{LC}}$$

Where:

f_{LC} = Output Filter LC Resonant Frequency = 1/(2 x π x sqrt(L x C_{OUT}))

5. Calculate the Bottom Feedback Resistor, $R_{FB(BOT)}$, value using Equation 4-6:

EQUATION 4-6:

$$R_{FB(BOT)} = \frac{R_{FB(TOP)}}{\left[\frac{V_{OUT}}{V_{REF}} - 1\right]}$$

Where:

V_{OUT}	=	Target Output Voltage
V_{REF}	=	Reference Voltage = 0.6V for MIC2129

6. Estimate the crossover frequency using Equation 4-7. If $f_{CO(EST)}$ is above $f_{SW}/5$, lower the C_{FF} value to increase the injected ripple voltage and go back to the step 2.

EQUATION 4-7:

$$f_{CO(EST)} = \frac{R_{INJ} \times C_{FF}}{2\pi \times L \times C_{OUT}} \times \frac{V_{OUT}}{4.5V \times 100ns \times f_{SW}}$$

Where:

L	=	Inductance
C_{OUT}	=	Output Capacitance
V_{OUT}	=	Output Voltage
f_{SW}	=	Switching Frequency

7a) Select C_{INJ} using the below equation to get phase margin larger than 60 degree if $f_{CO(EST)}$ calculated above meets Equation 5-9.

EQUATION 4-8:

$$C_{INJ} \geq \frac{1}{\pi \times R_{INJ} \times f_{CO(EST)}}$$

Using a lower C_{INJ} gives better load transient performance in DCM and CCM, but it reduces phase margin. The optimal value should be selected using an iterative approach.

To make sure that there is no overshoot at the end of soft start, C_{INJ} should be selected according to the criterion in Equation 4-9.

EQUATION 4-9:

$$C_{INJ} \leq C_{FF} \times \frac{R_{FB(TOP)}}{R_{FB(BOT)}}$$

Add a resistor in parallel with the soft start capacitor, connected to the SS pin, if $C_{INJ} > C_{FF} \times (R_{FB(TOP)}/R_{FB(BOT)})$. This ensures that there is no overshoot at the end of soft start. However, the V_{OUT} will ramp up with reducing slope during soft start and this results in longer soft start time. Use Equation 4-10 to select the parallel resistor.

EQUATION 4-10:

$$R_{SS} \geq \frac{0.8V}{I_{SS}}$$

Where:

I_{SS} = Soft Start Current Source = 1.2 µA

7b) Select C_{INJ} using the below guidelines if $f_{CO(EST)}$ is below $f_{SW}/10$ when the f_{CO} is limited by the minimum FB ripple voltage required. The user may need to follow this method mainly in lower V_{OUT} applications where the FB ripple voltage limits the f_{CO}. Assume $f_{CO} = f_{SW}/10$. Calculate the maximum Equivalent Series Resistance (ESR) of the output capacitor using Equation 4-11.

EQUATION 4-11:

$$ESR_{COUT} \leq \frac{\Delta V_{OUT\_TRANS}}{\Delta I_{LOAD\_STEP}}$$

Where:

ΔI_{LOAD_STEP} = Magnitude of the Load Transient

ΔV_{OUT_TRANS} = Acceptable Output Voltage Deviation during Load Transient

Calculate the output capacitance using Equation 4-12.

EQUATION 4-12:

$$C_{OUT} \geq \frac{1}{\pi \times f_{CO} \times ESR_{COUT}}$$

Calculate C_{INJ} using Equation 4-13.

EQUATION 4-13:

$$C_{INJ} = C_{FF} \times \frac{ESR_{COUT}}{2 \times \pi \times f_{CO} \times L} \times \frac{V_{OUT}}{4.5V \times 100\ ns \times f_{SW}}$$

Using too low a C_{INJ} may result in oscillations at the beginning of the soft start. These oscillations can be reduced either by using a higher C_{INJ} or C_{OUT}, by reducing the feedback ripple.

4.3.2 RIPPLE INJECTION CIRCUIT COMPONENTS SELECTION FOR RIPPLE INJECTION FROM SW NODE

Follow the below steps for selecting ripple injection circuit components when ripple injection from the SW node is used.

1. Calculate the product of R_{INJ} and C_{FF} for a given injected Feedback Ripple Voltage, ΔV_{FB}, using Equation 4-14. Choose ΔV_{FB} in the range from 40 mV to 250 mV. A good starting point for ΔV_{FB} is 50 mV.

EQUATION 4-14:

$$R_{INJ} \times C_{FF} = \frac{V_{OUT}}{\Delta V_{FB(MIN)}} \times (1 - D_{MAX}) \times T_{SW}$$

Where:

$\Delta V_{FB(MIN)}$ = Minimum Injected Feedback Ripple Voltage

V_{OUT} = Output Voltage

D_{MAX} = Maximum Duty Cycle

T_{SW} = Switching Period

2. Choose C_{FF} in the range from 0.47 nF to 10 nF.
3. Calculate R_{INJ} using the above equation.
4. Calculate the Top Feedback Resistor, $R_{FB(TOP)}$ using Equation 4-15.

EQUATION 4-15:

$$R_{FB(TOP)} \geq \frac{1}{2 \times \pi \times C_{FF} \times 0.8 \times f_{LC}}$$

Where:

f_{LC} = Output Filter LC Resonant Frequency = 1/(2 x π x sqrt(L x C_{OUT}))

5. Calculate the Bottom Feedback Resistor, $R_{FB(BOT)}$ using Equation 4-16:

EQUATION 4-16:

$$R_{FB(BOT)} = \frac{R_{FB(TOP)}}{\left[\frac{V_{OUT}}{V_{REF}} - 1\right]}$$

Where:

V_{OUT} = Target Output Voltage

V_{REF} = Reference Voltage = 0.6V for MIC2129

6. Estimate the crossover frequency using Equation 4-17 If $f_{CO(EST)}$ is above $f_{SW}/5$, lower the C_{FF} value to increase the injected ripple voltage and go back to the step 2.

EQUATION 4-17:

$$f_{CO(EST)} = \frac{R_{INJ} \times C_{FF}}{2\pi \times L \times C_{OUT}}$$

Where:

L = Inductance of Power Inductor

C_{OUT} = Output Capacitance

7a) Select C_{INJ} using Equation 4-18 to get phase margin larger than 60 degree if $f_{CO(EST)}$ calculated above meets Equation 5-9.

EQUATION 4-18:

$$C_{INJ} \geq \frac{1}{\pi \times R_{INJ} \times f_{CO(EST)}}$$

Using a lower C_{INJ} gives better load transient performance in DCM and CCM, but it reduces phase margin. The optimal value should be selected using an iterative approach.

Make sure that there is no overshoot at the end of soft start. C_{INJ} can be selected according to the criterion in Equation 4-19.

EQUATION 4-19:

$$C_{INJ} \leq C_{FF} \times \frac{R_{FB(TOP)}}{R_{FB(BOT)}}$$

It must be ensured that the maximum feedback ripple which occurs at the maximum operating input voltage is below 250 mV (clamp value is 300 mV). Exceeding this limit causes the output to go out of regulation.

7b) Select C_{INJ} using the below guidelines if $f_{CO(EST)}$ is below $f_{SW}/10$ when the f_{CO} is limited by the minimum FB ripple voltage required. The user may need to follow this method mainly in lower V_{OUT} applications where the FB ripple voltage limits the f_{CO}. Assume $f_{CO} = f_{SW}/10$. Ensure that the maximum Equivalent Series Resistance (ESR) of the output capacitor is calculated using Equation 4-11 and the output capacitance is calculated using Equation 4-12. Calculate C_{INJ} using Equation 4-20.

EQUATION 4-20:

$$C_{INJ} = C_{FF} \times \frac{ESR_{COUT}}{2 \times \pi \times f_{CO} \times L}$$

Using too low C_{INJ} may result in oscillations at the beginning of soft start. These oscillations can be reduced either by using higher C_{INJ} or C_{OUT}, by reducing feedback ripple.

4.4 Device Description

4.4.1 MODES OF OPERATION

Table 4-1 summarizes the MIC2129 modes of operation for different configurations of the MODE pin.

TABLE 4-1: OPERATING MODE SELECTION SUMMARY

MODE pin Configuration	MIC2129 mode of operation
GND	CCM mode (all the time)
VDD	HLL mode with CCM soft start. CCM to DCM transition occurs after 120% of the soft start time when zero inductor current is detected at light loads.
Unconnected	CCM mode with DCM soft start. DCM to CCM transition occurs when SS pin voltage reaches 0.6V (100% of soft start time). This feature is intended to be used when feedback ripple is injected using SW node instead of using INJ pin.

4.4.2 CONTINUOUS CONDUCTION MODE (MODE = GND)

When the MODE pin is connected to GND, MIC2129 always operates in Continuous Conduction Mode (CCM).

Figure 4-4 below explains CCM operation. The HSFET is turned on when the transconductance g_m amplifier output V_{gm} goes below the reference voltage V_{REF_COM} which is 0.6V. The HSFET remains on until the ON-time which is generated by the T_{ON} generator expires. The ON-time generated by the T_{ON} generator depends on the VIN and the frequency setting resistor. Once the ON-time ends, LSFET will be turned on until the V_{gm} goes below the 0.6V reference.

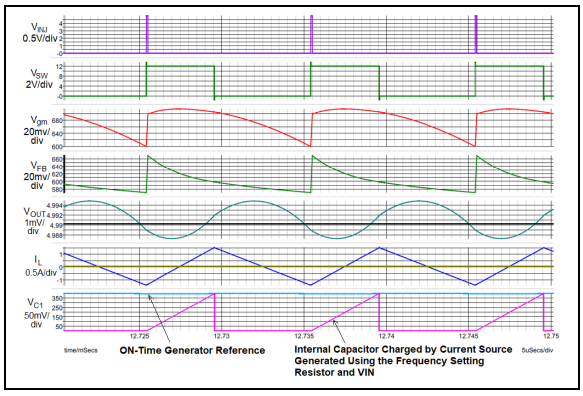


FIGURE 4-4: *MIC2129 Control Loop Steady-State Timing in Continuous Conduction Mode Operation.*

The ripple signal at V_{gm} which is necessary for Constant ON-time control is generated at the FBS node and is passed to the V_{gm} node using a low gain g_m amplifier. Ripple at the feedback is generated using the INJ pin and ripple injection components as explained in Section 4.3.1, Ripple Injection Circuit Components Selection for Ripple Injection from INJ Node.

4.4.3 HYPERLIGHT LOAD (HLL) MODE (MODE = VDD)

In Continuous Conduction mode, the inductor current can go negative at light loads. However, at light loads the MIC2129 can force the inductor current to operate in Discontinuous Conduction mode (DCM) and the inductor current does not go negative at light loads when MODE is set to HLL mode. When the MODE pin is connected to VDD, MIC2129 is in HLL mode and operates in CCM during soft start; CCM to DCM transition occurs after 120% of soft start time when zero inductor current is detected at light loads. In HLL mode, the efficiency is further optimized by shutting down all the non-essential circuits and minimizing the supply current. The MIC2129 wakes up and turns on the high-side MOSFET when the V_{gm} voltage drops below its 0.6V reference.

The MIC2129 has a zero-crossing comparator (ZC Detection) that monitors the inductor current by sensing the voltage drop across the low-side MOSFET during its ON-time. If the MIC2129 detects zero crossing, then the LSFET will be turned OFF and if there is no switching for 10 µs, the MIC2129 automatically powers down most of the IC circuitry and goes into a low-power mode (Sleep mode) after 10 µs.

Both high-side and low-side MOSFETs are kept in off state while the MIC2129 is in sleep mode. The load current is supplied by the output capacitors and V_{OUT} drops. If the drop of V_{OUT} causes V_{gm} to go below V_{REF_COM}, then all the circuits will wake up into normal Continuous Conduction mode. Figure 4-5 shows the steady-state control loop timing in Discontinuous Conduction mode.

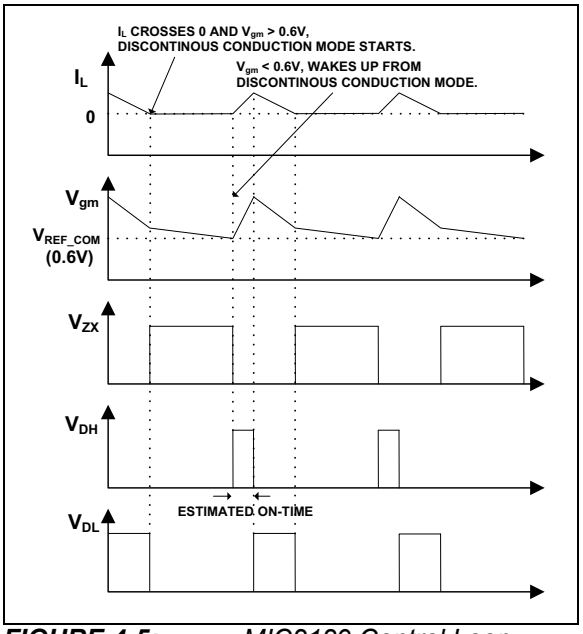


FIGURE 4-5: *MIC2129 Control Loop Steady-State Timing in Discontinuous Conduction Mode.*

During Discontinuous Conduction mode, the bias current of most circuits is reduced. As a result, the total device power supply current during Discontinuous Conduction mode is only about 700 µA, allowing the MIC2129 to achieve high efficiency in light load applications.

4.4.4 CCM WITH DCM SOFT START (MODE = UNCONNECTED)

When MODE pin is left unconnected, MIC2129 operates in DCM during soft start and transitions to CCM when SS pin voltage reaches 0.6V.

This feature is intended to be used when feedback ripple is injected using the SW node instead of using the INJ pin. Injecting feedback ripple using the SW node offers better start up performance compared with using the INJ pin in very low output voltage (0.8V or so), high current (10A, 20A, etc.) applications. These applications require higher crossover frequency to meet the output voltage tolerance during load dynamics. To achieve higher crossover frequency, the C_{FF} to C_{INJ} ratio should be higher. This increases the ripple voltage across C_{INJ} which can create oscillations at the beginning of soft start. These oscillations can be reduced using a series resistor and diode combination across R_{INJ} when feedback ripple is injected using INJ pin. The startup oscillations can be solved without these two components (a resistor and a diode) if feedback ripple is injected using the SW node.

With SW node injection, DCM startup is needed to ensure proper prebias startup performance. With the MODE pin left unconnected, DCM to CCM transition happens when the SS pin voltage reaches 0.6V.

The error amplifier reference is typically 13 mV lower than the SS voltage. So, the error amplifier reference is at 97.8% of the final 0.6V when the SS pin voltage is at 0.6V. At the instant when SS pin voltage reaches 0.6V, DCM to CCM transition happens and the error amplifier reference jumps from 97.8% to 100% as shown in Figure 4-6 (i.e. after the DCM to CCM transition happens, the reference does not follow the soft start pin voltage). This jump can create a momentary increase in inductor current so that feedback can catch the reference. Once the device transition to CCM is done, it always operates in CCM independent of the load current.

The g_m amplifier output clamp is reduced to 0.9V from 1.2V when MODE is left unconnected. This improves the startup behavior by reducing inductor current oscillations at the very beginning of the soft start. This is mainly visible in low output voltage, high load current applications where the output capacitance is huge. Figure 4-6 shows the Startup sequence when MODE pin is left unconnected.

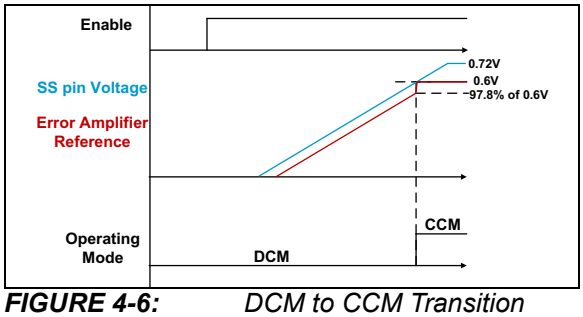


FIGURE 4-6: *DCM to CCM Transition when MODE is Unconnected.*

4.4.5 PRECISION ENABLE FUNCTION

The MIC2129 features precision enable input. The internal HVLDO is enabled only if the EN pin voltage is higher than its enable rising threshold of typically 1.2V with ±5% accuracy.

When the EN pin voltage is below its falling threshold, the MIC2129 enters Shutdown state. The EN pin enable threshold hysteresis is typically 65 mV.

The EN pin absolute maximum rating is the same as the VIN pin absolute maximum rating to allow customers to tie the EN pin to VIN for the device to start-up with VIN.

The EN input can be used as an external programmable input UVLO to disable the part when the input voltage falls below a target lower threshold and enable the device when the input voltage rises above a target upper threshold voltage. This is often used to prevent excessive battery discharge or early turn-on during start-up. This method is also recommended to prevent abnormal device operation in applications where the input voltage falls below the minimum of 4.5V. Figure 4-7 shows the connections to implement this method of UVLO. Equation 4-21 and Equation 4-22 can be used to determine the correct resistor values.

EQUATION 4-21:

$$R_{TOP} = R_{BOT} \times \left(\frac{V_{OFF}}{V_{ENTH} - V_{ENHYS}} - 1 \right), \text{ or}$$

$$R_{TOP} = R_{BOT} \times \left(\frac{V_{ON}}{V_{ENTH}} - 1 \right)$$

Where:

- R_{TOP} = Top Resistor of the VIN Voltage Resistor Divider
- R_{BOT} = Bottom Resistor of the VIN Voltage Resistor Divider
- V_{OFF} = Target V_{IN} Voltage below which Regulator turns off
- V_{ON} = Target V_{IN} Voltage above which Regulator Turns on
- V_{ENTH} = Device Enable Upper Threshold Voltage
- V_{ENHYS} = Enable Threshold Hysteresis Voltage

EQUATION 4-22:

$$V_{ON} = V_{OFF} \times \left(\frac{V_{ENTH}}{V_{ENTH} - V_{ENHYS}} \right)$$

A value of 20 kΩ, for R_{BOT} is a good first choice.

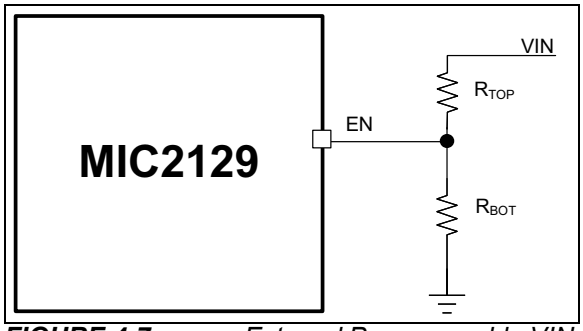


FIGURE 4-7: *External Programmable VIN UVLO Connections.*

4.4.6 SOFT START

Soft start (SS) reduces the power supply input surge current at startup by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up. A slower output rise time will draw a lower input surge current.

MIC2129 always starts up in CCM if the MODE pin is connected to either VDD or GND. The MIC2129 changes to DCM after SS pin voltage reaches 0.72V (120% of soft start time is reached) and zero inductor current is detected if the MODE pin is connected to

VDD. If MODE pin is left unconnected, startup is done in DCM until the SS pin voltage reaches 0.6V. Then, the device transitions from DCM to CCM.

The MIC2129 features adjustable soft start time. The soft start time can be adjusted by connecting capacitor (C_{SS}) between SS pin and GND pins as shown in the Figure 4-8 below. An internal current source (I_{SS}) charges the capacitor connected to SS pin. The SS pin voltage is used as the reference to the internal error amplifier while it is rising from 0V to internal reference of 0.6V. Once the SS pin voltage reaches to 0.6V, the reference to the error amplifier is switched to internal fixed 0.6V reference.

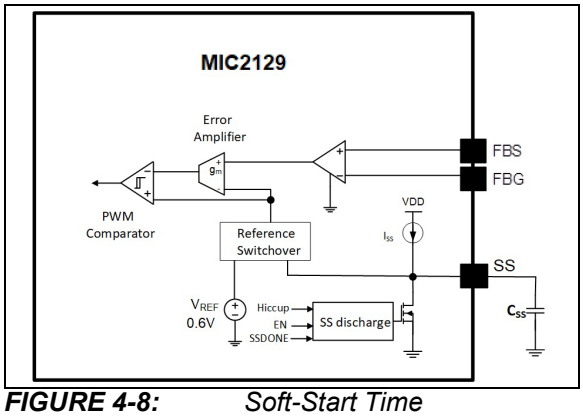


FIGURE 4-8: *Soft-Start Time Programming.*

The soft start capacitor value for the desired V_{OUT} soft-start ramp-up time can be calculated from Equation 4-23.

EQUATION 4-23:

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{REF}}$$

Where:

t_{SS} = Output Voltage Soft Start Ramp-up Time
V_{REF} = 0.6V Reference Voltage
I_{SS} = Internal Soft-start Current Source = 1.2 µA

Adding an additional resistor across C_{SS} as shown in Figure 4-9 helps in reducing V_{OUT} overshoot at the end of soft start when $C_{INJ} > C_{FF} \times R_{FB(TOP)}/R_{FB(BOTTOM)}$.

This is achieved by reducing the SS voltage slew rate when the SS voltage is close to the target value.

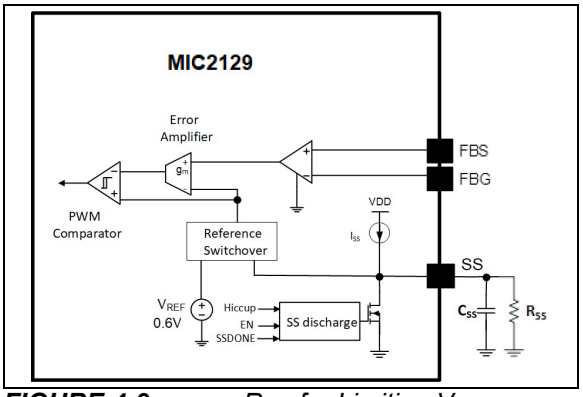


FIGURE 4-9: *R_{SS} for Limiting V_{OUT} Overshoot at the End of Soft-start.*

Note that the SS voltage goes above 0.72V (i.e the additional resistor across C_{SS} should not limit the SS pin voltage to 0.72V) as the device detects 0.72V at SS pin as SSDONE to change the mode from CCM to DCM when the MODE pin is set to HLL mode and zero inductor current is detected.

The following equation calculates the minimum value for the additional resistor across C_{SS}.

EQUATION 4-24:

$$R_{SS} > \frac{0.72V}{I_{SS}}$$

Where:

I_{SS} = Soft Start Current Source = 1.2 µA

After the device is enabled, a bias ready signal goes high after ≈4 ms. At this instant, the soft start current source (I_{SS}) is enabled. The soft start current, I_{SS}, charges the capacitor connected at the SS pin. The MIC2129 starts switching once the SS pin voltage is above the FB pin voltage.

The reference to the internal error amplifier is the SS pin voltage as long as the SS pin voltage is below the internal fixed reference of 0.6V.

The reference to the internal error amplifier switches from the SS pin voltage to the internal fixed reference of 0.6V once the SS pin voltage exceeds 0.6V.

Internal Soft Start Done (SSDONE) signal goes high once the SS pin voltage is 0.72V (which is 120% of the 0.6V reference). The soft-start capacitor at the SS pin is discharged once the SSDONE signal goes high.

4.4.7 CURRENT LIMIT (ILIM) (POSITIVE CURRENT LIMIT)

The MIC2129 uses either the $R_{DS(ON)}$ of the external low-side power MOSFET (LS FET) or an external current sense resistor to detect over-current conditions. Using the LS FET $R_{DS(ON)}$ for current sensing avoids additional cost, use of additional board space and power losses by a discrete current sense resistor. The following Figure 4-10 shows the equivalent current limit scheme used in MIC2129.

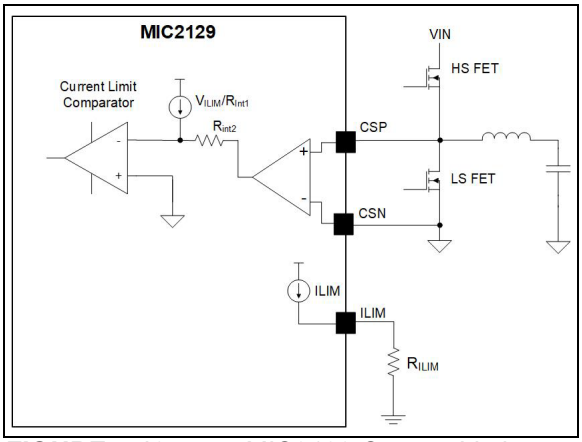


FIGURE 4-10: *MIC2129 Current-Limit Circuit with LSFET as Current-Sense Element.*

The current limit threshold can be set by connecting a resistor R_{ILIM} from ILIM to GND. An internal current source (I_{ILIM}) develops a voltage across R_{ILIM}. This voltage is converted into a current by an internal resistor (R_{int1}). This current is passed through another internal resistor R_{int2}. This voltage across R_{int2} is summed to the CS pin voltage and the summed voltage is compared with PGND to detect a current limit event as shown in Figure 4-10. The current limit is triggered when Equation 4-25 is satisfied.

EQUATION 4-25:

$$\left(I_{ILIM} \times R_{ILIM} \times \frac{R_{INT2}}{R_{INT1}}\right) + V_{CS} = 0$$

Where:

I_{ILIM}	=	ILIM Threshold Setting Current Source, 9.6 µA for resistor sensing and 19.2 µA for LS FET R_{DSON} sensing
R_{ILIM}	=	Current Limit Threshold Setting Resistor
R_{INT2}/R_{INT1}	=	Internal Voltage Gain, 0.25
V_{CS}	=	Current-Sense Voltage across Current-Sense Element

Based on the above equation, the current limit threshold is given by Equation 4-26.

EQUATION 4-26:

$$V_{CSTH(ILIM)} = I_{ILIM} \times R_{ILIM} \times 0.25$$

The current limit setting resistor R_{ILIM} can be determined from Equation 4-27.

EQUATION 4-27:

For DC overload in Hiccup or Latch-off CLS settings:

$$R_{ILIM} = \frac{\left\{\left(I_{CLIM} + \frac{\Delta I_{LPP}}{2}\right) \times R_{SENSE} \times F_{HEAT} + V_N\right\} \times 4}{I_{ILIM}}$$

For DC overload in Cycle-by-cycle CLS setting or Output Short-circuit Current Limit:

$$R_{ILIM} = \frac{\left(I_{CLIM} - \frac{\Delta I_{LPP}}{2}\right) \times R_{SENSE} \times F_{HEAT} \times 4}{I_{ILIM}}$$

Where:

I_{CLIM}	=	Desired Output Current Limit
ΔI_{LPP}	=	Ripple Inductor Current
R_{SENSE}	=	Resistance of Current-sense Element, can be LSFET R_{DSON} or fixed sense resistor
I_{ILIM}	=	Current Source at ILIM pin, 9.6 µA for resistor sensing and 19.2 µA for low-side MOSFET R_{DSON} sensing
F_{HEAT}	=	Heat-up Factor, ~1.5 for LSFET R_{DSON}, 1 for Fixed Sense Resistor
V_N	=	Residue Switching Spike Noise Voltage after Blanking Time, ~10 mV with 100 pF filter capacitor across CSP and CSN pins, and 100Ω filter resistor between Drain of LSFET and CSP pin

The current-sense circuit has a blanking time of 142 ns. The minimum OFF-time for current sensing is ~ 224 ns after this blanking expires.

The MIC2129 current limit threshold variation with temperature is selectable according to the external current sense element used. MIC2129 sets the ILIM source current and the corresponding temperature coefficient (Tempco) by detecting the sensing element. The ILIM source current and Tempco will be set to 19.2 µA and 5100 ppm/°C respectively if the current sense element is the LS FET R_{DSON}, to compensate for the positive Tempco of the external LS FET R_{DSON}. The ILIM source current and Tempco will be set to 9.6 µA and zero Tempco respectively if the current-sense element is an external current-sense resistor between the source of low-side MOSFET and PGND, since the fixed current-sense resistor has zero Tempco.

Detecting the current-sense element is done by sensing the CSP voltage while the high-side FET (HS FET) is ON.

The maximum positive current limit threshold of the MIC2129 is 300 mV.

4.4.8 CURRENT LIMIT OPERATING MODE SELECTION (CLS)

MIC2129 features a selectable operating mode when the current limit is detected. CLS pin is a 3-state pin that gives 3 selectable current limit operating modes as listed in Table 4-2.

Independent of the CLS status, the MIC2129 skips turning on the high-side driver (i.e. skips turning on the HS MOSFET) as long as the sensed current is higher than the set current limit threshold. The high-side driver and HS MOSFET are allowed to turn on again only when the sensed current signal has fallen below the set current limit threshold, and the next switching cycle starts.

For both Hiccup and Latch-off CLS settings, the over-current limit events are counted by an over-current limit counter. When Hiccup is set for the CLS setting and 15 consecutive switching cycles of over-current limit events are counted, the device enters Hiccup mode. In Hiccup mode, both high-side and low-side MOSFET drivers are OFF for a period of Hiccup time. The device will automatically restart with normal soft start after the Hiccup timer expires. When Latch-off is set for the CLS setting and the over-current limit counter reaches 15 counts, both the HS and LS MOSFET drivers are latched OFF. Cycling the Enable or cycling the VIN is required to re-start the device.

For DC overload in Hiccup or Latch-off CLS setting, the 15 over-current limit events are counted at the peak inductor current.

When the Cycle-by-cycle current limit is selected for the CLS setting, all the over-current limit events are not counted by the over-current limit counter. When the over-current limit threshold is reached in Cycle-by-cycle mode, the HS driver and HS MOSFET are skipped from turning on until the sensed current falls below the current limit, and the new switching cycle starts. The switching cycles continue this way and do not stop. This operation results in a consequence that the valley inductor current is regulated at the set current limit. This behavior is similar in an output overload or short-circuit condition.

Since the MIC2129 continues normal switching operations with valley inductor current regulated at the set current limit in Cycle-by-cycle CLS setting, the power MOSFETs and power inductor used in the buck converter must be able to handle the high current at the current limit level for the time of over-current operation, otherwise, these power train components will be damaged by the high-power operation.

TABLE 4-2: CURRENT LIMIT OPERATING MODE SELECTION

CLS status	Function	Description
VDD	Hiccup Mode	Both the MOSFET drivers (DL and DH) are OFF for a duration equal to "Hiccup timeout" which is equal to the 120% (100% if MODE = Float) of the SS time + ≈3 ms when the current limit counter reaches 15. The MIC2129 initiates a normal SS once the hiccup timeout elapses. If the current limit counter reaches 15 again during SS, the above sequence repeats.
Float	Latch-off	Both the MOSFET drivers (DL and DH) are OFF once the MIC2129 current limit counter reaches 15. To enable switching, either VIN cycling or Enable cycling is required.
GND	Cycle-by-Cycle Current Limit	In this mode, the MIC2129 does not stop switching even if it detects current limit. Instead, the MIC2129 skips turning on the DH driver as long as the sensed current is higher than the set current limit. This results in a behavior where the inductor valley current is regulated to the set current limit. The peak current under this operation depends on the input voltage, Inductor value, load impedance etc.

Figure 4-11 shows the events of actions while in over-current at shorted output when CLS pin is configured to Hiccup mode (i.e. CLS pin connected to VDD).

When the over-current limit event is detected after the 142 ns blanking time, the over-current limit counter starts counting the over-current limit event for each switching cycle. Once the over-current limit counter reaches 15, the capacitor connected at the SS pin is charged until it's voltage reaches 120% of 0.6V for a duration of a hiccup timeout period. During this period, the gate driver outputs of the MIC2129 (DH and DL) are disabled (i.e. the MIC2129 is in high impedance state). The inductor current discharges through the body diode of the low-side MOSFET until it reaches 0A.

After the hiccup timeout (120% of soft-start time) expires, the MIC2129 automatically attempts to restart and goes through a normal startup sequence shown in Figure 4-11.

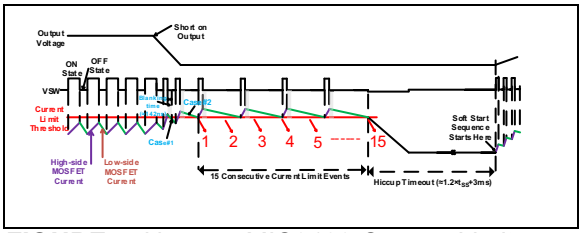


FIGURE 4-11: *MIC2129 Current Limit Event of Actions when CLS Pin is Configured to Hiccup Mode and the Valley Current Limit Relationship to Output Current.*

The total hiccup time (i.e. the duration in which the MIC2129 is in high impedance state where the DH and DL are in OFF state) can be approximated by the below equation:

EQUATION 4-28:

$$t_{Hiccup} \approx (1.2 \times t_{SS}) + 3ms$$

Where:

t_{SS} = Soft Start Time

4.4.9 NEGATIVE CURRENT LIMIT

The MIC2129 supports a cycle-by-cycle negative current limit in CCM. The negative current limit threshold in CCM depends on the positive current limit threshold set by the R_{ILIM} resistor connected to the ILIM pin and is given in Equation 4-29.

If the negative low-side MOSFET current triggers the negative current limit during the reversed inductor current in current sinking operation in CCM, the LS FET will be turned off and allow the negative reversed inductor current through the HS FET body diode back to the input bulk capacitor and input power supply. To prevent a huge reversed current over a persistent negative over current condition, the low-side MOSFET is turned back on after ~ 1 µs until the negative current limit is triggered again, maintaining the peak of reversed inductor current at the programmed negative current limit level.

EQUATION 4-29:

$$V_{CSTH\_NILIM} = [0.5 \times V_{CSTH\_ILIM}] - 3mV$$

Where:

V_{CSTH_NILIM} = Negative Current Limit Threshold

V_{CSTH_ILIM} = Positive Current Limit Threshold Set by the R_{ILIM} Resistor at ILIM pin

4.4.10 SELECTABLE GATE DRIVER VOLTAGE

The MIC2129 features a selectable gate drive voltage which allows user to use either standard or logic level MOSFETs. The selectable gate drive voltages are 5.2V, 7.5V or 10.5V. The PVDDSEL pin selects the gate drive voltage according to the following table.

TABLE 4-3: GATE DRIVER VOLTAGE SELECTION TABLE

PVDDSEL Pin	PVDD Voltage
VDD	10.5V
FLOAT	7.5V
GND	5.2V

The different gate drive supply voltage (PVDD) settings together with the high-voltage LDO or low-voltage EXTVDD LDO setting can have different impact on the conversion power loss and efficiency of the step-down converter as illustrated in Figure 4-12.

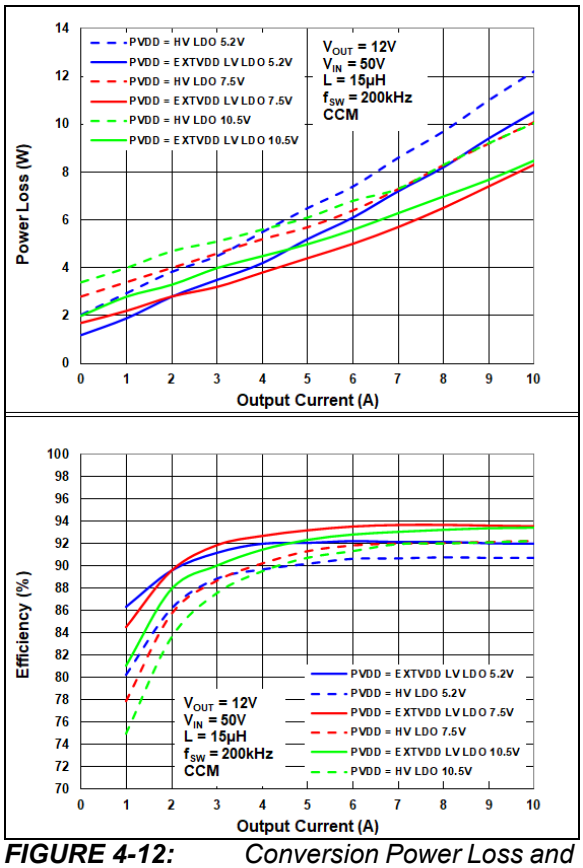


FIGURE 4-12: *Conversion Power Loss and Efficiency vs. I_{OUT} at Different PV_{DD} Voltage Settings (HS FET: 2x FDMS86201, LS FET: 1x BSC0302LS).*

The 5.2V PV_{DD} gate driver supply voltage is recommended for driving some logic level MOSFETs with smaller gate charge for achieving better efficiency at lighter output loads. This can be seen in Figure 4-12. The power loss is the smallest and the efficiency is the highest for output current less than 2A with the solid blue curve representing the 5.2V PV_{DD} voltage.

The 7.5V PV_{DD} gate driver supply voltage is recommended for driving MOSFETs with medium gate charge value and smaller R_{DSON} for achieving better efficiency at medium output load range applications. This can be shown in Figure 4-12 that the power loss is the lowest and the efficiency is the highest at output current in the range from 2A to 10A for the solid red curve representing the 7.5V PV_{DD} voltage.

The 10.5V PVDD gate driver supply voltage is recommended for driving MOSFETs with relatively large gate charge and much smaller Rdson for obtaining better efficiency at heavy output load applications larger than 10A. The extrapolation trend of Figure 4-12 indicates that the power loss is the lowest and the efficiency is the highest at output current larger than 10A for the solid green curve representing the 10.5V PV_{DD} voltage.

The solid curves denote the corresponding power loss and efficiency data with different PV_{DD} voltages (blue for 5.2V, red for 7.5V, green for 10.5V) generated from the EXTVDD low-voltage LDO, and the dotted curves denote the corresponding power loss and efficiency data with different PV_{DD} voltages generated from the high-voltage LDO. Due to the better thermal performance and efficiency of the EXTVDD low-voltage LDO, the solid curve data shows better performance than the dotted curve data of the same color as illustrated in Figure 4-12.

4.4.11 PVDD, EXTVDD AND VDD LDO

Figure 4-13 shows the MIC2129 internal LDOs' configuration. The MIC2129 features three internal LDOs: high-voltage LDO, low-voltage EXTVDD LDO and bias LDO. The high-voltage LDO and low-voltage LDO are used to supply PVDD voltage for the gate drivers from either the VIN or EXTVDD pins. The bias LDO is used to supply 4.5V VDD voltage for internal control circuits.

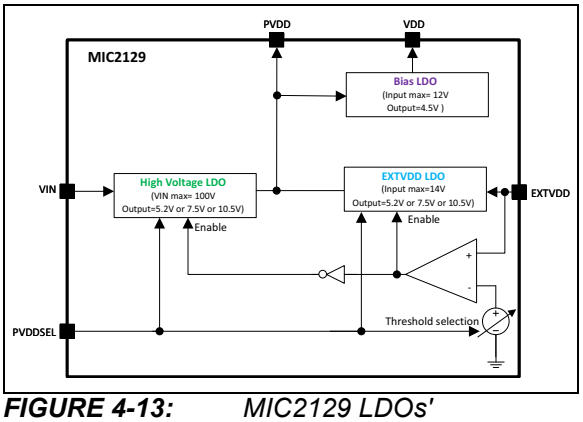


FIGURE 4-13: *MIC2129 LDOs' Configuration.*

Once the MIC2129 is enabled (EN pin voltage>EN rising threshold), the HV LDO (High Voltage LDO) and Bias LDO are enabled. The EXTVDD LDO is enabled if EXTVDD is above its rising threshold (which depends on the PVDD setting) and the Soft-Start is completed (i.e. once SS pin voltage reaches 120% of the 0.6V if MODE is connected to either VDD or GND and 100% of 0.6V if MODE is left unconnected). When the EXTVDD LDO is in disable state, it does not sink current from PVDD. The EXTVDD supports at most 14V on its input which allows the user to use the converter output up to 14V to power the MIC2129 drivers and internal bias. The EXTVDD rising threshold is adjusted automatically depending on the PVDDSEL selection. The LDO's are disabled while the device is in thermal shutdown.

TABLE 4-4: INTERNAL LDOS DETAILS

LDO	Input Voltage Range	Output Voltage	Active	Dropout Voltage
High Voltage LDO	Up to 100V	Selectable among 5.2V, 7.5V, 10.5V by PVDDSEL pin.	Active if EXTVDD voltage is below its falling V_{TH}.	Refer to the Electrical Characteristics table
EXTVDD LDO	Up to 14V	Selectable among 5.2V, 7.5V, 10.5V by PVDDSEL pin.	Active if EXTVDD voltage is above its rising V_{TH} (once PVDD is above its UVLO rising V_{TH}).	
Bias LDO	PVDD	4.5V		

4.4.12 POWER GOOD (PG)

The Power Good (PG) pin is an open-drain output, which is logic high when the output voltage is nominally over 90% of its steady-state voltage. A pull-up resistor of more than 10 kΩ should be connected from PG to VDD for the PG pin logic high indication when the VOUT is good and to minimize the power consumption for the PG pin logic low indication when the VOUT is not good. During soft start, the PG pin is held low and is allowed to be pulled high after VOUT has reached over 90% of the target level. The PG pin is pulled low when the output voltage is below 83% of the target level in steady-state.

4.4.13 INTERNAL COMPENSATION

Figure 4-14 shows the MIC2129 control loop equivalent circuit with internal compensation. There is an Internal compensation capacitor between FBS pin and the g_m amplifier output.

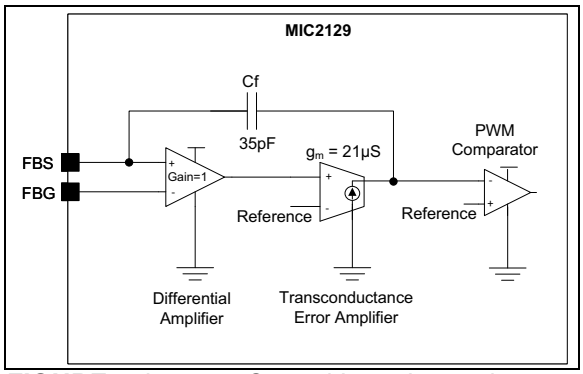


FIGURE 4-14: *Control Loop Internal Compensation.*

4.4.14 OUTPUT VOLTAGE REMOTE SENSE

The following Figure 4-15 shows the equivalent circuit of output voltage remote sense. The MIC2129 has a “unity gain” differential amplifier which translates the differential voltage across FBS and FBG pins to its output with respect to the MIC2129 GND. The closed loop formed by the error amplifier and power stage regulates the output of the differential amplifier to the internal reference of 0.6V.

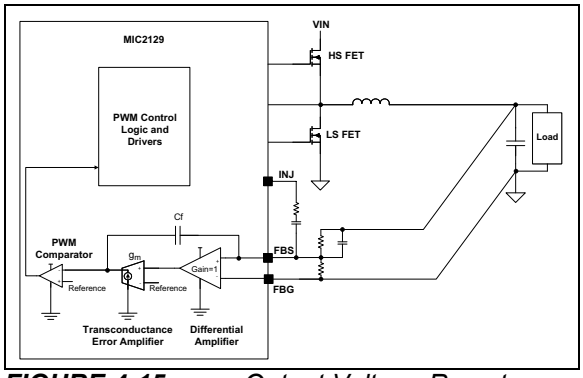


FIGURE 4-15: *Output Voltage Remote Sense.*

4.4.15 ADJUSTABLE SWITCHING FREQUENCY

The MIC2129 features programmable switching frequency from 100 kHz to 800 kHz by connecting a resistor (R_{FREQ}) between the FREQ pin and GND as shown in Figure 4-16. When a new on-time event is triggered, the T_{ON} is turned on at the T_{ON} generator and feeds the Control Logic to drive the DH high and a current source programmed by the RFREQ resistor charges up an internal capacitor C1. The voltage V_{C1} across the capacitor C1 is compared with a voltage V_{CM}.

The V_{CM} is an averaged voltage from the VSNS pin and divided down by an internal resistor divider with DC gain K_{VOUT} = 1/6 (i.e. $V_{CM} = V_{SNS(AVG)} \times K_{VOUT}$). When V_{C1} ramps up to equal to V_{CM}, the T_{ON} is turned off and this generates the length of the T_{ON} pulse.

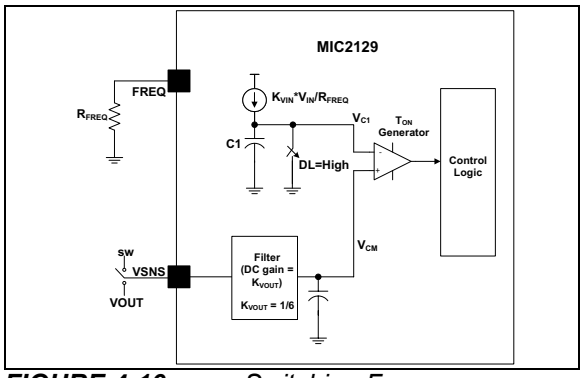


FIGURE 4-16: *Switching Frequency Setting and T_{ON} Generator Circuit.*

The On-Time can be calculated using Equation 4-30.

EQUATION 4-30:

$$T_{ON} = \frac{K_{VOUT}}{K_{VIN}} \times \frac{V_{SNSAVG}}{V_{IN}} \times R_{FREQ} \times C1$$

Where:

K_{VOUT}	=	Gain of Int. Resistor Divider Circuit at VSNS = 1/6
K_{VIN}	=	Gain of the Current Generator = 1/30
V_{SNSAVG}	=	Average Voltage of the VSNS Pin Voltage, which is always V_{OUT} (Output Voltage) whether VSNS is Connected to SW or V_{OUT}
R_{FREQ}	=	Resistor Connected from FREQ Pin to GND
$C1$	=	Internal Capacitor for ON-time and Frequency Programming

Equation 4-31 calculates the switching frequency for a given R_{FREQ}.

EQUATION 4-31:

$$f_{SW} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{T_{ON}}$$

By substituting T_{ON} from the Equation 4-30 in Equation 4-31, Equation 4-32 is derived as below:

EQUATION 4-32:

$$f_{SW} = \frac{K_{VIN}}{K_{VOUT} \times C1} \times \frac{1}{R_{FREQ}}$$

From the Equation 4-32, the switching frequency is inversely proportional to R_{FREQ} for a given K_{VIN}, K_{VOUT} and C1. The K_{VIN} = 1/30, K_{VOUT} = 1/6, C1 ≈ 10 pF. The equation can be further simplified with some adjustment to account for the actual internal component value as Equation 4-33.

EQUATION 4-33:

$$f_{SW} = \frac{20.4 \times 10^9}{R_{FREQ}}$$

K_{VOUT} limits the maximum V_{OUT} because the T_{ON} generator input does not support more than about 3V (i.e. $V_{CM(MAX)}$ = 3V). With K_{VOUT} = 1/6, and to allow adequate margin, VSNS can be shorted to the SW pin for most applications where V_{OUT} ≤ 14V. For V_{OUT} > 14V, VSNS should be tied to V_{OUT} using an external resistor divider as shown in Figure 4-17.

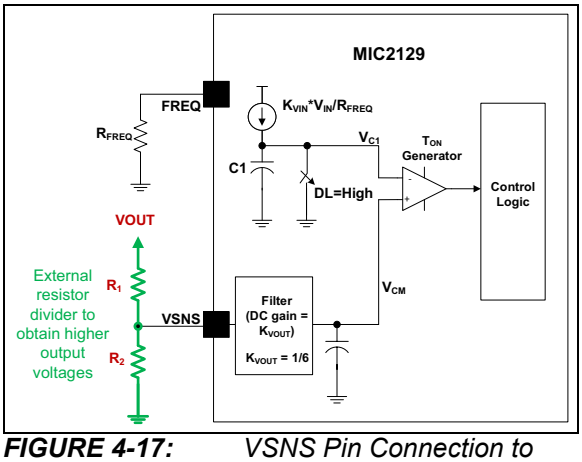


FIGURE 4-17: *VSNS Pin Connection to Obtain Higher Output Voltage.*

The VSNS node voltage must always be limited to 14V or less. For the external divider configuration at VSNS pin, the ON-time can be determined by Equation 4-34.

EQUATION 4-34:

$$T_{ON} = \frac{K_{VOUT(EXT)} \times K_{VOUT}}{K_{VIN}} \times \frac{V_{SNSAVG}}{V_{IN}} \times R_{FREQ} \times C1$$

Where:

$K_{VOUT(EXT)}$	=	Gain of the External Resistor Divider at VSNS Pin

Equation 4-35 calculates the switching frequency for a given R_{FREQ} with the external divider configuration for V_{OUT} > 14V applications.

EQUATION 4-35:

$$f_{SW} = \frac{K_{VIN}}{K_{VOUT(EXT)} \times K_{VOUT}} \times \frac{1}{C1 \times R_{FREQ}}$$

Given that K_{VIN} = 1/30, K_{VOUT} = 1/6, C1 = 10 pF, $K_{VOUT(EXT)}$ = R2/(R1+R2), Equation 4-35 can be simplified to Equation 4-36. The input impedance of VSNS is ~ 7 MΩ; therefore R1 and R2 must be < 7 MΩ to achieve good switching frequency setting accuracy.

EQUATION 4-36:

$$f_{SW} = \frac{R1 + R2}{R2} \times \frac{20.4 \times 10^9}{R_{FREQ}}$$

4.4.16 OUTPUT OVERVOLTAGE PROTECTION

The MIC2129 features output overvoltage protection (OVP) which triggers the MIC2129 to stop switching. OVP is detected at the FB pin and its threshold is typically 112% of V_{REF}. The input to the OVP comparator is the output of the remote sense amplifier. When the output of remote sense amplifier is higher than the OVP threshold for at least 18 µs (typ. OVP delay), the device stops switching.

Either EN cycling or power cycling is needed to enable the device back on, provided that VDD discharges below its falling threshold before either EN is pulled high or Input power is applied back.

4.4.17 THERMAL SHUTDOWN

The MIC2129 packages have an exposed pad (EP) to help mitigate IC junction temperature rise, especially for the higher power dissipation of the high-voltage LDO at high input voltage conditions.

The EP must be connected to the large ground plane of the PCB with sufficient thermal vias to allow the PCB to serve as an effective heatsink, spreading the heat away to the surrounding ambient.

When the junction temperature of the MIC2129 rises to the thermal shutdown upper threshold of +155°C (typical), thermal shutdown is triggered, and device enters shutdown during which switching is stopped and all the LDOs (HV LDO, EXTVDD LDO and Bias LDO) are kept off.

When the IC device's junction temperature falls below the thermal shutdown lower threshold of 140°C (typical), all the LDOs (HV LDO, EXTVDD LDO and Bias LDO) turn back on again and the MIC2129 buck converter soft starts again.

4.4.18 BREAK BEFORE MAKE TIME

Break Before Make (BBM) time ensures that both the HS FET and LS FET are not driven on simultaneously, preventing so-called shoot-through. Figure 4-18 shows the BBM timing diagram. In the diagram, the swON signal is the internal control logic signal to control the ON and OFF in each switching cycle, DL is the low-side gate driver signal, DH is the high-side gate driver signal, SW is the switching node signal.

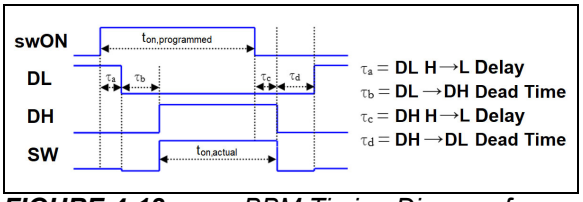


FIGURE 4-18: *BBM Timing Diagram for Forward Inductor Current Situation.*

τ_b includes a fixed 6 ns delay after DL drops below 1V and high side driver delay. Typical τ_b is 50 ns. Similarly, τ_d includes a fixed 6 ns delay after SW drops below 1V and the low side driver delay.

τ_a is DL high-to-low delay and τ_c is DH high-to-low delay.

For forward inductor current, SW is low during both dead times. Therefore, the true t_{ON} is shorter than the programmed t_{ON}. To compensate for this, an incoming T_{ON} pulse width at the swON signal is extended by ~43 ns which matches programmed t_{ON} and true t_{ON} for a typical simulation with C_{LOAD} = 3300 pF.

At light loads, SW node takes a long time to drop after DH goes low. As the Break-before-make logic requires SW to drop below 1V before DL is turned ON, the slow SW node fall at light load increases effective T_{ON}. This in turn increases T_{OFF} and hence f_{SW} reduces. To mitigate this, the maximum BBM time is limited to 100 ns.

4.4.19 MINIMUM OFF-TIME

The MIC2129 maintains DL input high for a duration at least equal to the current-sense blanking time (τ_{blk}) plus current-limit comparator settling time (τ_{cmp}) once it is high. Therefore, a minimum OFF-time is established, and it is necessary to ensure that the bootstrap capacitor C_{BST} has sufficient time to replenish during the OFF-time for the LS FET turn-on. This ensures that there is sufficient voltage across the C_{BST} to supply the high-side floating gate driver to turn on the HS FET during the ON-time. The following Figure 4-19 shows the timing diagram.

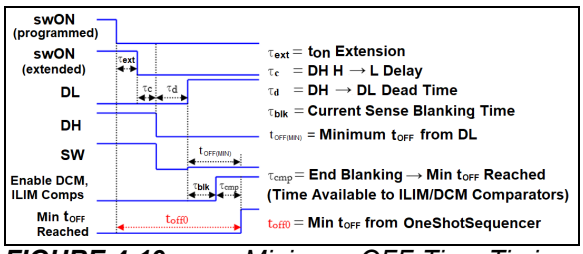


FIGURE 4-19: *Minimum OFF-Time Timing Diagram.*

The low-side gate driver minimum ON-time ($t_{OFF(MIN)}$) equals current-sense blanking time plus current-limit comparator settling time ($\tau_{blk} + \tau_{cmp}$).

The minimum OFF-time at the SW node equals the BBM time (τ_d) plus the DL minimum ON-time ($t_{OFF(MIN)}$). This ignores the external MOSFETs' gate turning OFF and ON times

4.4.20 MINIMUM CONTROLLABLE ON-TIME

The MIC2129 maintains DH input high for a duration at least equal to the “Minimum controllable ON-time” once it is high. This is to ensure that the LS FET is not turned on as long as the HS driver output is high once HS driver PWM logic is high. This protects the MOSFETs from shoot-through.

The minimum high-side PWM logic ON-time is larger than the level shifter delay plus HS Driver propagation delay plus HS driver rise time.

The design target for minimum controllable ON-time for MIC2129 is 100 ns (typical).

5.0 APPLICATION INFORMATION

5.1 Inductor Selection

Values for inductance, peak, and RMS currents are required to select the output inductor. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current. Generally, higher inductance values are used with higher input voltages and/or higher output voltages. Larger peak-to-peak ripple currents increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents also require higher output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value, and therefore a larger and more expensive inductor. Higher switching frequencies allow the use of a small inductance but increase power dissipation in the inductor core and MOSFET switching loss. A good rule-of-thumb is to set the ripple current to be 20% to 40% of the maximum DC output current of the buck converter. This typically provides a decent compromise on size, loss, cost, and transient performance. The inductance value of the inductor is calculated by Equation 5-1:

EQUATION 5-1:

$$L = \frac{V_{OUT} \times (Eff \times V_{IN(MAX)} - V_{OUT})}{Eff \times V_{IN(MAX)} \times f_{SW} \times DIR \times I_{OUT(MAX)}}$$

Where:

f_{SW}	=	Switching Frequency
DIR	=	Ratio of Inductor Ripple Current to Maximum DC Output Current, $\Delta I_{L(PP)}/I_{OUT(MAX)}$, about 0.2 to 0.4
$V_{IN(MAX)}$	=	Maximum Power Stage Input Voltage
Eff	=	Efficiency of the Buck Converter
$I_{OUT(MAX)}$	=	Maximum DC Output Current

The peak-to-peak inductor ripple current is calculated using Equation 5-2:

EQUATION 5-2:

$$\Delta I_{L(PP)} = \frac{V_{OUT} \times (Eff \times V_{IN(MAX)} - V_{OUT})}{Eff \times V_{IN(MAX)} \times f_{SW} \times L}$$

The maximum peak inductor current is equal to the maximum average output current plus one-half of the peak-to-peak inductor ripple current as given in Equation 5-3.

EQUATION 5-3:

$$I_{L(PK)MAX} = I_{OUT(MAX)} + 0.5 \times \Delta I_{L(PP)}$$

Where:

$I_{OUT(MAX)}$	=	Maximum Average DC Output Current

The RMS inductor current is used to calculate the I^2R losses in the inductor.

EQUATION 5-4:

$$I_{L(RMS)} = \sqrt{I_{OUT(MAX)}^2 + \frac{\Delta I_{L(PP)}^2}{12}}$$

Maximizing efficiency requires selecting the proper core material and minimizing the winding resistance. The high-frequency operation of the MIC2129 requires the use of ferrite materials for all but the most cost-sensitive applications. Lower-cost iron powder cores may be used but the increase in core loss reduces the efficiency of the buck converter. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized, although this usually comes at the expense of a larger inductor size. The power dissipated in the inductor is equal to the sum of the core and copper losses. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the magnetics vendor. Copper loss in the inductor is calculated by Equation 5-5:

EQUATION 5-5:

$$P_{INDUCTOR(Cu)} = I_{L(RMS)}^2 \times R_{WINDING}$$

The resistance of the copper wire, $R_{WINDING}$, increases with the temperature. The value of the winding resistance used should be at the operating temperature:

EQUATION 5-6:

$$R_{WINDING(HT)} = R_{WINDING(20^{\circ}C)} \times [1 + 0.0042 \times (T_H - T_{20^{\circ}C})]$$

Where:

T_H	=	Temperature of Wire Under Full Load
$T_{20^{\circ}C}$	=	Ambient Room Temperature
$R_{WINDING(20^{\circ}C)}$	=	Room Temperature Winding Resistance (usually specified by the manufacturer)

5.2 Output Capacitor Selection

The output capacitor is usually determined by its capacitance and equivalent series resistance (ESR). Voltage and RMS current capability are two other important factors in selecting the output capacitor. Recommended capacitor types are ceramic, low-ESR aluminum electrolytic, and aluminum-polymer dielectrics. The output capacitor's ESR is usually the main cause of the output ripple voltage in a steady-state, while the total output capacitance must be large enough to sustain and maintain the output voltage during load transient to meet the desired load transient output voltage requirement.

The total output ripple voltage is a combination of the ripple voltages caused by the ESR and output capacitance. The output ripple voltage of buck converter in steady-state can then be determined from Equation 5-7.

EQUATION 5-7:

$$\Delta V_{OUT(PP)} = \sqrt{\left(\frac{\Delta I_{L(PP)}}{8 \times C_{OUT} \times f_{SW}}\right)^2 + \left(\Delta I_{L(PP)} \times ESR_{COUT}\right)^2}$$

Where:

$\Delta V_{OUT(PP)}$	=	Peak-to-Peak Output Ripple Voltage
$\Delta I_{L(PP)}$	=	Peak-to-Peak Inductor Ripple Current
C_{OUT}	=	Output Capacitance
f_{SW}	=	Switching Frequency
ESR_{COUT}	=	ESR of Output Capacitor

The minimum output capacitance required for buck converter in steady-state can be estimated by Equation 5-8.

EQUATION 5-8:

$$C_{OUT} \geq \frac{\Delta I_{L(PP)}}{8 \times \Delta V_{OUT(PP)} \times f_{SW}}$$

To meet the load transient requirement, the output capacitance should also fulfill the Equation 5-9 for step-up load and Equation 5-10 for load release. The output capacitance value chosen must meet these three equations.

EQUATION 5-9:

$$C_{OUT} \geq \frac{\Delta I_{LOAD}}{\Delta V_{OUT(TRANS)} \times \pi \times f_{CO}}$$

Where:

ΔI_{LOAD}	=	Output Load Current Step in Load Transient
$\Delta V_{OUT(TRANS)}$	=	Magnitude of Output Voltage Drop in Step-up Load Transient
f_{CO}	=	Crossover Frequency and is about $f_{SW}/10$

EQUATION 5-10:

$$C_{OUT} \geq \frac{L \times (I_{L(PK)})^2}{(V_{OUT} + \Delta V_{O(MAX)})^2 - V_{OUT}^2}$$

Where:

$I_{L(PK)}$	=	Peak Inductor Current at Step-up Load
$\Delta V_{O(MAX)}$	=	Maximum V_{OUT} Overshoot at Load Release

The maximum value of the overall ESR of the output capacitor in steady-state is calculated by Equation 5-11.

EQUATION 5-11:

$$ESR_{COUT} \leq \frac{\Delta V_{OUT(PP)}}{\Delta I_{L(PP)}}$$

The maximum overall ESR value of the output capacitor should also meet the load transient requirement and is calculated by Equation 5-12. Then, the lower value from the two equations should be chosen for the output capacitor ESR.

EQUATION 5-12:

$$ESR_{COUT} \leq \frac{\Delta V_{OUT(TRANS)}}{\Delta I_{LOAD}}$$

As described in Section 4.1, Control Architecture, the MIC2129 requires at least 40 mV peak-to-peak ripple at the FBS pin to make the g_m amplifier and the error comparator behave properly.

Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitor's value should be much smaller than the ripple caused by the output capacitor ESR. If low-ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection method should be applied to provide the enough feedback voltage ripple. Please refer to Section 4.3.1, Ripple Injection Circuit Components Selection for Ripple Injection from INJ Node for more

details. The voltage rating of the output capacitor should be at least 25% greater than maximum output voltage.

The output capacitor RMS current is calculated by Equation 5-13:

EQUATION 5-13:

$$I_{COUT(RMS)} = \frac{\Delta I_{L(PP)}}{\sqrt{12}}$$

The power dissipated in the output capacitors is typically quite low and is calculated by Equation 5-14:

EQUATION 5-14:

$$P_{DISS(COUT)} = I_{COUT(RMS)}^2 \times ESR_{COUT}$$

5.3 Input Capacitor Selection

The input capacitors should employ both high-frequency ceramic capacitors and some larger bulk capacitance such as aluminum electrolytic type. The input capacitors are used to help attenuate ripple on the input and to supply current to the input during large output current transients. The input capacitors should be selected based on ripple voltage at V_{IN}, capacitance, ESR, ripple current rating, and voltage rating. Tantalum input capacitors may fail when subjected to high inrush currents, caused by turning the input supply on. A tantalum input capacitor's voltage rating should be at least two times the maximum input voltage to maximize reliability. Aluminum electrolytic, aluminum polymer, and multilayer polymer film capacitors can handle the higher inrush currents without voltage derating. The input ripple voltage depends on the output current and input capacitor's capacitance and ESR. The steady-state input voltage ripple can be estimated by Equation 5-15.

EQUATION 5-15:

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1 - D)}{Eff \times f_{SW} \times C_{IN}} + (I_{L(PK)} - I_{OUT} \times D) \times ESR_{CIN}$$

Where:

I_{OUT}	=	Output Current
D	=	Duty Cycle
f_{SW}	=	Switching Frequency
C_{IN}	=	Total Input Capacitance
ESR_{CIN}	=	Equivalent Series Resistance of Input Capacitor
$I_{L(PK)}$	=	Peak Inductor Current
Eff	=	Efficiency of Buck Converter

The capacitance required for the input capacitor in steady and transient states can be estimated by Equation 5-16:

EQUATION 5-16:

$$C_{IN(STEADY)} \geq \frac{I_{OUT(MAX)} \times D \times (1 - D)}{Eff \times f_{SW} \times \Delta V_{IN(STEADY)}}$$

$$C_{IN(TRANS)} \geq \frac{\Delta I_{LOAD}}{\pi \times f_{CO} \times \Delta V_{IN(TRANS)}}$$

The ESR of the total input capacitance can be determined by Equation 5-17:

EQUATION 5-17:

$$ESR_{CIN} \leq \frac{\Delta V_{IN}}{I_{OUT(MAX)} \times \left(1 + \frac{DIR}{2} - D_{MIN}\right)}$$

Where:

$I_{OUT(MAX)}$	=	Maximum Output Current
D_{MIN}	=	Minimum Duty Cycle, $V_{OUT(MIN)}/V_{IN(MAX)}$
DIR	=	$\Delta I_{L(PP)}/I_{L(AVG\_MAX)}$, about 0.2 to 0.4

The input capacitor must be rated for the input current ripple. The rated RMS value of input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current ripple is low, the RMS current rating of the input capacitor can be estimated from Equation 5-18:

EQUATION 5-18:

$$I_{CIN(RMS)} \approx I_{OUT(MAX)} \times \sqrt{D \times (1 - D)}$$

Where:

$I_{OUT(MAX)}$	=	Maximum Output Current

The power dissipated in the input capacitor can then be computed from Equation 5-19:

EQUATION 5-19:

$$P_{DISS(CIN)} = I_{CIN(RMS)}^2 \times ESR_{CIN}$$

The voltage rating of the input capacitor must be high enough to withstand the high input voltage. The recommended voltage rating is at least 1.25 times the maximum input voltage.

5.4 Power MOSFET Selection

Important parameters for MOSFET selection are:

- Voltage rating
- Current rating
- On-resistance
- Total gate charge

The voltage rating for both the high-side and low-side MOSFETs in the buck converter is essentially equal to the power stage input voltage VIN. A safety factor of 30% should be added to the $V_{IN(MAX)}$ while selecting the voltage rating of the MOSFETs to account for voltage spikes due to circuit parasitic elements as shown in Equation 5-20.

EQUATION 5-20:

$$V_{DS(RATING)} \geq V_{IN(MAX)} \times 1.3$$

The peak switch current for both the high-side and low-side MOSFETs in a buck converter is the same and is equal to the maximum peak inductor current as shown in Equation 5-21:

EQUATION 5-21:

$$I_{SWHS(PK)} = I_{SWLS(PK)} = I_{OUT(MAX)} + \frac{\Delta I_{L(PP)}}{2}$$

Where:

$I_{OUT(MAX)}$ = Maximum Output Current
$\Delta I_{L(PP)}$ = Peak-to-Peak Inductor Current

The RMS current rating of the high-side power MOSFET is approximated by Equation 5-22:

EQUATION 5-22:

$$I_{SWHS(RMS)} = I_{OUT(MAX)} \times \sqrt{D_{MAX}}$$

Where:

$D_{(MAX)}$ = Maximum Duty Cycle

The maximum duty cycle is calculated by Equation 5-23:

EQUATION 5-23:

$$D_{MAX} = \frac{V_{OUT(MAX)}}{Eff \times V_{IN(MIN)}}$$

Where:

$V_{OUT(MAX)}$ = Maximum Output Current
$V_{IN(MAX)}$ = Minimum Input Voltage
Eff = Efficiency of Buck Converter

The RMS current rating of the low-side power MOSFET is approximated by Equation 5-24.

EQUATION 5-24:

$$I_{SWLS(RMS)} = I_{OUT(MAX)} \times \sqrt{1 - D_{MAX}}$$

Where:

$D_{(MAX)}$ = Maximum Duty Cycle

The conduction loss of the high-side power MOSFET is calculated by Equation 5-25:

EQUATION 5-25:

$$P_{COND(HS)} = (I_{SWHS(RMS)})^2 \times R_{DSON(HS)}$$

Where:

$R_{DSON(HS)}$ = High-Side MOSFET ON Resistance

The conduction loss of the low-side power MOSFET is calculated by Equation 5-26.

EQUATION 5-26:

$$P_{COND(LS)} = (I_{SWLS(RMS)})^2 \times R_{DSON(LS)}$$

Where:

$R_{DSON(LS)}$ = Low-Side MOSFET ON Resistance

The switching loss of the high-side power MOSFET is estimated by Equation 5-27.

EQUATION 5-27:

$$P_{SWL(HS)} = V_{IN(MAX)} \times I_{OUT(MAX)} \times (t_R + t_F) \times f_{SW}$$

$$t_R = Q_{G(HS)} \times \frac{(R_{ONDHH} + R_{G(HS)})}{PV_{DD} - V_{TH(HS)}}$$

$$t_F = Q_{G(HS)} \times \frac{(R_{ONDHL} + R_{G(HS)})}{V_{TH(HS)}}$$

$$Q_{G(HS)} = 0.5 \times Q_{GSHS} + Q_{GDHS}$$

Where:

t_R = High-Side MOSFET Turn-on Transition Time
t_F = High-Side MOSFET Turn-off Transition Time
$Q_{G(HS)}$ = Switching Gate Charge of High-Side MOSFET
Q_{GSHS} = Gate-to-Source Charge of High-Side MOSFET
Q_{GDHS} = Gate-to-Drain Charge of High-Side MOSFET
R_{ONDHH} = High-Side Gate Driver Pull-up Resistance
R_{ONDHL} = High-Side Gate Driver Pull-Down Resistance
$R_{G(HS)}$ = Gate Resistance of High-Side MOSFET
$V_{TH(HS)}$ = High-Side MOSFET Gate-to-Source Threshold Voltage

The high-side MOSFET output capacitance discharge loss can be calculated by Equation 5-28.

EQUATION 5-28:

$$P_{COSS(HS)} = 0.5 \times C_{OSS(HS)} \times (V_{IN(MAX)})^2 \times f_{SW}$$

Where:

$C_{OSS(HS)}$ = High-Side MOSFET Output Capacitance

The LS FET body diode reverse recovery loss is actually dissipated in the HS FET and it is calculated by Equation 5-30.

EQUATION 5-29:

$$P_{BDQRR(LS)} = V_{IN(MAX)} \times Q_{RR(BDLS)} \times f_{SW}$$

Where:

$Q_{RR(BDLS)}$ = Reverse Recovery Charge of Low-Side MOSFET Body Diode

The total power dissipation of the high-side power MOSFET is the sum of the conduction loss, switching loss, MOSFET output capacitance discharge loss, and LS FET body diode reverse recovery charge loss as shown in Equation 5-30.

EQUATION 5-30:

$$P_{D(HS)} = P_{COND(HS)} + P_{SWL(HS)} + P_{COSS(HS)} + P_{BDQRR(LS)}$$

The high-side power MOSFET selected must be capable of handling the total power dissipation. To improve efficiency and minimize power loss, the power MOSFET should be selected with low on-resistance and optimum gate charge. On the other hand, the power dissipation in the low-side power MOSFET is mainly contributed by the conduction loss, and there is minimal switching loss for the low-side MOSFET in buck converter since the body diode of the low-side MOSFET is forward-biased before the turn-on and after the turn-off of the low-side MOSFET. This causes the voltage drop across the low-side MOSFET to be equal to its intrinsic body diode voltage during the turn-on and turn-off transition.

Apart from the conduction loss, the low-side MOSFET body diode forward conduction loss, and low-side MOSFET output capacitance discharge loss also contribute to the power dissipation in the low-side power MOSFET.

The low-side MOSFET body diode forward conduction loss during dead-time is calculated by Equation 5-31.

EQUATION 5-31:

$$P_{BDDT(LS)} = 2 \times I_{OUT(MAX)} \times V_{F(BD)} \times t_{DT} \times f_{SW}$$

Where:

$V_{F(BD)}$ = Forward Voltage of Low-Side MOSFET Body Diode

t_{DT} = Dead Time (~ 50 ns)

The low-side MOSFET output capacitance discharge loss can be calculated by Equation 5-32.

EQUATION 5-32:

$$P_{COSS(LS)} = 0.5 \times C_{OSS(LS)} \times (V_{IN(MAX)})^2 \times f_{SW}$$

Where:

$C_{OSS(LS)}$ = Low-Side MOSFET Output Capacitance

The total power dissipation of the low-side power MOSFET is estimated by Equation 5-33.

EQUATION 5-33:

$$P_{D(LS)} = P_{COND(LS)} + P_{BDDT(LS)} + P_{COSS(LS)}$$

Since low-side MOSFETs can be unintentionally turned on by the high dV/dt signal at the switching node, low-side MOSFETs with high C_{GS}/C_{GD} ratio and low internal gate resistance should be chosen to minimize the effect of dV/dt inducted turn-on.

5.5 Bootstrap Capacitor

The MIC2129's high-side gate drive circuits are designed to switch N-Channel external MOSFETs. The MIC2129 Functional Block Diagram shows an internal bootstrap diode is between PVDD and BST pins. An external bootstrap capacitor C_{BST} is needed to connect across the BST and SW pins to form a diode-capacitor bootstrap circuit. This circuits supply energy to the high-side gate drive circuit. A low-ESR ceramic capacitor should be used as the C_{BST} (refer to the Typical Application Circuits). The bootstrap capacitor C_{BST} is charged while the low-side MOSFET is on. When the high-side MOSFET driver is turned on, energy from C_{BST} is used to turn the high-side MOSFET on. A minimum of 0.1 µF low-ESR ceramic capacitor is recommended between BST and SW pins. The required value of C_{BST} can be calculated using Equation 5-34.

EQUATION 5-34:

$$C_{BST} = \frac{Q_{G(HS)}}{\Delta V_{CBST}}$$

Where:

$Q_{G(HS)}$ = Gate Charge of High-Side MOSFET

ΔV_{CBST} = Delta Voltage Drop across C_{BST}, Generally 50 mV to 100 mV

5.6 Setting Output Voltage

The MIC2129 requires two resistors to set the output voltage as shown by Figure 5-1.

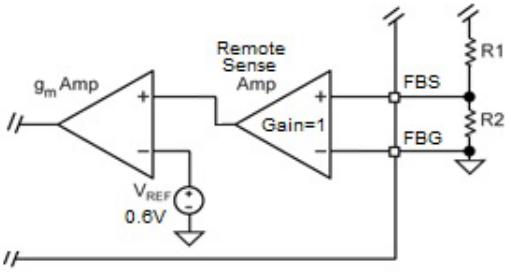


FIGURE 5-1: *Voltage-Divider Configuration.*

The output voltage is determined by Equation 5-35:

EQUATION 5-35:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

Where:

V_{REF} = 0.6V

A typical value of R1 can be between 3 kΩ and 100 kΩ. If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R1 is too small, it decreases the efficiency of the buck converter, especially at light loads. After R1 is selected, R2 can be calculated using:

EQUATION 5-36:

$$R2 = \frac{V_{REF} \times R1}{V_{OUT} - V_{REF}}$$

5.7 Power Dissipation in MIC2129

The MIC2129 features three Low Dropout Regulators (LDOs): a high-voltage LDO, a low-voltage LDO and a bias LDO. The high-voltage LDO and the low-voltage LDO are used to supply PVDD voltage at the PVDD pin from either the VIN pin or EXTVDD pin depending on the voltage at the EXTVDD pin. PVDD powers MOSFET drivers and VDD pin. The bias LDO is used to supply VDD voltage of 4.5V at the VDD pin from the PVDD. The VDD powers the internal circuitry.

In applications where the output voltage is ≥7V and ≤ 14V, it is recommended to connect EXTVDD to the output to reduce the power dissipation in the MIC2129, especially for high input voltage applications, to reduce the MIC2129 power dissipation and junction temperature and to improve the system efficiency. The power dissipation in the MIC2129 depends on whether or not the internal LDO is used, the gate charge of the external MOSFETs, and the switching frequency.

The power dissipation and junction temperature of the MIC2129 can be estimated using Equation 5-37, Equation 5-38 and Equation 5-39.

Power dissipation in the MIC2129 is calculated by Equation 5-37 when EXTVDD is not used.

EQUATION 5-37:

$$P_{IC} = V_{IN} \times (I_{G(TOTAL)} + I_Q)$$

$$I_{G(TOTAL)} = (Q_{G(HS)} + Q_{G(LS)}) \times f_{SW}$$

Where:

$I_{G(TOTAL)}$ = Total Average Gate Drive Current

I_Q = Quiescent Current of MIC2129

$Q_{G(HS)}$ = Gate Charge of High-Side MOSFET

$Q_{G(LS)}$ = Gate Charge of Low-Side MOSFET

Power dissipation in the MIC2129 is calculated by Equation 5-38 when EXTVDD is used.

EQUATION 5-38:

$$P_{IC} = V_{EXTVDD} \times (I_{G(TOTAL)} + I_Q)$$

Where:

V_{EXTVDD} = Voltage at EXTVDD Pin (7V ≤ VEXTVDD ≤ 14V typically)

$I_{G(TOTAL)}$ = Total Average Gate Drive Current

I_Q = Quiescent Current of MIC2129

The junction temperature of the MIC2129 can be estimated using Equation 5-39.

EQUATION 5-39:

$$T_J = P_{IC} \times \theta_{JA} + T_A$$

Where:

T_J = Junction Temperature of MIC2129

T_A = Ambient Temperature

P_{IC} = Power Dissipation of MIC2129

θ_{JA} = Junction-to-Ambient Thermal Resistance of MIC2129 (35°C/W typical for TSSOP Package, 43°C/W typical for VQFN Package)

The maximum recommended operating junction temperature for the MIC2129 is 125°C. Connecting EXTVDD to the output voltage (when V_{OUT} is ≥ 7V and ≤ 14V) significantly reduces the MIC2129 power

dissipation. This reduces the junction temperature rise as illustrated in Equation 5-40 example by comparing with the result in Equation 5-41 example with the following parameters: V_{IN} = 90V, V_{OUT} = 12V, $I_{G(TOTAL)}$ = 20 mA, I_Q = 1.5 mA, and maximum ambient temperature T_A = 85°C, MIC2129 package is TSSOP.

When the EXTVDD is used and the 12V output of the MIC2129 buck converter is used as the input to the EXTVDD pin, the MIC2129 junction temperature is calculated as shown in Equation 5-40. The junction temperature is significantly reduced from 152.7°C to 94.03°C when the EXTVDD is changed from not used to used.

EQUATION 5-40:

$$P_{IC} = 12V \times (20\ mA + 1.5\ mA)$$
$$P_{IC} = 0.258W$$
$$T_J = 0.258W \times 35\ ^\circ C/W + 85\ ^\circ C$$
$$T_J = 94.03\ ^\circ C$$

When the EXTVDD is not used, the MIC2129 junction temperature as calculated is shown in Equation 5-41.

EQUATION 5-41:

$$P_{IC} = 90V \times (20\ mA + 1.5\ mA)$$
$$P_{IC} = 1.935W$$
$$T_J = 1.935W \times 35\ ^\circ C/W + 85\ ^\circ C$$
$$T_J = 152.7\ ^\circ C$$

5.8 Thermal Measurements

It is a good idea to measure the IC's case temperature to make sure it is within its operating limits. Although this might seem an elementary task, it is easy to get false results. The most common mistake is to use the standard thermal couple that comes with a thermal meter. This thermal couple wire gauge is large, typically 22 gauge, and behaves like a heatsink, which results in a lower-case temperature measurement.

There are two methods of temperature measurement: using a smaller thermal couple wire or using an infrared thermometer. If a thermal couple wire is used, it must be constructed of 36 gauge wire or higher (smaller wire size) to minimize the wire heat-sinking effect. In addition, the thermal couple tip must be covered in either thermal grease or thermal glue to ensure that the thermal couple junction makes good contact with the case of the IC. Wherever possible, an infrared thermometer is recommended. The measurement spot size of most infrared thermometers is too large for an accurate reading on a small form factor ICs. However, an IR thermometer with a 1 mm spot size is a good choice for measuring the hottest point on the case. An optional stand can be used to makes it easy to hold the beam on the IC for long periods of time. In addition, a more advanced, convenient and accurate infrared thermal camera can be used, although such equipment is much more expensive.

6.0 PCB LAYOUT GUIDELINES

Note: To minimize EMI and output noise, follow these layout recommendations.

PCB layout is critical to achieve reliable, stable, and efficient performance. A ground plane is required to control EMI and minimize the inductance in power and signal return paths. Use star grounding technique between GND and PGND. Minimize trace lengths for high-current paths.

Follow these guidelines to ensure proper operation of the MIC2129 buck converter.

6.1 MIC2129

- Use wide traces to connect to the VDD, PVDD, EXTVDD and PGND pins.
- Connect a 2.2 µF ceramic capacitor to the VDD pin, and locate it as close as possible to the IC.
- Connect a 4.7 µF ceramic capacitor to the PVDD pin, and locate it as close as possible to the IC.
- Connect a 4.7 µF ceramic capacitor to the EXTVDD pin, and locate it as close as possible to the IC.
- Connect the Analog Ground pin (GND) directly to the analog ground planes. Do not route the GND pin to the PGND pad on the top layer.
- Do not flood analog ground plane or island around noisy high dv/dt and high di/dt source traces, e.g. switching node trace and gate drive traces
- Use thick traces and minimize trace length for the input and output power lines.
- Keep the analog signal and power grounds separate and connected at only one location.

6.2 Input Capacitor

- Use parallel input capacitors to minimize effective ESR and ESL of the input capacitor bank.
- Place input capacitors next to the high-side power MOSFETs.
- Place the input capacitors on the same side of the board and as close to the IC as possible.
- Connect the VIN supply to VIN pin through a 1.2Ω resistor and connect a 1 µF ceramic capacitor from VIN pin to GND pin. Keep both the VIN pin and GND connections short.
- Place several vias to the ground plane close to the input capacitors ground terminal.
- Use either X7R or X5R dielectric input ceramic capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of bulk capacitor can be placed in parallel with the high-frequency ceramic input capacitors.
- In Hot-plug applications, use one or more electrolytic bypass capacitors to limit the overvoltage spike seen on the input supply when power is suddenly applied.

6.3 Inductor

- Keep the inductor connection to the switch node (SW) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (SW) away from the remote sense traces and FBS and FBG pins.
- To minimize noise, place a ground plane under the inductor.
- The inductor can be placed on the opposite side of the PCB with respect to the IC. There should be sufficient vias on the power traces to conduct high current between the inductor and the IC and output load. It does not matter whether the IC or inductor is on the top or bottom as long as there is enough heatsink and air flow to keep the power components within their temperature limits. Place the input and output capacitors on the same side of the board as the IC.

6.4 Output Capacitor

- Use parallel output capacitors to minimize effective ESR and ESL of the output capacitor bank.
- Use a wide trace to connect the inductor to the output capacitors.
- The output capacitors' ground terminals should be connected to the PGND plane. This PGND copper plane on the top layer of the board should also encompass the input capacitors' ground terminals.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high current load trace can degrade the DC load regulation.

6.5 MOSFETs

- The MOSFET gate drive traces must be short and wide. The LS FET source terminal get tied to the PGND plane directly on the top layer and through multiple vias to the PGND plane on the bottom layer.

6.6 Current Sense

- Connect the CSP and CSN pins directly to the drain and source of the low-side power MOSFET respectively, or across current-sense resistor, and route the CSP and CSN traces together to accurately sense the voltage across the current-sense element to achieve accurate current sensing.

6.7 V_{OUT} Remote Sense

- The output voltage and output ground remote sense traces must be routed close together or on adjacent layers to minimize noise pickup. The traces should be routed away from the switch node, inductors, MOSFETs and other high dv/dt or di/dt sources.

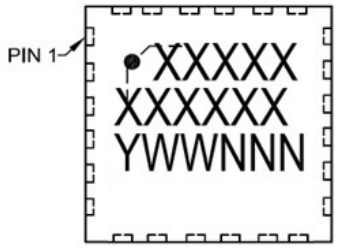
6.8 RC Snubber

- If it is needed, connect an RC snubber across switching node and PGND. Place the RC snubber as close to the switching node at the low-side MOSFET as possible.

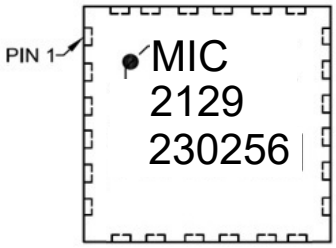
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

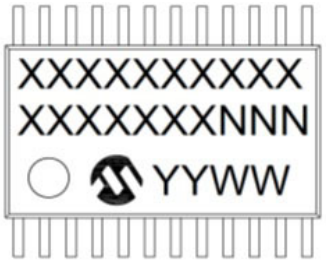
24-Lead VQFN



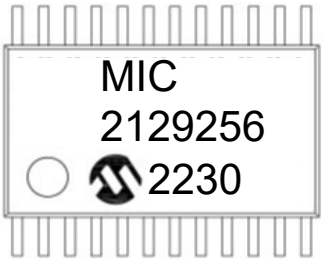
Example



24-Lead TSSOP



Example

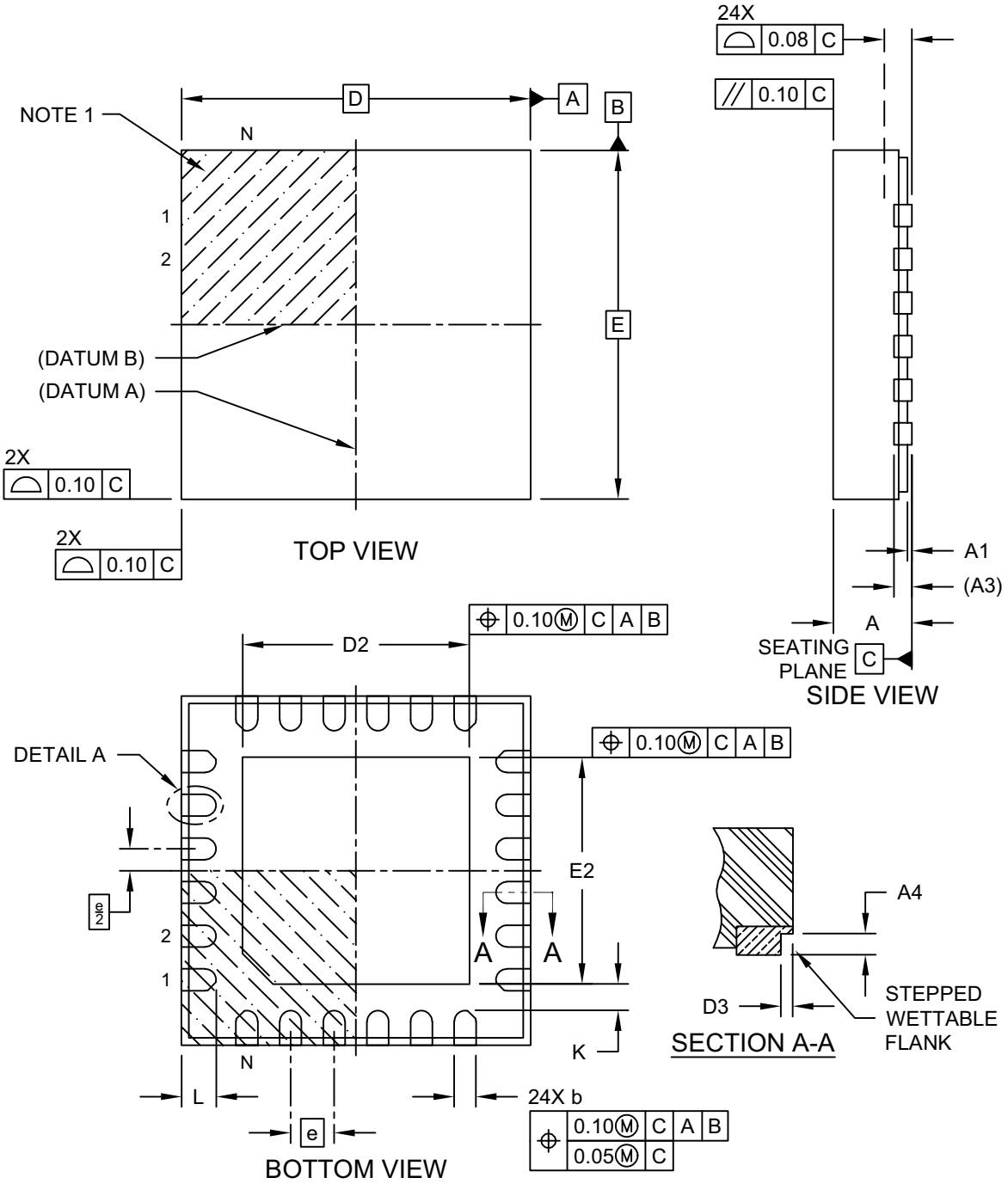


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or not include the corporate logo. Underbar (_) and/or Overbar (¯) symbol may not be to scale.

24-Lead Very Thin Plastic Quad Flat, No Lead Package (U3B) - 4x4 mm Body [VQFN] With 2.6mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy ZCY

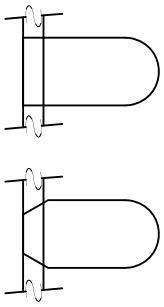
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



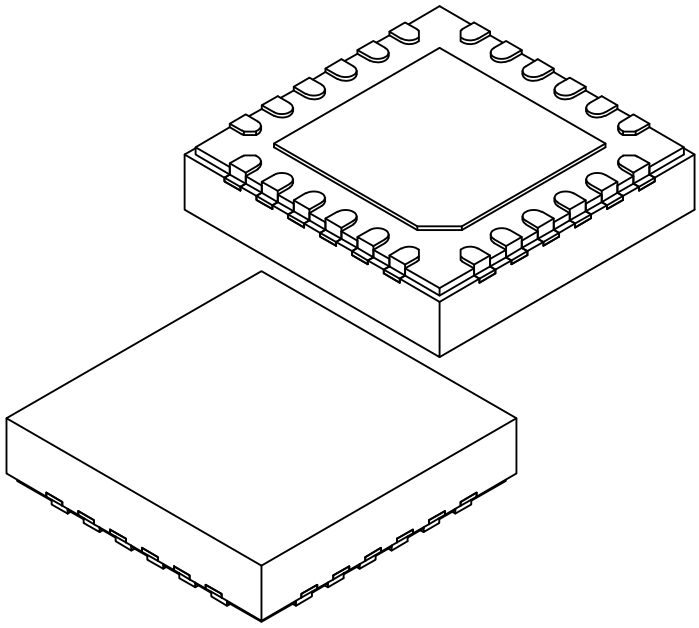
Microchip Technology Drawing C04-21483 Rev B Sheet 1 of 2

24-Lead Very Thin Plastic Quad Flat, No Lead Package (U3B) - 4x4 mm Body [VQFN] With 2.6mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy ZCY

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL 1
ALTERNATE TERMINAL CONFIGURATIONS



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		24	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.035	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.50	2.60	2.70
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.50	2.60	2.70
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-
Wettable Flank Step Length	D3	-	-	0.085
Wettable Flank Step Height	A4	0.10	-	0.19

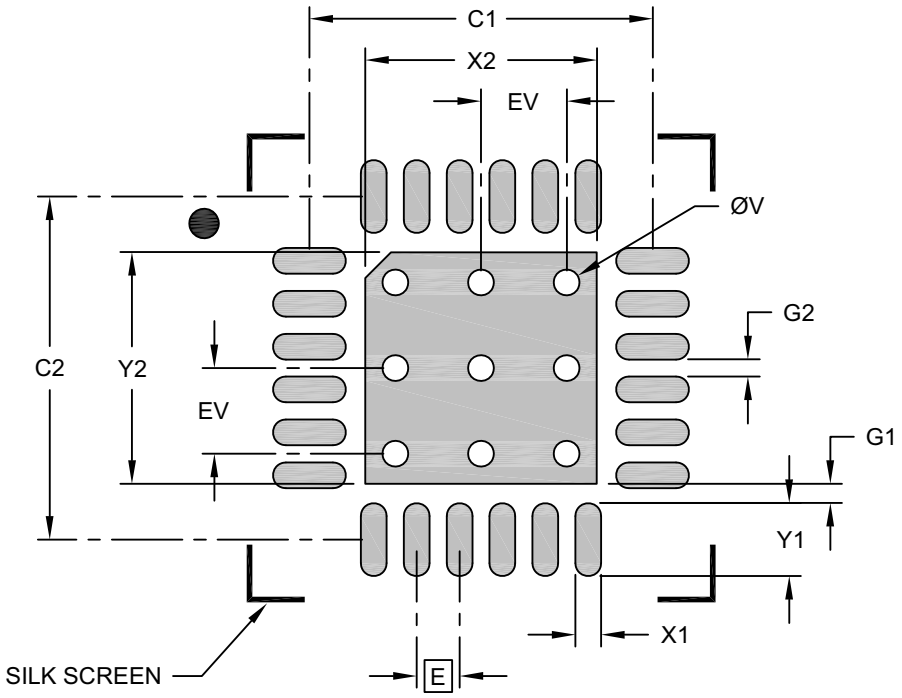
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21483 Rev B Sheet 2 of 2

24-Lead Very Thin Plastic Quad Flat, No Lead Package (U3B) - 4x4 mm Body [VQFN] With 2.6mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy ZCY

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			2.70
Optional Center Pad Length	Y2			2.70
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X24)	X1			0.30
Contact Pad Length (X24)	Y1			0.85
Contact Pad to Center Pad (X24)	G1	0.23		
Contact Pad to Contact Pad (20)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

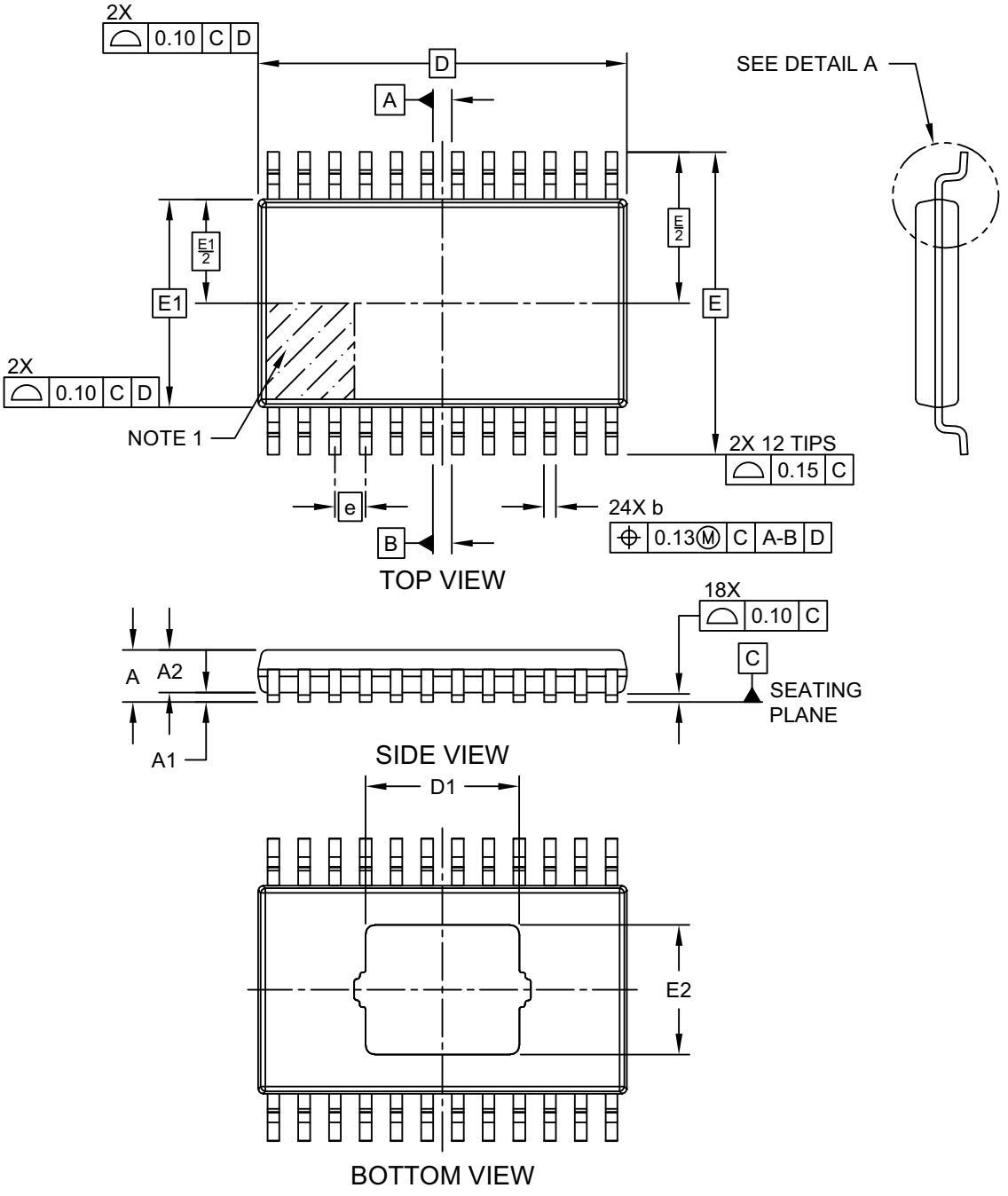
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23483 Rev B

24-Lead Thin Shrink Small Outline Package (2FW) - 4.4 mm Body [TSSOP]
With 3.25x2.84 mm Exposed Pad

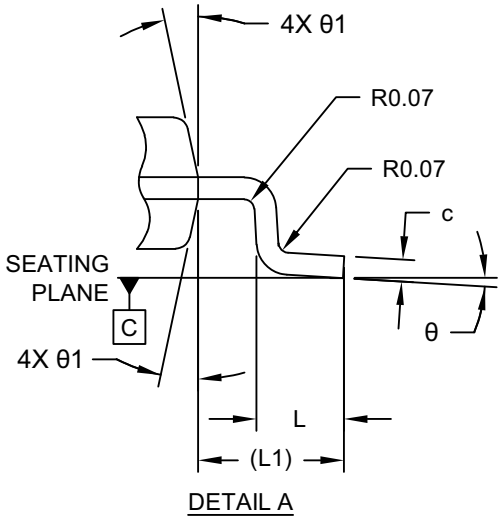
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

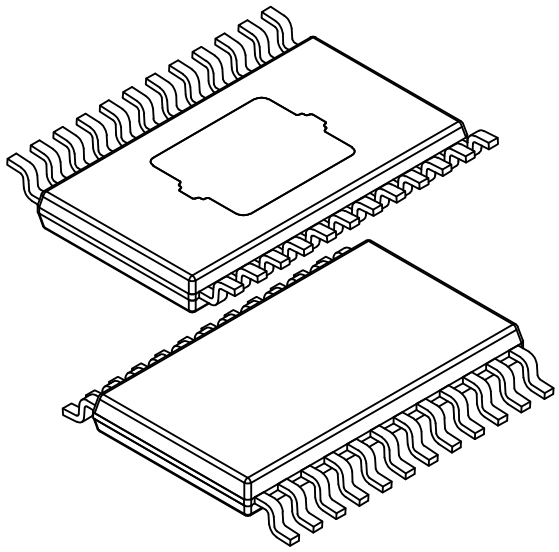


Microchip Technology Drawing C04-541 Rev A Sheet 1 of 2

24-Lead Thin Shrink Small Outline Package (2FW) - 4.4 mm Body [TSSOP] With 3.25x2.84 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		24	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.10
Standoff	A1	0.05	0.10	0.15
Molded Package Thickness	A2	0.85	0.90	0.95
Overall Length	D		7.80 BSC	
Overall Width	E		6.40 BSC	
Molded Package Width	E1		4.40 BSC	
Terminal Width	b	0.19	0.25	0.30
Terminal Thickness	c	0.09	0.15	0.20
Terminal Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Lead Bend Radius	R1	0.07	-	-
Lead Bend Radius	R2	0.07	-	-
Foot Angle	θ	0°	-	8°
Mold Draft Angle	θ1	5°	-	15°

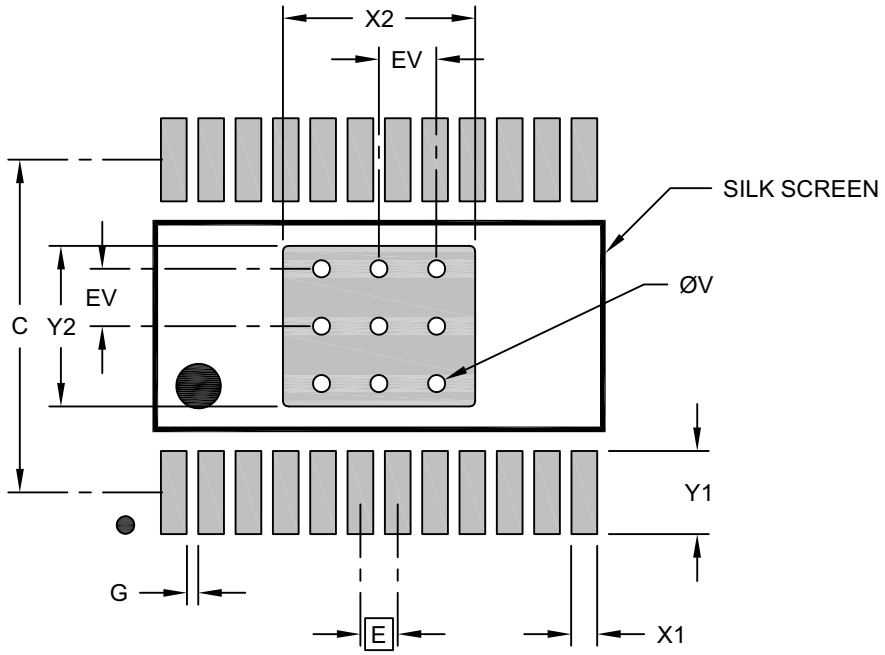
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-541 Rev A Sheet 2 of 2

24-Lead Thin Shrink Small Outline Package (2FW) - 4.4 mm Body [TSSOP] With 3.25x2.84 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Center Pad Width	X2			3.35
Center Pad Length	Y2			2.80
Contact Pad Spacing	C		5.80	
Contact Pad Width (X24)	X1			0.45
Contact Pad Length (X24)	Y1			1.45
Contact Pad to Contact Pad (X22)	G	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-541 Rev A

APPENDIX A: REVISION HISTORY

Revision A (December 2023)

- Initial release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X[(1)]	-X	/XXX	XXX
Device	Tape and Reel Option	Junction Temperature Range	Package	Qualification

Device:	MIC2129: 100V, DC-DC Step-down Controller with Selectable Gate Driver Voltage and Remote Sense	
Tape and Reel Option:	T	= 1000/Reel (for VQFN) = 2500/Reel (for TSSOP)
Junction Temperature Range:	E	= -40°C to +125°C, Extended Temperature Range
Package:	U3B	= 24-Lead 4 mm x 4 mm VQFN, Wettable Flank, Exposed Pad
	2FW	= 24-Lead 7.8 mm x 6.4 mm, 4.4 mm Body, TSSOP, Exposed Pad
Qualification:	Blank	= Standard Part
	VAO	= Automotive AEC-Q100 Qualified

Examples:

a) MIC2129T-E/U3B: 100V, DC-DC Step-down Controller with Selectable Gate Driver Voltage and Remote Sense, 1000/Reel, -40°C to +125°C Extended Junction Temperature Range, 24-Lead 4 mm x 4 mm, VQFN Exposed Pad Package.

b) MIC2129T-E/2FW: 100V, DC-DC Step-down Controller with Selectable Gate Driver Voltage and Remote Sense, 2500/Reel, -40°C to +125°C Extended Junction Temperature Range, 24-Lead 7.8 mm x 6.4 mm, 4.4 mm Body, TSSOP Exposed Pad Package.

c) MIC2129T-E/U3BVAO: 100V, DC-DC Step-down Controller with Selectable Gate Driver Voltage and Remote Sense, 1000/Reel, -40°C to +125°C Extended Junction Temperature Range, 24-Lead 4 mm x 4 mm, VQFN Exposed Pad Package, Automotive AEC-Q100 Qualified.

d) MIC2129T-E/2FWVAO: 100V, DC-DC Step-down Controller with Selectable Gate Driver Voltage and Remote Sense, 2500/Reel, -40°C to +125°C Extended Junction Temperature Range, 24-Lead 7.8 mm x 6.4 mm, 4.4 mm Body, TSSOP Exposed Pad Package, Automotive AEC-Q100 Qualified.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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