AN4254

Utilizing Enhanced Software Write Protection in 24CS Series Serial EEPROMs

Author: *Erik Fasnacht*
Microchip Technology Inc.

INTRODUCTION

Traditional I^2C Serial EEPROMs utilize hardware-based write protection that only allows locking or unlocking the entire memory array via an external pin, which severely limits the possible ways to protect data. The 24CS Series devices address this limitation with the addition of a 16-bit Configuration register, which allows the write protection behavior to be configured for legacy hardware write protection or enhanced software write protection.

Legacy hardware write protection uses the Write Protection (WP) pin to write-protect the entire memory array when the WP pin is '1'. As the name suggests, Legacy write protection mode behaves identically to standard I^2C Serial EEPROMs. However, many of today's applications can benefit from greater flexibility in managing data protection. For these applications, the 24CS provides the option to use enhanced software write protection, which allocates eight zones within the memory array that can be independently set to be write-protected. This added flexibility allows for the 24CS Series devices to provide much more granular data protection as required by the application.

The desired write protection settings are set via the Configuration register, which can be accessed by sending commands to a specific device address and word address. If desired, the Configuration register can be locked so that it is set to read-only and can no longer be modified, thereby making the current data protection scheme permanent. This application note is intended to demonstrate how to utilize the 16-bit Configuration register to setup data protection in your application.

Configuration Register Byte 0

The Configuration register format and bit definitions for the Most Significant Byte (MSB) is seen in Register 1. This byte contains status information along with bits for setting the current write protection behavior and locking the Configuration register.

REGISTER 1: CONFIGURATION REGISTER – BYTE 0

R-0	U-0	U-0	U-0	U-0	U-0	R/W	R/W
ECS	—	—	—	—	—	EWPM	LOCK
bit 15							bit 8

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ECS:** Error Correction State bit
- 1 = The previously executed read operation did require the use of the Error Correction Code (ECC) scheme
- 0 = The previously executed read operation did not require the use of the Error Correction Code (ECC) scheme

bit 14-10 **Unimplemented:** Read as ‘0’

bit 9 **EWPM:** Enhanced Software Write Protection Mode bit
- 1 = Enhanced Protection: WP pin is treated as a don’t care and the memory array is protected in accordance with the SWP bits defined in Register 2
- 0 = Legacy Protection (factory default): Entire memory array and Security register contents are protected via the WP pin

bit 8 **LOCK:** Lock Configuration Register bit
- 1 = The Configuration register is set to read-only (permanent)
- 0 = The Configuration register can be written to (factory default)

ERROR CORRECTION STATE (ECS) BIT

This bit is used when the user needs to determine whether the on-chip Error Correction Code (ECC) logic scheme has been invoked. The ECS bit will be set to logic '0' unless the previously executed read operation required the use of the ECC logic scheme. When this occurs, the ECS bit will set to logic '1'. The ECS bit will continue to read a logic '1' until another read operation is issued and the use of the ECC logic scheme was not required or a Power-on Reset (POR) event has occurred.

ENHANCED SOFTWARE WRITE PROTECTION MODE (EWPM) BIT

This bit is used to select between Legacy Hardware Write Protection mode (logic '0') and Enhanced Software Write Protection mode (logic '1'). Legacy Hardware Write Protection mode allows the entire memory array to be write-protected via the WP pin.

Enhanced Software Write Protection is a software write-protect feature where the memory array is divided into eight separate zones. Each zone is independent and is configured using the SWP[7:0] bits (Register 2).

Legacy Write Protection Mode

When the EWPM bit is set to logic '0', the 24CS Series utilizes a legacy hardware data protection scheme that allows the user to write-protect the entire memory contents when the WP pin is asserted (high). No write protection will be set if the WP pin is deasserted (low).

TABLE 1: LEGACY HARDWARE WRITE PROTECTION BEHAVIOR

WP Pin	Protected Address Range
1 (high)	Full Array
0 (low)	None

Enhanced Write Protection Mode

When the EWPM bit is set to logic '1', the 24CS Series is configured for a versatile software write protection scheme by segmenting the EEPROM array into eight independent zones. Each of the eight zones can be write-protected by programming the corresponding bit (see Register 2) in the Configuration register. The protection behavior can be made permanent by locking the Configuration register.

LOCK CONFIGURATION REGISTER (LOCK) BIT

This bit allows the user to lock the Configuration register by setting it to read-only so that it can no longer be modified. When the LOCK bit is set to logic '1', the current data protection scheme becomes permanent.

Configuration Register Byte 1

The Configuration register format and bit definitions for the Least Significant Byte (LSB) is seen in Register 2. This byte contains the eight independent Software Write Protection Memory Zone (SWP[7:0]) bits.

REGISTER 2: CONFIGURATION REGISTER – BYTE 1

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SWP7	SWP6	SWP5	SWP4	SWP3	SWP2	SWP1	SWP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

If EWPM = 1:

bit 7 **SWP7:** Software Write Protection Memory Zone 7 bit
1 = Memory Zone 7 is write-protected
0 = Memory Zone 7 is not write-protected

bit 6 **SWP6:** Software Write Protection Memory Zone 6 bit
1 = Memory Zone 6 is write-protected
0 = Memory Zone 6 is not write-protected

bit 5 **SWP5:** Software Write Protection Memory Zone 5 bit
1 = Memory Zone 5 is write-protected
0 = Memory Zone 5 is not write-protected

bit 4 **SWP4:** Software Write Protection Memory Zone 4 bit
1 = Memory Zone 4 is write-protected
0 = Memory Zone 4 is not write-protected

bit 3 **SWP3:** Software Write Protection Memory Zone 3 bit
1 = Memory Zone 3 is write-protected
0 = Memory Zone 3 is not write-protected

bit 2 **SWP2:** Software Write Protection Memory Zone 2 bit
1 = Memory Zone 2 is write-protected
0 = Memory Zone 2 is not write-protected

bit 1 **SWP1:** Software Write Protection Memory Zone 1 bit
1 = Memory Zone 1 is write-protected
0 = Memory Zone 1 is not write-protected

bit 0 **SWP0:** Software Write Protection Memory Zone 0 bit
1 = Memory Zone 0 is write-protected
0 = Memory Zone 0 is not write-protected

If EWPM = 0:

bit 7-0 Unused

SOFTWARE WRITE PROTECTION MEMORY ZONE (SWP[7:0]) BITS

These bits divide the memory array into eight separate zones. Each zone can be set independently from the other protection zones. The corresponding SWP bit must be set to a logic '1' to write-protect that zone.

Note: In Legacy Hardware Write Protection mode (EWPM = '0'), the SWP[7:0] bits are ignored. However, a dummy value must still be sent during the write sequence to initiate the internal write operation.

Accessing the Register

The value of the Configuration register can be determined by executing a random read sequence to a specific word address. Changing the value of the Configuration register is accomplished with a byte write sequence with specific data sent to the device.

DEVICE ADDRESS REQUIREMENTS

Accessing this register requires the use of '1011b' (Bh) as the device type identifier in the device address (see Table 2). Following the device type identifier are the hardware client address bits for which the values are determined by the device address input pins A2, A1 and A0. Finally, bit 0 is the Read/Write Select (R/$\overline{W}$) bit where a logic '1' is used for reading and a logic '0' is used for writing.

TABLE 2: CONFIGURATION REGISTER DEVICE ADDRESS BYTE

Memory Region	Device Type Identifier				Hardware Address Bits(1)			Read/Write
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Configuration Register	1	0	1	1	A2	A1	A0	R/$\overline{W}$

Note 1: The hardware client address bits must be set to logic '0' when using the SOT-23 package.

WORD ADDRESS REQUIREMENTS

When accessing the Configuration register, a 16-bit word address must be sent to the device. All bits in the word address are ignored except for bits A15, A11 and A10. Bits A15 and A11 must be set to logic '1' and bit A10 must be set to logic '0'. Refer to Table 3 and Table 4 for additional information.

TABLE 3: CONFIGURATION REGISTER WORD ADDRESS BYTE 0

Word Address	A15	A14	A13	A12	A11	A10	A9	A8
Word Address Byte 0	1	x	x	x	1	0	x	x

TABLE 4: CONFIGURATION REGISTER WORD ADDRESS BYTE 1

Word Address	A7	A6	A5	A4	A3	A2	A1	A0
Word Address Byte 1	x	x	x	x	x	x	x	x

WRITE OPERATION

When writing the Configuration register, a write sequence must be sent to the device that includes both data bytes (Byte 0 and Byte 1), along with a valid confirmation byte. Figure 1 illustrates an example Configuration register write sequence.

Confirmation Byte

In order for the internal write process to start, both data bytes (Byte 0 and Byte 1), along with a confirmation byte, need to be sent to the device. Sending anything other than these three bytes will cause the write cycle to abort and the contents of the Configuration register will not change.

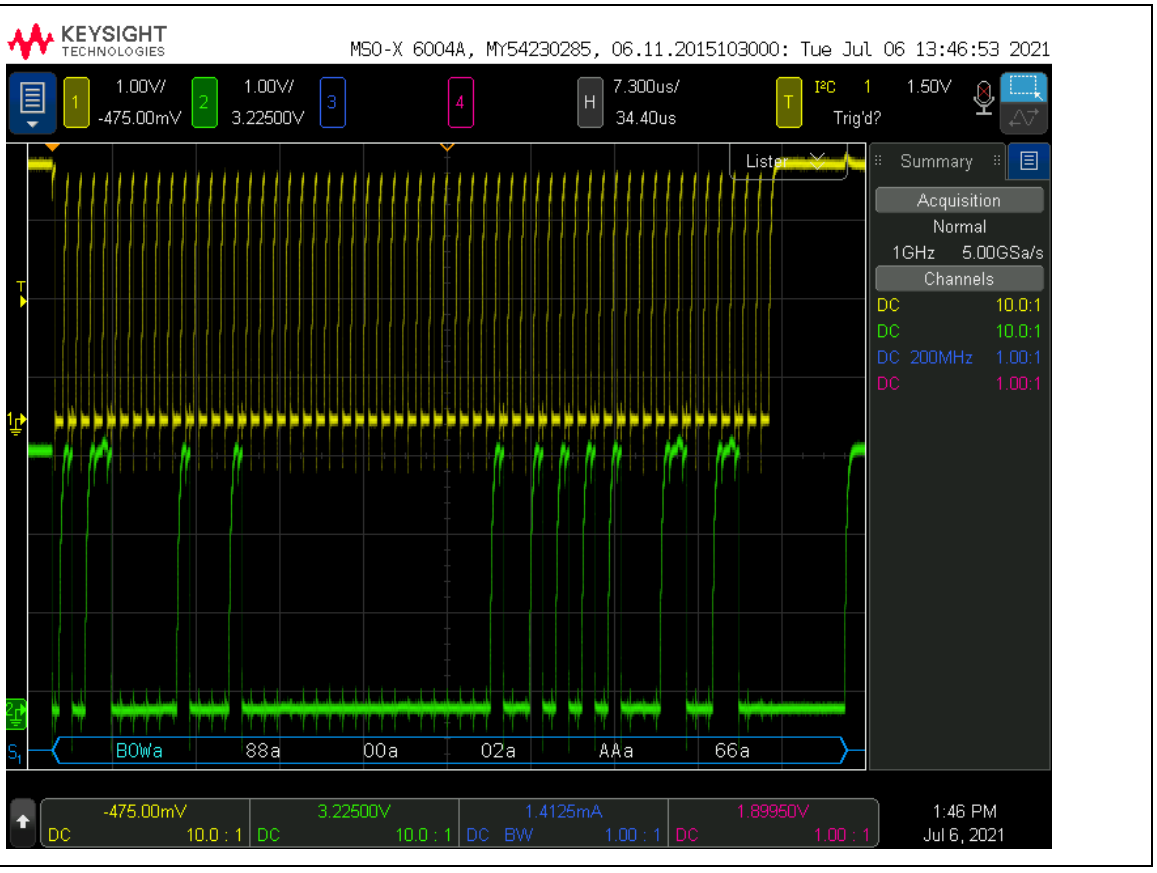
The data of the confirmation byte depends on the value being written to the LOCK bit. If the user intends to lock the Configuration register (LOCK = '1'), the confirmation byte must be 99h. If the user intends to leave the register unlocked (LOCK = '0'), the confirmation byte must be 66h. Table 5 illustrates the valid data values for the confirmation byte.

Note:	The Configuration register cannot be unlocked once it is locked.

TABLE 5: CONFIGURATION REGISTER CONFIRMATION BYTE

New LOCK Bit Value	D7	D6	D5	D4	D3	D2	D1	D0
1 (locked)	1	0	0	1	1	0	0	1
0 (unlocked)	0	1	1	0	0	1	1	0

FIGURE 1: CONFIGURATION REGISTER WRITE



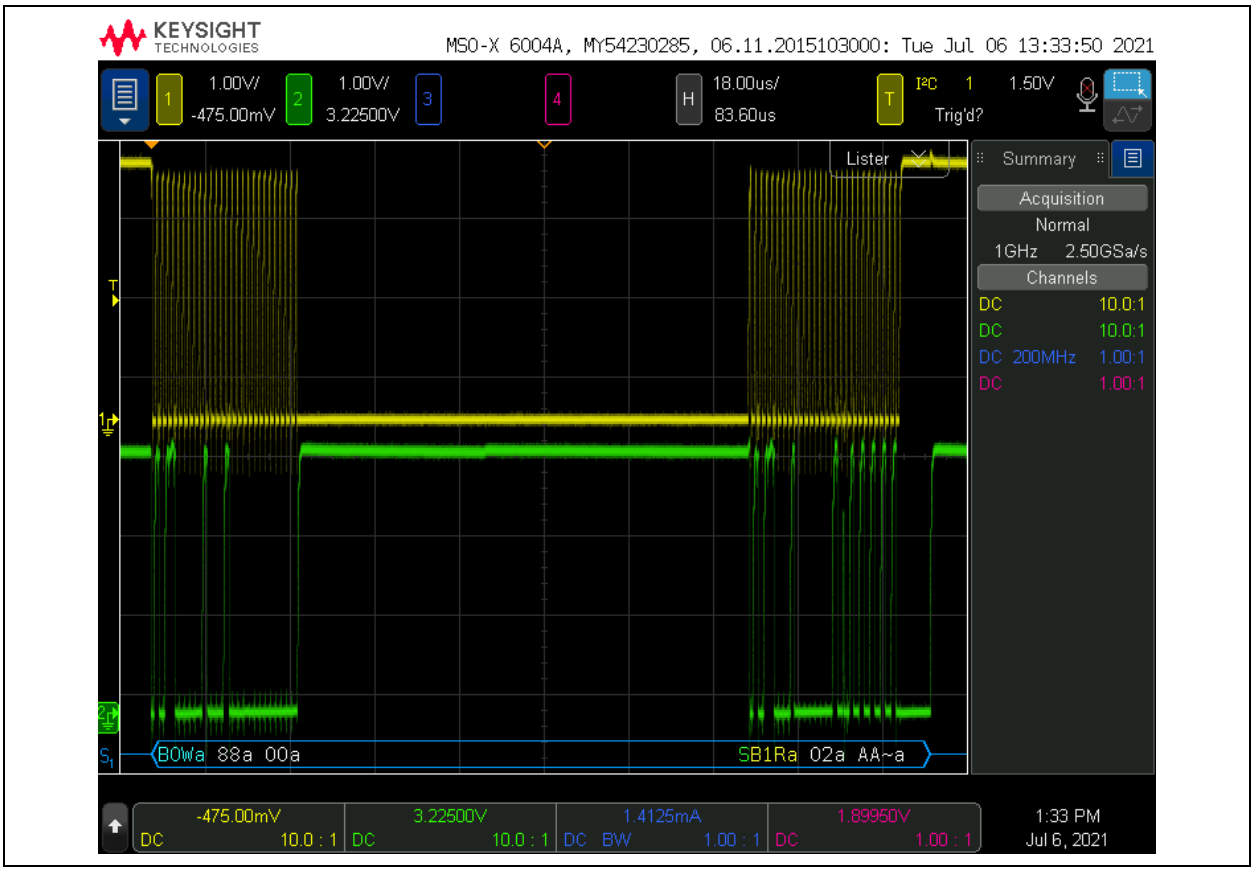
READ OPERATION

When reading the Configuration register, a random read sequence must be sent to the device.

Figure 2 illustrates an example of the Configuration register read sequence. It is not possible to read the contents of the Configuration register with a current address read sequence as the correct word address bytes must be sent to the device.

Note: The 24CS Series will automatically roll over from the second Configuration register data byte to the first data byte if the host continues to acknowledge the data bytes during the read operation.

FIGURE 2: CONFIGURATION REGISTER READ



CONCLUSION

This application note gives details on the flexible write protection the I^2C Configuration register offers. Details related to I^2C Configuration register and device operation can be found in the appropriate device data sheet found at www.microchip.com.

APPENDIX A: REVISION HISTORY

Revision A (10/2021)

Initial release of this document.

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