

Adding Flexibility by Using Multiple Footprints for I²C™ Serial EEPROMs

*Author: Chris Parris
Microchip Technology Inc.*

INTRODUCTION

For many years, the 8-lead SOIC package has been the most popular package for serial EEPROMs, but now smaller packages are becoming more and more commonplace. This offers a number of benefits; the reductions in footprint size and component height are some of the more obvious ones. Smaller packages also generally offer a cost advantage over their larger counterparts.

Currently, the SOT-23 package is one of the smallest packages available for serial EEPROMs, and its popularity has been growing significantly. However, while the SOIC is an industry-standard package available from all major EEPROM vendors, the SOT-23 package is still relatively new, especially in larger memory densities. When a new, smaller package is first released by a vendor, there is always an inherent lag before the package becomes available from all vendors. For example, Microchip was the first vendor to offer 32- and 64-Kbit I²C™ serial EEPROMs in a 5-lead SOT-23 package and it will take time before other vendors offer similar devices.

System designers can use the SOT-23 package and enjoy the associated benefits, or they can maintain a broad list of possible vendors. Now, by combining footprints, both can be done at the same time.

METHODOLOGY

By simply including multiple footprints for the serial EEPROM on your board, you can solve this issue. Normally, this would waste board space since only one footprint would be used for a given assembly. However, due to the SOT-23 package's extremely small size, you can fit a SOT-23 footprint within the same area as an SOIC footprint, as shown in Figure 1 and Figure 2. This allows you to combine multiple footprints with little to no wasted space. By following this technique, you gain the cost advantage associated with SOT-23 packages, but can still qualify a variety of different vendors. In addition, there are also a few other benefits that open up when this approach is employed.

This idea can also be applied to other 8-lead packages, such as the TSSOP and MSOP, if the application allows for a small amount of extra board space to be used.

FIGURE 1: COMBINED 5-LEAD SOT-23 AND 8-LEAD PACKAGE BLOCK DIAGRAM

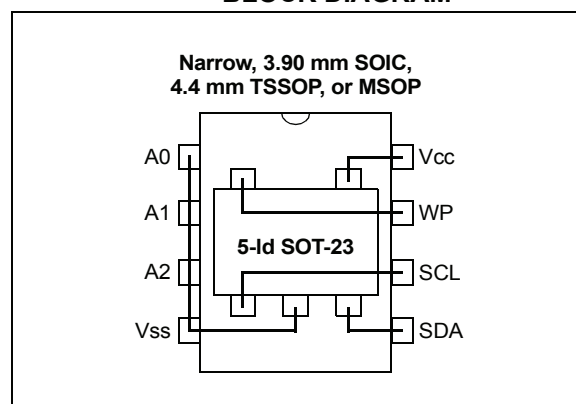
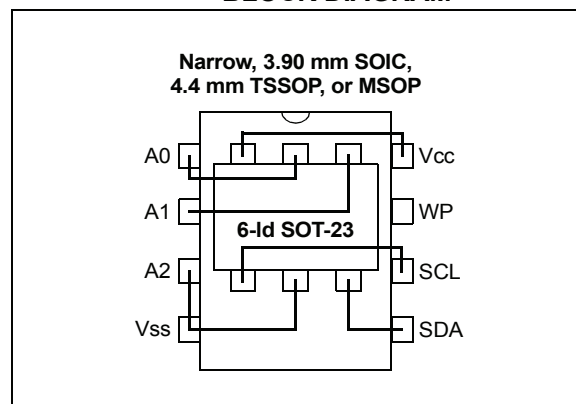


FIGURE 2: COMBINED 6-LEAD SOT-23 AND 8-LEAD PACKAGE BLOCK DIAGRAM



BENEFITS

Smaller packages offer a cost advantage while larger packages allow for a broader approved vendor list. So, naturally, including both footprints on your board gives you the opportunity to reap both benefits. But there is something else you gain only by combining footprints: flexibility.

The added flexibility is seen in two ways. First, with multiple footprints, your supply options are greatly expanded since you can now use multiple packages from each of many approved vendors. Second, your inventory management will become more flexible.

It is common to try to use the same devices in multiple applications. This simplifies inventory-related issues, and combining device orders results in higher volumes and thus, lower costs per device. Perhaps SOIC is sufficient for all of your current applications, but in the future you may need to use SOT-23. If you included a SOT-23 footprint on your current boards, you can seamlessly migrate them to SOT-23 as well, thereby reducing how many part numbers you need to order and store in inventory.

Note: The footprints included in your CAD package may need to be modified to provide enough space to include the SOT-23 footprint. Please see Microchip's "*Packaging Specification*" (DS00049) document for recommended footprint guidelines.

EXAMPLE 5-LEAD SOT-23 LAYOUTS

The following images show example layouts for combining a 5-lead SOT-23 package with an 8-lead SOIC, MSOP, or TSSOP package. All footprints are drawn according to Microchip's recommended guidelines. The layout can be done using a single layer of copper, so the images show only top copper, top silk screen, and top solder mask layers.

Note: Pins 1-3 (A0-A2) of the SOIC, TSSOP, and MSOP packages should be tied to Vss to match the functionality of 5-lead SOT-23 devices.

FIGURE 3: 5-LEAD SOT-23 AND 8-LEAD SOIC LAYOUT

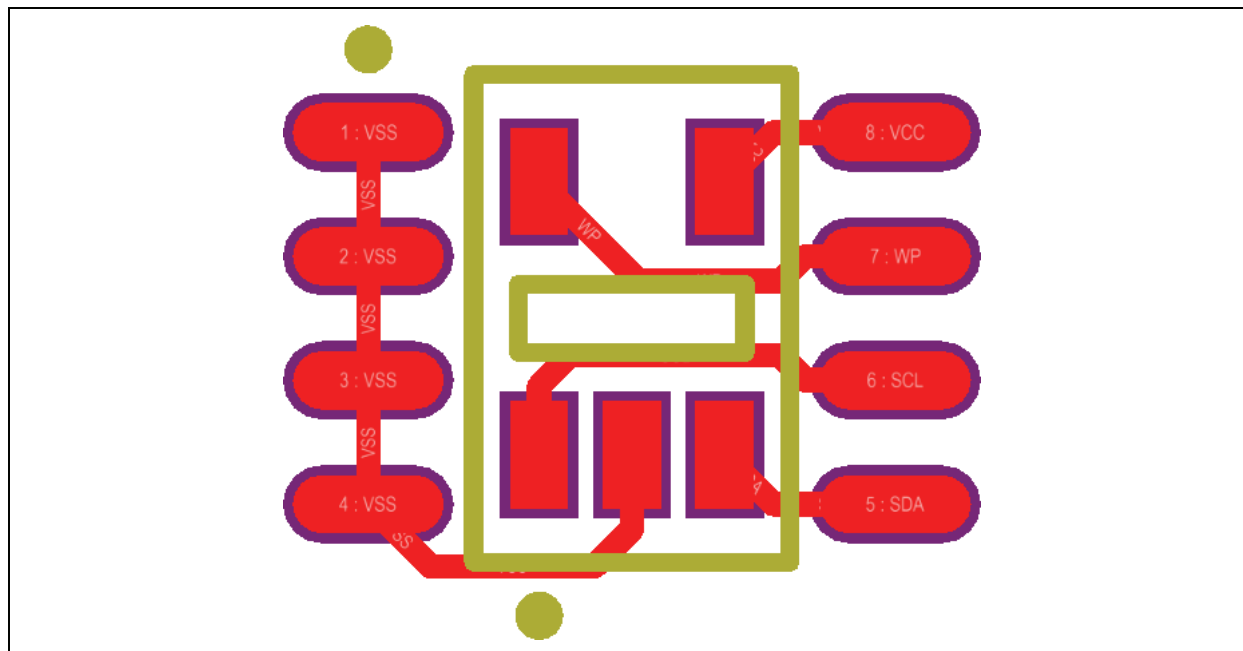


FIGURE 4: 5-LEAD SOT-23 AND 8-LEAD MSOP LAYOUT

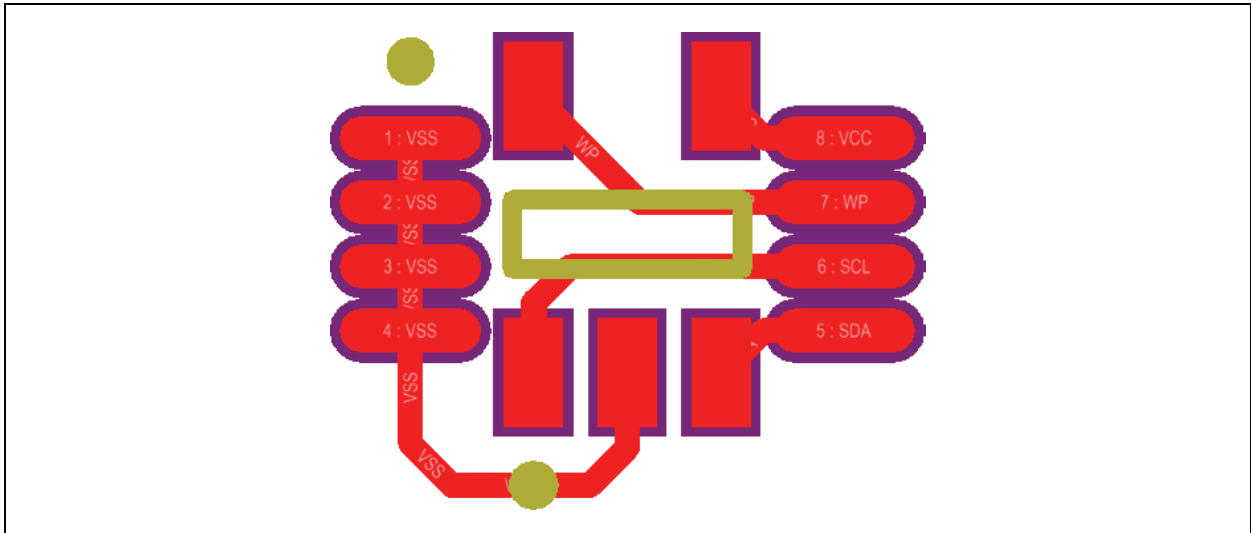
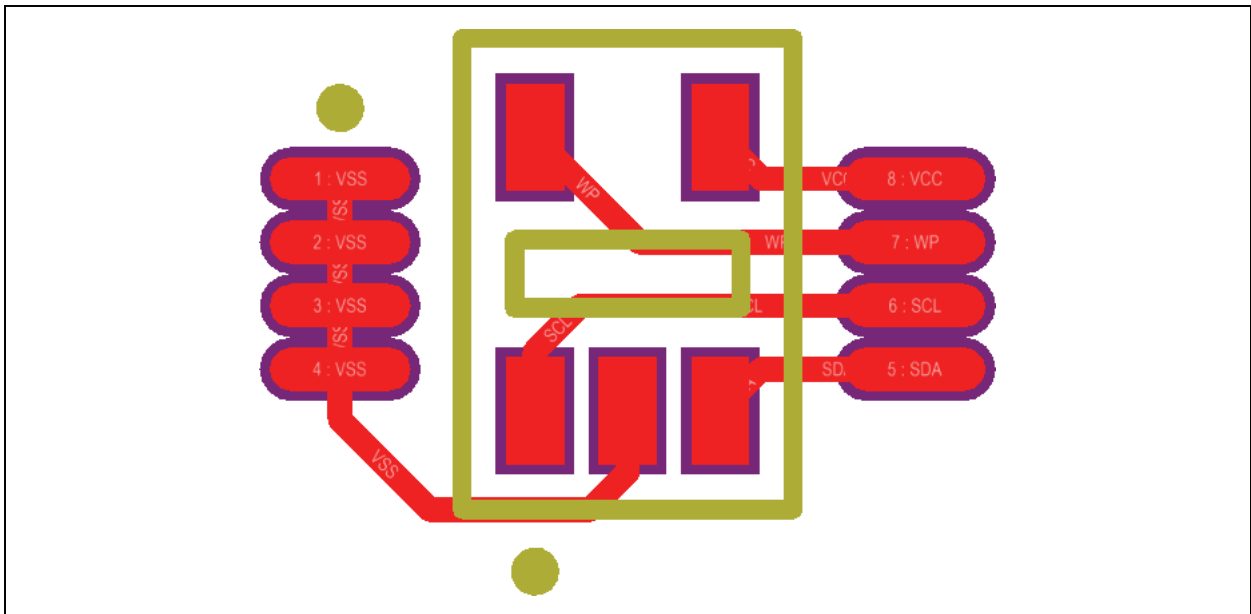


FIGURE 5: 5-LEAD SOT-23 AND 8-LEAD TSSOP LAYOUT



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EXAMPLE 6-LEAD SOT-23 LAYOUTS

The following images show example layouts for combining a 6-lead SOT-23 package with an 8-lead SOIC, MSOP, or TSSOP package. All footprints are drawn according to Microchip's recommended guidelines. The layout can be done using a single layer of copper, so the images show only top copper, top silk screen, and top solder mask layers.

Note: Pins 3 (A2) and 7 (WP) of the SOIC, TSSOP, and MSOP packages should be tied to Vss to match the functionality of 6-lead SOT-23 devices.

FIGURE 6: 6-LEAD SOT-23 AND 8-LEAD SOIC LAYOUT

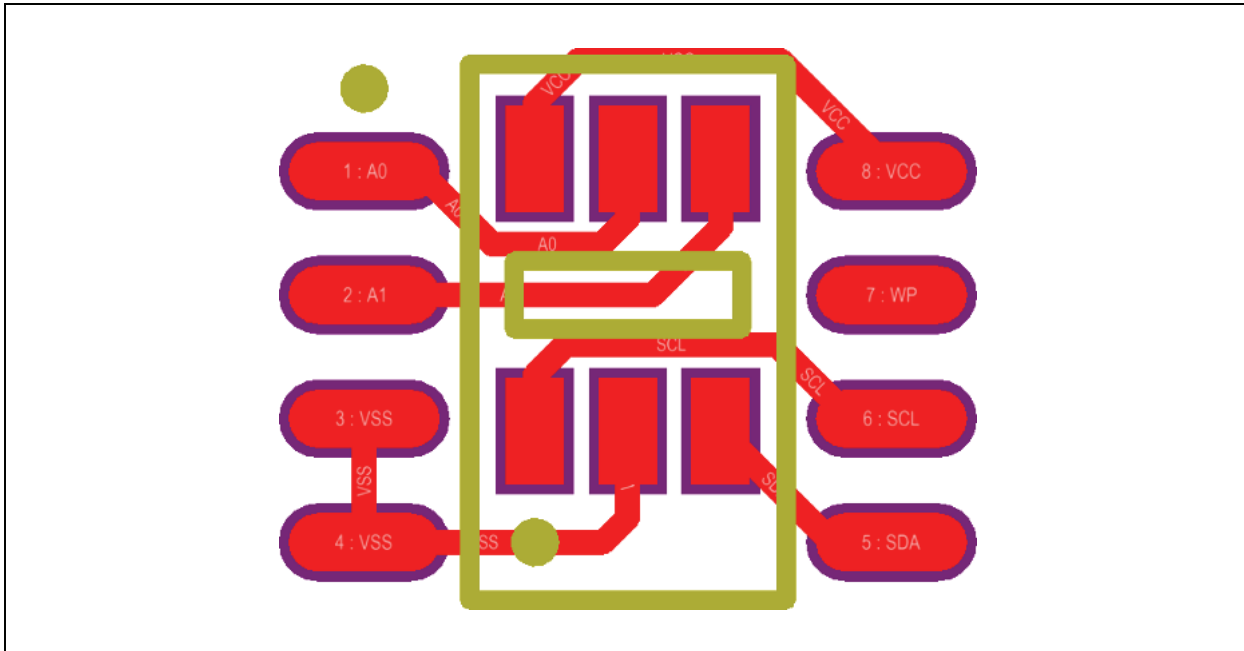


FIGURE 7: 6-LEAD SOT-23 AND 8-LEAD MSOP LAYOUT

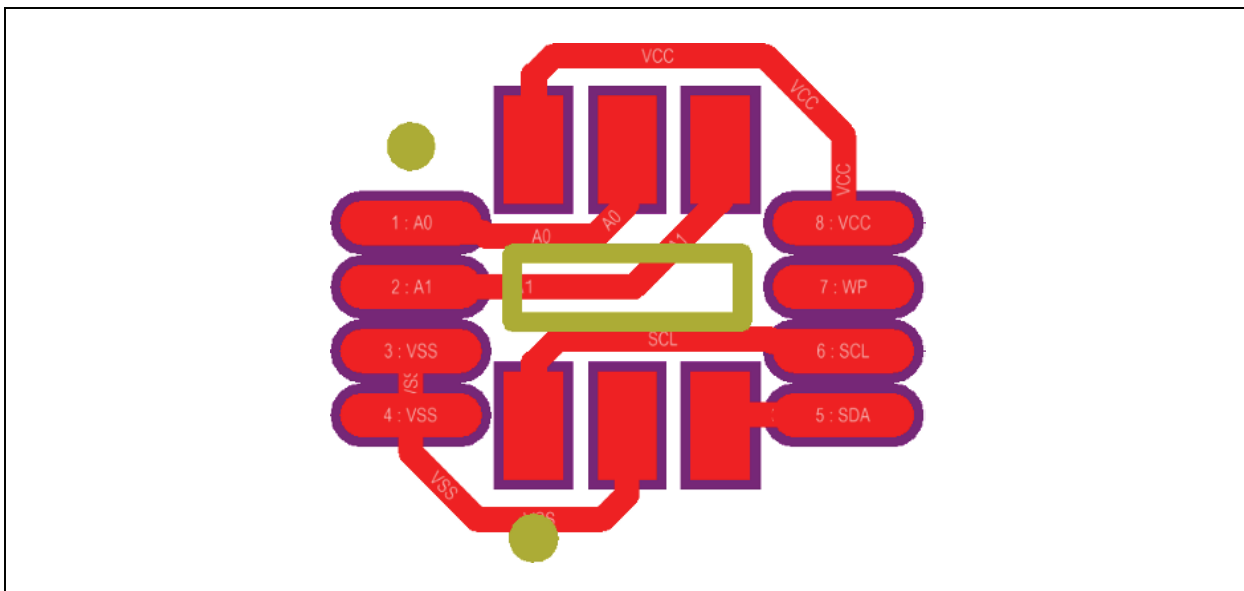
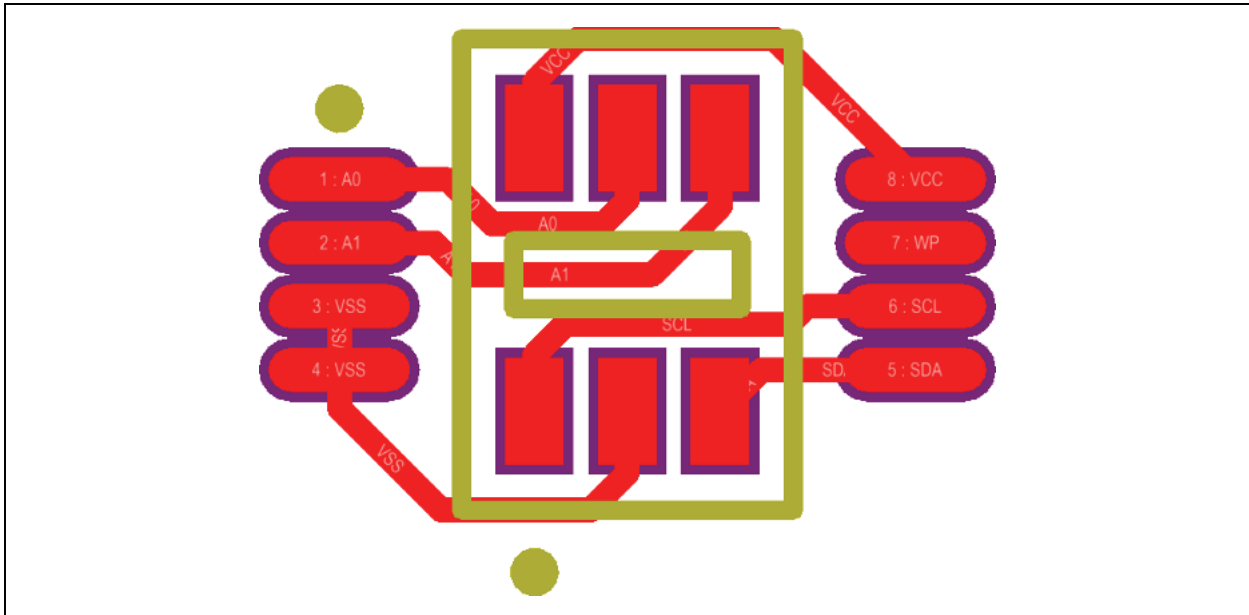


FIGURE 8: 6-LEAD SOT-23 AND 8-LEAD TSSOP LAYOUT



CONCLUSION

By utilizing the technique described in this application note, you can achieve the benefits of moving to the small SOT-23 package while maintaining the flexibility to use larger, 8-lead packages. In addition, you can maintain multiple approved vendors and gain advantages in inventory management. Implementing this technique requires very little additional board space, making it an ideal solution for many situations.

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APPENDIX A: REVISION HISTORY

Revision A (11/2011)

Initial Release.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

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