RoHS compliant

elmos

Sensor Signal Processor with SENT Interface

E520.33

PRELIMINARY INFORMATION – NOV 26, 2012

Features

- Optimized for resistive sensor bridges without external trim components
- Digital compensation for offset, sensitivity, non-linearity and temperature
- Configurable input range ±3 to ±400 mV
- Offset compensation up to ± 250 % FS
- 16-bit Delta Sigma ADC for the signal path
- Temperature compensation using on-chip sensor, bridge resistance, external diode, or external thermistor
- SENT interface for robust data transmission (according to SAE J2716 JAN2010)
- Digital programming using single-wire I/O shared with SENT terminal
- Supply: 4.75 ... 5.25V
- Over voltage and reverse polarity protection to ±18V; short circuit protection
- Comprehensive self test and diagnostic routines to detect sensor, supply or memory faults
- EEPROM memory stores calibration data

Applications

- New generation of automotive sensor transducers with SENT interface.
- Used for pressure, strain, force, torque, etc. based on resistive sensor bridges (e.g. piezo-resistive MEMS, thin/thick film on ceramic/steel, strain gauges, balance beam accelerometers).

Brief Functional Description

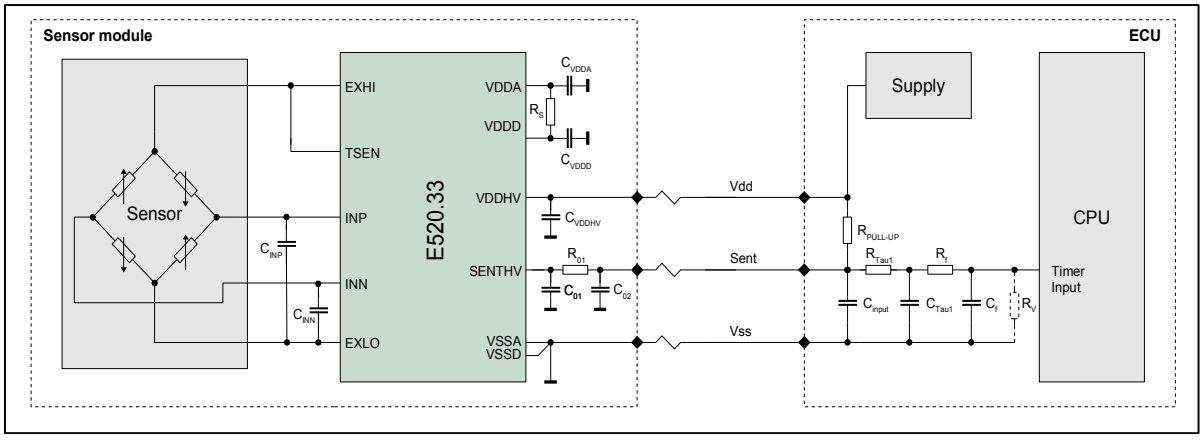
The E520.33 sensor signal processor amplifies and processes sensor signals with a variety of compensation, supply, output, diagnostic and interface options.
The programmable high CMRR input amplifier stage processes a wide range of sensor input spans and offsets. Both current and voltage bridge excitation are supported. A low-noise 16 bit delta sigma ADC digitizes the sensor signal. Temperature is measured by a dedicated 12 bit ADC internally, using the bridge resistance or an external thermistor. A linearization engine computes compensation for offset, sensitivity, non-linearity and temperature.
Extended self diagnostics and the SENT interface make it a perfect fit for new generation automotive electronic control units. A serial Input/Output interface (SIO) allows in-system calibration with only 3 wires connected to the outside. An embedded EEPROM stores configuration, calibration and custom user information.
The E520.33 is available in a 20-pin TSSOP package or as bare dice, and is qualified according to AEC-Q100 for -40°C to +125°C operation.

Ordering Information

Product ID	*Temperature range*	*Package*
E520.33	-40 ... +125°C	TTSOP20
E520.33-D	-40 ... +150°C	Dice *

** Contact factory for dice specifications*

Typical Operating Circuit



Functional Diagram

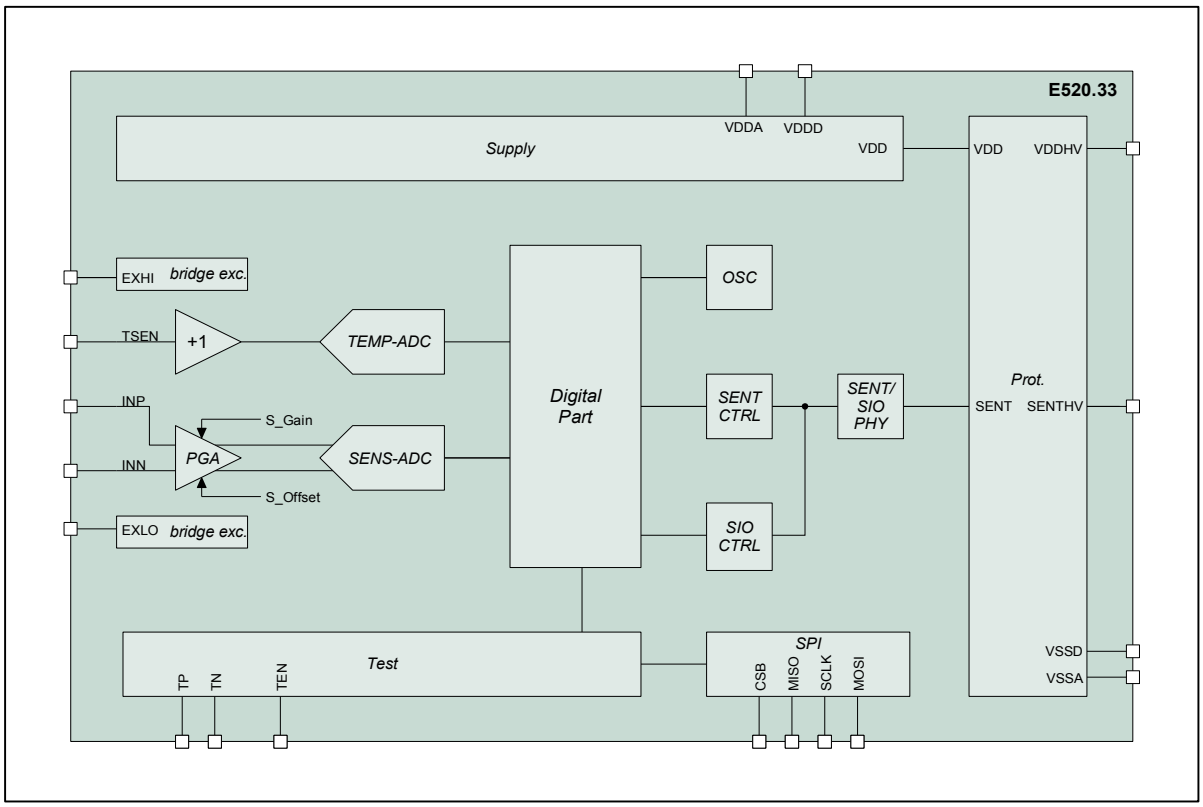


Fig. 1: Functional Block Diagram

Pin Configuration

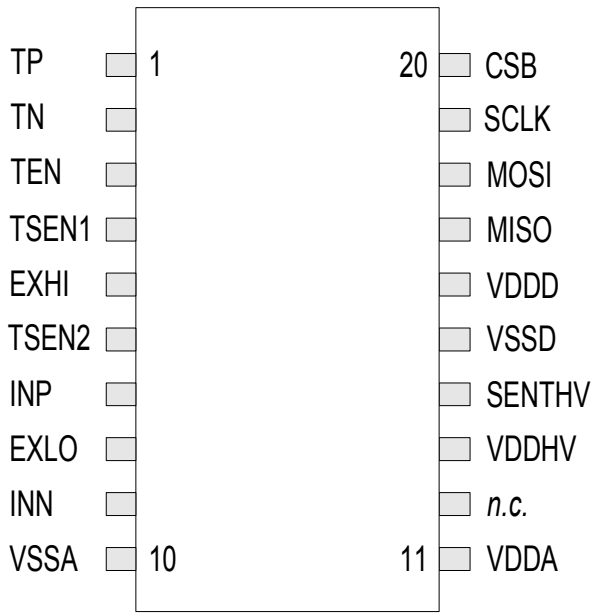


Fig. 2: Package pinout (top view not to scale)

Pin Description

Table 1: Pin description

No	*Name*	*Type* [1)]	*Description*
1	TP	D_IO	Test I/O. Leave unconnected in application!
2	TN	D_IO	Test I/O. Leave unconnected in application!
3	TEN	D_I	Test enable (active high). Connect to VSSD in application!
4	TSEN1	A_IO	Temp. sensor in / sensor substrate pull up/down configurable / positive analog test output
5	EXHI	A_O	Sensor bridge positive excitation
6	TSEN2	A_IO	Temp sensor in/ sensor substrate pull up/down configurable / negative analog test output
7	INP	A_I	Sensor signal positive input / positive analog test input
8	EXLO	A_O	Sensor bridge negative excitation
9	INN	A_I	Sensor signal negative input / negative analog test input
10	VSSA	S	Negative analog device supply
11	VDDA	A_IO	Internal analog supply voltage
12	n.c.		- not connected -
13	VDDHV	HV_S	High voltage supply
14	SENTHV	HV_A_IO	Protected SENT output; SIO port
15	VSSD	S	Negative digital device supply
16	VDDD	A_IO	Internal digital supply voltage
17	MISO	D_O	SPI data output (master in slave out)
18	MOSI	D_I	SPI data input (master out slave in)
19	SCLK	D_I	SPI clock input
20	CSB	D_I	SPI chip select (active low, pull up)

1) Explanation of Types: A = Analog, D = Digital, S = Supply, I = Input, O = Output, B = Bidirectional, HV = High Voltage

Package Information

Plastic Package

The product is available in a Pb free, RoHS compliant, 20 lead Thin Shrink Small Outline (TSSOP20) plastic package with only about 42 mm² (0.065 square inch) footprint area. For dimension details refer to JEDEC standard.

The device (packaged device only) has been qualified according to IEC 86 part 2-20 for the following soldering profile:

1.1.(200±5) °C, dwell time (50±5)s

2.2.(260±5) °C, dwell time <10 s

Bare Dice

Dice are delivered as wafers on foil. Sample volumes may be packed in waffle packs.

Sample volume:

Dice in waffle packs

Series volume: t.b.d.

Wafers: back grinded, not sawn

Wafer thickness after grinding: 400 µm ± 30 µm

Pad Layout

Fig. 3: Pad layout

Table 2: Pad coordinates, preliminary data

Pad	*X / µm* [1)]	*Y / µm* [1)]
TP **Do not bond this pad!**	809	3652
TN **Do not bond this pad!**	458	3652
TEN **Do not bond this pad!**	241	3652
TSEN1	69	2294
EXHI	69	1990
TSEN2	69	1315
INP	69	672
EXLO	69	427
INN	69	244
VSSA	649	72
VDDA	1848	72
VDDHV	2229	710
SENTHV	2168	1274
VSSD	2229	1902
VDDD	2229	2108
MISO	2228	2302
MOSI	2047	3652
SCLK	1826	3652
CSB	1606	3652

1) Center of bond pad, referred to lower left edge of IC.
For confirmation of pad coordinates please contact ELMOS Semiconductor AG for die delivery information.

1 Absolute Maximum Ratings

Stresses beyond these absolute maximum ratings listed below may cause permanent damage to the device. These are stress ratings only; operation of the device at these or any other conditions beyond those listed in the operational sections of this document is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. All voltages with respect to ground. Currents flowing into terminals are positive, drawn out of a terminal are negative.

No.	*Description*	*Condition*	*Symbol*	*Min*	*Max*	*Unit*
1	Negative supply voltage		V_{VSSA},V_{VSSD}	0	0	V
2	Positive supply voltage	over-voltage and reverse polarity protection	V_{VDDHV}	-18	18	V
3	I/O voltage SENTHV	over-voltage and reverse polarity protection	V_{SENTHV}	-18	18	V
4	DC current at VDDA and VDDD	1)	I_{VDDA}, I_{VDDD}	0	0	mA
5	Voltage at digital I/O pins		V_{DPIN}	-0.3	V_{VDDD} +0.3	V
6	Input current at digital pins		I_{DPIN}	-20	20	mA
7	Voltage at analog pins		V_{APIN}	-0.3	V_{VDDA} +0.3V	
8	Maximum voltage at TSEN1, TSEN2 pins	Both TSEN1 and TSEN2	V_{TSENx}		V_{EXHI} +0.3V 2)	
9	Input current at analog pins		I_{APIN}	-20	20	mA
10	Junction temperature		T_J	-40	+150	°C
11	Ambient temperature	packaged in TSSOP20	T_{AMB}	-40	+125	°C
12	Storage temperature (not supplied)	3)	$T_{ST,HOT1}$	-50	+125	°C
13	Storage temperature (not supplied)	< 500h, 3)	$T_{ST,HOT2}$	+125	+150	°C
14	Power dissipation		P_{TOT}		200	mW

1) Only a buffer capacitor is allowed to be connected to terminal VDDA and VDDD. No supply of any other external loads.

2) Or maximum limit for for V_{APIN}, whichever is lower

3) For moisture sensitive devices refer to JEDEC standard J-STD-033 for handling and using details. Storage at temperatures > 90°C for more than 96 h may affect the solderability of the devices. Storage is not considering packing materials such as tapes, reels, dry packs, foils, etc. Please contact ELMOS for packing material specifications.

2 ESD Protection

Description	*Condition*	*Symbol*	*Min*	*Max*	*Unit*
ESD HBM Protection		$V_{ESD(HBM)}$	-2	2	kV
ESD CDM Protection at all Pins	1)	$V_{ESD(CDM)}$	-500	500	V
ESD CDM Protection at Edge Pins	1)	$V_{ESD(CDM)C}$	-750	750	V

1) According to AEC-Q100-011 (CDM) chip level test

3 Recommended Operating Conditions

- Parameters are guaranteed within the range of recommended operating conditions unless otherwise specified.
- Operation beyond recommended operating conditions is not qualified and may affect device reliability.
- All voltages are referred to ground (0V).
- Currents flowing into the circuit have positive values.
- The first electrical potential connected to the IC must be GND.

No.	*Description*	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
1	Supply voltage		V_{VDDHV}	4.75	5.00	5.25	V
2	VDDHV buffer capacitor	1)	C_{VDDHV}	70	100	130	nF
3	VDDA / VDDD buffer capacitors	1)	C_{VDDA}, C_{VDDD}	70	100	130	nF
4	external supply connection VDDA - VDDD resistivity	8)	R_S	0	2	10	Ω
5	DC current at SENTHV		I_{SENTHV}	-1.2		+1.2	mA
6	Sensor bridge resistance	CV mode	R_B	0.8	5	20	kΩ
7	Overall current drawn from EXHI	CV mode	I_{EXHI}	-4.5			mA
8	Sensor bridge resistance	CC mode	R_B	0.8	5	15	kΩ
9	SENT receiver pullup resistor 5)		R_{PULLUP}	9.5		55	kΩ
10	SENT receiver input filter 1st stage resistor 5) 6)		R_{TAU1}	448	560	672	Ω
11	SENT receiver input filter 1st stage capacitance 5) 6)		C_{TAU1}	1.54	2.2	2.86	nF
12	SENT receiver input filter 1st stage time constant 5)		TAU1	0.74		1.73	µs
13	SENT receiver parasitic input capacitance 5)	7)	C_{IN}			100	pF
14	SENT receiver input filter 2nd stage time constant, determined by R_V, R_f and C_f 5)	2)	TAU2	0.6		1.4	µs
15	SENT transmitter EMI filter resistor 5) 9)		R_{01}	198	220	242	Ω
16	SENT transmitter EMI filter capacitance 5) 9)		C_{01}	1.54	2.2	2.86	nF
17	SENT transmitter EMI filter capacitance 5) 9)		C_{02}	1.54	2.2	2.86	nF
18	External capacitance between INN and EXLO 10)	optional	C_{INN}		1		nF
19	External capacitance between INP and EXLO 10)	optional	C_{INP}		1		nF
20	Junction temperature	normal operation	T_J	-40		+125	°C
21	Junction temperature	for max. 500h over life time 3)	T_J	+125		+150	°C

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
22	Junction temperature	for max. 4000h over life time 4)	T_J	+125		+150	°C
23	Junction temperature	during EEPROM programming	T_J	-40		+125	°C

1) Low ESR/ESL types required for EMC reasons.
2) R_f = 6.8kΩ typ., C_f = 220pF typ., R_v = 12kΩ typ.
3) With automatic EEPROM refresh disabled
4) With automatic EEPROM refresh enabled
5) See chapter 5.1.8
6) Overall tolerance must meet TAU1, TAU2
7) 500pF max wiring parasitic capacitance
8) If R_S = 0: C_{VDDA} = 150nF typ, C_{VDDD} = 0
9) Values correspond to a tick-time of 12µs, for other tick-times see separate application note
10) Prevention of electromagnetic disturbances

4 Electrical Characteristics

4.1 Analog Features

(T_{AMB} = -40°C to +125°C, unless otherwise noted. Typical values are at VDDHV = 5.0V, and T_{AMB} = +25°C. Positive currents flow into the device pins.)

Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Consumption, Voltage Monitor, and Power-On-Reset						
Current consumption	without sensor excitation current and SENT interface current, no output current at MISO	I_{VDDHV}		8.5	10	mA
3V mode low threshold rising edge (POR threshold)	VDDA, VDDD pins	$V_{VDD\_3L\_THRES}$	2.80	3.00	3.15	V
3V mode low hysteresis 1)	VDDA pin	$V_{VDD\_3L\_HYS}$	30	70	100	mV
POR hysteresis 1)	VDDD pin	V_{POR_HYS}	100		250	mV
3V mode Hi threshold rising edge	VDDA, VDDD pin	$V_{VDD\_3H\_THRES}$	3.45	3.60	3.85	V
3V mode high hysteresis 1)	VDDA, VDDD pin	$V_{VDD\_3H\_HYS}$	30	70	100	mV
5V mode low threshold rising and falling edge	VDDHV pin	$V_{VDD\_5L\_THRES}$	4.25	4.50	4.75	V
5V mode low hysteresis 1)	VDDHV pin	$V_{VDD\_5L\_HYS}$	30	70	100	mV
5V mode high threshold rising and falling edge	VDDHV pin	$V_{VDD\_5H\_THRES}$	5.25	5.50	5.65	V
5V mode high hysteresis 1)	VDDHV pin	$V_{VDD\_5H\_HYS}$	30	70	100	mV
Over-Voltage and Reverse Voltage Protection						
Over voltage threshold rising edge at pin VDDHV 1)		V_{VDDHV_THO}	5.65	6.00	6.35	V
Sensor Excitation						
Sensor positive excitation voltage (constant voltage mode = CVM)	-4.5mA < I_{EXHI} ≤ 0	V_{EXHI}	2.8	2.95	3.45	V
Sensor positive excitation output short circuit current limit (CVM)		$I_{EXHI,lim}$	-15		-7	mA
Sensor positive excitation voltage (constant current mode = CCM)		V_{EXHI}	1.2		V_{VDDA} - 0.50	V
Sensor excitation current (CCM)	CCUR = 0000b	I_{EXHI1}	-10%	-220	+10%	µA
Sensor excitation current (CCM)	CCUR = 0001b	I_{EXHI2}	-10%	-270	+10%	µA
Sensor excitation current (CCM)	CCUR = 0010b	I_{EXHI3}	-10%	-330	+10%	µA
Sensor excitation current (CCM)	CCUR = 0011b	I_{EXHI4}	-10%	-390	+10%	µA
Sensor excitation current (CCM)	CCUR = 0100b	I_{EXHI5}	-10%	-470	+10%	µA

Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Sensor excitation current (CCM)	CCUR = 0101b	I_{EXHI6}	-10%	-560	+10%	µA
Sensor excitation current (CCM)	CCUR = 0110b	I_{EXHI7}	-10%	-680	+10%	µA
Sensor excitation current (CCM)	CCUR = 0111b	I_{EXHI8}	-10%	-820	+10%	µA
Sensor excitation current (CCM)	CCUR = 1000b	I_{EXHI9}	-10%	-1.0	+10%	mA
Sensor excitation current (CCM)	CCUR = 1001b	I_{EXHI10}	-10%	-1.2	+10%	mA
Sensor excitation current (CCM)	CCUR = 1010b	I_{EXHI11}	-10%	-1.5	+10%	mA
Sensor excitation current (CCM)	CCUR = 1011b	I_{EXHI12}	-10%	-1.8	+10%	mA
Sensor excitation current (CCM)	CCUR = 1100b	I_{EXHI13}	-10%	-2.2	+10%	mA
Sensor excitation current (CCM)	CCUR = 1101b	I_{EXHI14}	-10%	-2.7	+10%	mA
Sensor excitation current (CCM)	CCUR = 1110b	I_{EXHI15}	-10%	-3.3	+10%	mA
Sensor excitation current (CCM)	CCUR = 1111b	I_{EXHI16}	-10%	-3.9	+10%	mA
Sensor Amplifier						
Full scale differential input voltage	Depending on GPGA, s. Table 4	$V_{INP} – V_{INN}$	± 3		± 400	mV
Programmable Amplifier Gain	GPGA = 0000b	G1	-10%	4.00	+10%	V/V
Programmable Amplifier Gain	GPGA = 0001b	G2	-10%	5.44	+10%	V/V
Programmable Amplifier Gain	GPGA = 0010b	G3	-10%	7.39	+10%	V/V
Programmable Amplifier Gain	GPGA = 0011b	G4	-10%	10.04	+10%	V/V
Programmable Amplifier Gain	GPGA = 0100b	G5	-10%	13.65	+10%	V/V
Programmable Amplifier Gain	GPGA = 0101b	G6	-10%	18.55	+10%	V/V
Programmable Amplifier Gain	GPGA = 0110b	G7	-10%	25.24	+10%	V/V
Programmable Amplifier Gain	GPGA = 0111b	G8	-10%	34.33	+10%	V/V
Programmable Amplifier Gain	GPGA = 1000b	G9	-10%	46.63	+10%	V/V
Programmable Amplifier Gain	GPGA = 1001b	G10	-10%	63.42	+10%	V/V
Programmable Amplifier Gain	GPGA = 1010b	G11	-10%	86.27	+10%	V/V
Programmable Amplifier Gain	GPGA = 1011b	G12	-10%	117.04	+10%	V/V
Programmable Amplifier Gain	GPGA = 1100b	G13	-10%	159.01	+10%	V/V
Programmable Amplifier Gain	GPGA = 1101b	G14	-10%	216.37	+10%	V/V
Programmable Amplifier Gain	GPGA = 1110b	G15	-10%	294.24	+10%	V/V
Programmable Amplifier Gain	GPGA = 1111b	G16	-10%	400.00	+10%	V/V
Input referred voltage noise density [1) 2)]	Thermal noise only, GPGA = 0000b .. 0010b	$e_{n,th,1..3}$		250		$\frac{nV/}{\sqrt{Hz}}$
Input referred voltage noise density [1) 2)]	Thermal noise only, GPGA = 0011b .. 1111b	$e_{n,th,4...16}$		150		$\frac{nV/}{\sqrt{Hz}}$

Description	Condition	Symbol	Min	Typ	Max	Unit
First stage saturation detector low threshold		$V_{SATTHLO}$		5.0	6.7	% V_{VDDA}
First stage saturation detector high threshold		$V_{SATTHHI}$	93.3	95.0		% V_{VDDA}
Sensor Offset Compensation						
Lowest input referred coarse compensation voltage (internally added)	V_{EXHI} -V_{EXLO}= 2.8V 3)	$V_{OFFSET,LO}$		-2.5		FSIVR 4)
Highest input referred coarse compensation voltage (internally added)	V_{EXHI} – V_{EXLO}= 2.8V 3)	$V_{OFFSET,HI}$		+2.5		FSIVR 4)
Offset compensation resolution (including sign) 5)		N		5		Bit
Total offset compensation error 2) 6)	V_{EXHI} -V_{EXLO} ≥ 2.8V	V_{ERROR}			0.25	LSB
Delta-Sigma Modulator of signal (SENS-ADC)						
Signal-to-noise ratio 2) 7)	Bandwidth: 0 ... f_{OUT}/2 (see Table 10, ch. 5.3)	SNR		90		dB
Total harmonic distortion 2)	Bandwidth 0 ... f_{OUT}/2 (see Table 10, ch. 5.3)	THD		-66		dB
No missing code 1)		MC			0	codes
Temperature Measurement Channel						
Differential FS-range input voltage	Int. reference, see Table 7, ch. 5.1.7	V_{TSEN}		± V_{VDDA}/2		
Differential FS-range input voltage	Ext. reference, s. Table 7, ch. 5.1.7	V_{TSEN}		± V_{EXHI}/2		
Temperature ADC resolution		RES_{TSEN}		14		Bits
Integral non-linearity 2)		INL_{TSEN}	-0.05		0.05	% FS
Maximum update rate		$RATE_{TSEN}$		500		Hz

1) Defined by design. Not subject to production test.

2) Not valid in low-power mode.

3) When V_{EXHI} - V_{EXLO} is not equal 2.8 V, the given values must be scaled proportionally. See 5.1.5.2 for details.

4) FSIVR means Full Scale Input Voltage Range at PGA input terminals INP, INN (gain dependent, see Table 5, 5.1.5.2).

5) From the full-scale range of V_{OFFSET_HI} - V_{OFFSET_LO}

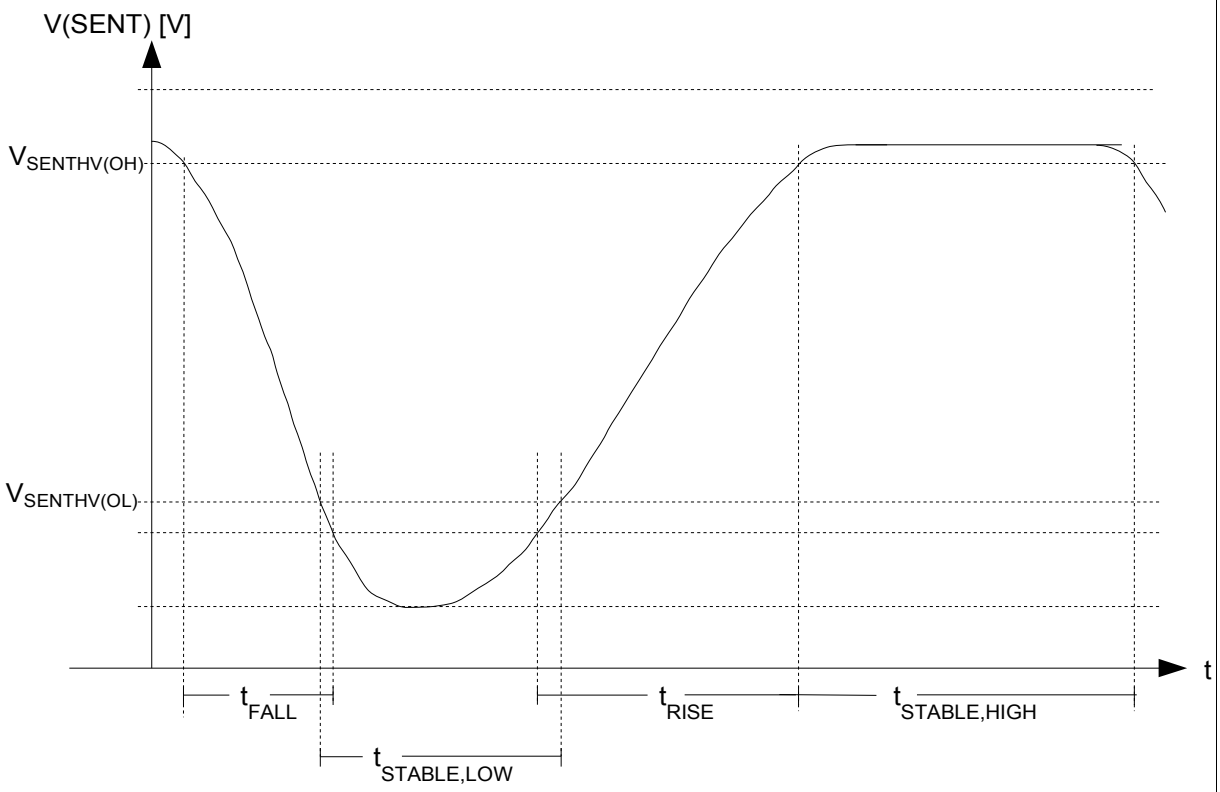
6) LSBs of the offset compensation voltage (full-scale range V_{OFFSET_HI} - V_{OFFSET_LO}, resolution N)

7) In CV mode. In CC mode in ratiometric measurements SNR will be 78dB, typically.

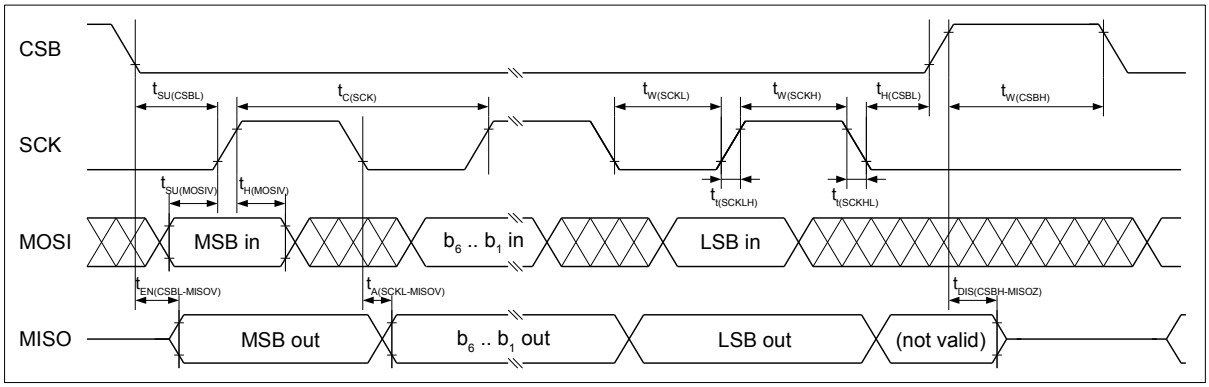
4.2 Digital Features

(T_{AMB} = -40°C to +125°C, unless otherwise noted. Typical values are at VDDHV = 5.0V, and T_{AMB} = +25°C. Positive currents flow into the device pins.)

Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
SENT Physical Interface						
Signal fall time, (see timing diagram below) 2)	clock tick = 12µs, measured at SENT, receiver connected	t_{FALL}			26	µs
Signal rise time, (see timing diagram below) 2)	clock tick=12µs, measured at SENT, receiver connected	t_{RISE}			72	µs
Low state output voltage 1	I_{SENTHV} < 0.1mA, measured at SENT-wire	$V_{SENTHV(OL1)}$			0.5	V
Low state output voltage 2	I_{SENTHV} < 0.52mA, measured at SENT-wire	$V_{SENTHV(OL2)}$			0.65	V
High state output voltage	I_{SENTHV}> -0.32mA, measured at SENT-wire	$V_{SENTHV(OH)}$	4.1			V
Sink current limitation		$V_{SENTHV(SINK)}$			15	mA
Source current limitation		$V_{SENTHV(SRC)}$	-10			mA
Tristate output leakage 1	T_J ≤ 125 °C; -5V < V_{SENTHV} < 5V	$V_{SENTHV(LEAK1)}$	-10		10	µA
Tristate output leakage 2 3)	VDDHV short with VSSA/VSSD and T_J = 150 °C, -5V<V_{SENTHV} < 5V 4)	$V_{SENTHV(LEAK2)}$	-60		60	µA
Low state duration, (see timing diagram below) 2)	clock tick=12µs, measured at SENT, receiver connected, pulse low for 5 clk ticks	$t_{STABLE,LOW}$	24			µs
High state duration, (see timing diagram below) 2)	clock tick=12µs, measured at SENT, receiver connected, pulse high for 7 clk ticks	$t_{STABLE,HIGH}$	24			µs
Threshold falling in SIO-mode		$V_{SENTHV(IL)}$	0.3			VDD
Threshold rising in SIO-mode		$V_{SENTHV(IH)}$			0.7	VDD



Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Oscillator						
Output frequency	Trimmed on-chip	f_{OSC}	7.6	8	8.4	MHz
Serial Peripheral Interface (SPI)						
SPI clock frequency	$C_{LOAD} \leq$ 50pF at MISO	$f_{SCK} = 1/t_{C(SCK)}$			8	MHz
time between two SPI frames [1]	f_{SYS} = 8MHz	$t_{W(CSBH,0)}$	1			µs
[1]	f_{SYS} = 4MHz	$t_{W(CSBH,1)}$	2			µs
[1]	f_{SYS} = 2MHz	$t_{W(CSBH,2)}$	4			µs
[1]	f_{SYS} = 1MHz	$t_{W(CSBH,3)}$	8			µs
MOSI setup time [1]		$t_{SU(MOSIV)}$	20			ns
CSB to MISO time [1]	C_{LOAD} = 50pF	$t_{EN(CSBL-MISOV)}$			40	ns
SCLK to MISO time [1]	C_{LOAD} = 50pF	$t_{SA(SCKL-MISOV)}$			40	ns



Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Digital Timing Parameters						
Digital reset delay 1)		t_{RESET}	100		500	µs
Duration of time window (modes of operation) 1)		t_{WINDOW}	4.5	5	5.5	ms
Time elapsed before diagnostic voltage monitoring is enabled 1)		t_{DIS_VMON}	1			ms
Sensor Diagnosis						
Threshold at INP, INN	$V_{EXHI} \geq 1.2V$	$V_{TH,SERR1}$	$0.87 \cdot V_{EXHI}$ - 30mV		$0.93 \cdot V_{EXHI}$ + 30mV	
Threshold at INP, INN	$V_{EXHI} \geq 1.2V$	$V_{TH,SERR2}$	$0.07 \cdot V_{EXHI}$ - 30mV		$0.13 \cdot V_{EXHI}$ + 30mV	
Threshold at EXHI		$V_{TH,SERR3}$	$0.21 \cdot V_{VDDA}$		$0.29 \cdot V_{VDDA}$	
RPU between EXHI and INP	SPU=1b	$R_{PU,INP}$	1		10	MΩ
RPU between EXHI and INN	SPU=1b	$R_{PU,INN}$	1		10	MΩ

1) Defined by design. Not subject to production test.

2) Values scale proportionally to tick-time, TX-filter corresponding to tick-time, according to application note.

3) ± 20 µA for VDDHV short with VSSA / VSSD and $T_J \leq 125$ °C.

4) Condition corresponds to ground loss with V_{VDDHV} = +5 V, V_{SENTHV} = 0 V; and supply loss with V_{SENTHV} = +5 V

5 Functional Description

5.1 Analog Part

The E520.33 Sensor Signal Processor (SSP) has been designed to meet the requirements of high precision automotive sensor applications. The digital SENT interface protocol (Single Edge Nibble Transmission, SAE J2716, see ch. 7) allows a robust transmission of the sensor signal to the supervisory electronic control unit (ECU).

The proprietary automotive proven high voltage sub micron CMOS process provides high resolution signal processing. Various programmable configuration options allow the adaptation to almost every bridge type resistive sensor.

The low noise programmable gain amplifier can be adapted to a wide range of sensor sensitivity values. A coarse sensor offset compensation close to the input is provided for best possible use of the input range of subsequent stages even with sensors showing significant offset values.

A high performance ΔΣ-converter uses optimized digital filters to give maximum resolution at the selected sample rate. The following compensation engine is based on 16 bit data processing to provide efficient reduction of temperature influences and non-linearity.

System calibration does not need additional terminals to be fed out of the module. The SENT interface terminal also serves as a Serial Calibration Interface (SIO) which can be invoked within a particular time frame after power up. It permits to read data from the device as well as writing configuration and calibration data to the embedded non-volatile memory.

5.1.1 General

Many sensor elements (e.g. MEMS, strain gauges, GMR) provide mV-signals derived from resistive bridge configurations. For further processing every sensor cell needs at least an amplification. The trend towards cost effective, factory calibrated sensor modules (transducers) implies the need for integrated electronics doing both amplification plus a compensation of higher order effects to achieve a linear dependence of the output signal related to physical input measure.

This automotive programmable signal processing IC with SENT interface provides sensor signal amplification, analog-to-digital conversion, and linearization with a simple user interface for calibration. A variety of configurations supports different types of sensors and applications.

A programmable gain input amplifier stage (PGA) provides a wide full scale input range and a coarse sensor offset compensation to meet the requirements of different kinds of sensors (focus on piezo resistive Si-based MEMS, ceramic cells, strain gauges, AMR/GMR sensors). A subsequent high resolution Δ Σ-ADC converts the analog signal to digital. Compensation for non-linearity and temperature dependence of the sensor output signal is then computed by a dedicated arithmetic unit. A set of coefficients in the non-volatile memory (NVM), which were programmed during factory calibration, allow to compensate for the individual behaviour of the particular sensor cell used. This is necessary due to large parameter distributions usually appearing even among a population of sensor cells coming from a single lot.

Factory in-system calibration is simplified by either a one wire interface (SIO) using the SENT interface terminal to write calibration and configuration data into the NVM, or by a digital interface (SPI) having access to the NVM.

An over-voltage and reverse polarity protection is mandatory for automotive applications. A built in self test (BIST) allows those customers purchasing bare dice to test the device after assembly.
Self diagnostic functions allow for system diagnosis capability during operation.

5.1.2 Supply

The device is supplied from a single supply of 5 V (typ.) between terminal VDDHV and VSSA, VSSD. The protection circuitry at VDDHV and VSSA, VSSD terminals prevents damage to the device in case of over-voltage or reverse polarity conditions within the specified maximum ratings.

An internal voltage regulator provides 3.3 V (typical) for digital and analog functions as well as for the sensor excitation.

All digital inputs provide CMOS thresholds related to VDDD. Digital outputs provide VDDD (3.3 V typ.) CMOS levels respectively. All analog inputs are limited to VDDA level.

The SENT terminal is designed for operation with a pull up resistor referred to (4.85 ... 5.15) V (receiver supply according to SAE J2716, s. ch. 7).

The protection circuitry prevents damage to the device in case of over-voltage or reverse polarity conditions at the supply terminals VDDHV and VSSA, VSSD within the specified maximum ratings.

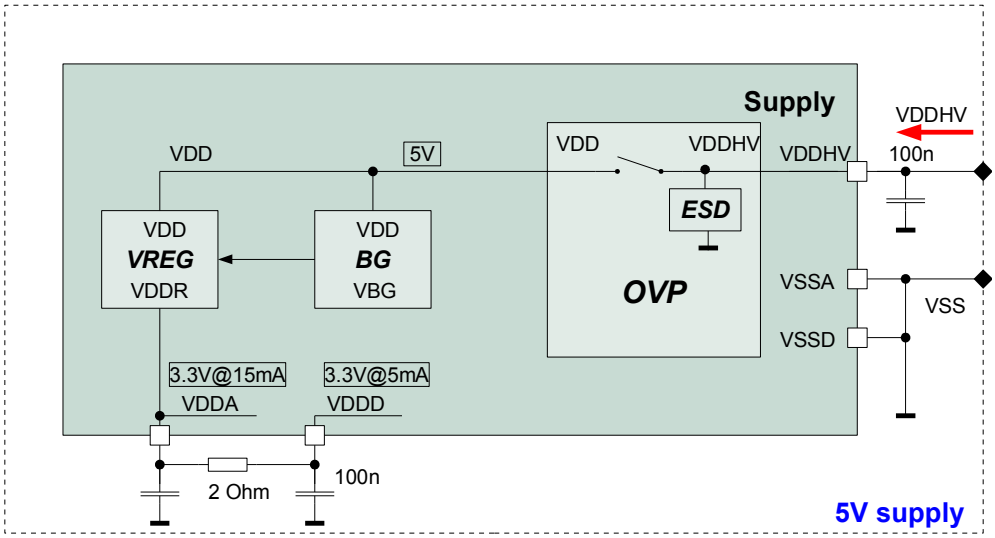


Fig. 4: Block diagram of 5V-supply concept

5.1.2.1 Power On Reset and Voltage Monitor

The voltage monitor block observes the VDD (5V), the VDDA (3.3V) and the VDDD (3.3V) voltages. It generates also the POR signal.

After power-up (POR) the output signals VDDOK, VMA3OK and VMD30K (see Fig. 5) are only valid if the bandgap voltage and the bias currents are trimmed. After trimming a settling time must be considered.

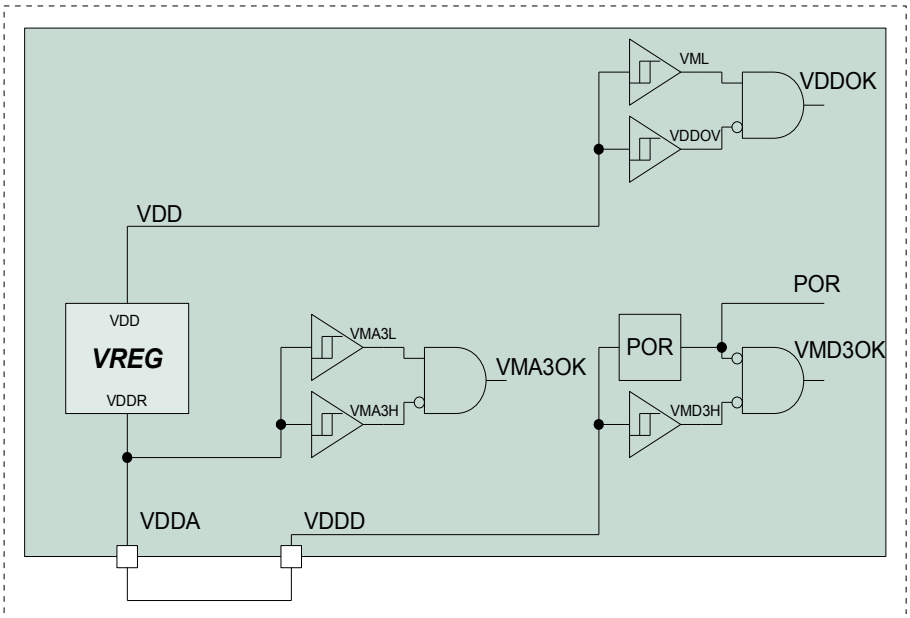


Fig. 5: Block diagram of voltage monitor and power-on reset

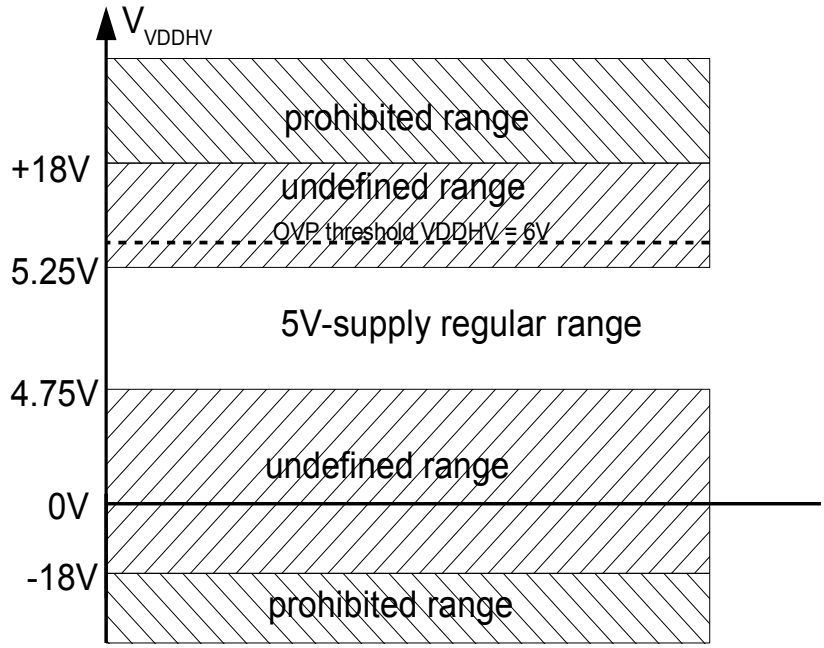


Fig. 6: Applicable levels of 5V-supply VDDHV

5.1.3 Over Voltage and Reverse Voltage Protection

OVP/RVP block is designed for over-voltage and reverse voltage protection of the external pin VDDHV preventing a penetration the extremely large and low external voltage to internal device parts.

Pin VDDHV is opened for transmit of an external supply voltage to internal net VDD for V_{VDDHV}<6V, with the optimal range inside 4.75V ... 5.25V. Pin VDDHV is closed for V_{VDDHV} up to -18V, i.e. reverse voltage mode, and is closed for V_{VDDHV} > 6V, up to 18V, i.e. over-voltage mode. Thus, the internal supply VDD of the chip is turned off when V_{VDDHV} > 6V or V_{VDDHV} < 2V.

Table 3: Effect of incorrect external connections / wiring

Connections	V_{VSSA} , V_{VSSD}	V_{SENTHV}	V_{VDDHV}	*Comment*
normal connections	0V	0V ... 5V	5V	normal operation
supply reversal	5V	0V ... 5V	0V	potentials at VDDHV and SENTHV below ground protected by OVP-circuit. SENTHV is high-Z. Leakage at SENTHV slightly pulls input of ECU high.
supply over-voltage	0V	0V ... 5V	18V	over-voltage condition detected by OVP-circuit. SENTHV high-Z
supply reversal with over-voltage	18V	0V ... 5V	0V	potentials at VDDHV and SENTHV deeply below ground protected by OVP-circuit. SENTHV is high-Z. Leakage at SENTHV slightly pulls input of ECU high.
SENTHV and VSS shorted	0	0	5V	current limitation activated when SENT is driven high. Refer to description of digital part for reaction of the chip
SENTHV and VDDHV shorted	0	5V	5V	current limitation activated when SENT is driven low. Refer to description of digital part for reaction of the chip
SENTHV and VDDHV shorted at over-voltage	0	18V	18V	over-voltage detected
SENTHV and VSS swapped	0 ... 5V	0V	5V	chip is poorly supplied via pull-down in ECU. chip will be in under-voltage condition. SENTH in HIGH-Z Leakage current at SENTHV flowing into ECU-input. Not detectable by ECU
SENTHV and VDDHV swapped	0	5V	0 ... 5V	chip is poorly supplied via pullup in ECU. Chip will be in under-voltage condition. Not detectable by ECU
pin order rotated	0 ... 5V	5V	0	chip is unsupplied, possibly with reverse supply. Not detectable by ECU
pin order rotated	5V	0V	0 ... 5V	chip is unsupplied, possibly with reverse supply. Not detectable by ECU

5.1.4 Sensor Excitation

Two modes for sensor bridge excitation are provided: constant current (CC) mode and constant voltage (CV) mode. The excitation mode can be selected with configuration register SENSIF.EXMODE.

Constant Voltage Mode (CV)

In CV mode a voltage regulated from the internal supply voltage VDDA is used for sensor excitation. Regulation is based on the internal bandgap voltage. As small variations of EXHI over process, supply voltage, and temperature ranges can still occur, the EXHI pin voltage is fed back as a reference for the signal conditioning in order to maintain ratiometric operation. The same applies to pin EXLO which is internally connected to VSSA.

Constant Current Mode (CC)

In CC mode a programmable excitation current is applied to the bridge. For e.g. Si-MEMS pressure sensors the CC excitation offers an inherent coarse compensation of temperature dependent sensor properties. At the same time, the voltage at EXHI carries information on the sensor device temperature.

The current can be programmed in 16 steps by the configuration register SENSIF.CCUR. The resulting current values follow the IEC E12 sequence (see Electrical Characteristics, section “Sensor excitation”).

5.1.5 Sensor Amplifier

This device is optimized for sensors forming a resistive bridge. It covers a broad range of bridge resistor values and sensitivity values. Versatile configuration options and a high performance signal acquisition chain allow adaptation to many types of sensors for pressure, strain, force, torque, acceleration etc. (e.g. piezo-resistive MEMS, thin/thick film on ceramic/steel, balance beam accelerometers, strain gauges).

5.1.5.1 Programmable Gain Amplifier (PGA)

A high performance, low noise, and low offset programmable gain amplifier (PGA) copes with a large range of full scale differential input voltages. Superior signal to noise ratio enables low sensitivity sensor signal conditioning down to about 1 mV/V sensor full scale sensitivity. The PGA provides a differential output for the following sensor ADC.

A configurable switch at the input allows for adaptation of the sensor signal's polarity (configuration register SENSIF.POL).

The amplification can be programmed to 16 values arranged in a harmonic sequence in order to be able to find an optimum adaptation to the sensitivity of the particular sensor (configuration register SENSIF.GPGA). A coarse compensation of the input-referred offset up to ±250 % of the full-scale signal can be performed (configuration registers SENSIF.OPOL and SENSIF.OPGA).

Table 4: PGA - Maximum input common mode range and signal voltages

Gain (typical)	*Input common-mode voltage range V_{CMIN} [% V_{VDDA}] 1) (min.)*	*Full-Scale differential signal voltage range [mV] (min.)*
4.00	29 - 71	± 400
5.44	23 - 77	± 294
7.39	19 - 81	± 216
10.04	29 - 71	± 159
13.65	23 - 77	± 117
18.55	19 - 81	± 86.2
25.24	29 - 71	± 63.4
34.33	23 - 77	± 46.6
46.63	19 - 81	± 34.3
63.42	16 - 84	± 25.2
86.27	14 - 86	± 18.6
117.04	12 - 88	± 13.7
159.01	11 - 89	± 10.0
216.37	10 - 90	± 7.39
294.24	9 - 91	± 5.44
400.00	9 - 91	± 4.00

1) Specified as % V_{VDDA}, because V_{EXHI} - V_{EXLO} depends on excitation mode (CV or CC) and on temperature (in CC mode)

5.1.5.2 Sensor Offset Compensation

A coarse compensation of the sensor offset voltage in the second amplifier stage allows an efficient use of the sensor amplifier gain settings and, therefore, the dynamic range of the following sensor ADC.

Offsets up to ±250% of the full scale input voltage range (FSIVR) can be compensated for by using the 4-bit configuration register SENSIF.OPGA and the polarity setting SENSIF.OPOL. The register combination can be programmed with values ranging from -15 to +15. Table 5 shows which input-referred offset compensation voltage corresponds to which {OPOL,OPGA[3:0]} setting when $V_{EXHI} – V_{EXLO} = 2.8$ V.

Values in Table 5 are given in the units of FSIVR. The FSIVR is dependent on the chosen PGA gain setting (configured by SENSIF.GPGA, see Table 4).

The compensation voltage is proportional to V_{EXHI} - V_{EXLO}. When V_{EXHI} - V_{EXLO} is not equal to 2.8 V, the compensation voltage resulting from the chosen OPGA setting must be scaled proportionally (for example, if V_{EXHI} - V_{EXLO} = 3 V, {OPOL,OPGA[3:0]} = 01111b, i.e. +15, adds a compensation voltage of 2.679 · FSIVR to the input signal).

Table 5: Sensor offset compensation - Input referred offset compensation voltage for different settings of SENSIF.OPOL and SENSIF.OPGA

{OPOL , OPGA[3:0]}$_{decimal}$	*{OPOL , OPGA[3:0]}$_{binary}$*	*Input-referred offset compensation voltage when V_{EXHI} - V_{EXLO} = 2.8 V* 1)
+15	01111b	+2.500 · FSIVR
+14	01110b	+2.333 · FSIVR
+13	01101b	+2.167 · FSIVR
+12	01100b	+2.000 · FSIVR
+11	01011b	+1.833 · FSIVR
+10	01010b	+1.667 · FSIVR
+9	01001b	+1.500 · FSIVR
+8	01000b	+1.333 · FSIVR
+7	00111b	+1.167 · FSIVR
+6	00110b	+1.000 · FSIVR
+5	00101b	+0.833 · FSIVR
+4	00100b	+0.667 · FSIVR
+3	00011b	+0.500 · FSIVR
+2	00010b	+0.333 · FSIVR
+1	00001b	+0.167 · FSIVR
0	X0000b	0
-1	10001b	-0.167 · FSIVR
-2	10010b	-0.333 · FSIVR
-3	10011b	-0.500 · FSIVR
-4	10100b	-0.667 · FSIVR
-5	10101b	-0.833 · FSIVR
-6	10110b	-1.000 · FSIVR
-7	10111b	-1.167 · FSIVR
-8	11000b	-1.333 · FSIVR
-9	11001b	-1.500 · FSIVR
-10	11010b	-1.667 · FSIVR
-11	11011b	-1.833 · FSIVR
-12	11100b	-2.000 · FSIVR
-13	11101b	-2.167 · FSIVR
-14	11110b	-2.333 · FSIVR
-15	11111b	-2.500 · FSIVR

1) Given polarities are valid with SENSIF.POL=0b. When SENSIF.POL=1b, inputs are cross-connected and the polarities of the input-referred offset compensation voltages have to be inverted.

5.1.6 ΔΣ Modulator for Sensor Signal Chain (SENS-ADC)

After the coarse sensor offset compensation and amplification the sensor signal is fed to a single bit, 2nd order ΔΣ ADC with fully differential input. Its digital filter (see ch. 5.3) is programmable in order to adapt the resolution and the sampling interval to the application requirements.

The ΔΣ modulator reference is configurable to be either a fix internal reference or to track the bridge voltage V_{EXHI} - V_{EXLO} (register SENSIF.SREF).

To ensure ratiometric operation of the signal acquisition chain the ΔΣ modulator reference has to track V_{EXHI} - V_{EXLO}. Nevertheless the non-ratiometric configuration is provided, too, for a maximum of flexibility (e.g. for constant-current excitation mode to use inherent pre-compensation).

The ΔΣ ADC output provides 16 bit words including the sign.

5.1.7 Temperature Channel

General

The temperature acquisition runs independently from the sensor signal acquisition. Therefore the sensor signal is sampled periodically without interruptions necessary for temperature measurement.

Besides an internal temperature measurement the analog input terminals TSEN1 and TSEN2 provide different possibilities to connect external temperature sensors to the device.

The configuration register TEMPIF.TMODE controls the type of temperature sensor to be used.

External temperature sensors can be connected to either TSEN1 or TSEN2. This is configured in the configuration register TEMPIF.TSEN1 and TEMPIF.TSEN2.

For all types of temperature sensors, the voltage signal is finally fed to the TEMP-ADC for conversion to a digital value. The TEMP-ADC reference voltage is selected automatically to be either a fixed internal reference or to track the bridge voltage V_{EXHI} - V_{EXLO}, depending to the type of temperature sensor selected. To achieve sufficient resolution for the different kinds of temperature sensors without the need for a complicated programmable gain and offset compensation circuitry, a high resolution ADC is used.

Pin Assignment

By configuration (refer to TEMPIF.TSEN1, TEMPIF.TSEN2) each of the pins TSEN1 and TSEN2 can be individually assigned to serve either as

- temperature measurement input or
- sensor substrate/shield connection (pulled to V_{EXHI} / V_{EXLO} by current source)

Note: Only one of the two inputs (either TSEN1 or TSEN2) may configured to serve as temperature channel input.

Table 6: Configuration of TSEN1 / TSEN2

TSEN1 / TSEN2	*Connection to Temperature-ADC*	*PU- / PD-current*
00b	No	None (High-Z)
01b	No	PD-current to EXLO
10b	No	PU-current to EXHI 1)
11b	Yes	Depending on TMODE

1) With constant current sensor excitation (CC mode), this pull-up current reduces the current flowing into the sensor bridge.

On-chip temperature measurement

- **TEMPIF.TMODE = 00b**
  In this mode the forward voltage of three series-connected and current biased internal junction-diodes is used to measure the temperature. In this mode an internal voltage is used as reference for the temperature ADC.
  TSEN1/TSEN2 can both be used either as sensor substrate or shield connections.

Temperature measurement by evaluation of the sensor bridge resistance

- **TEMPIF.TMODE = 01b**
  In this mode the temperature dependent voltage across the sensor bridge (V_{EXHI}) is used to measure the temperature.
  In order to avoid saturation in the temperature ADC, V_{EXHI} is measured against a fixed internal voltage V_{CM} of about 1.6V (V_{CM} - V_{EXHI} is used as input to the temperature ADC).
  This mode requires the sensor excitation to be configured for CC-mode.
  In this mode an internal voltage is used as reference for the temperature ADC.
  In this mode the EXHI-signal is connected internally to the temperature ADC, i.e. TSEN1 / TSEN2 can both be used either as sensor substrate or shield connections.

Temperature measurement using an external diode

- **TEMPIF.TMODE = 10b**
  In this mode the forward voltage drop $V_{EXHI} – V_{TSEN1/2}$ across an external diode connected at the anode to the positive sensor supply V_{EXHI} and the cathode to either TSEN1 or TSEN2 is used as input to the temperature ADC. A bias current is flowing into the selected TSEN1/2 pin to bias the diode. Note that with constant current sensor excitation (CC Mode), this bias current reduces the current flowing into the sensor bridge.
  In this mode an internal voltage is used as reference for the temperature ADC.
  One of the inputs TSEN1 or TSEN2 must be connected to the external diode and configured as temperature signal input TEMPIF.TSEN1/2 = 11b - the unused pin TSEN1 or TSEN2 can both be used either as sensor substrate or shield connections.

Temperature measurement using an external thermistor

- **TEMPIF.TMODE = 11b**
  In this mode a half bridge consisting of a fixed resistor (EXHI-side) and a thermistor (EXLO-side) form a temperature dependent resistive divider. The temperature dependent voltage at the connection is fed to the temperature ADC.
  In order to avoid saturation in the TEMP-ADC, TSEN1/2 is measured against a fixed internal voltage V_{CM} of about 1.6V ($V_{CM} – V_{TSEN1/2}$ is used as input to the temperature ADC).
  In this mode the bridge excitation voltage (V_{EXHI} - V_{EXLO}) is used as reference for the TEMP-ADC.
  One of the inputs TSEN1 or TSEN2 must be connected to the external resistor and configured as temperature signal input TEMPIF.TSEN1/2 = 11b - the unused pin TSEN1 or TSEN2 can both be used either as sensor substrate or shield connections.

Table 7: Temperature measurement modes

TMODE	*positive TEMP-ADC input*	*negative TEMP-ADC input*	*V_{REF} for TEMP-ADC*	*PU/PD-current at selected TSEN1 or TSEN2*	*typical full scale range tFSR (single-ended)* 1)
00b	internal Diodes	VCM	internal	not applicable	V_{Diodes} from V_{VSSA} to V_{VDDA}
01b	VCM	EXHI	internal	not applicable	V_{EXHI} from V_{VSSA} to V_{VDDA}
10b	EXHI	TSEN1/2	internal	PD-current	$V_{TSEN1/2}$ from V_{EXHI} - $V_{VDDA}/2$ to V_{EXHI} + $V_{VDDA}/2$
11b	VCM	TSEN1/2	V_{EXHI} - V_{EXLO}	High-Z	V_{TSENx} from $V_{CM} – V_{EXHI}$ /2 to V_{CM} + V_{EXHI} /2

1) Input voltages must be within the range $V_{VSSA} < V_{IN} < V_{VDDA}$

5.1.8 SENT Physical Interface

The SENT physical interface provides a slope controlled push-pull output driver, which complies to the requirements of the SAE J2716 standard (see ch. 7).

For protection the driver is current limited. Exceeding this limit will cause the ERRC.CLIM error bit to be set, see chapter 5.5.10. This will in turn cause the driver to be turned off, see chapter 5.4.4.4.

Required external circuitry is given in the following picture. Values for the external components are given in chapter Recommended Operating Conditions (pg. 6).

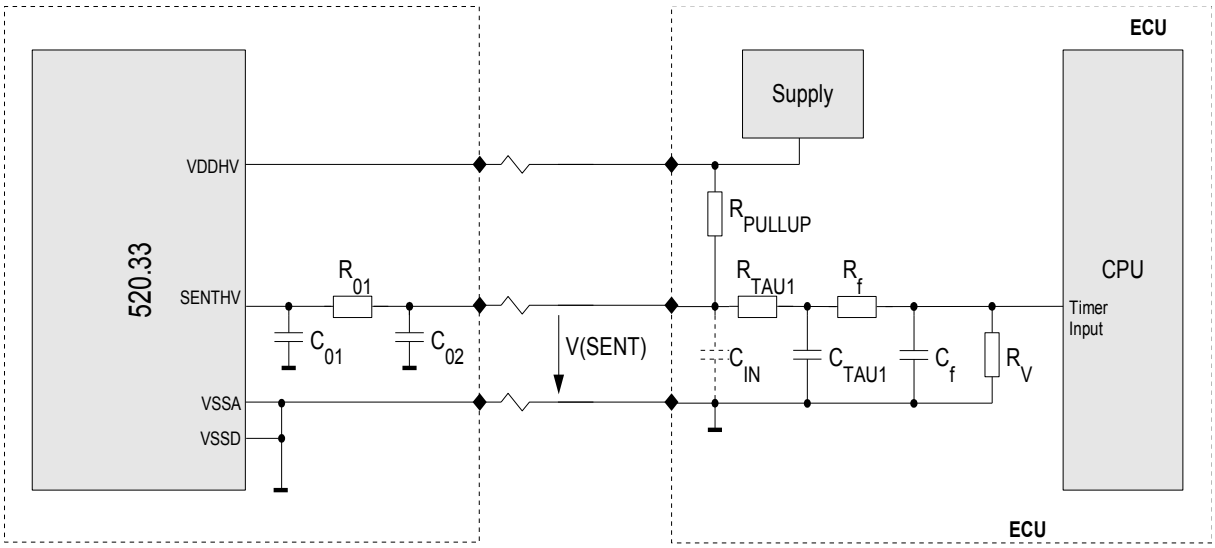


Fig. 7: External circuitry for SENT transmitter and receiver

5.2 Digital Part

The digital part supports the entire device control including:

- The management of all interfaces (SIO, SPI & SENT)
- Calibration process support (programming interface)
- The calculation of the sensor characteristics compensation
- Various diagnostic functions

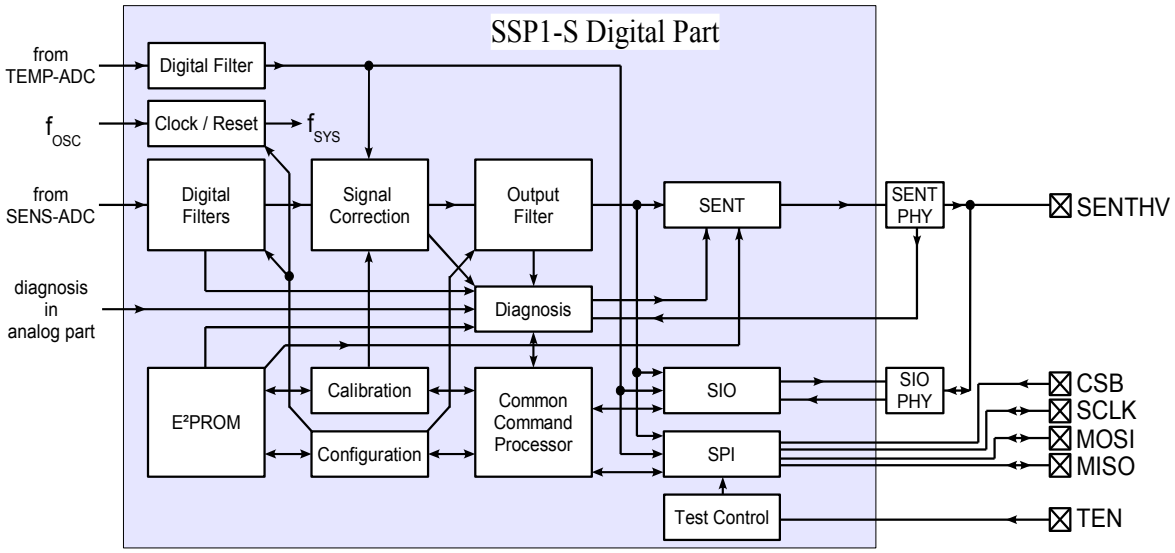


Fig. 8: Functional block diagram of the digital part

5.2.1 Serial Input/Output (SIO)

The Serial Input/Output interface is provided in order to ease calibration and configuration. To achieve true 1-wire operation the SIO is connected to the SENTHV pin.

It provides access to the internal command processor for configuration and calibration purposes and to measurement results (raw data as well as processed data). The SIO data transmission uses the Manchester Code (Bi-Phase-L, falling edge is a logical 1) with a typical baud rate of 14.400 bit/s.

Basically the SIO supports all commands processed by the Common Command Processor (CCP), refer to chapter "Common Command Processor" (see ch. 5.4.5).

5.2.1.1 SIO Byte Format

Data is transferred byte wise. Each byte is preceded by a start bit which is always one. The SIO uses the Manchester code for data transfer. Each Manchester coded bit includes either a falling ('1') or a rising edge ('0') in the middle of a 69.4 µs bit interval.

The timing tolerance for bit time and the middle of the bit is ±6%.

To ensure proper decoding of the received data the bus level should be low since reception of the preceding bit or should be low at least two bit times.

After the start bit the MSB is transferred first.

The first rising edge indicates the start of the byte transmission. Note that if the LSB is a '0', the bus line must be driven back to 0V again.

5.2.2 Serial Peripheral Interface (SPI)

The SPI (Serial Peripheral Interface) compatible interface provides access to the internal command processor for configuration and calibration purposes and to measurement results (raw data as well as processed data).

For the command format reference refer to the Common Command Processor description (see 5.4.5).

5.2.2.1 SPI Byte Format

The follwing diagram illustrates the SPI byte format (Fig. 9). Data is updated on the MISO or MOSI lines at the falling clock edge and latched with the rising clock edge, with MSB first. The minimum time between two SPI frames is limited (refer to $t_{W(CSBH)}$, ch. 4.2, section “Serial Peripheral Interface”). The MISO line is at high impedance when CSB is inactive (high).

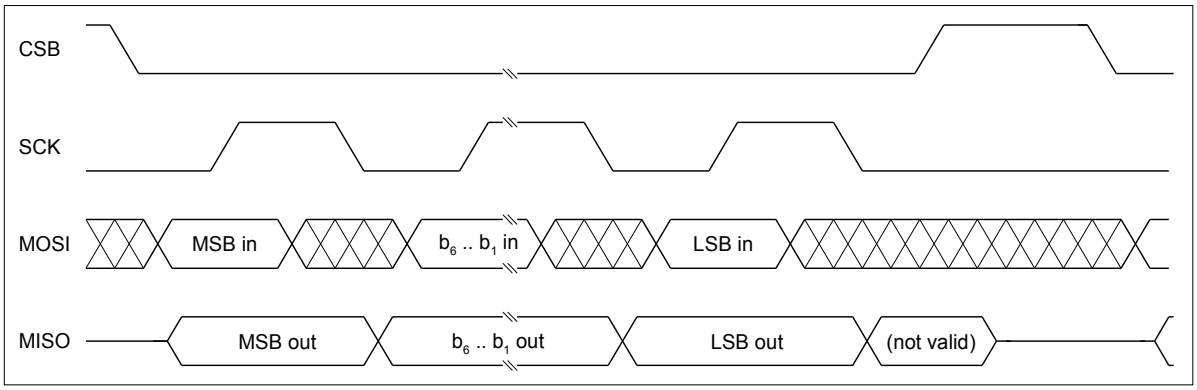


Fig. 9: SPI Byte format

5.2.3 Clock and Reset Control

The clock and reset control unit is responsible for delaying the power-on reset by time t_{RESET} (refer to ch. 4.2, section “Digital timing parameters”).

To reduce the digital power consumption this block provides also the possibility to configure the system clock between four choices (see also chapter 5.3). With the register DIGCONF.FSYS_OM the system clock frequency can be configured (Table 8).

Table 8: System Clock Configuration

FSYS_OM[1:0]	*system clock f_{SYS} [MHz]*
00	8
01	4
10	2
11	1

5.2.4 Configuration Memory

A dedicated part of the RAM is called the configuration RAM. It controls the behaviour of the SSP, see the following Table 9.

There is also EEPROM memory with the same size. The RAM will be initialized with the EEPROM contents after a reset. Afterwords, it is possible to overwrite the RAM contents in configuration mode (not in ***operational mode***). The effect of having done this can be measured immediately. The changes can be made permanent by programming the RAM contents into the EEPROM.

Within the following CCP modes (see 5.4.5.1), the EEPROM contents will be regularly copied into the configuration RAM:

- SENT only mode (***operational mode***)
- SENT mode (***operational mode***)
- CCP mode (***operational mode***)

The copying does not happen in the CCP window mode.

When switching from ***configuration mode*** to ***operational mode*** , the addresses 0x98 (MTYPE) to 0xAA (SID4) are overwritten by data that is stored in the EEPROM.

Two independent measures prevent inadvertent or unwanted programming of the EEPROM are implemented:

1. To avoid inadvertent / malice write access:
   The write access to the EEPROM is restricted to the CCP window mode (see 5.4.5.1) which is intended for end of line configuration and calibration purposes. All other CCP modes do not allow to enter ***configuration mode*** and therefore EEPROM write commands to the EEPROM are not executed. Once another mode than the CCP window mode has been selected with finishing the configuration/calibration (see SCOM.MOD and section 5.4.5.1), there's no more write access to the EEPROM neither via SPI nor via SIO. The EEPROM is locked.
2. To avoid accidental write access (e.g. provoked by transient disturbances):
   A sophisticated lock mechanism secures any write access execution. It consists of a lock counter which is incremented during the individual steps of the write access to the EEPROM, i.e. the data to write have to be stored on the EEPROM input register at a specific lock counter value, and the final control signal to program the addressed EEPROM cell can only be set at another particular lock counter value. The lock counter itself is secured with 4 parity bits. Any attempt to execute a write access to EEPROM at a wrong lock counter state or with a lock counter parity error is suppressed and provokes a reset. This lock mechanism is a part of the logic consistency monitor (see 5.5.10).

Table 9: Configuration memory mapping

Address	*Name*	*Description*
0xB0	CRC16	*default : 0x0000* **Bit [15:0]** = 16 bit EEPROM CRC signature
0xAE	TX	*default : 0x0000* **Bit [15:8]** = Slow Channel Temperature Characteristic TX1[7:0] (ID 0x12) **Bit [7:0]** = Slow Channel Temperature Characteristic TX2[7:0] (ID 0x13)
0xAC	TY	*default : 0x0000* **Bit [15:8]** = Slow Channel Temperature Characteristic TY1[7:0] (ID 0x14) **Bit [7:0]** = Slow Channel Temperature Characteristic TY2[7:0] (ID 0x15)
0xAA	SID4	*default : 0x0000* **Bit [15:12]** = free, r/w only by SPI or SIO **Bit [11:0]** = Sensor ID#4 (ID 0x2C)
0xA8	SID3	*default : 0x0000* **Bit [15:12]** = free, r/w only by SPI or SIO **Bit [11:0]** = Sensor ID#3 (ID 0x2B)
0xA6	SID2	*default : 0x0000* **Bit [15:12]** = free, r/w only by SPI or SIO **Bit [11:0]** = Sensor ID#2 (ID 0x2A)

Address	*Name*	*Description*
0xA4	SID1	*default : 0x0000* **Bit [15:12]** = free, r/w only by SPI or SIO **Bit [11:0]** = Sensor ID#1 (ID 0x29)
0xA2	PY2	*default : 0x0000* **Bit [15:12]** = Slow Channel Temperature Characteristic TY2[11:8] (ID 0x15) **Bit [11:0]** = SENT 12-bit Pressure Index Y2 (ID 0x0A)
0xA0	PY1	*default : 0x0000* **Bit [15:12]** = Slow Channel Temperature Characteristic TY1[11:8] (ID 0x14) **Bit [11:0]** = SENT 12-bit Pressure Index Y1 (ID 0x09)
0x9E	PX2	*default : 0x0000* **Bit [15:12]** = Slow Channel Temperature Characteristic TX2[11:8] (ID 0x13) **Bit [11:0]** = Physical Value Pressure Index X2 (ID 0x08)
0x9C	PX1	*default : 0x0000* **Bit [15:12]** = Slow Channel Temperature Characteristic TX1[11:8] (ID 0x12) **Bit [11:0]** = Physical Value Pressure Index X1 (ID 0x07)
0x9A	MCODE	*default : 0x0000* **Bit [15:12]** = free, r/w only by SPI or SIO **Bit [11:0]** = Manufactor Code (ID 0x05)
0x98	MTYPE	*default : 0x0000* **Bit [15:12]** = free, r/w only by SPI or SIO **Bit [11:0]** = Manufactor Type (ID 0x04
0x96	DIGCOEF	*default : 0x0000* ***Digital coefficients for temperature pre-processing :*** (refer to ch. 5.4.1) **Bit [1:0]** = DIGCOEF.TGAIN : temperature data gain (left shift) **Bit [7:2]** = DIGCOEF.TOFF : signed temperature data offset ***Digital coefficient for output low pass :*** (refer to chapter 5.4.2) **Bit [14:8]** = DIGCOEF.ALP : Low pass coefficient **Bit [15]** = DIGCOEF.DISLP : Filter disable 0b = enabled 1b = disabled
0x94	C0	*default : 0x0000* 16 bit coefficient c0 : sensor offset
0x92	C1	*default : 0x0000* 16 bit coefficient c1 : sensor gain
0x90	C2	*default : 0x0000* 16 bit coefficient c2 : temperature coefficient of sensor offset (1st order)
0x8E	C3	*default : 0x0000* 16 bit coefficient c3 : temperature coefficient of sensor offset (2nd order)
0x8C	C4	*default : 0x0000* 16 bit coefficient c4 : temperature coefficient of sensor offset (3rd order)
0x8A	C5	*default : 0x0000* 16 bit coefficient c5 : temperature coefficient of sensor gain (1st order)

Address	*Name*	*Description*
0x88	C6	*default : 0x0000* 16 bit coefficient c6 : temperature coefficient of sensor gain (2nd order)
0x86	C7	*default : 0x0000* 16 bit coefficient c7 : temperature coefficient of sensor gain (3rd order)
0x84	C8	*default : 0x0000* 16 bit coefficient c8 : 2nd order non-linearity coefficient
0x82	C9	*default : 0x0000* 16 bit coefficient c9 : 3rd order non-linearity coefficient
0x80	C10	*default : 0x0000* 16 bit coefficient c10 : temperature coefficient of 2nd order non-linearity
0x7E	DIGCONF	*default : 0x0000* ***Digital configuration :*** **Bit [1:0]** = DIGCONF.FSYS_OM : select system clock, see chapter 5.2.3 **Bit [3:2]** = DIGCONF.FILT_OM : select filter configuration, see chapter 5.3 **Bit [7:4]** = reserved **Bit [8]** = DIGCONF.RFSH_EN: EEPROM refresh enable, see chapter 5.4.7 0b: EEPROM refresh is disabled 1b: EEPROM refresh is enabled ***Digital coefficient for sensor pre-processing:*** (see chapter 5.4.1) **Bit [10:9]** = DIGCONF.SGAIN : sensor data gain (shift right) **Bit [15:11]** = reserved
0x7C	SENSIF	*default : 0x0000* ***Sensor interface configuration:*** (see chapters 5.1.4 and 5.1.5) **Bit [3:0]** = SENSIF.CCUR : constant current select in CC mode **Bit [7:4]** = SENSIF.GPGA : PGA gain setting **Bit [11:8]** = SENSIF.OPGA : absolute offset setting of PGA **Bit [12]** = SENSIF.OPOL : PGA offset polarity 0b = positive 1b = negative **Bit [13]** = SENSIF.EXMODE : sensor excitation mode 0b = Constant Voltage (CV) excitation 1b = Constant Current (CC) excitation **Bit [14]** = SENSIF.POL : sensor input polarity 0b = Normal 1b = Reverse **Bit [15]** = SENSIF.SREF: sensor ADC reference connection 0b = internal 1b = external (V_{EXHI} - V_{EXLO})

Address	*Name*	*Description*
0x7A	TEMPIF	*default : 0x0000* ***Temperature channel configuration:*** (see chapter 5.1.7) **Bit [1:0]** = TEMPIF.TSEN1 : TSEN1 pin assignment 00b = Off (TSEN1 floating) 01b = Pull down to EXLO 10b = Pull up to EXHI 11b = On (TSEN1 can be connected to TEMP_ADC) **Bit [3:2]** = TEMPIF.TSEN2 : TSEN2 pin assignment 00b = Off (TSEN2 floating) 01b = Pull down to EXLO 10b = Pull up to EXHI 11b = On (TSEN2 can be connected to TEMP_ADC) **Bit [5:4]** = TEMPIF.TMODE : temperature measurement mode 00b = On-chip temperature measurement with 3 diodes 01b = Sensor bridge resistance evaluation (only in CC mode) 10b = External diode forward voltage measurement, ADC inputs between TSEN1/2 and EXHI 11b = External thermistor, ADC inputs between TSEN1/2 and VCM **Bit [6]** = TEMPIF.ENTSENT : Enable temperature transmission on SENT interface 0b : Temperature transmission disabled ; Sensor Type **P/S** 1b : Temperature transmission enabled ; Sensor Type **P/S/t** **Bit [15:7]** = reserved

Address	*Name*	*Description*
0x78	OUTCONF	*default : 0x0000* ***Additional configurations :*** **Bit [3:0]** = OUTCONF.TCKSEL: SENT clock tick (T_{TICK}) selection 0000b = 12 µs 0001b = 3 µs 0010b = 4 µs 0011b = 5 µs 0100b = 6 µs 0101b = 8 µs 0110b = 10 µs 0111b = 12 µs 1000b = 16 µs 1001b = 24 µs 1010b = 32 µs 1011b = 40 µs 1100b = 48 µs 1101b = 64 µs 1110b = 80 µs 1111b = 90 µs Tick time is independent of system clock configuration DIGCONF.FSYS_OM (see chapter 5.4.4) **Bit [4]** = OUTCONF.SPU: Sensor pull-up (selects sensor diagnosis output) (see chapter 5.5) **Bit [5]** = OUTCONF.NPP: no SENT Pause Pulse 0b : pause pulse 1b : no pause pulse (see chapter 5.4.4) **Bit [6]** = OUTCONF.EN_LOWPOW: enable analog low power mode 0b : disabled 1b : enabled **Bit [7]** = OUTCONF.SELDRV_PADS: select pad driving capability (pads: MISO, TP & TN) 0b : low drive 1b : high drive **Bit [15:8]** = reserved
0x76	SCOM	*default : 0x0000* ***Communication configurations :*** **Bit [2:0]** = SCOM.MOD:CCP mode selection, see chapter 5.4.5.1 000b: CCP window mode (default, factory/end of line use) 001b: reserved 010b: reserved 011b: reserved 100b: SENT only mode (operational mode) 101b: SENT mode (operational mode) 110b: CCP mode (operational mode) 111b: reserved **Bit [3]** = SCOM.RD_ONCE: Read signal data once 0b: each pressure sample can be read out multiple using the GETSIG command 1b: each pressure sample can only be read out once. Following requests will not be acknowledged (NACK) until a new pressure sample is available. This is only valid for SPI or SIO read out. **Bit [15:4]** = reserved

Address	*Name*	*Description*
0x74	ENERR	*default : 0x0000* ***Error Enable Register:*** see chapter 5.5.10
0x66	BISTSTAT	*Not stored on EEPROM !* ***BIST Status Register:*** see chapter 5.5.10 Register is read/writeable.
0x64	ERRC	*Not stored on EEPROM !* ***Error Code Register:*** see chapter 5.5.10 Register is read/writeable.
0x62	MASKERRC	*Not stored on EEPROM !* ***Masked Error Code:*** see chapter 5.5.10 Register is read only !

5.3 Sensor Signal Path

The following picture shows a block diagram of the SSP's entire sensor signal path.

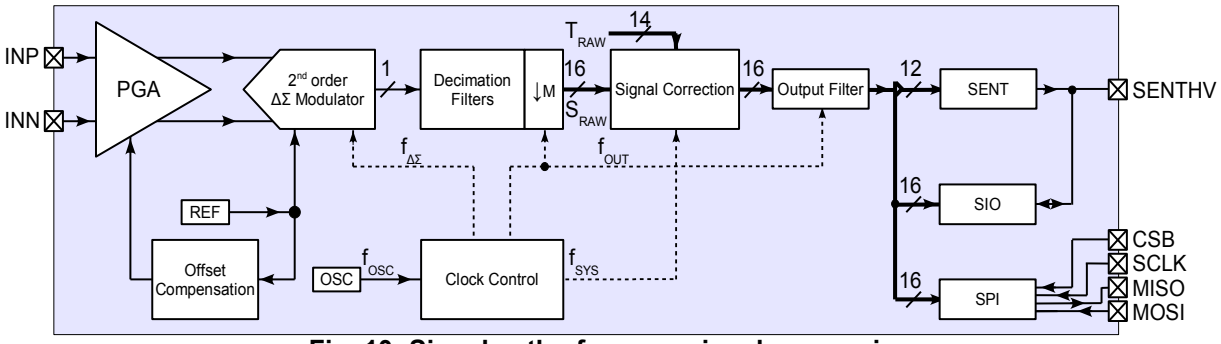


Fig. 10: Signal path of sensor signal processing

The following Table 10 summarizes all important parameters of the signal path for all possible configurations.

Table 10: Signal path parameters

No.	*FSYS_OM*	*f_{SYS} [MHz]*	*FILT_OM*	*f_{OUT} [kHz]*	*max. accuracy 1) [ENOB]*	*t_{STEP} 2) [µs]*
1	0x00b	8	0x00b	3.91	15.5	< 696
2	0x00b	8	0x01b	3.91	14.5	< 618
3	0x00b	8	0x10b	3.91	13.0	< 583
4	0x00b	8	0x11b	3.91	11.0	< 447
5	0x01b	4	0x00b	1.95	15.5	< 1382
6	0x01b	4	0x01b	3.91	14.5	< 928
7	0x01b	4	0x10b	3.91	13.5	< 750
8	0x01b	4	0x11b	3.91	11.5	< 672
9	0x10b	2	0x00b	0.98	15.5	< 2754
10	0x10b	2	0x01b	1.95	14.5	< 1846
11	0x10b	2	0x10b	1.95	13.5	< 1620
12	0x10b	2	0x11b	1.95	11.5	< 1460
13	0x11b	1	0x00b	0.49	15.5	< 5498
14	0x11b	1	0x01b	0.98	14.5	< 3682
15	0x11b	1	0x10b	0.98	13.5	< 3220
16	0x11b	1	0x11b	0.98	11.5	< 2910

1) Maximum possible accuracy of analog-to-digital conversion (without correction).

2) Step response from INP/INN to SENT or SPI registers with disabled output filter. Additional time constant from output filter ($\tau_{OUTFILT}$) can be found in chapter 5.4.2.

The first parameter is the system clock f_{SYS}. The system clock can be switched in four steps between 1 to 8 MHz, which leads to four different digital power modes. $I_{CONS,DIG}$ is an estimation of the typical current consumption of the digital part.

For each power mode there are four different filter settings available. The settings differ in output rate (f_{OUT}), accuracy and step response (t_{STEP}). The settings are chosen to cover a sufficient range of the system-related compromise between accuracy and speed, i.e. to get higher accuracy with a slower step response and to get a faster step response with lower accuracy.

The system clock frequency can be selected with DIGCONF.FSYS_OM, see ch. 5.2.3. An independent filter setting can be selected with DIGCONF.FILT_OM.

5.4 Signal Processing and Mode Control

5.4.1 Sensor Signal Correction

The sensor and the temperature signal are first processed by digital filters as a part of the ΔΣ-ADCs to gain digitized raw data with an accuracy up to 16 bit for sensor (S_{RAW}) and 14 bit for temperature raw data (T_{RAW}), see Fig. 10.

The raw data can be read via SIO / SPI by the CCP command GETSIG (refer to Table 24, pg. 49) as 16-bit unsigned values (SRAW[15:0] & TRAW[15:0]).

A dedicated arithmetic unit processes the incoming raw data of the sensor S_{RAW} and the temperature T_{RAW} to compensate for temperature dependence for the sensor's offset, sensitivity and nonlinearities up to 3rd order.

The following table summarizes the calibration coefficients required for the sensor calibration. The coefficients c0 ... c10 are computed externally during calibration, and consecutively have to be stored in the embedded EEPROM calibration data area (see Table 9, ch. 5.2.4).

Table 11: Definition of coefficients of the sensor data correction algorithm

Symbol	*Description*
c_0	sensor offset
c_1	sensor gain
c_2	temperature coefficient of sensor offset 1st order
c_3	temperature coefficient of sensor offset 2nd order
c_4	temperature coefficient of sensor offset 3rd order
c_5	temperature coefficient of sensor gain 1st order
c_6	temperature coefficient of sensor gain 2nd order
c_7	temperature coefficient of sensor gain 3rd order
c_8	2nd order non-linearity coefficient
c_9	3rd order non-linearity coefficient
c_{10}	temperature coefficient of 2nd order non-linearity

5.4.2 Digital Output Averaging Filter

The update rate of the corrected sensor output P_{CORR} is f_{OUT} (see Table 10). To adjust P_{CORR} to a possibly lower transfer rate of the digital interfaces, i.e. to avoid aliasing effects, a configurable output filter is implemented.

This filter is described by the following difference equation:

$$P_{\mathrm{DIGOUT}}(n+1) = P_{\mathrm{DIGOUT}}(n) + a_{\mathrm{LP}} \cdot \left(P_{\mathrm{CORR}}(n) - P_{\mathrm{DIGOUT}}(n) \right)$$

This filter is a 1st order recursive low pass with the transfer function:

$$H(z) = \frac{a_{\mathrm{LP}} z^{-1}}{1 - (1 - a_{\mathrm{LP}}) z^{-1}}$$

The filter can be configured with DIGCOEF.ALP and DIGCOEF.DISLP. DIGCOEF.DISLP = 1 disables the filter. DIGLP.ALP[6:0] is the coefficient a_{LP}, a 7-bit unsigned fractional value, so it is always positive and in the range from 2^{-7} to $1 - 2^{-7}$ (1/128 ... 127/128). If DIGLP.ALP is zero the filter is also disabled. Disabled in this case means, the digital output is left unfiltered.

The decimal value of a_{LP} can be calculated as:

$$a_{\mathrm{LP,dec}} = \sum_{i=0}^{6} \mathrm{ALP}[i] \cdot 2^{i-7}$$.

The time constant of the output filter can be approximated by:

$$\tau_{\mathrm{OUTFILT}} = \frac{1}{\arccos\left(\frac{4c-c^2-1}{2c}\right) \cdot f_{\mathrm{OUT}}}$$, where: $c = 1 - a_{\mathrm{LP}}$ and f_{OUT} the sampling frequency.

Finally the time to settle to $n \cdot \tau_{\mathrm{OUTFILT}}$ is:

$$T_{\mathrm{settle},n\tau} = n \cdot \tau_{\mathrm{OUTFILT}} - \frac{1}{f_{\mathrm{OUT}}}$$

Note: If the digital averaging low pass is used, the original step response (ref. to Table 10) is enlarged!

5.4.3 Modes of Operation

The SSP has three modes of operation:

- **Operational mode**

Within this mode continuously pressure measurement takes place. Access to the application memory is restricted to read access depending in SCOM.MOD (refer to 5.4.5.1). Furthermore various self-tests are running continuously in this mode.

- **Configuration mode**

This mode can only be entered in **CCP window mode** (SCOM.MOD = 000b), so the entrance to configuration mode is restricted by a time window after power-on (see Electrical Characteristics, section “Digital Timing Parameters”).

In this mode all CCP commands are executable. This includes configuration and calibration of the device by writing the RAM and EEPROM memories.

Pressure is not measured continuously within this mode. If a corrected pressure value is requested by GETSIG (see Table 24, pg. 49), the recent raw data S_{RAW} is first corrected and then sent out.

- **Diagnostic mode**

This mode can only be entered in **SENT mode** (SCOM.MOD = 101b). The entrance to diagnostic mode is restricted by a time window after power-on, see (see Electrical Characteristics, section “Digital Timing Parameters”).

In this mode all CCP read commands are executable, but write access to the RAM and EEPROM memories by WRITE or EEUPD is suppressed (refer to chapter 5.4.5.3); the EEPROM is locked.

Pressure is not measured continuously within this mode. If a corrected pressure value is requested by GETSIG (refer to Table 24, pg. 49), the recent raw data S_{RAW} is first corrected and then sent out.

5.4.4 SENT Protocol Description

The SSP provides a SENT signal output. This protocol is specified by the SAE J2716 standard (ch. 7) and described below.

SENT (**S**ingle **E**dge **N**ibble **T**ransmission) is a one wire protocol that encodes data nibbles (four bits) by one pulse per nibble. The pulse length is measured between two falling edges and reflects the nibble value. The minimum nibble pulse length is 12 clock ticks (representing the nibble value 0x0) and the maximum nibble pulse length is 27 clock ticks (12 + 15 ticks, representing 0xF).

The communication is unidirectional: the SSP slave sends pressure signal values autonomously whereas the master acts as a receiver only.

5.4.4.1 SENT Message Format

Each so called SENT *message* consists of ten (OUTCONF.NPP = 1b : nine) negative pulses on the transmission line. The following picture illustrates one sent message without the optional pause pulse.

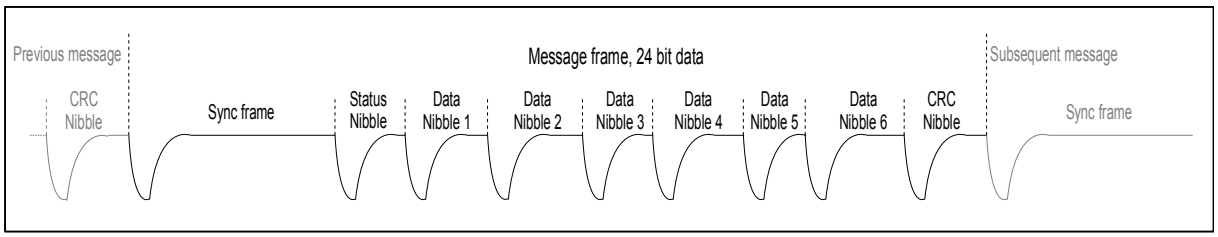


Fig. 11: SENT message without pause pulse (OUTCONF.NPP = 1b)

The “atomic unit” of time measurement in the context of the SENT protocol is called a *clock tick* (T_{TICK}). By default this time is 12 µs long, but other values can be configured with OUTCONF.TCKSEL. The selected tick time is independent of the system clock setting DIGCONF.FSYS_OM.

The message starts with the *sync frame* which is always 56 clock ticks long. This pulse is used by the receiver to detect the start of that message and to measure the transmitters clock tick time. Next is the *status nibble*, followed by six data nibbles and a check sum nibble (CRC). Since the pulse times depend on the transmitted values (except for the sync frame) the length of such a message is not fixed. With the OUTCONF.NPP configuration bit being cleared (see 5.2.4) a *pause pulse* can be added after the CRC nibble. The length of that pulse is always adapted to the previously sent data such that a constant message length of 282 clock ticks is guaranteed, see the following picture.

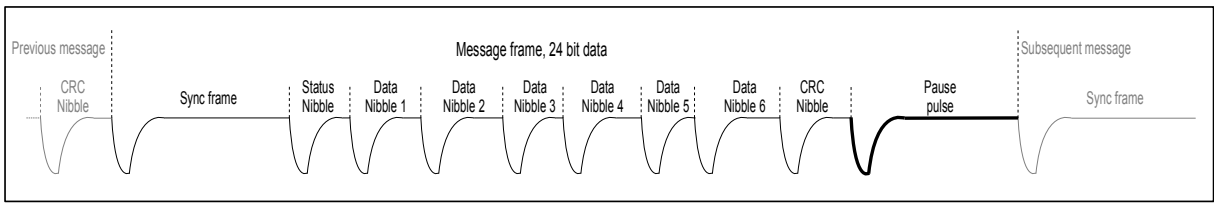


Fig. 12: SENT message with pause pulse (OUTCONF.NPP = 0b)

5.4.4.1.1 Status Nibble

The status nibble bits contain the following data:

- Bit 0 is set if and only if an error is present. In this case the transmitted pressure value is either 0 (initialization error, during device initialization) or 4090 (diagnostic error, otherwise), see below.
- Bit 1 is 0.
- Bit 2 and 3 contain information for serial data transmission, see below (5.4.4.2).

5.4.4.1.2 Data Nibbles

Pressure values are always transmitted within 3 nibbles, resulting in 12 bits.

SENT standardizes several application specific protocols of which the SSP provides the protocol called "P/S" (secure pressure sensor).

The 6 data nibbles contain the following information:

- Data nibbles 1 to 3 contain pressure information. The pressure value is sent as a 12-bit unsigned integer number, the most significant nibble first.
- Data nibble 4 and 5 contain an 8-bit rolling counter, most significant nibble first. This modulo-256 counter is incremented with every message.
- Data nibble 6 is the inverted data nibble 1.

Additional data is provided via *enhanced serial messages*, see below (5.4.4.2).

Some values of data nibbles 1 to 3 (pressure data) are reserved for special purposes, see the following table.

Table 12: Error codes in data nibbles

signal interpretation	*signal value*
unused error codes	4091 … 4095
diagnostic error	4090
unused error code	4089
high clamp	4088
pressure data	2 … 4087
low clamp	1
initialization	0

Details about the diagnostic error are provided within the enhanced serial message with ID 0x01, see below.

The initialization code is sent during device initialization.

5.4.4.1.3 CRC Nibble

The CRC nibble contains check sum data. It's generation is defined in the SAE J2716 standard (ch. 7).

5.4.4.2 Serial Data

The status nibble embeds two bits for so called *serial data transmission*. 18 of these bit pairs that are transmitted in 18 consecutive messages result in one *enhanced serial message*. This is called the *slow channel* whereas data that is transmitted within the data nibbles belongs to the *fast channels*.

The format of enhanced serial messages (with 8-bit ID) is shown in the following picture:

SENT message number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Status nibble bit 3	1	1	1	1	1	1	0	0	ID[7:4]				0	ID[3:0]				0
Status nibble bit 2	CRC6[5:0]						DATA[11:0]											

Fig. 13: Enhanced serial message format

An enhanced serial message carries 8-bit ID information and 12-bit data information (the SSP does not support 4-bit ID messages). Additionally a 6-bit CRC check sum allows for integrity checking (ch. 7). A subset of all possible IDs is sent in a repetitive manner.

The available enhanced serial message IDs are defined in the following table. For most IDs the transmitted value originates from the EEPROM memory, see chapter 5.2.4.

Table 13: Enhanced serial message IDs

ID[7:0]	*DATA[11:0] description according to SENT standard*	*DATA[11:0] origin*
0x01	Diagnostic Error Code	see Table 14
0x03	Sensor Type	TEMPIF.ENTSENT=0b : DATA[11:0] = 0x003 (**P/S**) TEMPIF.ENTSENT=1b : DATA[11:0] = 0x005 (**P/S/t**)
0x04	Manufacturer Type	DATA[11:0] = MTYPE
0x05	Manufacturer Code	DATA[11:0] = MCODE
0x06	SENT standard revision	DATA[11:0] = 0x003 (SAE J2716 Information Report, JAN2010, ch. 7)
0x07	Pressure characteristic X1	DATA[11:0] = PX1[11:0]
0x08	Pressure characteristic X2	DATA[11:0] = PX2[11:0]
0x09	Pressure characteristic Y1	DATA[11:0] = PY1[11:0]
0x0A	Pressure characteristic Y2	DATA[11:0] = PY2[11:0]
0x10	Temperature data (unsigned)	DATA[11:0] = T[11:0] 1)
0x12	Temperature characteristic X1	DATA[11:0] = TX1[11:0] 1)
0x13	Temperature characteristic X2	DATA[11:0] = TX2[11:0] 1)
0x14	Temperature characteristic Y1	DATA[11:0] = TY1[11:0] 1)
0x15	Temperature characteristic Y2	DATA[11:0] = TY2[11:0] 1)
0x29	Sensor ID #1	DATA[11:0] = SID1[11:0]
0x2A	Sensor ID #2	DATA[11:0] = SID2[11:0]
0x2B	Sensor ID #3	DATA[11:0] = SID3[11:0]
0x2C	Sensor ID #4	DATA[11:0] = SID4[11:0]

1) Only for sensor type selection **P/S/t** (TEMPIF.ENTSENT=1b)

The following table lists the diagnostic error codes in descending order of priority (which matters if two different error codes are valid at the same time).

The error code depends on the ERRC and ENERR registers, see chapter 5.5.10. This dependency is given in the "details" column.

Table 14: Diagnostic error codes (DEC)

value	*definition*	*details*
0x000	no error	
0x003	initialization error	1. Power on EEPROM self-test failed : this code is sent, then reset and retest. 2. Any enabled error occurs during initialization, after initialization next DEC identifies error
0xA00	sensor short check failed	SERR3 and ENSERR3
0xA01	sensor connections check failed	(SERR1 and ENSERR1) or (SERR2 and ENSERR2)
0xA02	EEPROM signature error	BISTSTAT.EEBISTERR, also mapped to ERRC.SIGERR
0xA03	error in arithmetic unit	AUERR and ENAUERR
0xFyy	other error 1)	bit 0: SIGERR = CROBISTERR or EEBISTERR bit 1: V3ERR and ENV3ERR bit 2: SAMPSAT and ENSAMPSAT bit 3: SADCSDAT and ENSADCSAT bit 4: TADCSAT and ENTADCSAT bit 5: TNORMSAT and ENTNORMSAT bit 6: CORRSAT and ENCORRSAT 2) bit 7: SENTERR and ENSENTERR

1) All errors with DEC 0xFyy are transmitted parallel, there is no priority

2) The pressure output on SENT is saturated according to SENT standard, this error bit should be disabled (ENERR.ENTNORMSAT = 0b) to prevent fast channel error code 4090. Use only in CCP mode (SCOM.MOD = b110).

- The SSP does not support the SENT standard's "short serial messages".
- The sending of enhanced serial data is looped according to the following two schemes depending on TEMPIF.ENTSENT, i.e. if it is configured as **P/S** sensor or **P/S/t** sensor.

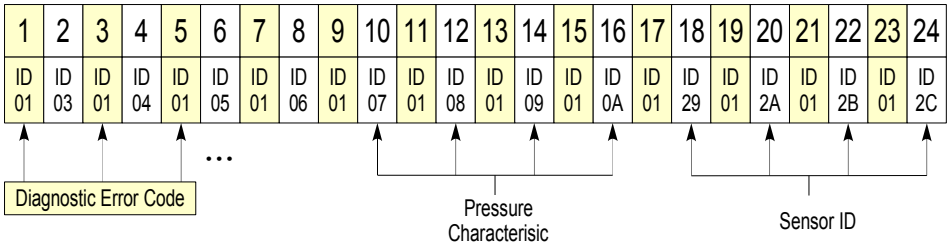


Fig. 14: Slow channel message cycle for TEMPIF.ENTSENT=0b (P/S)

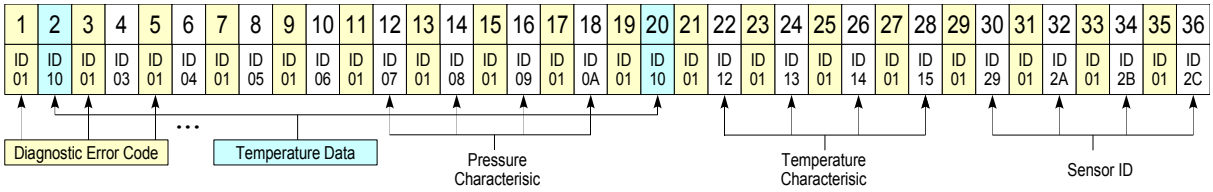


Fig. 15: Slow Channel Message Cycle for TEMPIF.ENTSENT=1b (P/S/t)

5.4.4.3 Temperature Data on Slow Channel

If the SSP is configured as sensor type **P/S/t** with ENTSENT = 1b the normalized temperature *T* is transmitted via SENT slow channel. This temperature has a specific characteristic which is also transmitted via SENT slow channel with the characteristic values *TX1*, *TX2*, *TY1* and *TY2*. With this characteristic values the transmitted temperature *T* can be mapped to the SENT standard temperature characteristic (SAE J2716 standard, see ch. 7).

The equation

$$T_{ABSOLUT}(K) = 200 + \frac{1}{8} \cdot [TX1 + \frac{(TX2 - TX1)}{(TY2 - TY1)} \cdot (T - TY1)]$$

transforms T into an absolute temperature value $T_{ABSOLUT}$ with unit °K, where $T_{ABSOLUT}$ is a 12-bit unsigned fixed-point number with binary point between bit 2 and bit 3 (data range 0.125 to 511 : 200.125 °K to 711 °K).

Note: T has its own saturation characteristic, i.e. $T_{ABSOLUT}$ covers only a sub-interval within the SENT standard temperature range.

5.4.4.4 Error Handling

Depending on the configuration, the SSP will perform several power-on self tests after power-up. During this test no SENT messages will be transmitted.

If one of the power-on self tests Logic BIST, RAM BIST or ROM BIST fails then the SSP reruns the test until it is pass. During this time SENTHV stays high ohmic.

If the power-on self test EEPROM BIST fails then the SSP transmits the fast channel error value 4090 until a complete slow channel diagnostic error code "initialization error" has been transmitted (ID 0x01 with DATA 0x003). Afterwards the SSP resets itself and restarts the initialization procedure, including the power-on EEPROM self-test.

If the tests succeeded the SSP will still be within it's initialization phase until valid pressure values are available. During this phase the SSP will transmit the fast channel initialization signal (code 0). If an enabled error happens during this phase then fast channel error value 4090 is sent, the SENT error flag is set and 0x003 is sent on slow channel's diagnostic code.

When an enabled error occurs while the SSP transmits valid pressure values then the fast channel error value 4090 is transmitted with set error flag (status bit 0) until the error has disappeared. The slow channel diagnostic error code transmits information about the error source and all error flags in ERRC are reset. If no enabled error is present any more the next diagnostic error code will be 0x000.

For short intermediate errors the error flag and the fast channel error value 4090 is sent for at least 3 subsequent fast frames. In this case it can happen that the slow channel diagnostic code to identify the intermediate error is transmitted when the fast channel already sends valid pressure values.

When the SENT output driver detects an error the error bit ERRC.SENTERR is set. If the SENT error indicator is enabled with ENERR.ENSENTERR = 1b the fast error value 4090 is sent with the error bit set and on slow channel the diagnostic error code 0xFyy is sent with bit 7 set.

The following Fig. 16 depicts a flow chart of the diagnostic error code handling.

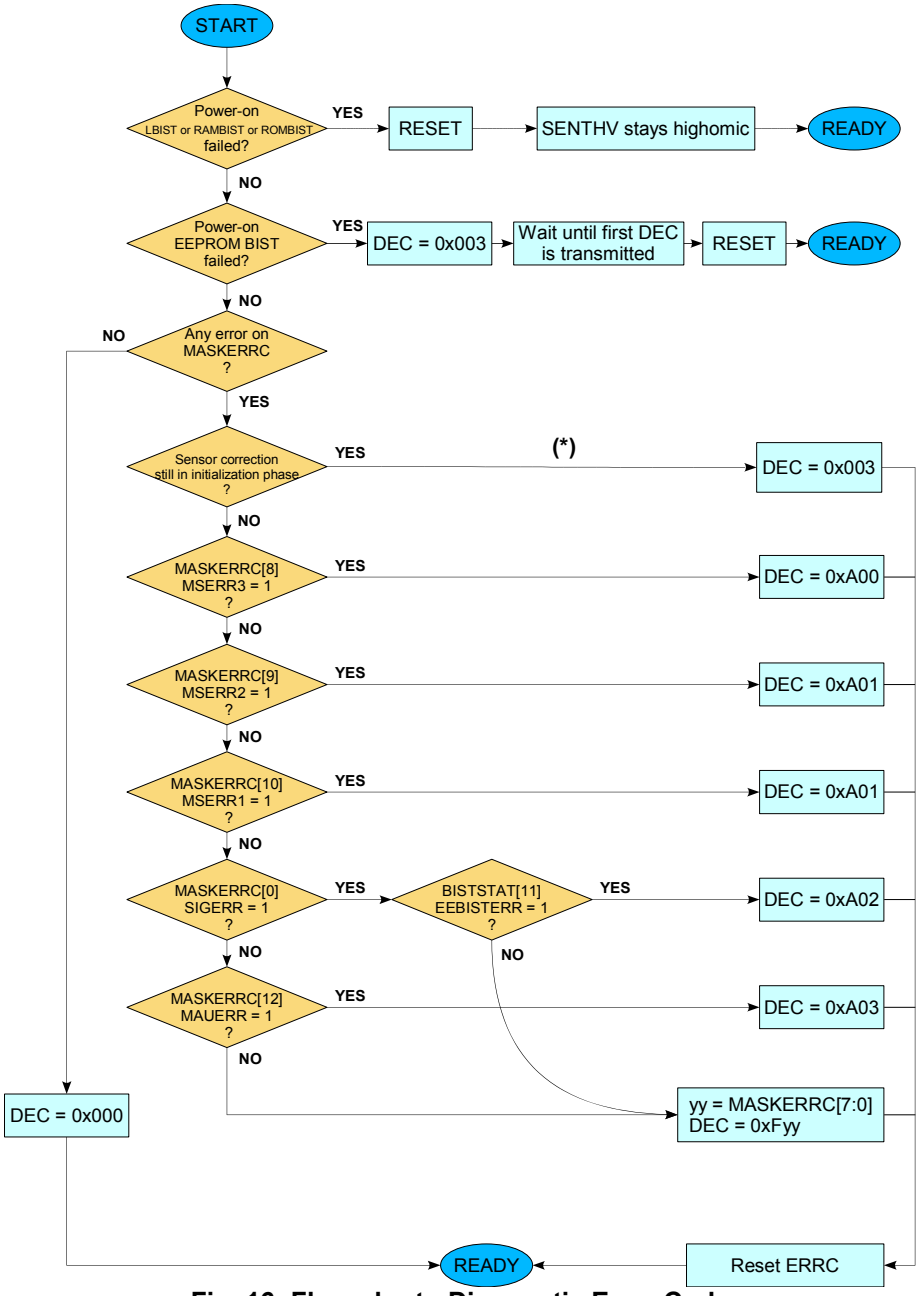


Fig. 16: Flow chart - Diagnostic Error Code

(*) Any error enabled during initialization; after initialization next DEC determines error.

5.4.5 Common Command Processor (CCP)

Besides the SENT output the device provides access to calibration and configuration functions. Thus this device provides a SPI compatible interface and a Serial Input/Output (SIO) which realizes a one wire interface function by pin sharing with the SENTHV pin

A Common Command Processor (CCP) processes incoming commands and responds respectively, independent on where the command came from. Thus a flexible configuration using different types of user interfaces for a maximum of convenience and flexibility is possible.

In any case the device behaves as slave, in particular it will never initiate a communication.

Not all commands are applicable in all operation modes, for details see 5.4.5.3.

5.4.5.1 Common Command Processor Modes

After power-on first the reset delay elapses (see 5.2.3). Then the SSP enters ***operational mode*** and a time window opens for the duration t_{WINDOW}. (see ch. 4.2, section “Digital Timing Parameters”). This time window is used to restrict the entrance into the ***configuration mode*** and the ***diagnostic mode*** . The time window is active only once per power-on, i.e. after reception of a RESET command the time window will *not* be activated.

The CCP supports the following four different access modes:

1. **CCP window mode** (default, SCOM.MOD = 000b, **factory/end of line use**)
   During the time window after power-on the SENT output is in high impedance.
   a) When the ENACONF command does not arrive within the time window then the ***configuration mode*** cannot be entered. The SSP stays permanently in ***operational mode*** , the SENTHV output becomes active and the SIO is disabled. Digital communication is then restricted to the SPI interface.
   b) When the ENACONF command arrives via SIO or SPI within the time window then the ***configuration mode*** is entered and the SENT output stays in high impedance. By issuing the OPERATE command the mode can be changed from ***configuration mode*** to ***operational mode*** . The SSP will then behave like in a) unless another CCP mode has been selected.
   If any other command than ENACONF, or a NOP command via SPI, is received during time window then the time window will be closed immediately and ***operational mode*** is entered.
2. **SENT only mode** (SCOM.MOD = 100b, ***operational mode***)
   During a shortened time window after power-on the SENT output is in high impedance, but neither ***configuration mode*** nor ***diagnostic mode*** can be entered. When the time window has elapsed the SENT output signal is permanently available, digital communication via SIO or SPI is not possible.
3. **SENT mode** (SCOM.MOD = 101b, ***operational mode*** and ***diagnostic mode***)
   During the time window after power-on the SENT output is in high impedance. The ***configuration mode*** cannot be entered.
   a) When the ENADIAG command does not arrive within the time window then the **diagnostic mode** cannot be entered. The SSP stays permanently in operational mode, the SENTHV output becomes active and the SIO is disabled. Digital communication is then restricted to the SPI interface.
   b) When the ENADIAG command arrives via SIO or SPI within the time window then the ***diagnostic mode*** is entered and the SENT output stays in high impedance. By issuing the OPERATE command the mode can be changed from ***diagnostic mode*** to ***operational mode*** . The SSP will then behave like in a).
   If any other command than ENADIAG, or a NOP command via SPI, is received during time window then the time window will be closed immediately and ***operational mode*** is entered.
4. **CCP mode** (SCOM.MOD = 110b, ***operational mode***)
   The SENT output is high impedant, the SIO and SPI interfaces are always enabled. Neither ***configuration mode*** nor ***diagnostic mode*** cannot be entered.

The modes can be selected with the configuration register SCOM.MOD.

5.4.5.2 CCP Command Format

The bus master initiates communication by sending a command to the SSP. A command is a sequence of two to five bytes. The first byte in this sequence is the command code, the last byte is the check sum. The bytes in between are parameters for the command. The check sum is the sum of all it's preceding bytes plus one modulo 256. The NOP command is special, because it requires no check sum.

After command reception, the SSP requires some processing time to generate an answer. This processing time causes a delay that depends on the command code.

In case of SIO communication, the answer will be sent autonomously by the SSP when the delay has elapsed.

In case of SPI communication the SSP cannot send data autonomously. Therefore the bus master can

- either wait, until the delay has elapsed and then get the answer
- or poll the SSP.

When the delay has elapsed, the answer can be retrieved by the bus master. This involves also sending a new byte to the SSP.

When the bus master tries to retrieve data from the SSP before the answer has been generated, then the SPI will sent a zero. This mechanisms facilitate the polling technique.

As a special case, it is possible to read out the SSP via SPI without having issued a command, before. In this case the SSP will answer as if the GETSIG command would have been issued before. This command is used to read out pressure or temperature.

For SIO communication, there is a delay between command reception and generation of the answer. During this time the SSP switches the SENTHV pin to high impedance.

5.4.5.2.1 SIO Communication Protocol Example

The following picture shows a SIO protocol example during ***configuration mode*** . Two commands are transmitted by the bus master. The first command is a WRITE command that writes a 16-bit value into the user RAM. The second command GETSIG is used to retrieve pressure measurement data.

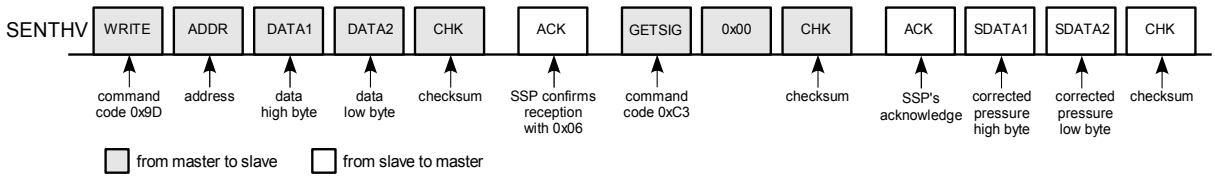


Fig. 17: SIO Communication protocol example

5.4.5.2.2 SPI Communication Protocol Example

In the following Fig. 18 an example SPI communication protocol is shown for the command WRITE.

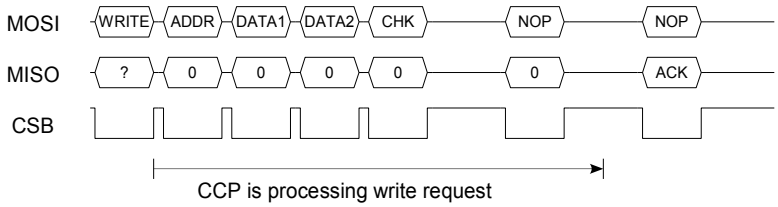


Fig. 18: SPI protocol example WRITE

First the SPI master transfers the WRITE command sequence (five bytes, including checksum). The first byte is the WRITE command code. After it's reception the SSP starts processing this command. From that moment on the SSP will answer zeros until the command has been processed and an ACK (0x06) is sent. The very first byte that is answered by the SSP still belongs to the previous command's answer.

The following NOP commands are used to poll whether the SSP has finished processing the WRITE command. This is the case with the second NOP.

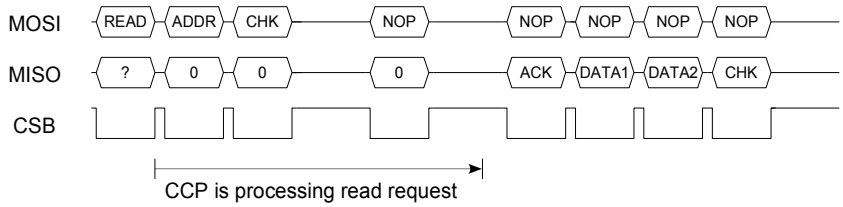


Fig. 19: SPI protocol example READ

The second example in Fig. 19 depicts a sequence for the command READ. First the READ command sequence (three bytes, including check sum) is transmitted. The first byte is the READ command code, followed by the address of the byte to read and finally the check sum. Again the SSP will answer zeros until the command has been processed and an ACK (0x06) is sent. The complete answer for a READ command contain 4 bytes, first the acknowledge, then two data bytes, high byte first, and finally the check sum.

5.4.5.2.3 SPI Readout without a Preceding Command

It is also possible to read out the pressure and temperature signals via the SPI interface without having to issue a command before.

When the answer for the last command has been sent by the SSP, then any further data that is read out, is pressure/temperature data. This happens, when further NOP commands are issued. Then the data that is sent by the SSP resembles the answer to a GETSIG command with the exception that bit 3 of the first byte is one instead of zero.

The GETSIG command (see Table 24, pg. 49) can be used to determine, whether the raw or corrected pressure signal and additionally the temperature signal should be transmitted, see Fig. 20.

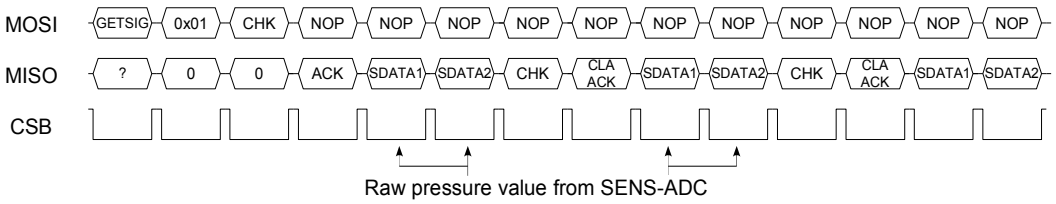


Fig. 20: SPI commandless response: Pressure (RD_ONCE = 0b)

With SCOM.RD_ONCE = 1b the SSP answers with a CLA_NACK (0x1D, commandless response not acknowledge) as long as no new pressure data is available. When a new pressure value is available the answer starts with the CLA_ACK (0x0E, commandless response acknowledge) followed by two or four data bytes, depending on the last GETSIG command. Last byte is, as always, the check sum.

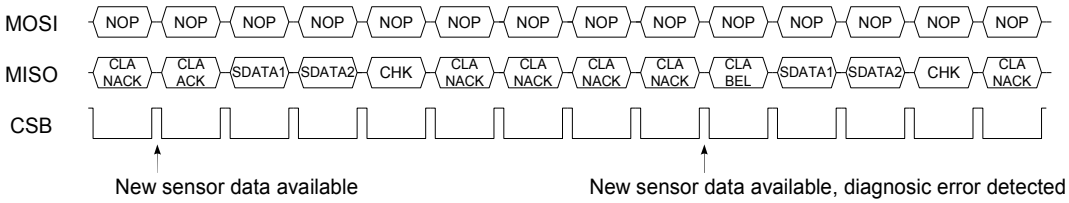


Fig. 21: SPI commandless response: Pressure (RD_ONCE = 1b)

The answer can start with a CLA_ACK (0x0E), if no error is present or with a CLA_BEL (0x0F), if an enabled error is detected (see second answer in Fig. 21 and Fig. 22).

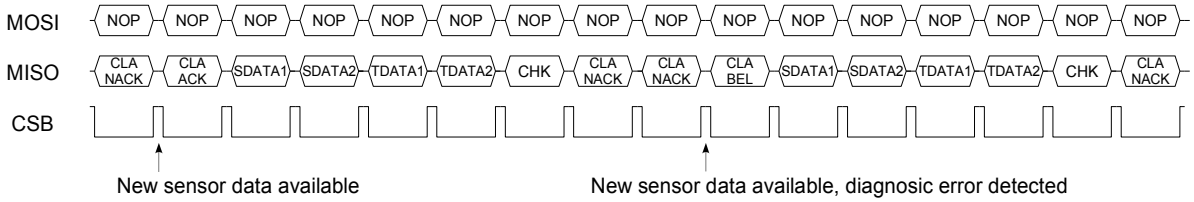


Fig. 22: SPI commandless response: Pressure and Temperature (RD_ONCE = 1b)

5.4.5.3 CCP Commands

Table 15: Command table

Command Name	*Command Code*	*Description*
ENACONF	0x84	Activate ***configuration mode***
ENADIAG	0x8C	Activate ***diagnostic mode***
READ	0x93	Read 16 bit value from configuration memory (refer to 5.2.4)
WRITE	0x9D	Write 16 bit value to configuration memory (refer to 5.2.4)
EEUPD	0xA3	Update EEPROM, all changes on RAM are stored on EEPROM
READEE	0xD3	Read EEPROM and store on RAM
OPERATE	0xAB	Switch to ***operational mode***
BIST	0xB3	Execute built-in self-tests
GETSIG	0xC3	Read pressure / temperature value
GETELID	0xCA	Read ELMOS Device ID
RESET	0xE2	Resets the device
NOP	0x89	No operation, only for SPI

Table 16: Command ENACONF

Command Name	*ENACONF - enable configuration mode*
Function	Activates configuration mode to communicate (read and write) with the SSP
Validity	Only valid during the time window (t_{WINDOW}, see Electrical Characteristics) after power-on when SCOM.MOD = 000b (CCP window mode)
Command Code	Byte 1 : 0x84
Following Bytes	Byte 2 : 0xE5 (constant) Byte 3 : 0x5E (constant) Byte 4 : 0xC8 (check sum)
Answer	Byte 1 : • 0x06 (ACK). if configuration mode is entered • 0x15 (NACK), if command, any parameter or check sum is invalid

Table 17: Command ENADIAG

Command Name	*ENADIAG - enable diagnostic mode*
Function	Activates diagnostic mode to communicate (read only) with the SSP
Validity	Only valid during the time window (t_{WINDOW}, see Electrical Characteristics) after power-on when SCOM.MOD = 101b (SENT mode)
Command Code	Byte 1 : 0x8C
Following Bytes	Byte 2 : 0xE5 (constant) Byte 3 : 0x5E (constant) Byte 4 : 0xD0 (check sum)
Answer	Byte 1 : • 0x06 (ACK), if diagnostic mode is entered • 0x15 (NACK), if command, any parameter or check sum is invalid

Table 18: Command READ

Command Name	***READ - read 16 bit value***
Function	Read a 16 bit value from given address
Validity	• Configuration mode • Diagnostic mode • Operational mode, if SCOM.MOD = 000b or 101b (only SPI) or 110b (SIO & SPI)
Command Code	Byte 1 : 0x93
Following Bytes	Byte 2 : Configuration memory address (must be even, see Table 9) Byte 3 : check sum

Answer	Byte 1 :
	• 0x06 (ACK)
	  • Byte 2 - Byte 4 will be sent
	• 0x15 (NACK), if address or check sum is invalid
	  • no further Byte will be sent
	Byte 2 : High byte of configuration memory
	Byte 3 : Low byte of configuration memory
	Byte 4 : check sum

Table 19: Command WRITE

Command Name	***WRITE - write a 16 bit value***
Function	Write a 16 bit value to given address
Validity	Only valid in configuration mode, so SCOM.MOD must contain 000b. **There are two exceptions :** Addresses 0x64 (ERRC) and 0x66 (BISTSTAT) are also writeable in • Diagnostic mode and in • Operational mode if SCOM.MOD = 000b or 101b (only SPI) or 110b (SIO & SPI)
Command Code	Byte 1 : 0x9D
Following Bytes	Byte 2 : Configuration memory address (must be even, see Table 9) Byte 3 : High Byte to write Byte 4 : Low Byte to write Byte 5 : check sum
Answer	Byte 1 : • 0x06 (ACK), if value has been written • 0x15 (NACK), if command, address or check sum is invalid

Table 20: Command EEUPD

Command Name	*EEUPD - EEPROM update*
Function	Changes on the RAM data are stored to the EEPROM
Validity	Only valid in configuration mode, so SCOM.MOD must contain 000b.
Command Code	Byte 1 : 0xA3
Following Bytes	Byte 2 : reserved (0x01) Byte 3 : check sum
Answer	Byte 1 : • 0x06 (ACK), if update successful • 0x15 (NACK), if command or check sum is invalid

Table 21: Command READEE

Command Name	*READEE - read EEPROM content*
Function	Read EEPROM and store to RAM and registers
Validity	• Configuration mode • Diagnostic mode
Command Code	Byte 1 : 0xD3
Following Bytes	Byte 2 : 0x00 Byte 3 : 0xD4 (check sum)
Answer	Byte 1 : • 0x06 (ACK), if reading has finished • 0x15 (NACK), if command, parameter or check sum invalid

Table 22: Command OPERATE

Command Name	*OPERATE- switch into operational mode*
Function	Switch to operational mode
Validity	• Configuration mode • Diagnostic mode
Command Code	Byte 1 : 0xAB
Following Bytes	Byte 2 : 0x00 Byte 3 : 0xAC (check sum)
Answer	Byte 1 : • 0x06 (ACK) • 0x15 (NACK), if command or check sum invalid

Table 23: Command BIST

Command Name	***BIST - execute BIST***
Function	Execute the built-in self-tests
Validity	• Configuration mode • Diagnostic mode
Command Code	Byte 1 : 0xB3
Following Bytes	Byte 2 : select a test step: • 0x01 : ROM BIST (ROBIST_DONE, ROBISTERR) • 0x02 : RAM BIST (RABIST_DONE, RABISTERR) • 0x03 : EEPROM BIST (EEBIST_DONE, EEBISTERR) • 0x04 : Arithmetic Unit BIST (AUBIST_DONE, AUBISTERR) • 0x05 : Logic BIST (LBIST_DONE, LBISTERR) Byte 3 : check sum

Answer	Byte 1 :
	• 0x06 (ACK), if selected test starts
	• 0x15 (NACK), if command, parameter or check sum invalid
	After the selected test is done, the corresponding DONE flag in BISTSTAT register and - in case of an error - the corresponding error flag in BISTSTAT register is set. Use the READ command on BISTSTAT to check the flags and determine the result:
	• DONE flag :
	  • 0b : test not done
	  • 1b : test has finished
	• ERR flag :
	  • 0b : no error detected
	  • 1b : test failed

Table 24: Command GETSIG

Command Name	*GETSIG - read pressure or temperature value*
Function	Read pressure or temperature value according to selection, returned values are not limited
Validity	• Configuration mode • Diagnostic mode • Operational mode if SCOM.MOD = 000b or 101b (only SPI) or 110b (SIO & SPI) **Note:** If in configuration mode or in diagnostic mode a corrected pressure value is requested, first the correction of the recent uncorrected pressure is performed before it is sent out (time duration : t.b.d).
Command Code	Byte 1 : 0xC3

Following Bytes	Byte 2,
	• Bit[0]
	  • 0b : select corrected pressure
	  • 1b : select uncorrected pressure
	• Bit[1]
	  • 0b : don't select temperature
	  • 1b : select temperature (normalized if bit[0] = 0b or raw if bit[0] = 1b)
	• Bit[7:2] : unused (don't care)
	Byte 3 : check sum

Answer	Byte 1 :
	• 0x06 (ACK), if answer is ready
	• 0x07 (BEL), if answer is ready and an enabled error is present (refer to 5.5.10)
	  • if received Byte2[1] = 0b: (without temperature) Byte 2 - 3 and check sum will be sent
	  • else received Byte2[1] = 1b: (with temperature) Byte 2 - 5 and check sum will be sent
	• 0x15 (NACK), if check sum is invalid
	Byte 2 : High byte of pressure
	Byte 3 : Low byte of pressure
	Byte 4 : High byte of temperature
	Byte 5 : Low byte of temperature
	Final Byte : check sum

Table 25: Command GETELID

Command Name	***GETELID - read ELMOS Device ID***
Function	Read ELMOS Device ID
Validity	• Configuration mode • Diagnostic mode • Operational mode if SCOM.MOD = 000b or 101b (only SPI) or 110b (SIO & SPI)
Command Code	Byte 1 : 0xCA
Following Bytes	Byte 2 : 0xCB (check sum)

Answer	Byte 1 :
	• 0x06 (ACK), if answer is ready
	  • Byte 2 - 6 will be sent
	• 0x15 (NACK), if check sum is invalid
	  • no further Byte will be sent
	Byte 2 - 5 : ELMOS ID, high Byte first
	Byte 6 : check sum

Table 26: Command RESET

Command Name	***Reset***
Function	Reset the device without leaving recent operation mode
Validity	• Configuration mode • Diagnostic mode • Operational mode if SCOM.MOD = 000b or 101b (only SPI) or 110b (SIO & SPI)
Command Code	Byte 1 : 0xE2
Following Bytes	Byte 2 : 0xE3 (check sum)
Answer	The reset happens, and no answer is sent.

Table 27: Command NOP

Command Name	*NOP*
Function	No operation. Only for SPI operation to read out answers from the SSP.
Validity	• Configuration mode • Diagnostic mode • Operational mode when SCOM.MOD = 000b (SIO & SPI), 101b (only SPI) or 110b (SIO & SPI)
Command Code	Byte 1 : 0x89
Following Bytes	-
Answer	Depends on previous commands. **For commandless answer:** CLA_ACK (0x0E) acknowledge , followed by 2 or 4 bytes data and a final check sum. If an enabled error is detected CLA_BEL (0x0F) is send instead of CLA_ACK. If SCOM.RD_ONCE = 1b, CLA_NACK (0x1D) is send until a new pressure value is available (refer to 5.4.5.2.3).

5.4.6 Power-on Control

During power-on the SSP will start with voltage monitoring being disabled, i.e. all ENERR bits are cleared, see chapter 5.5.10. After time t_{DIS_VMON} all ENERR bits will be initialized with the corresponding EEPROM contents to enable the desired voltage monitoring settings.

Depending on the settings in the ENERR register, the SSP will process various power-on self-tests, see chapter 5.5.10. These self-tests are applied after elapsing of the time window t_{WINDOW} = 5 ms (typical).

The minimum total start-up time is 6 ms. Depending of configuration (system clock, power-on self tests, ...) the startup time can be significantly longer.

5.4.7 EEPROM Refresh

The EEPROM memory is regularly checked for weak cells to refresh their contents. The EEPROM refresh can be enabled/disabled by the SCOM.RFSH_EN bit.

5.5 Diagnosis

This chapter summarizes all diagnostic functions of the SSP. If any diagnosis detects an error in ***operational mode*** , specific error codes are transmitted via the SENT interface. During ***configuration*** , ***diagnostic mode*** and ***operational mode*** all error cases can be read via the Error Code Register (ERRC), the Masked Error Code (MASKERRC) and the BIST Status Register (BISTSTAT) (refer also to chapter 5.5.10).

5.5.1 Sensor Diagnosis

The chip provides surveillance for the sensor and its connections to the device. The following events can be detected:

1. open at bridge excitation EXHI, EXLO
2. short of bridge excitation (between EXHI and EXLO)
3. short of sensor outputs (INP, INN) to bridge excitation (EXHI,EXLO)
4. open at sensor outputs INP, INN (with sensor pull-ups enabled)

These faults are detected by 5 comparators and signalled by 3 corresponding flags in the ERRC register (see Table 28, and chapter 5.5.10).

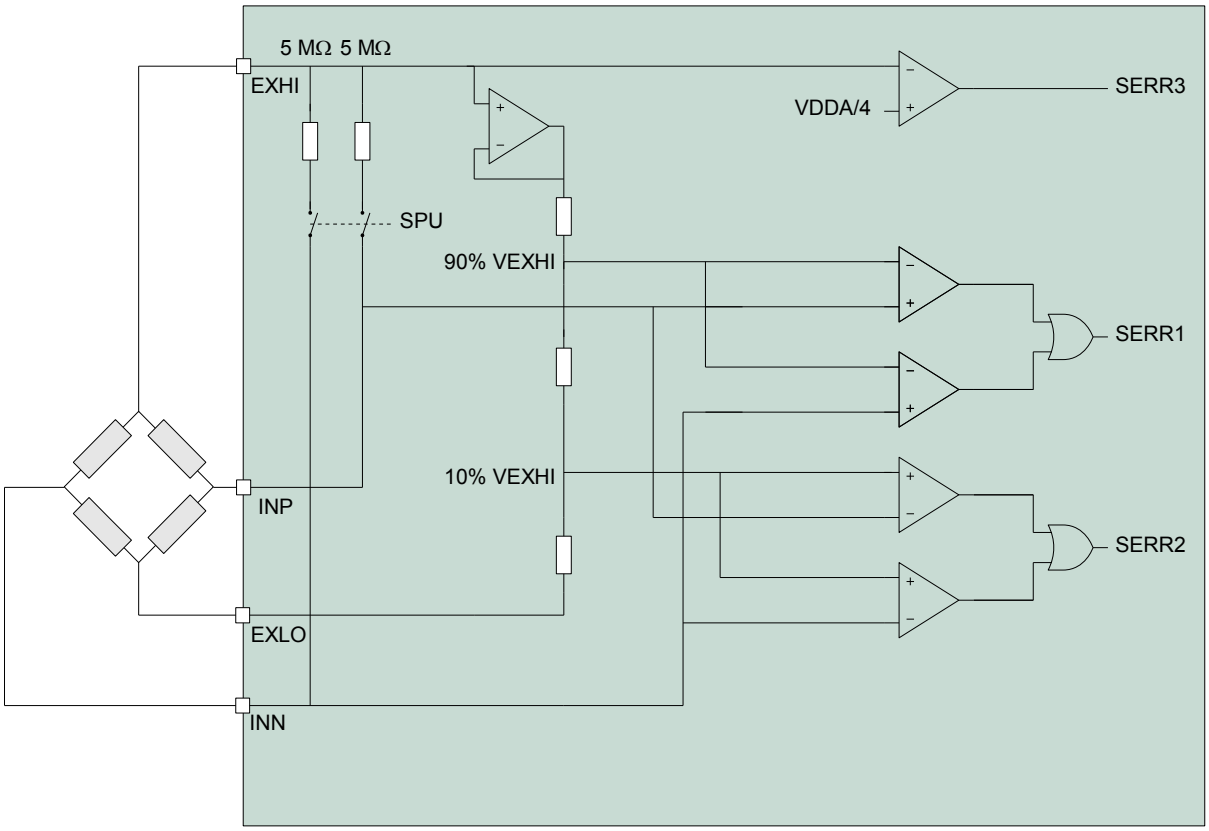


Fig. 23: Block diagram "sensor diagnosis"

The individual SENT fault indicators can be enabled by ENSERR.ENSERR1-3, (see Table 28).

Table 28: Sensor diagnosis flags

Fault	*SPU-Bit*	*detected fault condition*	*Fault Indicator*
INP, INN short to EXHI	X	VINP > 90% VEXHI or VINN > 90% VEXHI	ERRC.SERR1, if enabled: DEC = 0xA01
INP, INN short to EXLO	X	VINP < 10% VEXHI or VINN < 10% VEXHI	ERRC.SERR2, if enabled: DEC = 0xA01
EXHI short to EXLO	X	VEXHI < VDDDA/4	ERRC.SERR3, if enabled: DEC = 0xA00
EXHI open	X	VINP < 10% VEXHI or VINN < 10% VEXHI	ERRC.SERR2, if enabled: DEC = 0xA01
EXLO open	X	VINP > 90% VEXHI or VINN > 90% VEXHI	ERRC.SERR1, if enabled: DEC = 0xA01
INP, INN open	1	VINP > 90% VEXHI or VINN > 90% VEXHI	ERRC.SERR1, if enabled: DEC = 0xA01

5.5.2 Supply Diagnosis

The chip provides general system surveillance in order to detect ground or supply loss and if any of the supply voltages (VDDHV, VDDA, VDDD) is out of range.

Ground / Supply Loss

In case of ground loss in the connection ECU - Sensor Module, VSS of the Sensor Module will get pulled towards the positive supply of the Sensor Module by the current consumption of the Sensor Module. For configurations with a PD-resistor Rpd at SENT inside the ECU, the voltage at SENT will remain close to GND of the ECU and thus inside the diagnostic level range. On the Sensor Module SENT will thus be well below VSS. Any leakage current ILEAK flowing out of the SENT-pin will cause voltage drop across the PD-resistor in the ECU and thus raise the measured voltage. In order for it to remain within the diagnostic level range RPD * Ileak must be less than 2.5% FSR. This imposes a maximum upon the value of RPD.

The opposite situation occurs for VSUP loss with a PU-resistor RPU inside the ECU. The leakage current flowing into the SENTHV pin then similarly imposes a maximum for the value of RPU.

Configurations with a PD-resistor are robust against leakages at pin SENT in case of VSUP loss and configurations with a PU-resistor are robust against at pin SENT in case of GND loss.

In case of any of these failures being detected the SENTHV output goes to high impedance and the SSP is not operating.

Voltage monitoring

The voltage monitor observes the 5V supply VDDHV as well as the internal 3.3V supply voltages VDDA and VDDD. If any of the voltages leave their ranges the fault indicator is enabled with ENERR.ENV3ERR and ENERR.ENV5ERR.

The fault indicators are:

1. VDDHV out of range :

Set V5ERR in ERRC, the SENTHV pin gets high impedant as long as the error is present.

2. VDDA or VDDD out of range :

Set V3ERR in ERRC, set error flag in SENT status nibble, send error code 4090 on fast channel and diagnostic error code 0xFyy with bit 1 set on slow channel.

5.5.3 Oscillator Diagnosis

If the Oscillator fails the SENTHV output goes to high impedance. The SSP is not operating.

5.5.4 Amplifier Diagnosis

In case of saturation in the sensor amplifier the error flag ERRC.SAMPSAT is set.

If the SENT fault indicator is enabled with ENERR.ENSAMPSAT = 1b, the error flag in the SENT status nibble is set, error code 4090 is sent on fast channel and DEC = 0xFyy with bit 2 set is sent on slow channel.

5.5.5 ADC Diagnosis

If the analog-to-digital conversion is out of range in the sensor ADC or the temperature ADC the error flags ERRC.SADCSAT / ERRC.TADCSAT are set.

If the corresponding SENT fault indication is enabled with ENERR.ENSADCSAT = 1b / ENERR.ENTADCSAT = 1b, the error flag in the SENT status nibble is set, error code 4090 is sent on the fast channel and the diagnostic error code 0xFyy with bit 3 / bit 4 set is sent on the slow channel.

5.5.6 Arithmetic Diagnosis

Saturation

The SSP's arithmetic unit is able to detect two faults during sensor signal correction (refer to 5.4.1):

1. The temperature value is out of range after temperature pre-processing (normalization)
2. The corrected sensor value is out of range

If these values are out of range the corresponding error flags ERRC.TNORMSAT / ERRC.CORRSAT are set.

If the dedicated SENT fault indication is enabled with ENERR.ENTNORMSAT = 1b / ENERR.ENCORRSAT = 1b the error flag in the SENT status nibble is set, error code 4090 is sent on the fast channel and the diagnostic error code 0xFyy with bit 5 / bit 6 set is sent on the slow channel.

Note: If the SENT interface is used, the SENT fault indicator for the corrected sensor value should be disabled (ENERR.ENCORRSAT = 0b), because the pressure output on SENT is saturated according to SENT standard (see ch. 7) and should not transmit FC error code 4090 in this case. The SENT fault indicator for the normalized temperature value should be enabled (ENERR.ENTNORMSAT = 1b), even when the SSP is configured as type **P/S/t**, because a saturated temperature value falsifies the corrected pressure value.

Arithmetic Unit BIST

Furthermore the SSP provides a built-in self-test for the arithmetic unit (AUBIST). The AUBIST SENT fault indication can be enabled with ENERR.ENAUBIST = 1b. If not disabled with ENERR.DISCYCTST = 1b, the AUBIST runs continuously during ***operational mode*** performing a functional test of the arithmetic unit. If AUBIST fails the error flag ERRC.AUERR = BISTSTAT.AUBISTERR is set, the error flag in the SENT status nibble is set, error code 4090 is sent on the fast channel and the diagnostic error code 0xA03 is sent on the slow channel.

In ***configuration*** or ***diagnostic mode*** the AUBIST can also be triggered by the CCP command BIST (refer to chapter 5.4.5.3). Results can be read from BISTSTAT.AUBISTERR and BISTSTAT.AUBIST_DONE.

5.5.7 Memory Diagnosis

The SSP is able to perform various tests concerning ROM, RAM and EEPROM memory.

ROM BIST

A ROM build-in self-test performing a 16 bit standard CRC is implemented to run continuously during ***operational mode*** . This cyclic ROM BIST can be disabled with ENERR.DISCYCTST = 1b.

In case of a fault in this test BISTSTAT.CROBISTERR and ERRC.SIGERR are set, the error flag in the SENT status nibble is set, error code 4090 is sent on the fast channel and the diagnostic error code 0xFyy with bit 0 set is sent on the slow channel. The fault indication for the ROM BIST has not to be enabled, it is always active.

The ROM BIST can be configured by ENERR.ENPOSTRO = 1b to run completely after power-on. If the power-on ROM BIST fails BISTSTAT.ROBISTERR is set, and the SSP initiates a reset to rerun the test. During the whole time SENTHV stays high ohmic.

As a third possibility in ***configuration*** or ***diagnostic mode*** this test can be triggered by the command BIST (refer to chapter 5.4.5.3). In this case the test result can be read on BISTSTAT.ROBISTERR and BISTSTAT.ROBIST_DONE.

RAM BIST

A RAM build-in self-test can be configured by ENERR.ENPOSTRA = 1b to run after power-on or it can be triggered by the command BIST (refer to chapter 5.4.5.3) in ***configuration*** or ***diagnostic mode*** . In both cases the results can be read on BISTSTAT.RABIST_DONE and BISTSTAT.RABISTERR. In case of failing in power-on RAM BIST the SSP initiates a reset to rerun the test. During the whole time SENTHV stays high ohmic.

EEPROM Tests

To provide highest surveillance on the configuration data stored on the EEPROM two different methods are implemented in the SSP :

1. Each EEPROM byte is equipped with an ECC to correct 1 bit errors.
   If in any operation mode a bit error is detected ERRC.ECCERR is set.
2. To detect multi bit errors additionally a 16 bit standard CRC over the EEPROM configuration data is performed. In any case of a failure of this test BISTSTAT.EEBISTERR is set.
   In ***operational mode*** this test runs continuously and the fault indicator on the SENT interface is the error flag in the SENT status nibble, error code 4090 on the fast channel and the diagnostic error code 0xA02 on the slow channel. This cyclic BIST can be disabled with ENERR.DISCYCTST = 1b.
   In ***configuration*** or ***diagnostic mode*** the EEPROM check sum test can also be triggered by the BIST command and the result could be read from BISTSTAT.EEBISTERR and BISTSTAT.EEBIST_DONE.

The EEPROM BIST runs also always after power-on. In case of failing the error flag in the SENT status nibble is set, error code 4090 is sent on the fast channel and the diagnostic error code 0x003 (initialization error) is sent on the slow channel. When the complete DEC is transmitted a reset is generated to rerun the test. During the re-initialization and the re-test SENTHV is driven high.

The standard CRC for ROM and EEPROM BIST routines use the polynome

$$x^{16}+x^{12}+x^{5}+1$$

to sum up byte by byte.

5.5.8 Logic Diagnosis

Logic BIST

For production test the SSP's digital part is equipped with scan paths. In the logic build-in self-test the scan paths are stimulated by the SSP's LBIST engine and a check sum is calculated and compared to the desired value.

The LBIST can be configured by ENERR.ENPOSTL = 1b to run after power-on or it can be triggered by the command BIST (refer to chapter 5.4.5.3) in ***configuration*** or ***diagnostic mode*** . In both cases the result can be read from BISTSTAT.LBIST_DONE and BISTSTAT.LBISTERR. In case of failing in power-on LBIST the SSP initiates a reset to rerun the test. During the whole time SENTHV stays high ohmic.

Logic Control Consistency Monitor

To avoid accidental failures, e.g. provoked by transient disturbances, a logic control consistency monitor is implemented. This monitor observes the correct logic control flow of the EEPROM write access (refer also to chapter 5.2.4), the continuous copying process from EEPROM to RAM, the signal correction, the data to send via SENT interface, the execution of CCP commands and all continuously running tests.

If the LCC monitor detects any inconsistency in the logic control flow a system reset is generated and ERRC.LCCERR is set. After reset the initialization is performed without the enabled build-in self-tests.

5.5.9 SENT Diagnosis

When the SENT output driver detects an error (e.g. due to an external short), then ERRC.SENTERR is set. As long as the error is present fast channel error code 4090 is sent with the error flag set. The next diagnostic error code will send 0xFyy with bit 7 set on the slow channel while the fast channel transmits valid sensor data.

5.5.10 Diagnosis Registers

For fault diagnosis following four registers/signals are used (Table 29).

Table 29: Diagnosis registers

Register	*Address*	*Description*
ERRC	0x64	Error Code Register (read/write)
ENERR	0x74	Enable Error Register (read/write)
MASKERRC	0x62	Masked Error Code (read only)
BISTSTAT	0x66	BIST Status Register (read/write)

The Enable Error Register is used to enable errors to be indicated on SENT protocol. The error flag in the SENT status nibble (bit 0 = ERROR) is generated depending on the Masked Error Code.

A detailed description of the specific Diagnostic Error Code on the SENT slow channel can be found in chapter 5.4.4.2

The occurrence of an enabled error will be indicated via messages on the SENT interface. There are two exceptions:

1. A logic control consistency error (LCCERR) will cause the SSP to be reset. Then the SSP will initialize again, omitting the power-on self-tests.
2. In case of VDDHV out of range (V5ERR and ENV5ERR), the SENTHV output will be set to high impedance state. The SENTHV output returns to normal operation immediately when the fault is not present any more.

Table 30: Error code and enable error registers

Bit	*ERRC register*	*ENERR register*	*Description*	*DEC[1)]*
0	SIGERR	refer to Table 31	Memory signature error	0xFyyh : bit0
1	V3ERR	ENV3ERR	VDDA or VDDD out of range error	0xFyyh : bit1
2	SAMPSAT	ENSAMPSAT	Sensor amplifier saturation	0xFyyh : bit2
3	SADCSAT	ENSADCSAT	Sensor ADC out of range	0xFyyh : bit3
4	TADCSAT	ENTADCSAT	Temperature ADC out of range	0xFyyh : bit4
5	TNORMSAT	ENTNORMSAT	Saturation after temperature normalization	0xFyyh : bit5
6	CORRSAT	ENCORRSAT	Signal correction saturation	0xFyyh : bit6
7	SENTERR	ENSENTERR	Error on SENTHV	0xFyyh : bit7
8	SERR3	ENSERR3	sensor error 3: EXHI short to EXLO	0xA00h
9	SERR2	ENSERR2	sensor error 2: INP, INN short to EXLO or EXHI open	0xA01h
10	SERR1	ENSERR1	sensor error 1: INP, INN short to EXHI or EXLO open or if **SPU = 1** : INP, INN open	0xA01h
11	ECCERR	refer to Table 31	EEPROM ECC error	-
12	AUERR	ENAUBIST	arithmetic unit BIST failed	0xA03h
13	V5ERR	EN5ERR	VDD out of range error	high Z
14	LCCERR	refer to Table 31	Logic control consistency error	reset
15	*unused*	DISCYCTST	Disable all continuously running self tests (cyclic EEBIST, ROMBIST & AUBIST)	-

1) Diagnostic Error Codes for errors during ***operational mode***

Besides the upper mentioned bits the ENERR register provides three further bits for configuring a power-on self-test (POST), see the following Table 31.

Table 31: Power-on self-test bits of ENERR register

Bit	*ENERR register*	*description*
0	ENPOSTL	enable logic BIST during POST
11	ENPOSTRO	enable ROM BIST during POST
14	ENPOSTRA	enable RAM BIST during POST

At last the BISTSTAT register (Table 32) contains all results of the built-in self-tests. There are two connections between registers ERRC and BISTSTAT:

1. ERRC.AUERR = BISTERR.AUBISTERR
2. ERRC.SIGERR = BISTSTAT.CROBISTERR or BISTSTAT.EEBISTERR

Table 32: BIST status register (0x66)

Bit	*BISTSTAT register*	*description*	*fault indicator / DEC[1)]*
0	LBIST_DONE	Logic BIST has been done	-
1	ROBIST_DONE	ROM BIST has been done	-
2	RABIST_DONE	RAM BIST has been done	-
3	EEBIST_DONE	EEPROM BIST has been done	-
4	AUBIST_DONE	Arithmetic unit BIST has been done	-
5	CROBIST_DONE	Continuous ROM BIST has been done	-
7,6	*unused*	-	-
8	LBISTERR	Logic BIST failed after command in **configuration/diagnostic mode** or after power-on.	after power-on : reset
9	ROBISTERR	ROM BIST failed after command in **configuration/diagnostic mode** or after power-on.	after power-on : reset
10	RABISTERR	RAM BIST failed after command in **configuration/diagnostic mode** or after power-on.	after power-on : reset
11	EEBISTERR	EEPROM BIST failed after command in **configuration/diagnostic mode** or after power-on or during continuous BIST in **operational mode**.	after power-on : 0x003 operational mode : 0xA02
12	AUBISTERR	Arithmetic unit BIST failed after command in **configuration/diagnostic mode** or during continuous BIST in **operational mode**.	operational mode : 0xA03
13	CROBISTERR	Continuous ROM BIST failed in **operational mode**.	0xFyy (bit 0)
14,15	*unused*	-	-

1) Diagnostic Error Codes for BIST errors during ***operational mode***

5.5.11 Diagnosis via CCP

When the SENT interface is not used in ***operational mode*** , e.g. in CCP mode (SCOM.MOD = 110b), the whole diagnosis has to be handled via the diagnosis registers (refer to chapter 5.5.10).

SIO

When the sensor data is read out via SIO in ***operational mode*** with the command GETSIG, an enabled error is indicated by the answer's first byte BEL (0x07), refer to Table 24. In this case the ERRC register or MASKERRC and the BISTSTAT register should be read by the READ command to determine the error source. During the masters error handling the error flags on ERRC and BISTSTAT and maybe additional the done flags on BISTSTAT should be cleared by the WRITE command to determine with the next GETSIG, if the error is still present.

SPI

When the sensor data is read out via SPI in ***operational mode*** with the command GETSIG, the behaviour is the same as via SIO.

Commandless answer via SPI

If the SPI is used by commandless answer (refer to chapter 5.4.5.2.3) an enabled error is indicated by a CLA_BEL (0x0F) and the error handling has to be performed via READ and WRITE command as described above.

There is one difference in comparing to SENT error indication:

If VDDHV is out of range (V5ERR) and the fault indication is enabled with ENERR.ENV5ERR = 1b also a BEL (0x07) / CLA_BEL (0x0F) is the first byte answered. This specific error can not be read out via SIO directly, because the output driver is switched off (refer to 5.5.2). When VDDHV is in range again V5ERR indicates that the voltage was out of range.

5.5.12 Diagnosis Overview

The following Table 33 summarizes all diagnostic functions.

Table legend:

Exe : P : execution after power-up

Exe : T : execution is triggered

Exe : C : execution continuously

Ena : EN : enabled by EEPROM bit (refer to chapter 5.5.10)

Ena : COM : triggered by command (refer to chapter 5.4.5.3)

Ena : DIS : cyclic test can be disabled with ENERR.DISCYCTST

Opmode : OPM : in operational mode only

Opmode : CFM & DGM : in configuration and diagnostic mode only

FC : SENT fast channel

DEC : SENT Diagnostic Error Code on slow channel (refer to chapter 5.4.4.2)

ERRC : Error Code Register (refer to chapter 5.5.10)

BISTSTAT : BIST Status Register (refer to chapter 5.5.10)

Table 33: Diagnosis Overview

Diagnosis	*Exe | Ena*	*Opmode*	*Fault Indicator*
Sensor output open wire (INP or INN)	C | EN	CFM&DGM OPM	ERRC[9:10] (SERR2,SERR1) ERRC[9:10];FC = 4090;DEC = 0xA01
Sensor output (INP or INN) short to sensor supply (EXHI or EXLO)	C | EN	CFM&DGM OPM	ERRC[9:10] (SERR2,SERR1) ERRC[9:10];FC = 4090;DEC = 0xA01
Sensor supply open circuit (EXHI or EXLO)	C | EN	CFM&DGM OPM	ERRC[9:10] (SERR2,SERR1) ERRC[9:10];FC = 4090;DEC = 0xA01
Sensor supply short circuit (EXHI-EXLO)	C | EN	CFM&DGM OPM	ERRC[8] (SERR3) ERRC[8];FC = 4090;DEC = 0xA00
Device GND loss	C | always	always	SENTHV : high Z , no operation
Device supply loss	C | always	always	SENTHV : high Z , no operation
Supply VDDHV (5V) out of range	C | EN	CFM&DGM OPM	ERRC[13] (V5ERR) ERRC[13] ; SENTHV : high Z

Diagnosis	*Exe | Ena*	*Opmode*	*Fault Indicator*
Internal supplies VDDA/VDDD (3.3V) out of range	C | EN	CFM&DGM OPM	ERRC[1] (V3ERR) ERRC[1];FC = 4090;DEC = 0xFyy (bit 1)
Oscillator fails	C | always	always	SENTHV : high Z , no operation
Sensor amplifier saturation	C | EN	CFM&DGM OPM	ERRC[2] (SAMPSAT) ERRC[2];FC = 4090;DEC = 0xFyy (bit 2)
Sensor ADC out of range	C | EN	CFM&DGM OPM	ERRC[3] (SADCSAT) ERRC[3];FC = 4090;DEC = 0xFyy (bit 3)
Temperature ADC out of range	C | EN	CFM&DGM OPM	ERRC[4] (TADCSAT) ERRC[4];FC = 4090;DEC = 0xFyy (bit 4)
Arithmetic Unit BIST	T | COM C | EN & DIS	CFM&DGM OPM	BISTSTAT[12] (AUBISTERR) ; ERRC[12] (AUERR) BISTSTAT[12];ERRC[12];FC = 4090;DEC = 0xA03
Saturation after temperature normalization	C | EN	CFM&DGM OPM	ERRC[5] (TNORMSAT) ERRC[5];FC = 4090;DEC = 0xFyy (bit 5)
Corrected sensor signal is saturated	C | EN	CFM&DGM OPM	ERRC[6] (CORRSAT) ERRC[6];FC = 4090;DEC = 0xFyy (bit 6)
ROM signature error	P | EN T | COM C | DIS	- CFM&DGM OPM	BISTSTAT[9]; reset ; SENTHV : high Z [1)] BISTSTAT[9](ROBISTERR) BISTSTAT[13](CROBISTERR);ERRC[0];FC = 4090; DEC = 0xFyy (bit 0)
RAM test error	P | EN T | COM	- CFM&DGM	BISTSTAT[10]; reset ; SENTHV : high Z [1)] BISTSTAT[10] (RABISTERR)
EEPROM signature error	P | always T | COM C | DIS	- CFM&DGM OPM	BISTSTAT[11];FC = 4090; DEC = 0x003 BISTSTAT[11] (EEBISTERR) ;ERRC[0] (SIGERR) BISTSTAT[11];ERRC[0];FC = 4090;DEC = 0xA02
EEPROM ECC error	C | always	always	ERRC[11] (ECCERR)
Logic BIST error	P | EN T | COM	- CFM&DGM	BISTSTAT[8]; reset ; SENTHV : high Z [1)] BISTSTAT[8]; (LBISTERR)
Logic control consistency check	C | always	always	ERRC[14] (LCCERR) ; reset [2)]
Error on SENTHV	C | EN	CFM&DGM OPM	ERRC[7] (SENTERR) ERRC[7];FC = 4090;DEC = 0xFyy (bit 7)

1) In case of failing of this self-test after power-on the SSP is reset, the self-test is repeated and SENTHV stays high Z, because operation might be not secured in that case.

2) In case of a logic control consistency error the SSP is reset. There's no indication by DEC, because operation might be not secured in that case. Subsequent to the reset the initialization sequence indicates that a fault has occurred.

6 List of Abbreviations

Term	*Explanation*
BIST	Build-In Self-Test
CCP	Common Command Processor
CRC	Cyclic Redundancy Check
DEC	Diagnostic Error Code
ECC	Error-Correcting Code
LCC	Logic Control Consistency
POST	Power-on Self-Test
SENT	Single Edge Nibble Transmission
SIO	Serial Input / Output
SPI	Serial Peripheral Interface
SSP	Sensor Signal Processor

7 Related Documents

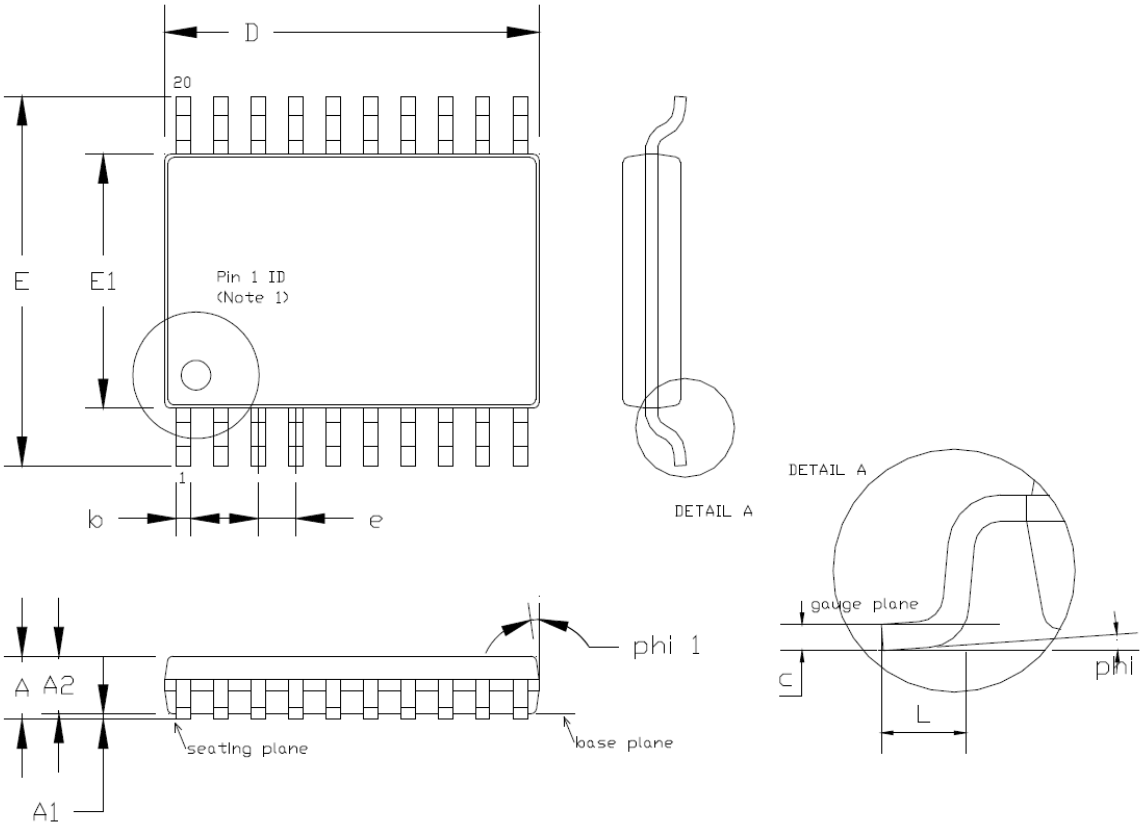
[1] SAE J2716 Information Report JAN2010,

8 Package Information

The E520.33 is available in a Pb free, RoHs compliant, TSSOP20 plastic package according to JEDEC MO-153F, variant AC.

The package is classified to Moisture Sensitivity Level 3 (MSL 3) according to JEDEC J-STD-020 with a soldering peak temperature of (260 + 5)°C.

Note: Thermal resistance junction to ambient RTH,JA is 89°C/W, based on standard JESD-51-5.



Description	Symbol	mm			inch		
		min	typ	max	min	typ	max
Package height	A	--	--	1.20	--	--	0.047
Stand off	A1	0.05	--	0.15	0.002	--	0.006
Package body thickness	A2	0.80	1.00	1.05	0.031	0.039	0.041
Width of terminal leads, inclusive lead finish	b	0.19	--	0.30	0.007	--	0.012
Thickness of terminal leads, inclusive lead finish	c	0.09	--	0.20	0.004	--	0.008
Package length	D	6.40	6.50	6.60	0.252	0.256	0.260
Package width	E		6.40 BSC			0.252 BSC	
Package body width	E1	4.30	4.40	4.50	0.169	0.173	0.177
Lead pitch	e		0.65 BSC			0.026 BSC	
Length of terminal for soldering to substrate	L	0.45	0.60	0.75	0.018	0.024	0.030
Angle of lead mounting area	phi [°]	0	--	8	0	--	8
mold release angle	phi1 [°]		12 REF			12 REF	
Number of terminal positions	N		20			20	

Note: Dimensions in mm are are true, inch dimensions contain rounding errors.

9 Record of Revisions

Rev.	Description of change	Date
.01	Initial version	2012-Jan-03
.02	Ch. 1: Maximum voltage ratings of TSEN1/2 added Ch. 4: Separate tables for Analog (4.1) and Digital Features (4.2) 4.1: Corrected limits of $V_{VDD\_3H\_THRES}$ Corrected typical value of V_{EXHI} (Constant voltage mode) Corrected maximum value of V_{EXHI} (Constant current mode) Sensor amplifier: Removed parameters V_{CM} and t_{90} Added footnote “not valid in low-power mode” to V_{ERROR} , SNR, THD, and INL_{TSEN} . Changed definition of missing codes (MC) 4.2: SENT physical interface: Added timing diagram in table SPI: Corrected system clock; added timing diagram in table 5.1.4: Corrected description of “Constant Voltage Mode (CVM)” 5.1.5: Removed figure (detail block diagram “Sensor Amplifier”) 5.1.6: Removed figure (block diagram of $\Delta\Sigma$ modulator) 5.1.7: Table 6 Footnote added. Corrected description of TSEN1/2 for substrate bias and shielding features. Table 7 Correction of full scale range for external thermistor 5.1.8: Removed figure “SENT signal at interconnection wire” (see 4.2) 5.2.2: Updated Fig. 10 (SPI byte format), timing diagram moved to 4.2 5.3: Table 10, deleted last column (current consumption) 5.4: Description of sensor signal correction (5.4.1) updated. 5.4.4.3: Corrected formula for temperature calculation 5.4.5.1: Corrected description for 1) and 3) (NOP command) 5.4.6: Description of power-on control updated 5.5.10: Description updated Ch. 7: Updated reference of SAE J2716	2012-Nov-14

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