FULLY TESTED AND INTEROPERABLE

Lattice Ethernet Solutions

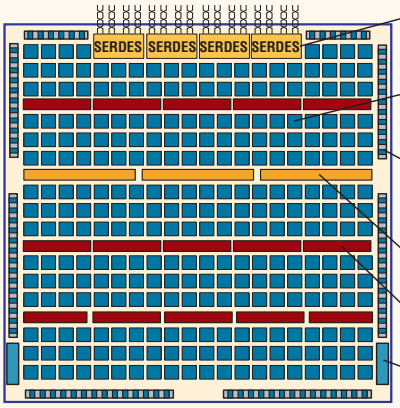
Ready-to-Use Ethernet Portfolio

Lattice provides customers with low cost and low power programmable solutions that are ready-to-use right out of the box. A full suite of tested and interoperable solutions is available for Ethernet applications, including:

- FPGAs with Embedded Ethernet-compliant SERDES
- A Complete Portfolio of Soft and Hard IP Cores for 10GbE, 2.5GbE, 1GbE, and 10/100 Ethernet Stacks
- Application Specific Development Boards, Systems and Reference Designs
- Test and Interoperability Reports for PMA, PCS and MACs

Silicon: Industry Leading Programmable Ethernet Platforms

LatticeECP3™ Low Cost FPGA



Embedded 3.2Gbps SERDES support PCI Express, Ethernet (XAUI, 1GbE, SGMII), CPRI, OBSAI & 3G/HD/SD-SDI.

Programmable Function Unit (PFU) perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions.

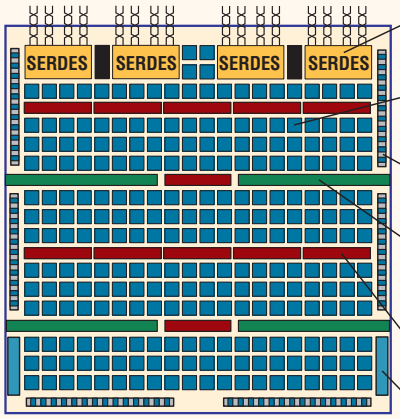
Pre-Engineered Source Synchronous Support implements DDR3 at 800Mbps, SPI4.2 at 750Mbps and generic interfaces up to 1Gbps.

sysDSP™ Blocks implement multipliers, adders, subtractors, accumulators.

sysMEM Embedded Block RAM (EBR) provides 18kbit dual port RAM.

sysCLOCK PLLs & DLLs for clock management.

LatticeSC™ Extreme Performance FPGA



Quad SERDES + Embedded PCS – each channel runs from 600Mbps to 3.8Gbps with 105mW power dissipation.

Programmable Function Unit (PFU) perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions.

Programmable I/O Cells (PICs) include PURESPEED™ buffers that support over 20 I/O standards.

Structured ASIC Block (MACO™) provides 50,000 usable gates for increased performance, density and lower power.

sysMEM™ Embedded Block RAM (EBR) provides 18kbit dual port RAM.

sysCLOCK™ PLLs & DLLs for clock management.

LatticeECP3 Features

- **Low Cost Digital SERDES**
  - Ideal for low cost chip-to-chip and small factor backplane applications
  - Exceeds XAUI Tx and Rx requirements
  - 1000BaseX Jitter Compliant
- **Up to 16 Channels per Device**
  - Useful for multi-port switching
- **Complete End-to-End Solution**
  - Soft XAUI PCS and 10GbE MAC implementations available
  - Soft SGMII and TS-MAC implementations available
- **Very Low SERDES Power (~110mW Per Channel Typical @ 3.2Gbps)**
- **Low Cost FPGA Fabric**
  - High end features at low cost

LatticeSC Features

- **High Performance Analog SERDES**
  - Exceeds XAUI TX and RX requirements
  - Ideal for long Ethernet-based backplanes
- **Up to 32 Channels per Device**
  - Useful for multi-port switching
- **Data Rates Up to 3.8 Gbps**
  - Exceeds XAUI baud rate specifications
- **Complete End-to-End Solution**
  - Rich PCS functionality
  - flexiMAC™ supports both GbE and 10GbE MACs, saves cost and power
  - Soft SGMII and TS-MAC implementation available
- **Very Low SERDES Power (105mW Per Channel Typical @ 3.125Gbps)**
- **Extreme Performance FPGA Fabric**
  - 500MHz block level performance

Intellectual Property: Rich Portfolio of Hard & Soft IP

Physical Coding Sub-Layer

XAUI PCS
Platform: ECP3
- Soft IP
- Compliant to IEEE802.3ae for XAUI
- Implements TX and RX State Machines
- XGMII Interface to FGPA Fabric

GbE & SGMII PCS
Platform: ECP3 ECP2M SC/M
- Soft IP
- Compliant to IEEE802.3z
- MAC or PHY Modes (Pin Selectable)
- RX and TX State Machines and Autonegotiation
- Rate Adaptation for 10/100 MII Frames
- 8-bit GMII MAC Interface

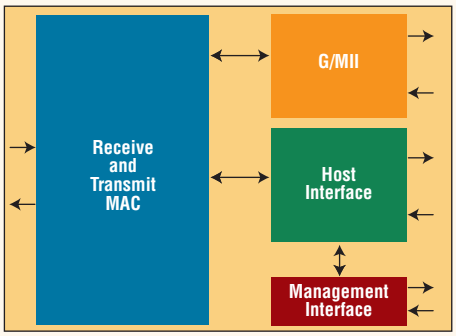
flexiPCS™
Platform: SCM
- Hard PCS Block
- Supports IEEE802.3ae XAUI and IEEE GbE PCS
- GMII (GbE) and XGMII Interfaces to FPGA Fabric

flexiPCS Multiprotocol PCS

Media Access Controllers

Tri-Speed MAC
Platform: ECP3 ECP2/M XP2 SC
- Soft IP
- 10/100/1000 Mbps Operation
- Compliant to IEEE 802.3z
- Generic FIFO Interface
- Programmable IPG
- TX and RX Statistics Vectors
- Multicast Address Filtering
- MII/GMII Interface
- Management Interface
- FCS on TX and RX
- Supports:
  - Full Duplex control with PAUSE frames
  - VLAN tagged frames
  - Automatic padding of short frames
  - Automatic re-transmission on collision
  - Broadcast and multicast frames
  - Jumbo packets (up to 8192 bytes)

TRI-SPEED MAC BLOCK DIAGRAM



10GbE MAC
Platform: ECP3 ECP2/M SC
- Soft IP
- Compliant to IEEE802.3ae-2002
- Optional HiGig/+ Capability for Broadcom StrataXGS I/II Switches (LatticeSC only)
- XAUI or XGMII Interface
- System Aide FIFO Interface
- Programmable IPG
- TX and RX Statistics Vectors
- Multicast Address Filtering
- MDIO Interface
- Supports:
  - Full duplex control with PAUSE frames
  - VLAN tagged frames
  - Automatic padding of short frames
  - FCS on TX and RX
  - Jumbo packets

flexiMAC
Platform: SCM
- Implemented on MACO Structured ASIC Technology
- Can be Configured as a 10G or 1G MAC
- Saves Up to 5K LUTs in FPGA Real Estate
- Low Power Implementation (100mW max)
- No IP Licensing Fees

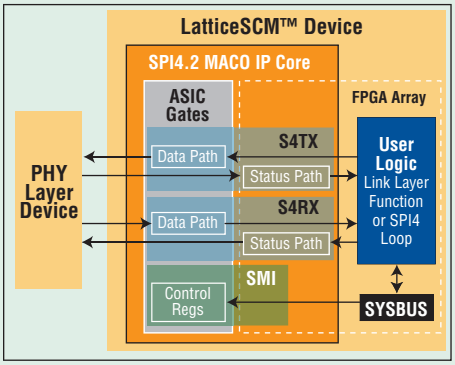
flexiMAC Multiprotocol Engine

2.5GbE MAC
Platform: SC
- Soft IP Bundle
- 10/100/1000 Mbps Operation
- Compliant to IEEE 802.3z
- Generic FIFO interface
- Programmable IPG
- TX and RX Statistics Vectors
- Multicast Address Filtering
- MII/GMII Interface
- Management Interface
- FCS on TX and RX
- Supports:
  - Full Duplex control with PAUSE frame
  - VLAN tagged frames
  - Automatic padding of short frames
  - Automatic re-transmission on collision
  - Broadcast and multicast frames
  - Jumbo packets

System Interfaces

MACO SPI4.2
Platform: SCM
- Implemented on MACO Structured ASIC Technology
- Very Low Power (0.85W)
- Saves 4K LUTs in FPGA LUTs
- Maximum 1Gbps Bandwidth
- No IP Licensing Fee

MACO SPI4.2 BLOCK DIAGRAM



Soft SPI4.2
Platform: ECP3 ECP2/M SC/M
- Industry Best Performance
  - High performance FPGAs: LatticeSC/M at 1Gbps with dynamic alignment
  - Industry best perfromance for low-cost FPGAs: LatticeECP3, ECP2/M (750Mbps with static alignment)
- Support for 256 Logic Channels
- Highly Configurable
  - Selectable 64/128b bus width
  - Run-time user controls for TX idles, packing and training patterns
  - Programmable internal FIFO thresholds
  - Variable minimum burst sizes
  - Variable packet sizes
  - Selectable status reporting (RAM or Transparent)

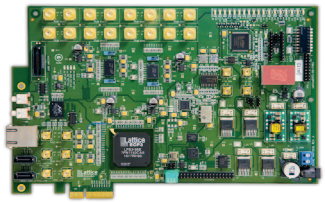
XAUI to SPI4.2 Fabric Interface
Platform: SCM
- Hard and Soft IP Bundle
- Bundle Includes:
  - No-charge Bridge Reference design with source code
  - SPI4.2 MACO (No IP licensing fee)
  - 10GbE MAC IP
- Optional HiGig+® Capability for Broadcom® StrataXGS® I/II Switches
- Single Instance Fits into LatticeSC15 Device
  - 17x17 256fpBGA – industry's smallest footprint (by 40%)
  - Lowest power SERDES at 3.125Gbps (105mW)
  - Lowest power SPI4.2 implementation (0.85W)
- Maximum Bandwidth of 12.5Gbps
- Tested with Broadcom StrataXGS Switches
- Lattice Developed and Supported

Development & Evaluation Systems

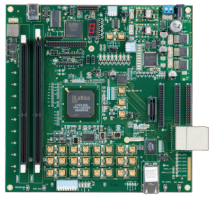
Lattice Ethernet Evaluation Platforms

	Board Name	Ethernet Interfaces	Other Interfaces	Memory Interfaces
LatticeECP3 Evaluation Platforms	Serial Protocol Board	• SMAs for SERDES (4 channels) • RJ-45	• PCIe x4 Edge Finger • SMAs for LVDS I/O	• DDR3 Component (8 bit) • DDR2 Component (18 bit)
	I/O Protocol Board	• SMAs for SERDES (4 channels) • RJ-45	• SPI4.2 Connector • SMAs for LVDS I/O	• DDR3 Memory Dual DIMM (64 bit) • DDR2 Component (18 bit)
LatticeECP2M™ Evaluation Platforms	PCI Express x4	• SMAs for SERDES (3 channels) • Breakout Card for RJ-45	• PCIe x4 Edge Finger • SMAs for LVDS I/O • BNC for SMPTE	• DDR2 Component (18 bit)
	SERDES Evaluation	• SMAs for SERDES (4 channels) • RJ-45 • SFP Optical Cage (SGMII)	• PCIe x1 Edge Finger	• DDR2 Component (18 bit)
LatticeSC Evaluation Platforms	Communications LFSC25-900	• SMAs for SERDES (8 channels) • SFI for MSA300 • Breakout Card for RJ-45	• SPI4.2 • SMAs for LVDS I/O	• DDR2 SODIMM (64 bit)
	PCI Express x4 LFSC80-1152	• SMAs for SERDES (4 channels) • Breakout Card for RJ-45	• PCIe x4 Edge Finger • SMAs for LVDS I/O	• DDR2 Component (18 bit)
	PCI Express x1 LFSC25-900	• SFP Optical Cage (SGMII) • RJ-45	• PCIe x1 Edge Finger • SMAs for LVDS I/O • SATA	• RLDRAM and QDR2 (18 bit)

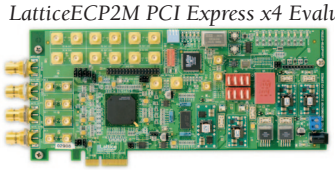
LatticeECP3 Serial Protocol Board



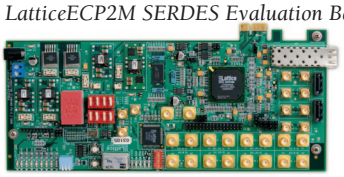
LatticeECP3 I/O Protocol Board



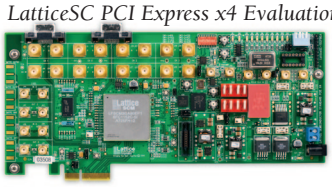
LatticeECP2M PCI Express x4 Evaluation Board



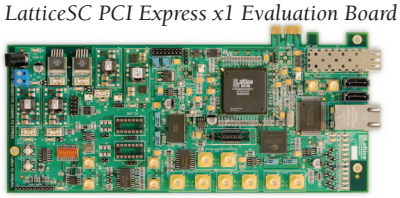
LatticeECP2M SERDES Evaluation Board



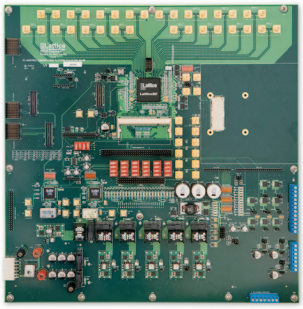
LatticeSC PCI Express x4 Evaluation Board



LatticeSC PCI Express x1 Evaluation Board



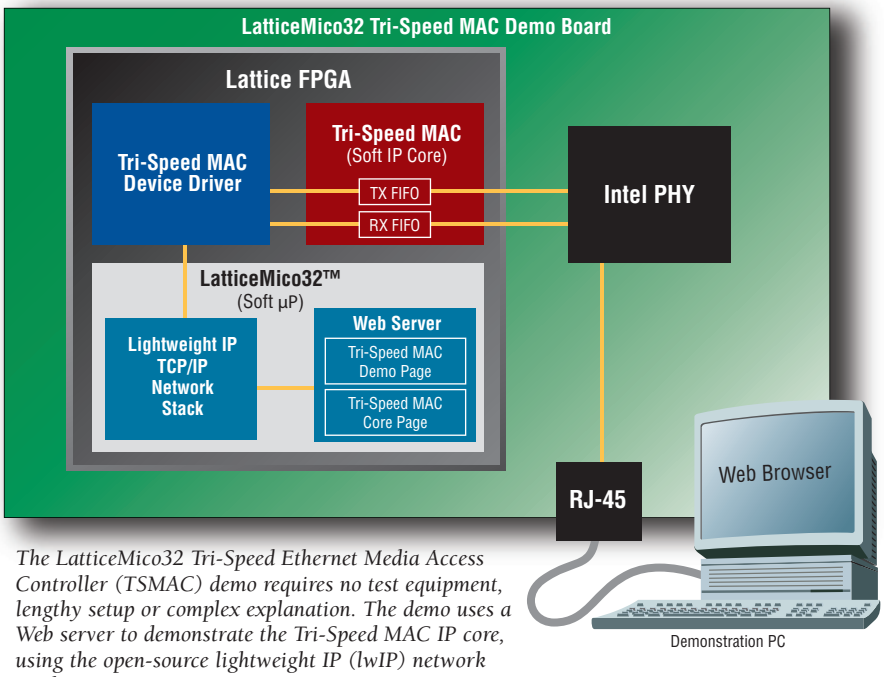
LatticeSC Communications Evaluation Board



Lattice Tri-Speed Ethernet MAC Development System

The LatticeMico32 Tri-Speed Ethernet Media Access Controller (TSMAC) demo shows the capability of the TSMAC IP core to function in a real network environment.

- Uses Lattice open source LatticeMico32 soft RISC processor
- Web server application
- Includes MAC device drivers and open source lightweight IP (lwIP) stack



The LatticeMico32 Tri-Speed Ethernet Media Access Controller (TSMAC) demo requires no test equipment, lengthy setup or complex explanation. The demo uses a Web server to demonstrate the Tri-Speed MAC IP core, using the open-source lightweight IP (lwIP) network stack.

Testing and Usability

Hardware Testing

Lattice tests all critical components of the Ethernet stack rigorously, and puts a great deal of emphasis on interoperability with proven 3rd party silicon platforms. The following test documentation is available for customer review.

PMA ELECTRICAL CHARACTERIZATION

See Lattice technical note TN1084 and supplements (available under NDA) for ANSI11.2 and IEEE802.3-2002 Electrical Tests for LatticeECP3, LatticeECP2M and LatticeSC SERDES.

INTEROPERABILITY

The following test and interoperability documentation is available for customer review:

Lattice Device Family	Ethernet Protocol	Marvell Alaska 88E1111/881112	Broadcom StrataXGS	PMC Sierra PM3388
LatticeECP3	1GbE PMA/PCS	✓	✓	
	SGMII PMA/PCS	✓		
LatticeSC	1GbE PMA/PCS	✓	✓	
	SGMII PMA/PCS	✓	✓	
	2.5GbE PMA/PCS		✓	
	XAUI PMA/PCS	✓	✓	
	HiGig+ PMA/PCS		✓	
	1GbE flexiMAC		✓	
	2.5GbE Soft MAC		✓	
	10GbE flexiMAC		✓	
	HiGig+ MAC		✓	
	SPI4.2			✓

Lattice IPexpress™ Tool

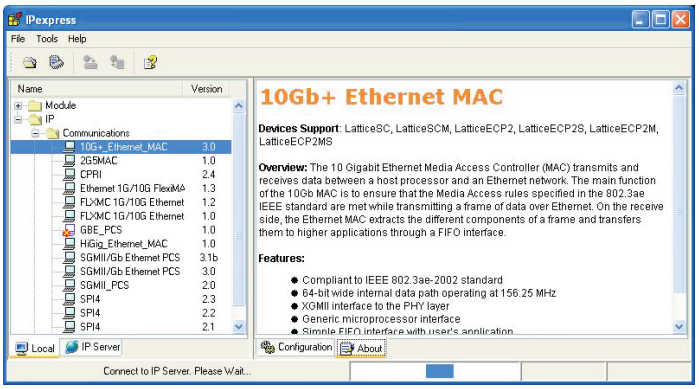
The IPexpress tool revolutionizes the way users design with Lattice IP cores and greatly simplifies IP design. The IPexpress design flow enables users to fully parameterize IP in real-time. The designer can then instantiate the user-configured IP and complete the design process, including full timing simulation and bitstream generation.

VIEW IP CORES AVAILABLE FOR DOWNLOAD

From the Lattice IP Server Tab within IPexpress, you can view available ispLeverCORE™ user-configurable IP cores for download.

INSTALL OR DOWNLOAD IP CORES

You can download and install ispLeverCORE user-configurable IP cores on your computer, or you can simply download them and install them later.



Lattice's IPexpress tool can be used to easily configure both MACO hard IP and Lattice's growing selection of soft IP cores.

Lattice Ethernet Portfolio Guide

	LatticeECP3	LatticeECP2™	LatticeXP2™	LatticeSC
PMA	• XAUI • GbE (1000BaseX) • XGMII • GMII/RGMII • MII/RMII	• XGMII • GMII/RGMII • MII/RMII	• GMII/RGMII • MII/RMII	• XAUI • HiGig+ • GbE (1000BaseX) • XGMII • GMII/RGMII • MII/RMII
Serial PCS	• Soft XAUI • Soft GbE • Soft SGMII			• Hard flexiPCS (GbE, 2.5GbE & XAUI) • Soft SGMII
MACs	• Soft 10GbE MAC • Soft Tri-Speed MAC (10/100/1000)			• Hard flexiMAC (1GbE & 10GbE) • Soft Tri-Speed MAC (10/100/1000) • Soft 2.5GbE MAC • Soft 10GbE MAC • Soft HiGig+ MAC
SPI4.2	• Soft SPI4.2			• Hard SPI4.2 on MACO & Soft SPI4.2
Reference Designs	• RGMII to GMII Bridge			• XAUI to SPI4.2 Bridge • HiGig+ to SPI4.2 Bridge • RGMII to GMII Bridge
Development Platforms	• Boards with SMA Connectors, SGMII Cage & RJ-45 Connectors • Interoperability Platforms • Processor based Demo with TCP/IP Stack • Reference Drivers	• Boards with RJ-45 Connectors • Processor based Demonstration with TCP/IP Stack • Reference Drivers		• Boards with SMA Connectors, SGMII Cage & RJ-45 Connectors • Interoperability Platforms • Processor based Demo with TCP/IP Stack • Reference Drivers

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