CMX90A006 2 W 860 – 930 MHz Linear PA

Description

The CMX90A006 is a two-stage linear RF power amplifier in QFN package, delivering +33 dBm of output power at 1 dB gain compression over the frequency range of 860 – 930 MHz, applicable to license-free bands.

Operating over a wide supply voltage range of 2.5 – 5.25 V to enable system level optimization and suitable for single cell Lithium batteries.

CMX90A006 is highly integrated for ease of use, reducing external component count and board space. The RF input is internally matched to 50 Ω, whilst the output match is implemented externally to optimize performance for each application.

The use of InGaP HBT process technology provides excellent reliability and balance between efficiency, gain and linearity. CMX90A006 is intended as a final stage ISM band PA in wireless applications.

Applications

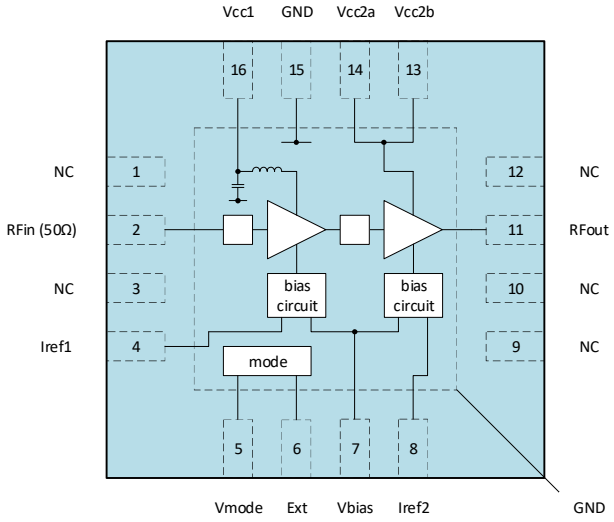
- UHF RFID readers
- Smart meters e.g. AMR / AMI
- Asset tracking
- Wireless modules
- IoT / M2M
- SRD / ISM bands (868 / 915 MHz)
- Lithium battery powered systems

4x4mm VQFN-16 Package

Product Features

- Frequency range 860 – 930 MHz
- Supply voltage 2.5 – 5.25 V
- P1dB +33 dBm @ 4.0 V
- OIP3 +42 dBm @ 26 dBm per tone
- RF input matched to 50 Ω
- Small signal gain 33 dB
- High PAE 52 % @ Psat
- Shut-down and output power control

Block Diagram



Ordering Information

Part Number	Description
CMX90A006Q7-R710	7” Reel with 1,000 pieces
CMX90A006Q7-R350	13” Reel with 5,000 pieces
EV90A006	Evaluation board

Absolute Maximum Ratings

Parameter	Rating
RF Input Power	+13 dBm
Device Voltage (Vcc1, Vcc2)	+5.5 V
Case Temperature (Tc)	-40 to +85 °C
Junction Temperature (Tjmax)	147 °C (MTTF = 10^6 hours)
Storage Temperature	-40 to +125 °C
ESD Sensitivity	HBM >500 V (Class 1B); CDM >1000 V (Class C3)
MSL Level	Level 3

Exceeding the maximum ratings may result in damage or reduced device reliability.

Thermal Characteristics

Parameter	Rating
Thermal Resistance (Rjc)	22 °C/W

Thermal resistance is junction-to-case, where case refers to the exposed die pad on the backside which is in contact with the board.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Operating Frequency Range	860		930	MHz
Quiescent Current (Icq)		206		mA
Case Temperature (Tc)	-40		+85	°C
Device Voltage (Vcc1, Vcc2)	2.5	4.0	5.25	V
Bias Voltage (Vbias)	2.5	4.0	5.25	V
Iref1 Current		4.1	15.0	mA
Iref2 Current		4.7	15.0	mA

The device will be tested under certain conditions, but performance is not guaranteed over the full range of recommended operating conditions.

ESD Caution

CMX90A006 incorporates ESD protection circuitry. However, ESD precautions are strongly recommended for handling and assembly. Ensure that devices are protected from ESD in antistatic bags or carriers when being transported. Personal grounding is to be worn at all times when handling these devices.

RoHS Compliance

All devices supplied by CML Micro are compliant with RoHS directive (2011/65/EU), containing less than the permitted levels of hazardous substances.

Electrical Specification

Measured results on the EV90A006 evaluation board including PCB losses.

Zo = 50 Ω, Vcc = Vbias = +4 V, Vref = +4V (Vref = Vref1 = Vref2), High Gain Mode, Ta = +25 °C (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Frequency		860		930	MHz
P1dB			33		dBm
Psat			33.5		dBm
Small Signal Gain	Pin = -20 dBm		33		dB
PAE	900 MHz, Psat		52		%
OIP3	900 MHz, Pout = +26 dBm/tone		42		dBm
Current Consumption (Icc)	900 MHz, Psat		1.1		A
Input Return Loss	Pin = -20 dBm		-20		dB
Output Return Loss	Pin = -20 dBm		-10		dB
2Fo	900 MHz, P1dB		-35		dBc
3Fo	900 MHz, P1dB		-75		dBc
Ruggedness	Psat, all phase angles, Vcc = Vbias = 5 V		>10:1		
Quiescent Current (Icq)	RF OFF		206		mA
Standby Current	Vcc current in standby mode, RF OFF		< 1		uA
Vbias Current	RF OFF		5.5		mA
Vbias Current	Pout = P1dB		12		mA
Vref1, 2 (Standby)	PA placed into standby mode	0		1.5	V
Vref Current	Vref1 & 2 total current. See applications section for further details.		8.8		mA
Turn-On Time	Vref = 0 V to 4 V		TBD		ns
Turn-Off Time	Vref = 4 V to 0 V		TBD		ns

Pin Assignments

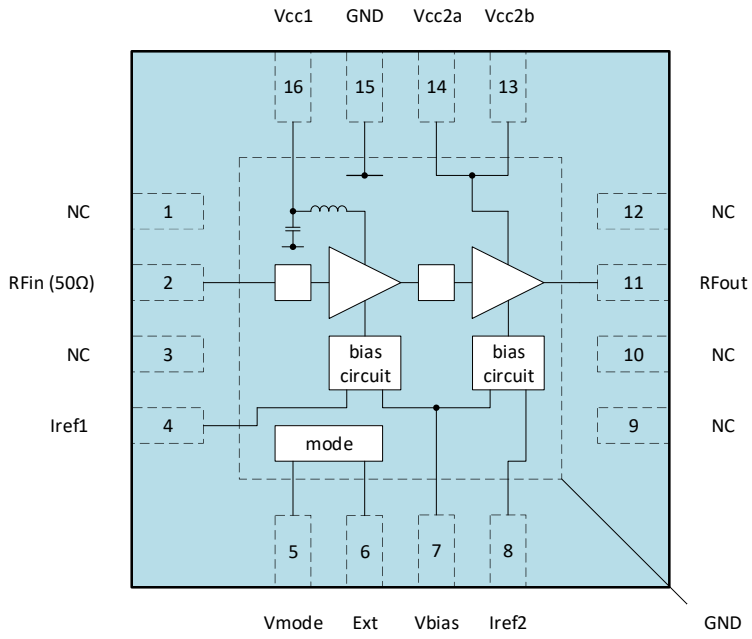


Figure 1 - Top View

Pin	Name	Description
1	NC	Connect to GND
2	RFin	RF input. Internally matched to 50 Ω. An external DC-blocking capacitor is required.
3	NC	Connect to GND
4	Iref1	Sets bias current to driver stage. Regulated voltage and external series resistor required. Also used for on/off and power control.
5	Vmode	Control device input
6	Ext	Control device output
7	Vbias	Supplies bias current to both bias circuits.
8	Iref2	Sets bias current to final stage. Regulated voltage and external series resistor required. Also used for on/off and power control.
9	NC	Connect to GND
10	NC	Connect to GND
11	RFout	RF output. External matching to 50 Ω and DC-blocking capacitor required.
12	NC	Connect to GND
13	Vcc2b	Collector supply to final stage
14	Vcc2a	Collector supply to final stage
15	GND	Connect to GND
16	Vcc1	Collector supply to driver stage with integrated RF choke
Die pad	GND	DC and RF ground. Exposed die pad must be connected to GND.

Notes

CML recommends that all no connect (NC) pins are connected to ground.

The bottom exposed die pad must be connected to the ground plane on the board, note guidance given in the application information section.

Typical Performance

The following plots show typical performance characteristics of CMX90A006 measured on the evaluation board (Part Number - EV90A006).

Test conditions unless otherwise noted:-

Vcc = Vbias = +4.0 V, Vref = +4.0 V, Ta = +25 °C, Zo = 50 Ω.

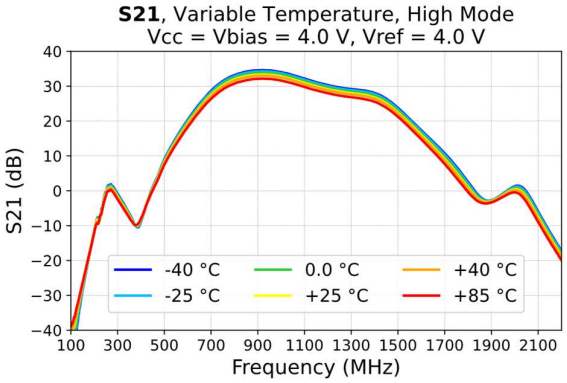


Figure 2 - Small Signal Gain (S21)

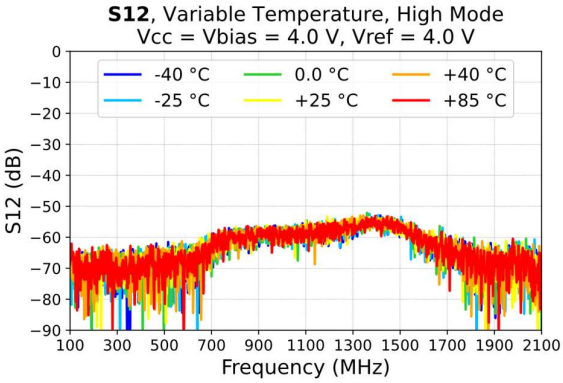


Figure 3 - Reverse Isolation (S12)

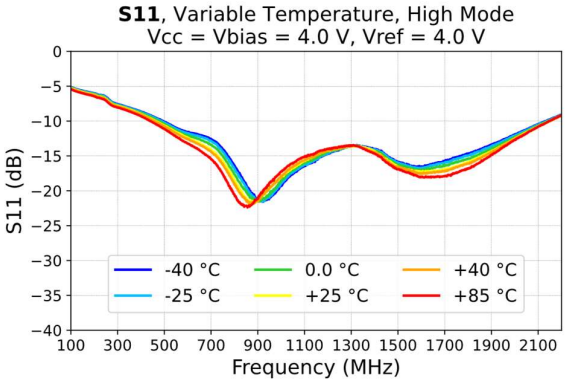


Figure 4 - Input Return Loss (S11)

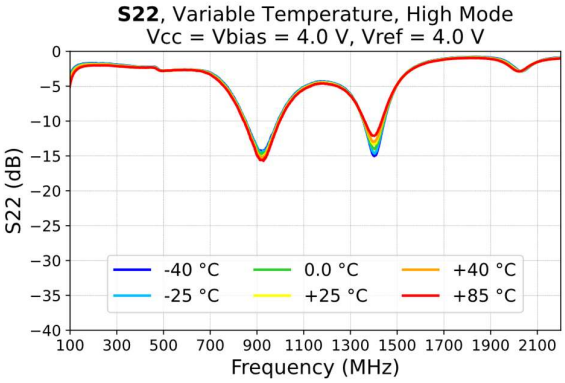


Figure 5 - Output Return Loss (S22)

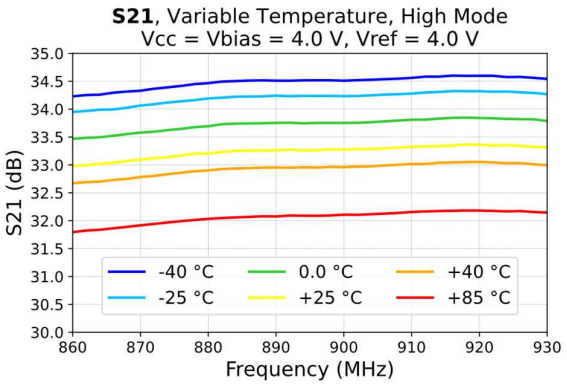


Figure 6 - Small Signal Gain (S21)

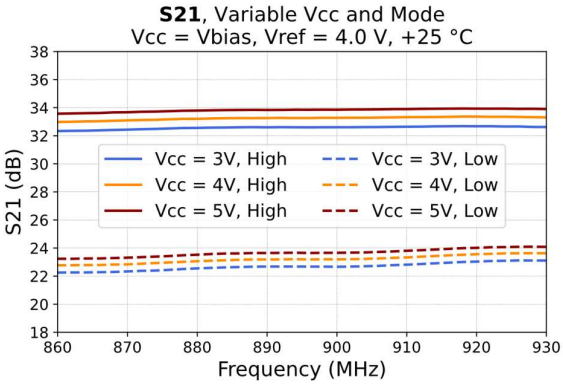


Figure 7 - Small Signal Gain (Low and High Modes)

Test conditions unless otherwise noted:-
Vcc = Vbias = +4.0 V, Vref = +4.0 V, Ta = +25 °C, Zo = 50 Ω.

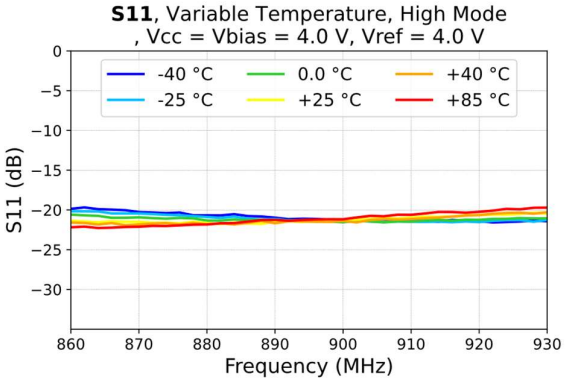


Figure 8 - Input Return Loss (S11)

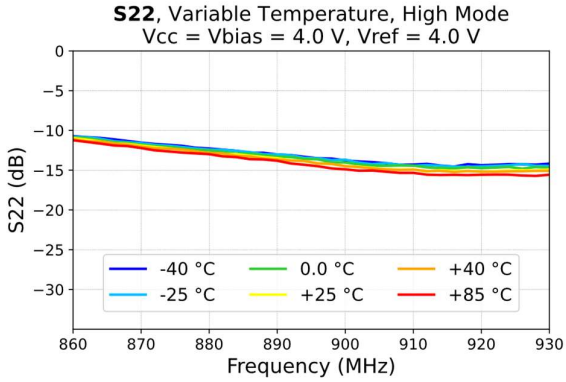


Figure 9 - Output Return Loss (S22)

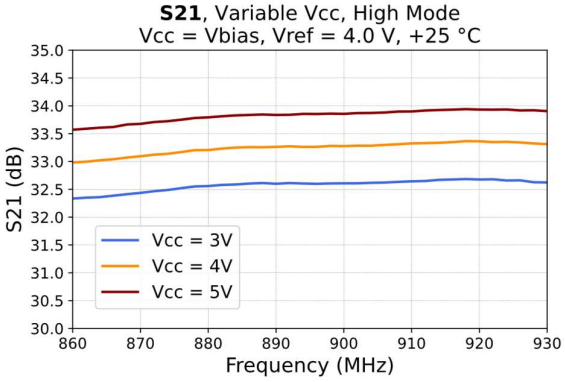


Figure 10 - Small Signal Gain vs. Vcc

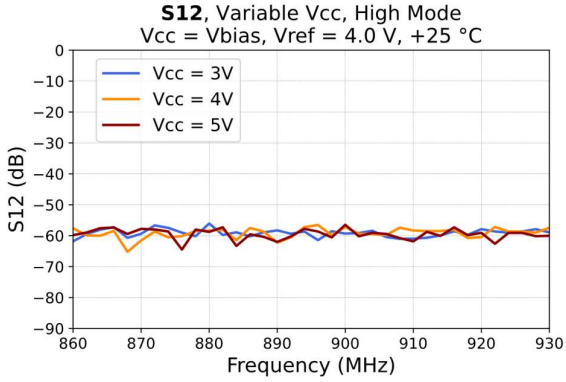


Figure 11 - Reverse Isolation vs. Vcc

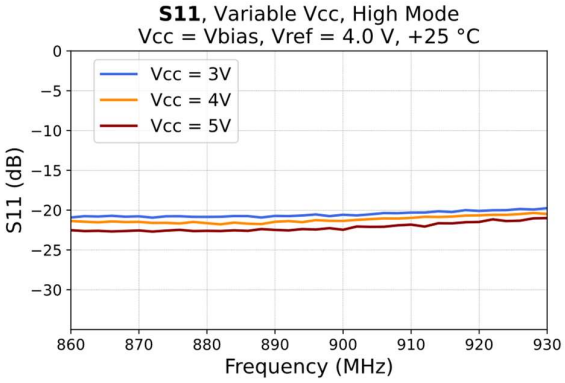


Figure 12 - Input Return Loss vs. Vcc

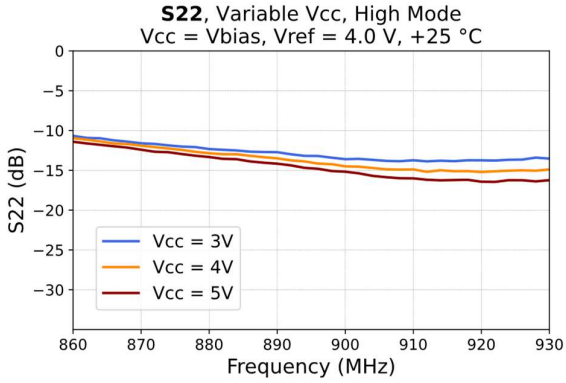


Figure 13 - Output Return Loss vs. Vcc

Test conditions unless otherwise noted:-
Vcc = Vbias = +4.0 V, Vref = +4.0 V, Ta = +25 °C, Zo = 50 Ω.

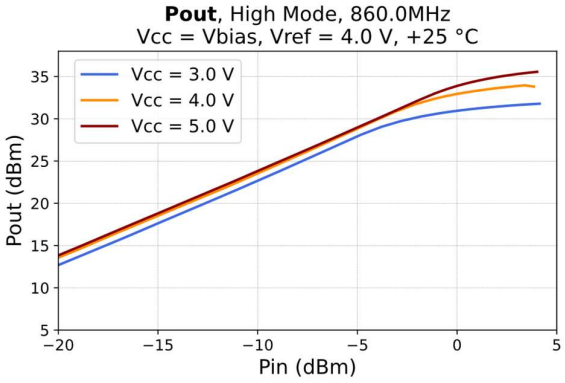


Figure 14 - Output Power vs. Input Power at 860 MHz

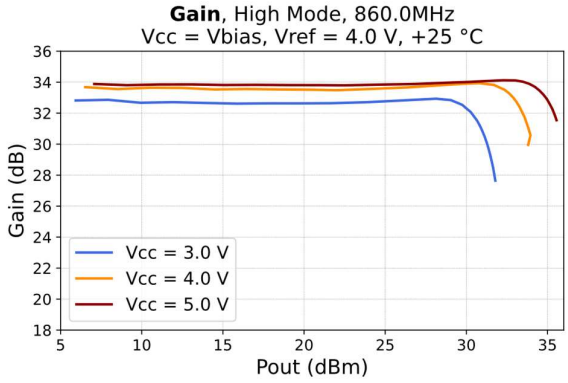


Figure 15 - Gain vs. Output Power at 860 MHz

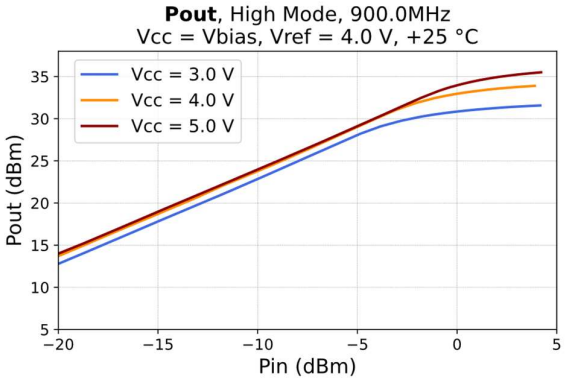


Figure 16 - Output Power vs. Input Power at 900 MHz

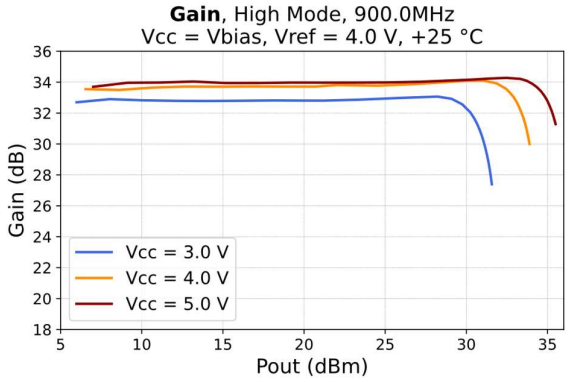


Figure 17 - Gain vs. Output Power at 900 MHz

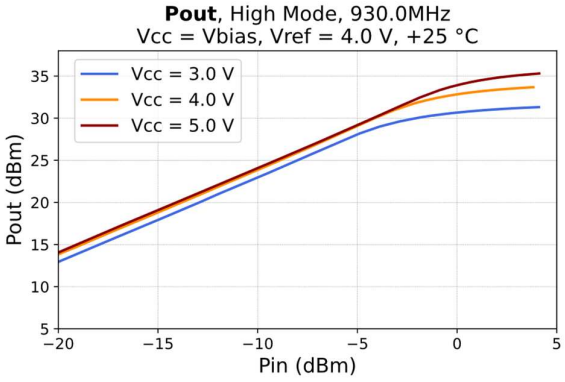


Figure 18 - Output Power vs. Input Power at 930 MHz

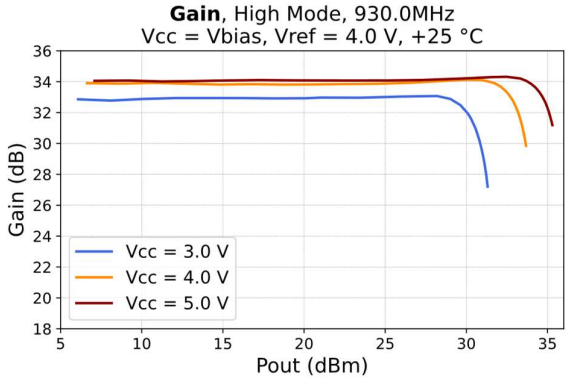


Figure 19 - Gain vs. Output Power at 930 MHz

Test conditions unless otherwise noted:-
Vcc = Vbias = +4.0 V, Vref = +4.0 V, Ta = +25 °C, Zo = 50 Ω.

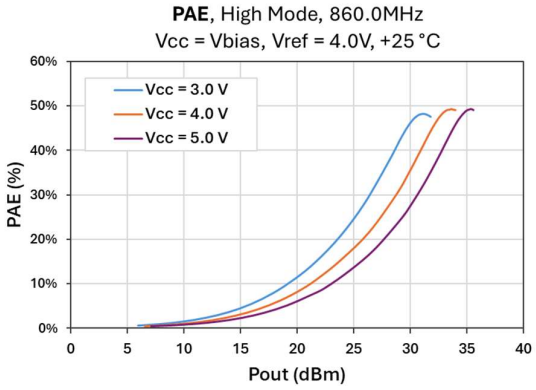


Figure 20 - PAE vs. Output Power at 860 MHz

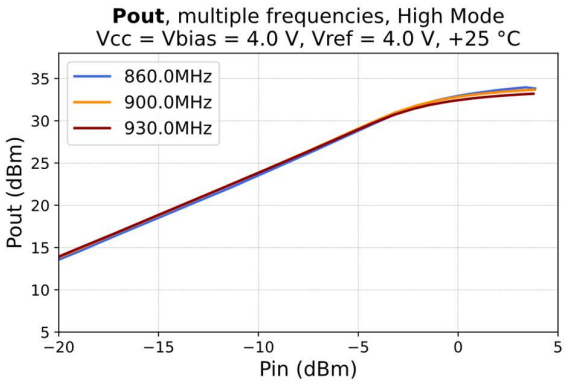


Figure 21 - Output Power vs. Input Power

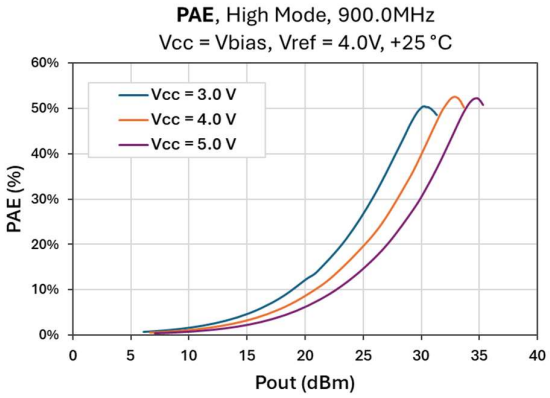


Figure 22 - PAE vs. Output Power at 900 MHz

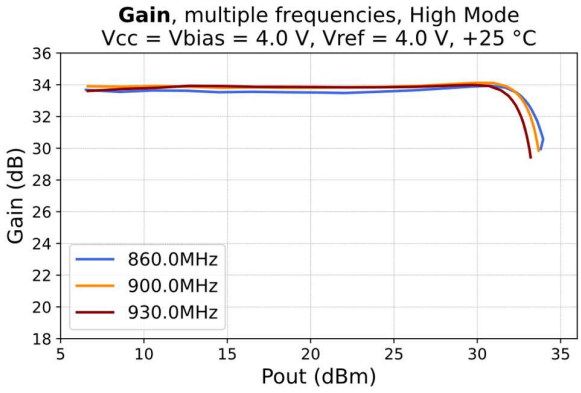


Figure 23 - Gain vs. Output Power

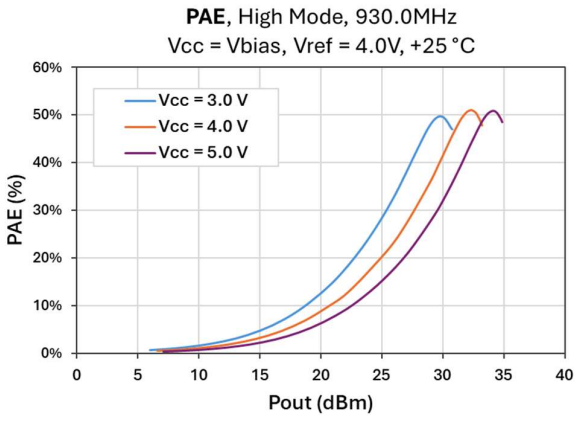


Figure 24 - PAE vs. Output Power at 930 MHz

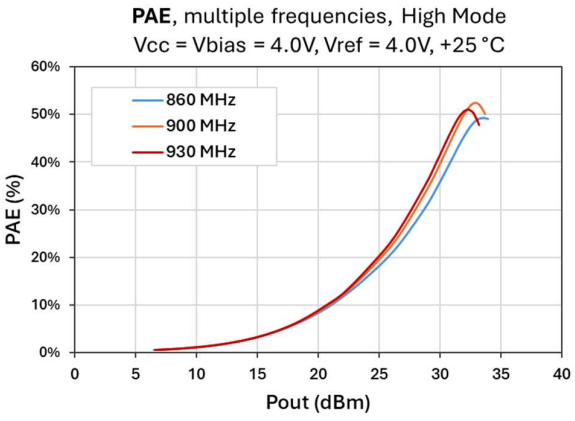


Figure 25 - PAE vs. Output Power

Test conditions unless otherwise noted:-
Vcc = Vbias = +4.0 V, Vref = +4.0 V, Ta = +25 °C, Zo = 50 Ω.

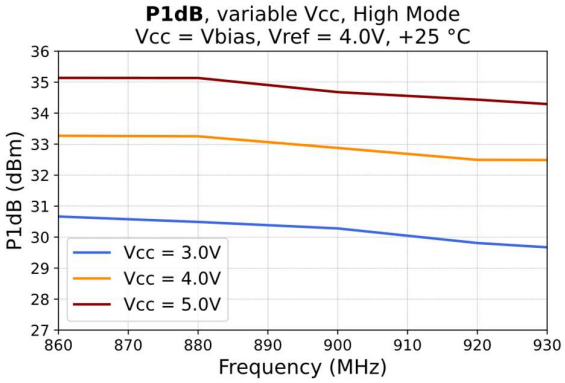


Figure 26 - P1dB vs. Frequency

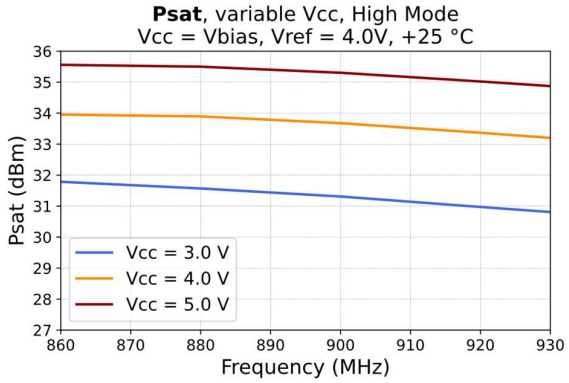


Figure 27 - Psat vs. Frequency

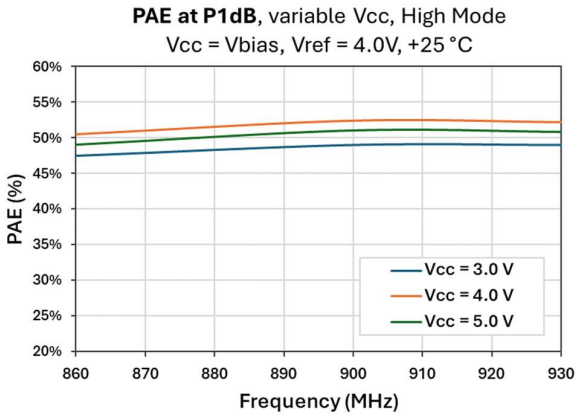


Figure 28 - PAE at P1dB

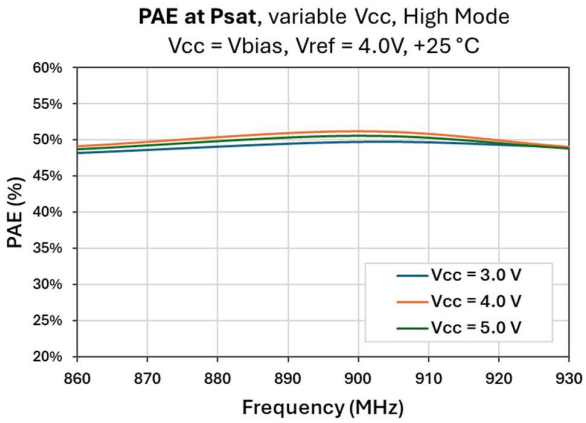


Figure 29 - PAE at Psat

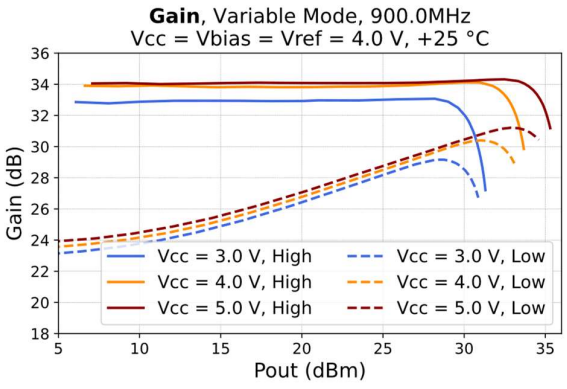


Figure 30 - Gain vs. Pout at 900 MHz (Low and High Modes)

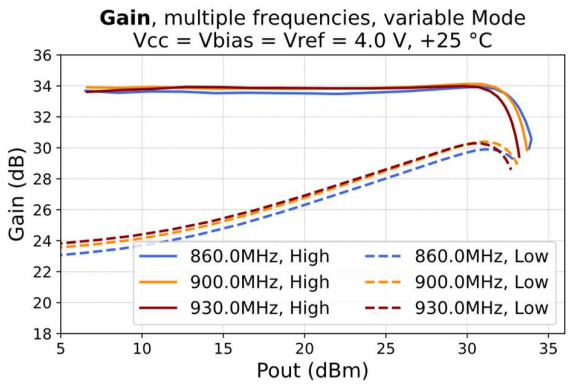


Figure 31 - Gain vs. Pout (Low and High Modes)

Test conditions unless otherwise noted:-
Vcc = Vbias = +4.0 V, Vref = +4.0 V, Ta = +25 °C, Zo = 50 Ω.

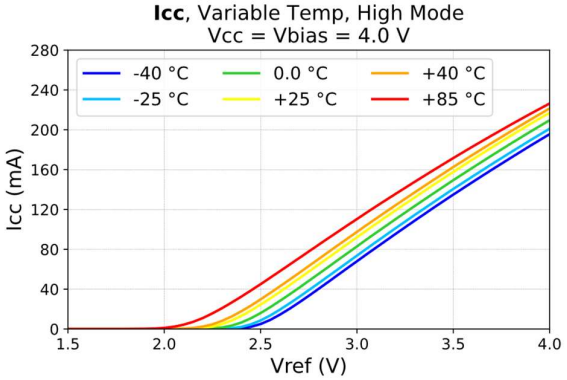


Figure 32 - Icc vs. Vref over Temp

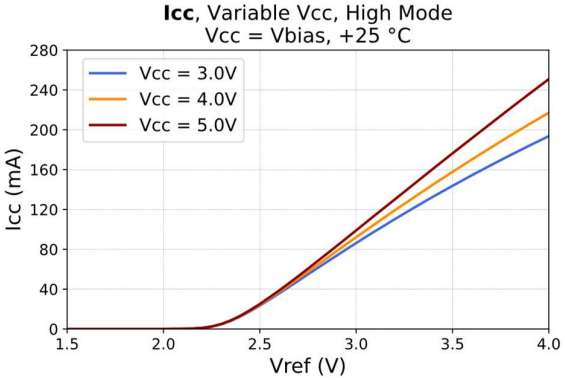


Figure 33 - Icc vs. Vref over Vcc

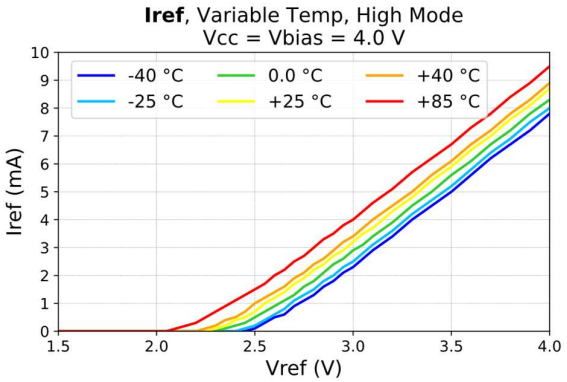


Figure 34 - Iref vs. Vref over Temp

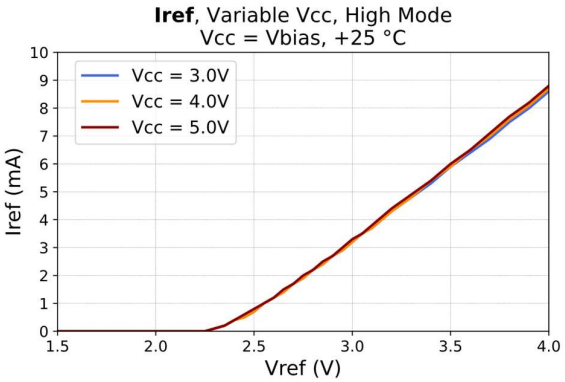


Figure 35 - Iref vs. Vref over Vcc

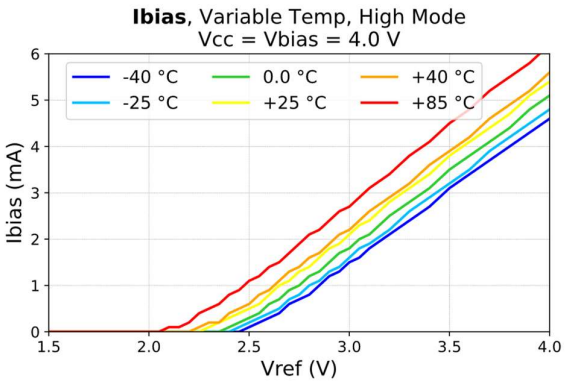


Figure 36 - Ibias vs. Vref over Temp

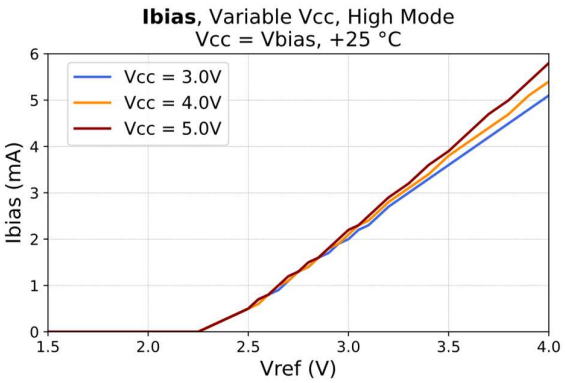


Figure 37 - Ibias vs. Vref over Vcc

Test conditions unless otherwise noted:-
Vcc = Vbias = +4.0 V, Vref = +4.0 V, Ta = +25 °C, Zo = 50 Ω.

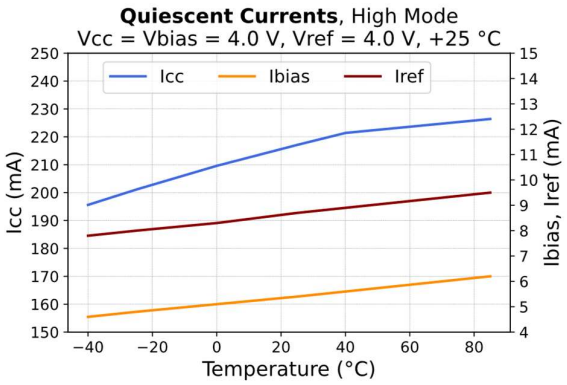


Figure 38 - Idle Currents vs. Temp

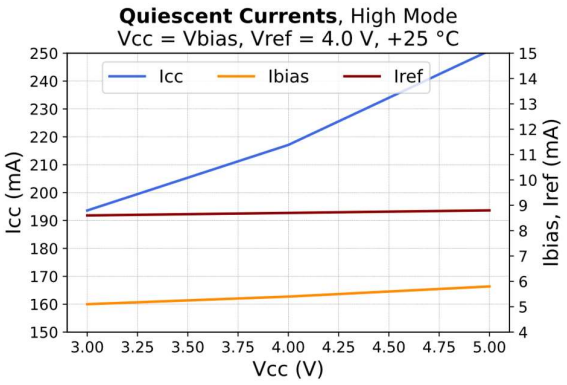


Figure 39 - Idle Currents vs. Vcc

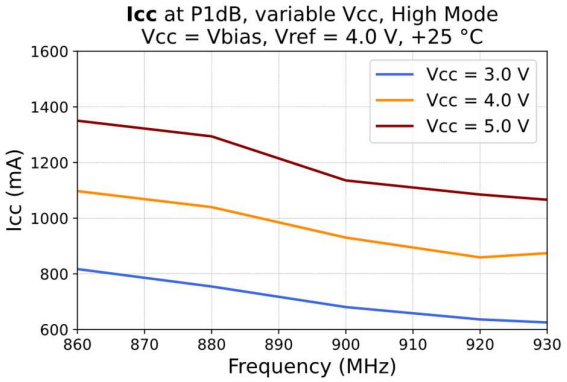


Figure 40 - Icc at P1dB

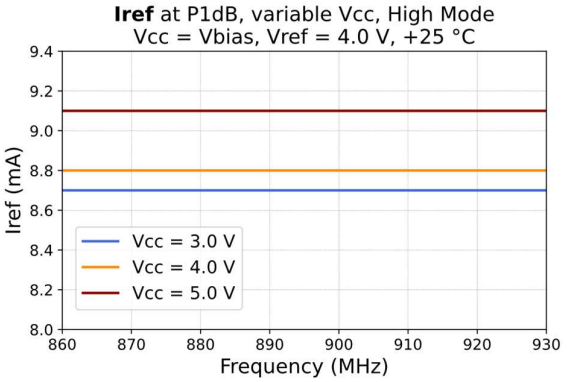


Figure 41 - Iref at P1dB

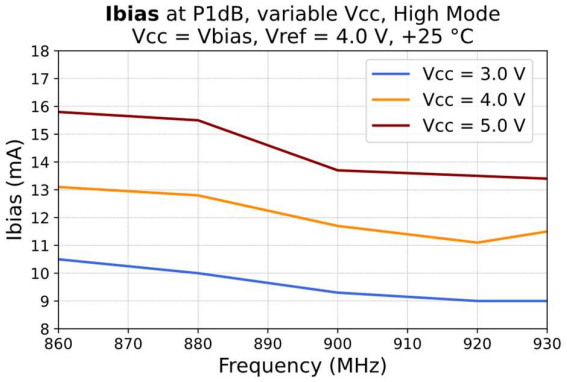


Figure 42 - Ibias at P1dB

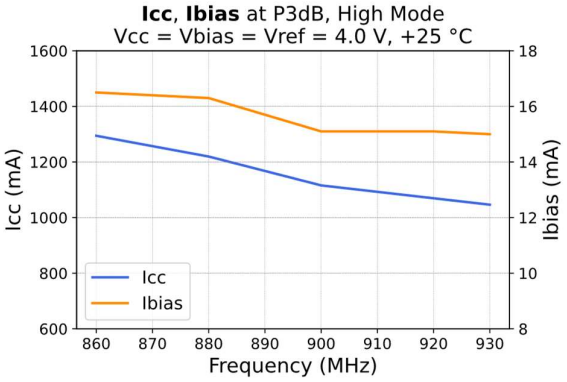


Figure 43 - Icc and Ibias at P3dB

Test conditions unless otherwise noted:-
Vcc = Vbias = +4.0 V, Vref = +4.0 V, Ta = +25 °C, Zo = 50 Ω.

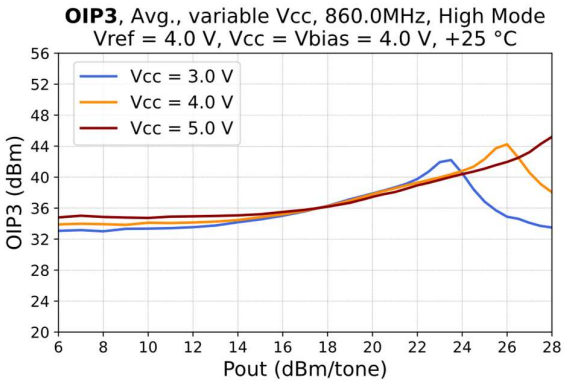


Figure 44 - OIP3 vs. Pout at 860 MHz

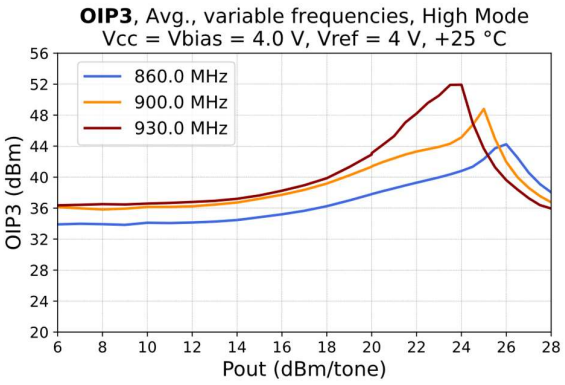


Figure 45 - OIP3 vs. Pout

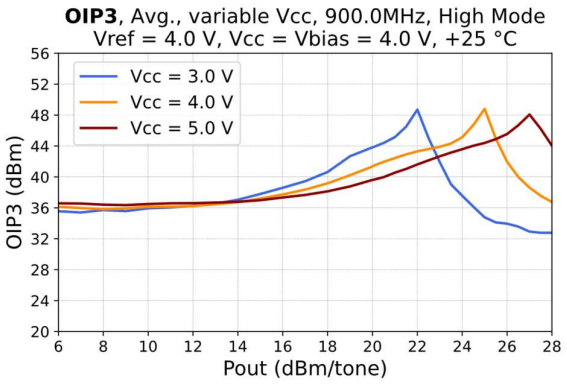


Figure 46 - OIP3 vs. Pout at 900 MHz

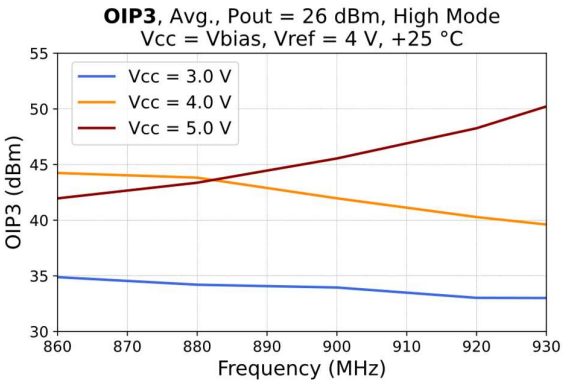


Figure 47 - OIP3 vs. Frequency at Pout = 26 dBm/tone

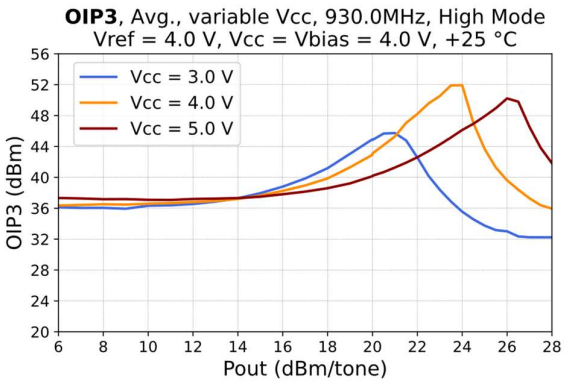


Figure 48 - OIP3 vs. Pout at 930 MHz

Test conditions unless otherwise noted:-
Vcc = Vbias = +4.0 V, Vref = +4.0 V, Ta = +25 °C, Zo = 50 Ω.

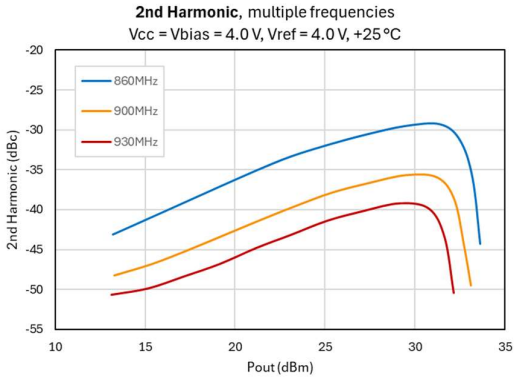


Figure 49 - Second Harmonic vs. Pout

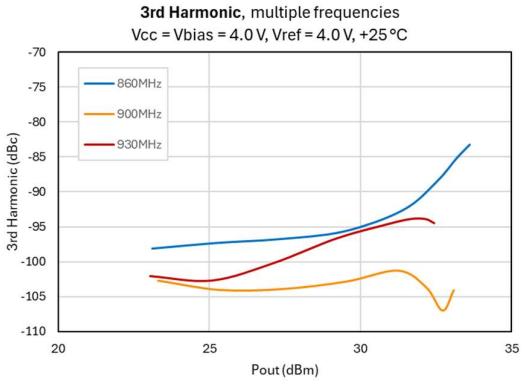


Figure 50 - Third Harmonic vs. Pout

Application Information

Schematic Diagram

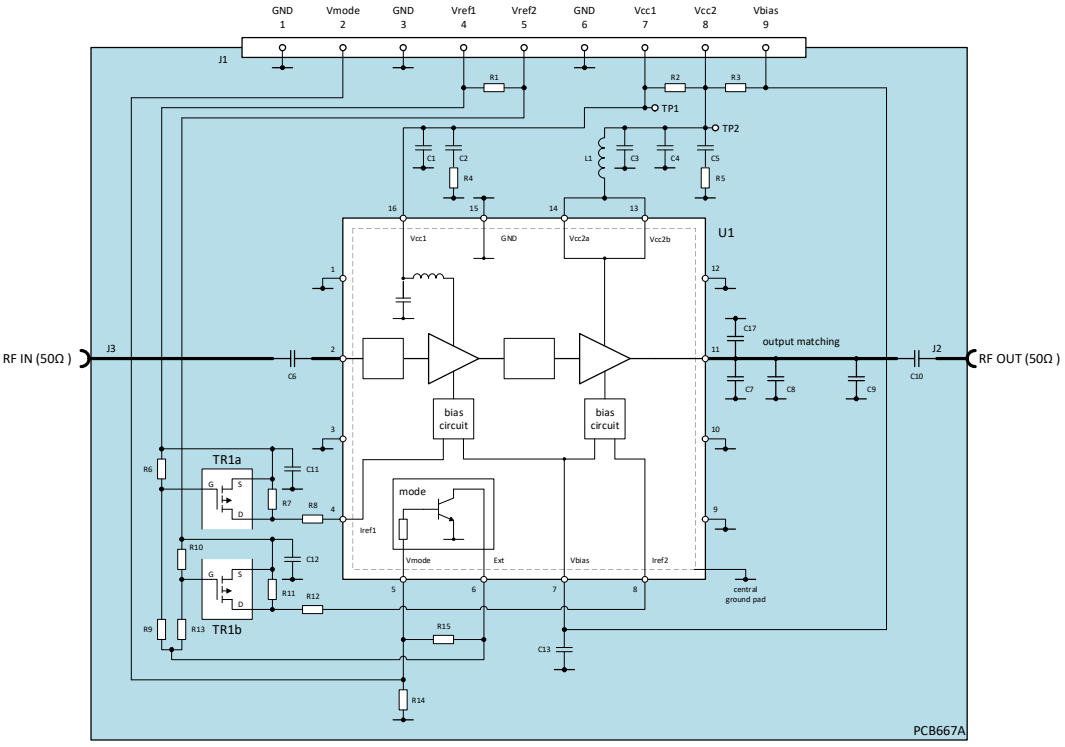


Figure 51 - EV90A006 Schematic

Bill Of Materials (BOM)

Reference Designator	Value	Size	Description
C1, C4, C11, C12	10 nF	0402	X7R, 16 V, +/-10 %
C2	DNF	0603	
C3	47 pF	0402	COG, 25 V, +/-5 %
C5, C13	10 uF	0603	X5R, 10 V, +/-10 %
C6, C10	100 pF	0402	COG, 25 V, +/-5%
C7, C17	8pF	0402	COG, 50 V, +/-0.1pF
C8	5.6pF	0402	COG, 50 V, +/-0.1pF
C9	5.1pF	0402	COG, 50 V, +/-0.1pF
L1	15nH	0603	Coilcraft: 0603AF-15NXJR, +/-5%
R1, R2, R3, R15	DNF	0402	
R4	DNF	0603	
R5	1R0	0602	0.1 W, +/-1%
R6, R10, R14	100k	0402	0.063 W, +/-1%
R7, R11	1k1	0402	0.063 W, +/-1%
R8	357R	0402	0.063 W, +/-1%
R9, R13	82k	0402	0.063 W, +/-1%
R12	316R	0402	0.063 W, +/-1%
TR1	ONSemi: NTZD3152P dual p-channel MOSFET		
U1	CMX90A006Q7		
J1	9-way 0.1” pin header		
J2, J3	Molex: 73251-1150		

Note:
DNF = Do Not Fit

PCB Layout

Careful layout of the printed circuit board (PCB) is essential for stable RF and good thermal performance. The recommended layout, including the ground via pattern underneath the device, may be taken from the evaluation board (Part Number EV90A006). See the following section for recommendations on best thermal and RF design.

The PCB consists of four-layer FR-4 with a total thickness of 1.592 mm (Figure 52) and the EV90A006 PCB (Figure 53) is 50 mm x 50 mm. The microstrip RF input and output width is 0.38 mm.

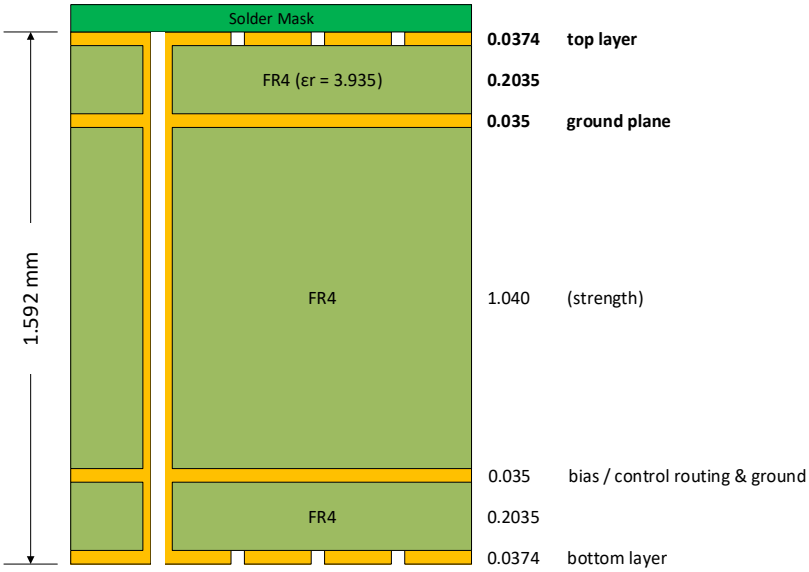


Figure 52 - EV90A006 PCB Layer Stack

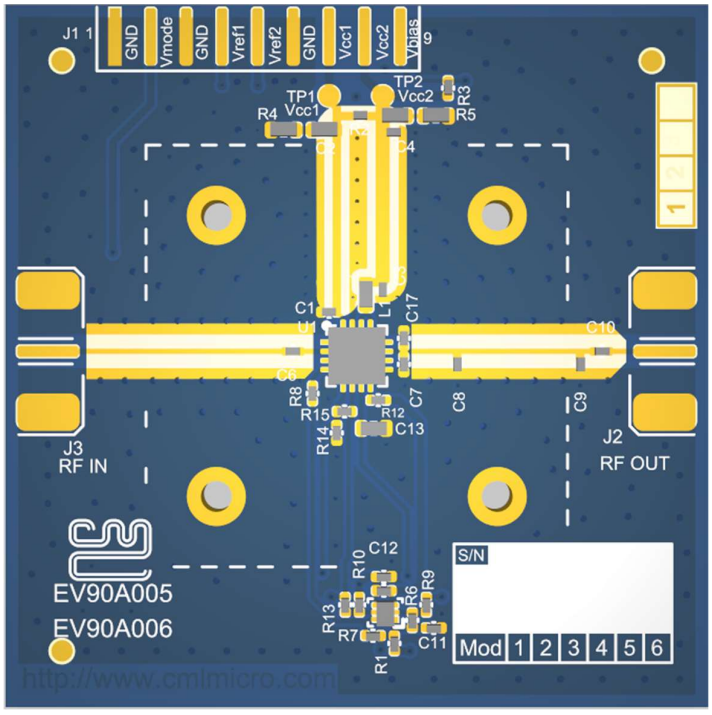


Figure 53 - EV90A006 PCB Top Layer View

Thermal and Stability Design

The primary RF/DC ground and thermal path is via the exposed die pad on the backside of the package, which must be connected to the PCB ground plane. An array of plated through-hole vias directly underneath the die pad area is essential to conduct heat away and minimise ground inductance. A typical solution should have 9 grounding vias connecting the top layer to the bottom layer, with inner diameter of 0.2 mm (and 0.025 mm plating) on a 0.9 mm grid pattern. The vias do not need to be filled. The PCB layout should provide a thermal radiator appropriate for the intended operation, adding as much copper to inner and outer layers as possible to avoid excessive junction temperature.

Device junction temperature (Tj) can be calculated using Tj = Tc + (Pdiss x Rjc) where Pdiss = Pdc + Pin - Pout and Tc is the case temperature on the backside of the package (die pad) in contact with the PCB.

A heatsink should be used if the thermal performance of the PCB layout is not adequate and particularly if the user is running the device continuous at high output power. The heatsink should be attached to the rear of the PCB using mounting screws positioned close to the device to ensure good contact with the ground via pattern. The backside of the PCB is clear of solder resist to enable a heatsink to be applied and it is recommended to use thermal grease to ensure good contact between the PCB and the heatsink.

A low inductance connection as described between the central ground pad and the board RF ground plane prevents unwanted gain peaking and instability due to internal ground path feedback.

RFin & RFout Matching

The CMX90A006 RFin (pin 2) is internally matched to 50 Ω and just requires a DC blocking capacitor (C6 on EV90A006).

The RFout (pin 11) requires matching to 50 ohms. At 900 MHz, the target impedance the matching circuit should present to the device is 3.42-j0.42. The matching network on EV90A006 consists of three sections that step up this impedance to 50 Ω. These are formed from lengths of 50 Ω impedance transmission line and shunt capacitors. The three sections are TL1 & C7//C17, TL2 & C8 and TL3 & C9 (Figure 54). From this point the impedance is 50 Ω to the output via a DC blocking capacitor (C10).

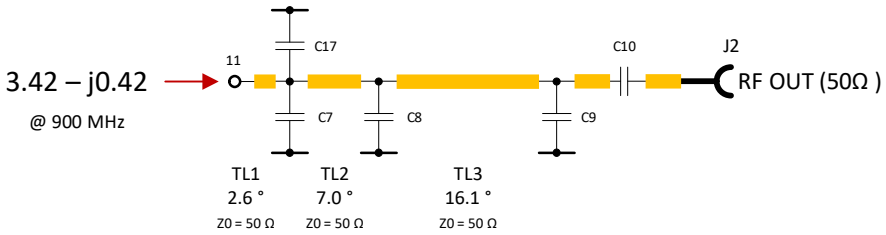


Figure 54 – Diagram of the EV90A006 Output Matching Network

Vcc1 & Vcc2 Pins

Vcc1 provides the collector supply to stage 1 with integrated RF choke, internal RF decoupling and ESD protection diodes. Vcc2a & Vcc2b are internally connected and should be externally connected together to provide a low resistance path for the collector supply to stage 2. An external inductor (L1) capable of carrying the DC current under all operating conditions and associated RF decoupling is required. No internal ESD protection is possible on these pins as they are RF hot.

Vbias Pin

The Vbias pin provides the supply to the internal bias circuits and the associated base current to the two amplifier stages. To consolidate power supplies the Vbias pin can be connected to Vcc without affecting the performance of the device. This pin is protected by ESD diodes.

Iref1 & Iref2 Pins

The quiescent bias current of each stage is proportional to the current into the associated Iref pin. This current is set by a series resistor from the Vref regulated supply. These resistors are 357 Ω (R8, Iref1) and 316 Ω (R12, Iref2) on the EV90A006, resulting in the following currents with Vref = 4 V:

Iref1 = (Vref1 – (2 x Vbe)) / (Rext + Rint)

Current into Iref1 = (4 – (2 x 1.237)) / (357 + 24) = 4.1 mA, Resulting in a typical Icq1 of 29 mA.

Current into Iref2 = (4 – (2 x 1.233)) / (316 + 13) = 4.7 mA, Resulting in a typical Icq2 of 177 mA.

These bias points have been selected for optimum PA efficiency. It is possible to achieve these same currents from higher or lower Vref supplies by appropriate selection of the series resistors. To ensure correct bias circuit operation the current into either Iref1 or Iref2 should not exceed 15 mA. These pins are protected by ESD diodes.

EV90A006 Mode Switching

The EV90A006 has additional switches TR1a and TR1b. When these are closed, the board is in normal 'High mode' with the quiescent currents set by R8 and R12 as above. When they are open, the board is in 'Low mode' with quiescent currents set by R7 + R8 and R11 + R12 resulting in lower quiescent current and 10 dB reduction in small-signal gain:

Current into Iref1 = (4 – (2 x 1.209)) / (1100 + 357 + 24) = 1.07 mA, Resulting in a typical Icq1 of 8.4 mA.

Current into Iref2 = (4 – (2 x 1.193)) / (1100 + 316 + 13) = 1.13 mA, Resulting in a typical Icq2 of 51.1 mA.

The two external switches are controlled via the mode switch integral to the CMX90A006. This allows easy control from a low voltage, low current source. The operating mode is selected according to the following table:

Vmode	Gain Mode (small-signal)	Typical Quiescent Current (Icq1 + Icq2)	Comments
2 V	High Gain	206 mA	Normal operating mode
0 V	Low Gain	59.5 mA	Small-signal gain reduced by 10dB

Standby Mode

The EV90A006 can be put into standby mode by setting Vref (Vref1 and Vref2) low (<1.5V) to disable the bias circuits. The total Vref current in High mode is ~ 8.8 mA from 4 V. If a lower control voltage or control current is required, the Vmode input can be used by removing R7 and R11 from the board. The mode switch now operates to enable the EV90A006:

Vmode	Gain Mode (small-signal)	Typical Quiescent Current (Icq1 + Icq2)	Comments
2 V	High Gain	206 mA	Normal operating mode
0 V	Standby	< 1 µA	Standby mode

Mode Switch

The CMX90A006 includes an independent transistor switch that can be used for various purposes. The EV90A006 board uses it to control the gain mode as described above. This transistor is configured as shown below with ESD protection and a series resistor to the transistor base. The Vbe of the transistor is ~ 1.2 V and is therefore compatible with CMOS input levels. For higher voltage control, an external series resistor can be used to limit the current and protect the Vmode input ESD diodes (pin 5) by keeping the voltage at pin 5 around 2 V. For example, a 39 kΩ series resistor can be used from a 5 V control.

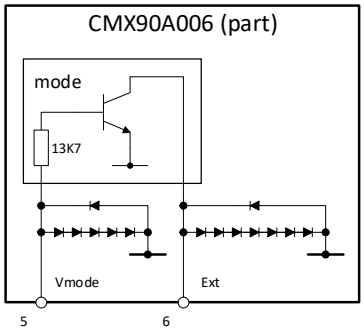


Figure 55 – Vmode Pin Internal Configuration

Power Ramping

Vref can also be used to ramp the CMX90A006 output power up or down to support burst signals and TDD systems. By varying Vref between 1.5 V and 4 V (typ.) the output power can be adjusted by more than >75 dB (Figure 56).

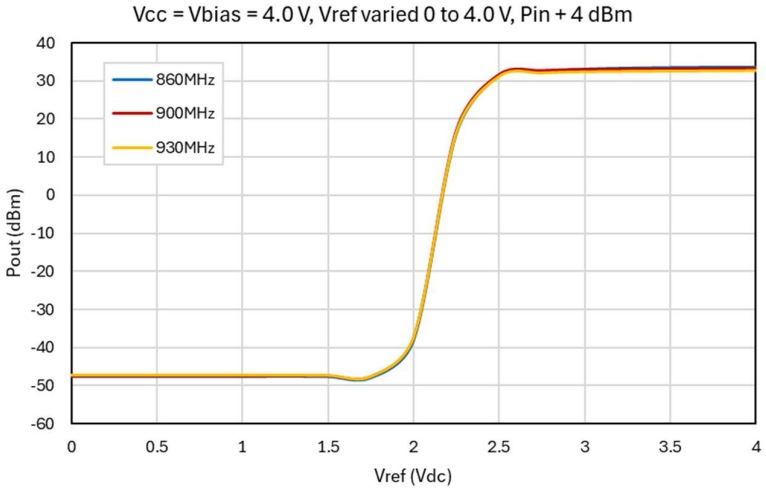


Figure 56 - Vref Power Control

Evaluation Board and Bias Procedure

Ensure an adequately rated attenuator is placed between the output of the amplifier (RFout) and 50 Ω RF test equipment. The amplifier RFin should be connected to a signal generator with RF OFF. A dual power supply will be needed, with output of +4.0 V @ 2 A for the collector voltages (Vcc = Vcc1 and Vcc2) and bias circuit (Vbias) and +4.0 V for the reference voltage (Vref). Use good quality cables to minimise any voltage drop between the PSU and evaluation board. Connect the power supply with RF off and ensure that the evaluation board consumes the correct quiescent current (Icq). Although it is good practice to enable the Vcc & Vbias supply before the Vref supply, in general, power supply sequencing is not necessary. If the quiescent current is correct, enable the RF signal with a low level, for example RFin = -30 dBm, to begin with to ensure the device is not overdriven. Ensure the test signal is within the recommended frequency range of the device and that the output signal measured on the test equipment complies with small signal gain, before continuing with any further tests.

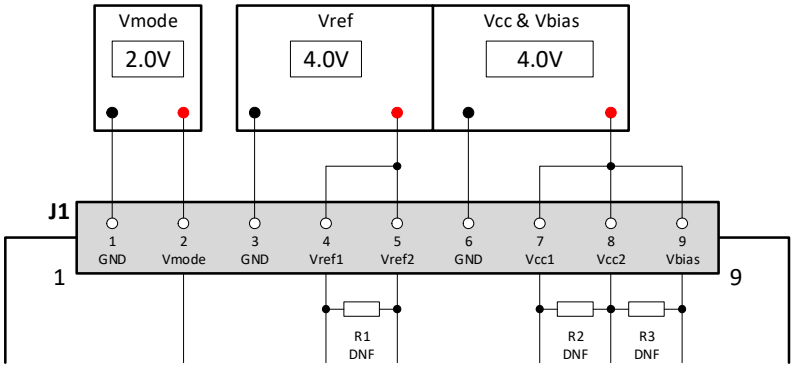


Figure 57 – EV90A006 Standard Power Supply Connections

R1, R2 and R3 are DNF (do not fit) on EV90A006 so that individual currents into each pin can be measured.

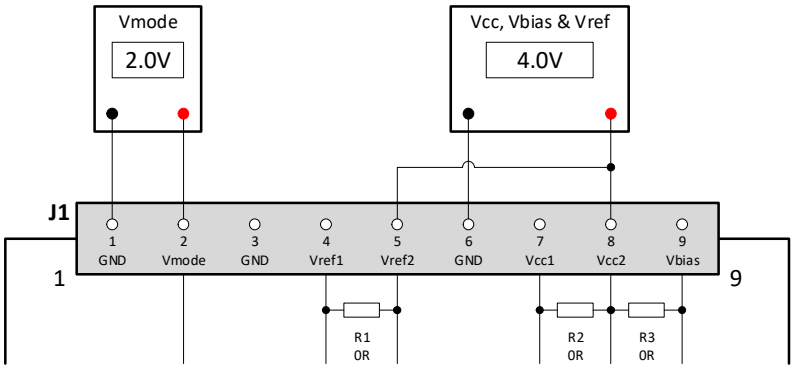


Figure 58 - Alternative EV90A006 Power Supply Connections with R1, R2 and R2 fitted

Fit R1 (0 Ω): For a single Vref supply connected to J1 pin 5.
Fit R2 (0 Ω): For a single Vcc supply connected to J1 pin 8.
Fit R3 (0 Ω): In combination with R2, for a single supply for Vcc & Vbias connected to J1 pin 8.

Ruggedness

To prevent possible damage to the device, care should be taken to ensure that the VSWR of the load that the CMX90A006 is working into does not exceed the limits in the Electrical Specification.

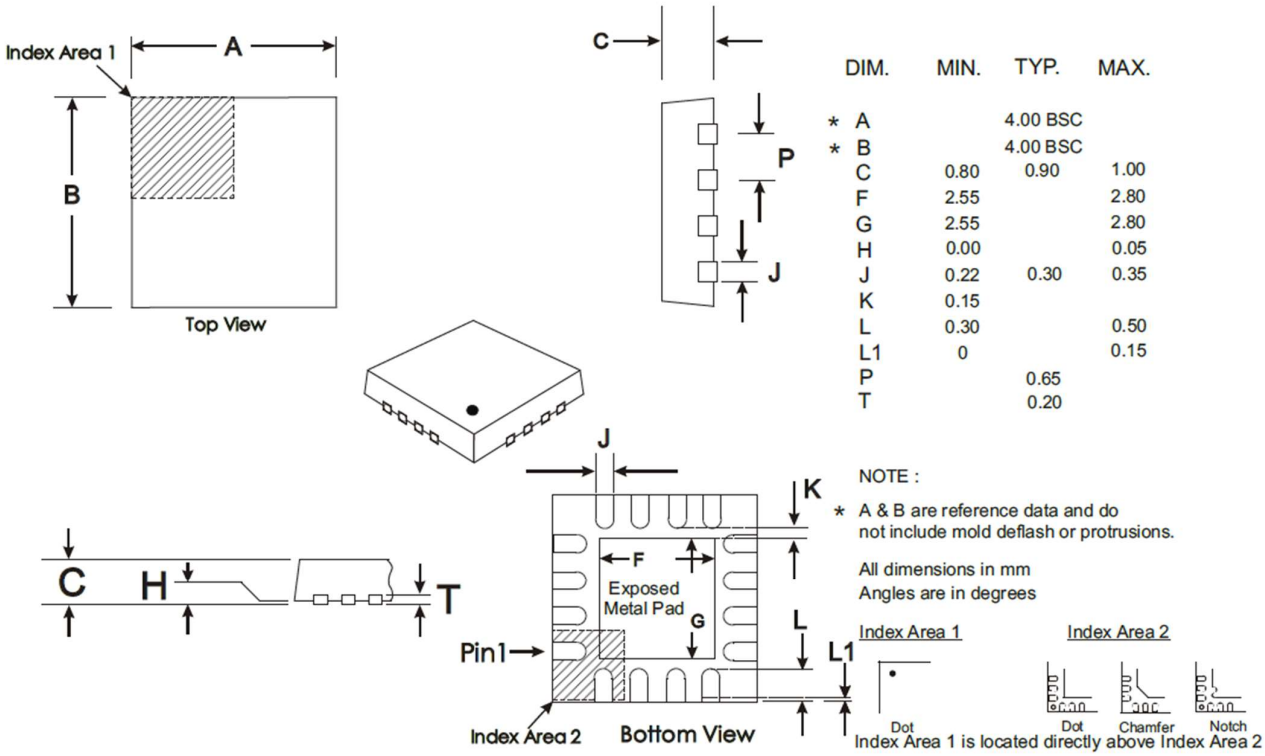
A typical transmit system will have couplers, filtering, transmit/receive switching and antenna matching between the PA and the antenna. These all need to be designed carefully to ensure a good 50 Ω match is presented to the PA that is above the minimum return loss limits over the whole operating frequency range.

External effects on the antenna impedance should also be considered. Proximity to other objects and surfaces can change the antenna impedance significantly, resulting in the return loss presented to the PA falling below the limit and therefore subsequent damage to the PA.

If there is an external antenna connector on the equipment, it should be assumed that the wrong antenna might get connected or that the transmitter may be operated with no antenna connected.

Package Outline

16-lead 4x4mm VQFN Package (Q7)



DIM.	MIN.	TYP.	MAX.
* A		4.00 BSC	
* B		4.00 BSC	
C	0.80	0.90	1.00
F	2.55		2.80
G	2.55		2.80
H	0.00		0.05
J	0.22	0.30	0.35
K	0.15		
L	0.30		0.50
L1	0		0.15
P		0.65	
T		0.20	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

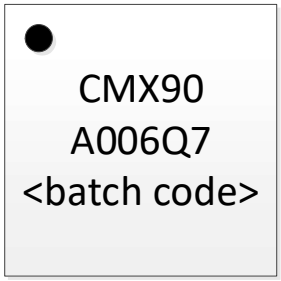
All dimensions in mm
Angles are in degrees

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Package Marking

Pin 1 indicator (dot) and 3 rows of text for device identification.



Line 1: CMX90 SµRF series

Line 2: 6-character part code

Line 3: Batch code

Revision History

Issue	Description	Date
1.0	First approved release	4th September 2024

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