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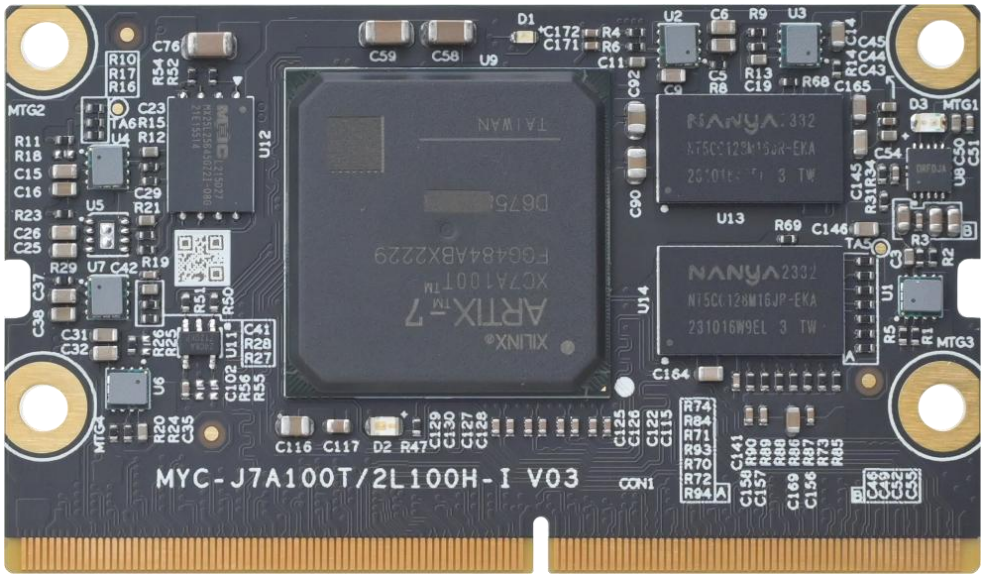
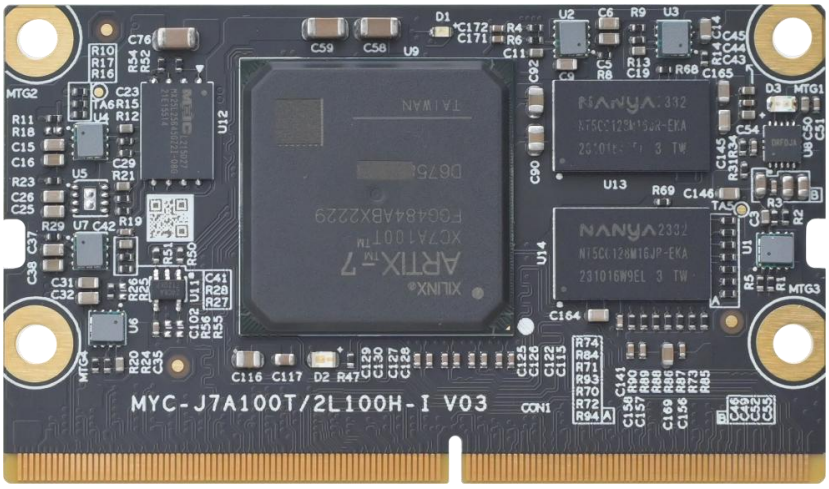
MYC-J7A100T System-On-Module Overview

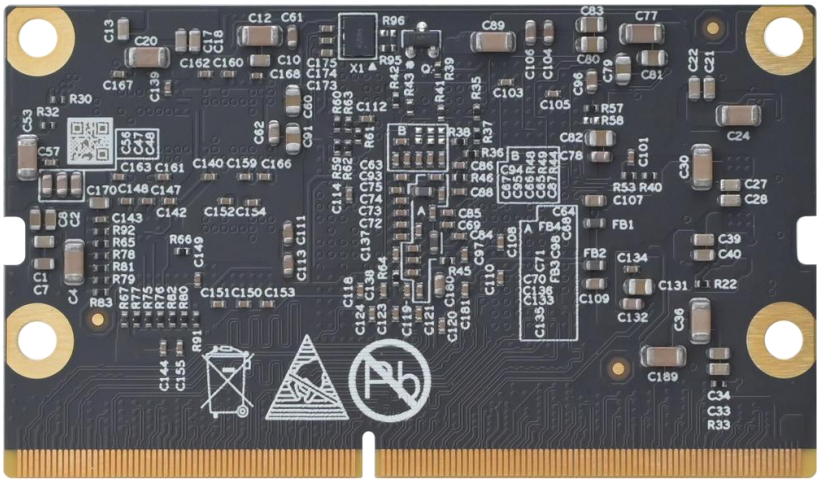


- ✓ *AMD/Xilinx XC7A100T Artix-7 FPGA (XC7A100T-2FGG484I)*
- ✓ *512MB DDR3, 32MB QSPI FLASH, 32KB EEPROM*
- ✓ *0.5mm Pitch 260-pin MXM Gold-finger-edge-card Connector*
- ✓ *Support Working Temperature Ranging from -40 to 85 Celsius*
- ✓ *Supports Development by Xilinx's Vivado Design Suite*

Measuring only 69.6mm by 40mm, the MYC-J7A100T is a compact System-on Module (SoM) based on the powerful AMD/Xilinx XC7A100T FPGA (XC7A100T-2FGG484I), which belongs to the Xilinx Artix-7 family. Additionally, it features onboard 512MB DDR3, 32MB QSPI FLASH, and 32KB EEPROM. A variety of IO signals are available through the 0.5 mm pitch 260-pin MXM gold-finger-edge-card connector, facilitating easy connection with MYIR's standard base board of the MYD-J7A100T development board or customized base boards from users. Furthermore, the MYC-J7A100T SOM provides a total of 178 FPGA IOs, four pairs of GTP high-speed transceiver interfaces, and one JTAG interface. Among the 178 FPGA IOs, 80 operates at 3.3V level, while the remaining 98 are user-configurable with various levels (1.2/1.35/1.5/1.8/2.5/3.3V). It is suitable for various fields, including industrial control, automation, communication, computing, and more.



MYC-J7A100T Top-view

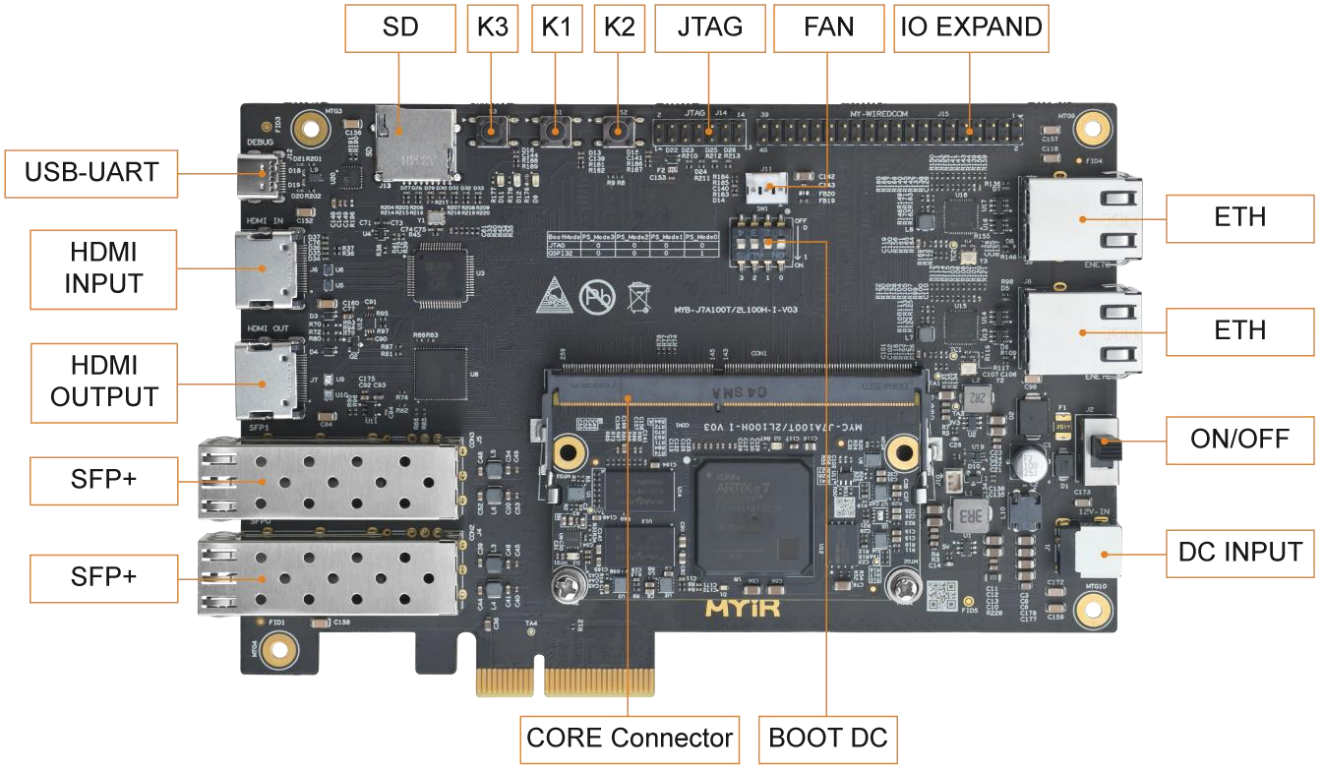


MYC-J7A100T Bottom-view

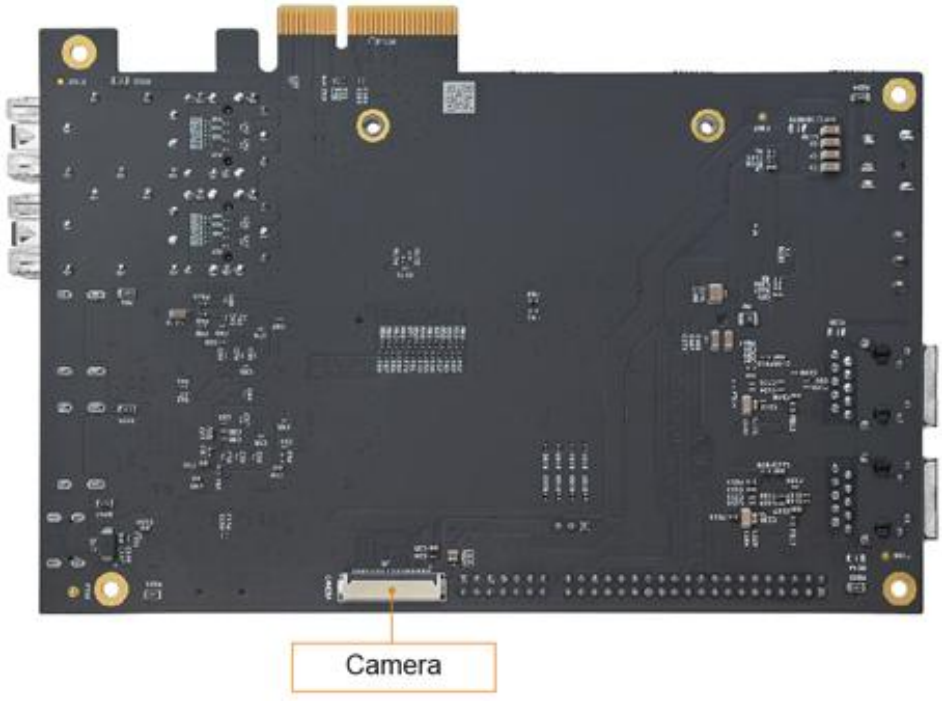
MYIR offers the MYD-J7A100T Development Board for evaluating the MYC-J7A100T SOM. This extensive development board not only demonstrates the capabilities of the MYC-J7A100T but also provides a convenient and efficient means for developers to explore its features and functionalities. Its expansion board interfaces with the MYC-J7A100T SOM via a 0.5mm pitch, 260-pin MXM gold-finger-edge-card connector. The MYD-J7A100T uses a 12V/2A DC power supply and boasts a diverse range of peripheral interfaces, including two Gigabit Ethernet ports, two SFP+ interfaces, a PCIe 2.0 interface, HDMI input and output interfaces, a DVP camera interface, a Micro SD slot, a USB-UART interface, and a FAN interface. Additionally, a 2.5mm pitch 2x 20-pin IO expansion interface offers further expansion capabilities, allowing users to connect additional peripherals or modules as required.

MYIR provides a range of Vivado sample codes for testing purposes, enabling users to quickly get started with developing their solutions. The MYD-J7A100T Development Board serves as an excellent platform for evaluating and developing applications based on the MYC-J7A100T SOM and other Artix-7 FPGA solutions.

MYIR also provides optional enhancements for the board, such as the MY-CAM011B Camera Module, and the MY-WIREDCOM RPI Module (RS232/RS485). These additions significantly expand the board's functionality, enabling users to enjoy versatile capabilities tailored to their specific project requirements.



MYD-J7A100T Development Board Top-view



MYD-J7A100T Development Board Bottom-view

Hardware Specification

The AMD/Xilinx Artix®-7 family of FPGAs has redefined cost-sensitive solutions by cutting power consumption in half from the previous generation while providing best-in-class transceivers and signal processing capabilities for high bandwidth applications. Built on the 28nm HPL process, these devices deliver best in class performance-per-watt. Together with the MicroBlaze(TM) soft processor, Artix-7 FPGAs are ideal for products like portable medical equipment, military radios, and compact wireless infrastructure. Artix-7 FPGAs meet the needs of size, weight, power, and cost (SWaP-C) sensitive markets like avionics and communications.

The MYC-J7A100T uses the XC7A100T-2FGG484I device, offering an extensive range of features including up to 101,440 logic cells, 4,860 Kb of Block RAM, 240 DSP slices, 929 GMAC/s, 8 GTP transceivers capable of reaching speeds up to 6.6Gb/s, x4 Gen2 PCIe interface, and a total of 285 I/O pins, all contained within the FGG484 package.

AMD Artix™ 7 FPGAs – Resources & Packaging

Important: Verify all data in this document with the device data sheets.

		Transceiver Optimization at the Lowest Cost and Highest DSP Bandwidth (1.0V, 0.95V, 0.9V)							
	Device Name	XC7A12T	XC7A15T	XC7A25T	XC7A35T	XC7A50T	XC7A75T	XC7A100T	XC7A200T
Logic Resources	Logic Cells	12,800	16,640	23,360	33,280	52,160	75,520	101,440	215,360
	Slices	2,000	2,600	3,650	5,200	8,150	11,800	15,850	33,650
	CLB Flip-Flops	16,000	20,800	29,200	41,600	65,200	94,400	126,800	269,200
Memory Resources	Maximum Distributed RAM (Kb)	171	200	313	400	600	892	1,188	2,888
	Block RAM/FIFO w/ ECC (36 Kb each)	20	25	45	50	75	105	135	365
	Total Block RAM (Kb)	720	900	1,620	1,800	2,700	3,780	4,860	13,140
Clock Resources	CMTs (1 MMCM + 1 PLL)	3	5	3	5	5	6	6	10
I/O Resources	Maximum Single-Ended I/O	150	250	150	250	250	300	300	500
	Maximum Differential I/O Pairs	72	120	72	120	120	144	144	240
Embedded Hard IP Resources	DSP Slices	40	45	80	90	120	180	240	740
	PCIe® Gen2[1]	1	1	1	1	1	1	1	1
	Analog Mixed Signal (AMS) / XADC	1	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1	1
	GTP Transceivers (6.6 Gb/s Max Rate)[2]	2	4	4	4	4	8	8	16
Speed Grades	Commercial Temp (C)	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended Temp (E)	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3
	Industrial Temp (I)	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L
	Package[3b, 4] / Dimensions (mm) / Ball Pitch (mm)	Available User I/O: 3.3V SelectIO™ HR I/O (GTP Transceivers)							
	CPG236 / 10 x 10 / 0.5		106 (2)		106 (2)	106 (2)			
	CPG238 / 10 x 10 / 0.5	112 (2)		112 (2)					
	CSG324 / 15 x 15 / 0.8		210 (0)		210 (0)	210 (0)	210 (0)	210 (0)	
	CSG325 / 15 x 15 / 0.8	150 (2)	150 (4)	150 (4)	150 (4)	150 (4)			
	FTG256 / 17 x 17 / 1.0		170 (0)		170 (0)	170 (0)	170 (0)	170 (0)	
	SBG484 / 19 x 19 / 0.8								285 (4)
Footprint Compatible	FGG484[5] / 23 x 23 / 1.0		250 (4)		250 (4)	250 (4)	285 (4)	285 (4)	
	FBG484[5] / 23 x 23 / 1.0								285 (4)
Footprint Compatible	FGG676[6] / 27 x 27 / 1.0						300 (8)	300 (8)	
	FBG676[6] / 27 x 27 / 1.0								400 (8)
	FFG1156 / 35 x 35 / 1.0								500 (16)

1. Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates.

2. Represents the maximum number of transceivers available. Note that the majority of devices are available without transceivers. See the Package section of this table for details.

3. Leaded package option available for all packages. See DS180, 7 Series FPGAs Overview for package details.

4. Device migration is available within the Artix 7 family for like packages but is not supported between other 7 series families.

5. Devices in FGG484 and FBG484 are footprint compatible.

6. Devices in FGG676 and FBG676 are footprint compatible.

AMD Artix-7 FPGAs - Resources & Packaging

The MYC-J7A100T module features the XC7A100T-2FGG484I FPGA and is characterized as below:

Mechanical Parameters

- Dimensions: 69.6mm x 40mm
- PCB Layers: 12-layer design
- Power supply: +5V/ 3A
- Working temperature: -40~85 Celsius (industrial grade)

FPGA

- AMD/Xilinx XC7A100T Artix-7 FPGA (XC7A100T-2FGG484I)

Memory and Storage

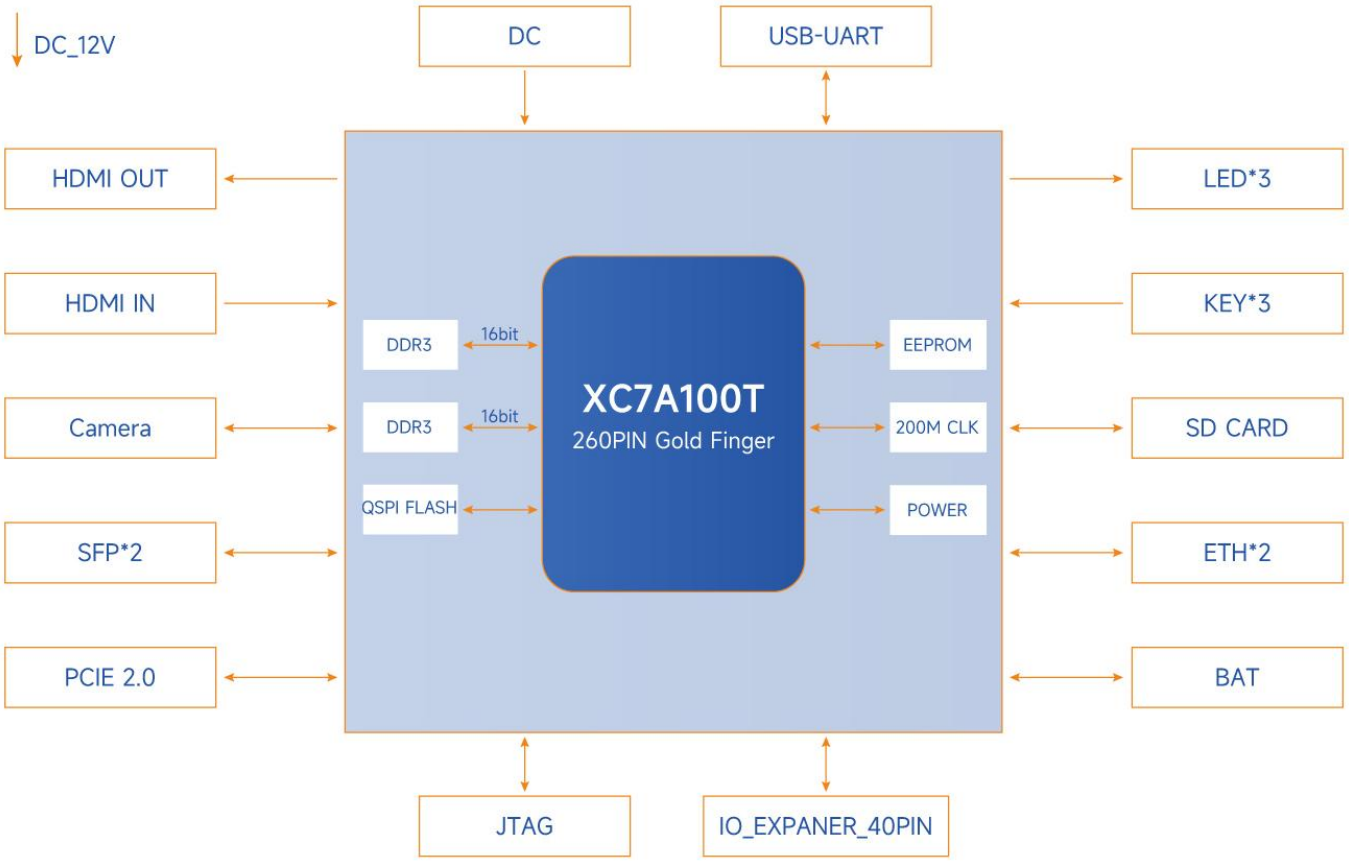
- 512MB DDR3
- 32MB QSPI FLASH
- 32KB EEPROM

Signals Routed to Expansion Interface

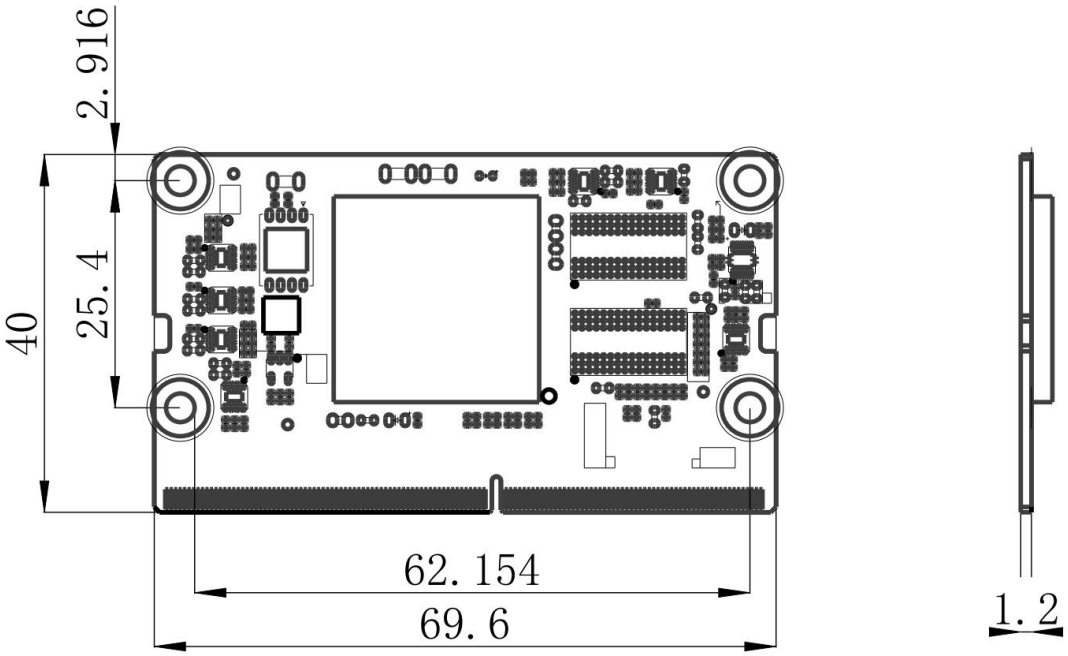
- 0.5mm pitch 260-pin MXM Gold-finger-edge-card expansion interface

Item	Number of I/Os	Description
Bank13	35	There are 178 I/Os in total, which are defined according to different requirements. Signal lines with the same function are located on the same bank.
Bank14	45	
Bank15	48	
Bank16	50	
MGTP	20	High-Speed Serial Interfaces
JTAG	4	JTAG Debug

MYC-J7A100T Function Block Diagram



MYD-J7A100T Development Board Function Block Diagram



MYC-J7A100T Dimensions Chart (Unit: MM)

Software Features

MYIR provides a range of Vivado sample codes for testing purposes, enabling users to quickly get started with developing their solutions based on MYIR's MYD-J7A100T development board. The provided project files are listed in below table:

Vivado Project File	Description	Source Code
led_test	User LED Test	YES
key_test	Development Board Keys Test	YES
uart_test	UART Test	YES
hdmi_out_test	HDMI Output Interface Test	YES
ddr_test	DDR3 Test	YES
sd_hdmi_out	SD Card Read/Write Function Test	YES
hdmi_in_ddr_hdmi_out	HDMI Input Interface Test	YES
ov2659_ddr_hdmi_out	Camera Output Display Test	YES
sfp_test	SFP Loopback Test	YES
pcie_test	PCIe Read/Write Function Test	YES
udp_cmos_rgmii	Ethernet UDP Function Test	YES

MYD-J7A100T Software Features

Order Information

Product Item	Part No.	Packing List
MYC-J7A100T System-On-Module	MYC-J7A100T-32Q512D-I	✓ One MYC-J7A100T SOM
MYD-J7A100T Development Board	MYD-J7A100T-32Q512D-I	✓ One MYD-J7A100T Development Board ✓ (including MYC-J7A100T SOM) ✓ One 12V/2A Power adapter ✓ One USB Type A to Type C cable ✓ One Quick Start Guide
MY-CAM011B Camera Module	MY-CAM011B	**Add-on Options** ✓ MY-CAM011B Camera Module ✓ MY-WIREDCOM RPI Module
MY-WIREDCOM RPI Module (RS232/RS485)	MY-WIREDCOM	

Note:

1. The MYD-J7A100T Development Board comprises one MYC-J7A100T SOM mounted onto the base board. If you require additional SOMs, you may place orders for extras.

2. Bulk discounts are available. For inquiries, kindly contact MYIR.

3. We cater to custom design requests based on the MYD-J7A100T, whether it involves reducing, adding, or modifying the existing hardware components to suit the customer's specific needs.

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