

PSMN9R5-100PS

N-channel 100 V 9.6 mΩ standard level MOSFET in T0220
17 October 2013 Product data sheet

1. General description

Standard level N-channel MOSFET in a TO220 packages qualified to 175C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

2. Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive

3. Applications

- DC-to-DC converters
- Load switching
- Motor control
- Server power supplies

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	100	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; <u>Fig. 1</u>	-	-	89	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 2</u>	-	-	211	W
Static characte	eristics					
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ °C};$ Fig. 13	-	8.16	9.6	mΩ
Dynamic chara	acteristics					
Q_{GD}	gate-drain charge	V _{GS} = 10 V; I _D = 60 A; V _{DS} = 50 V;	-	23	-	nC
Q _{G(tot)}	total gate charge	<u>Fig. 14; Fig. 15</u>	-	82	-	nC
Avalanche rug	gedness					,
E _{DS(AL)S}	non-repetitive drain- source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 89 A; V_{sup} ≤ 100 V; unclamped; R_{GS} = 50 Ω	-	-	177	mJ



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	mb	D
2	D	drain	 	
3	S	source		G T A
mb	D	mounting base; connected to drain		mbb076 S
			TO-220AB (SOT78)	

6. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
PSMN9R5-100PS	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78			

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN9R5-100PS	PSMN9R5-100PS

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	100	V
V_{DGR}	drain-gate voltage	$T_j \le 175 ^{\circ}\text{C}; T_j \ge 25 ^{\circ}\text{C}; R_{GS} = 20 \text{k}\Omega$	-	100	V
V _{GS}	gate-source voltage		-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 100 °C; <u>Fig. 1</u>	-	63	Α
		V _{GS} = 10 V; T _{mb} = 25 °C; <u>Fig. 1</u>	-	89	Α
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 \text{ °C}$; Fig. 3	-	355	Α

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Symbol	Parameter	Conditions	Min	Max	Unit
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 2</u>	-	211	W
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
T _{sld(M)}	peak soldering temperature		-	260	°C
Source-drai	in diode				
I _S	source current	T _{mb} = 25 °C	-	89	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$	-	355	Α
Avalanche i	ruggedness				,
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_{D} = 89 A; $V_{sup} \le$ 100 V; unclamped; R_{GS} = 50 Ω	-	177	mJ

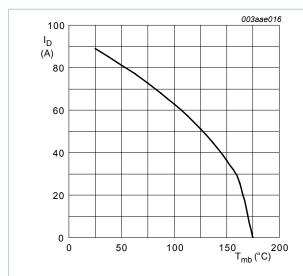


Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{\rm GS} \geq 10~V$$

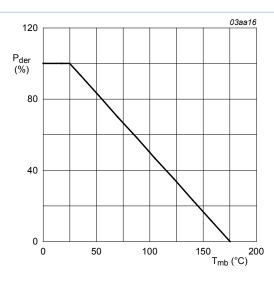


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

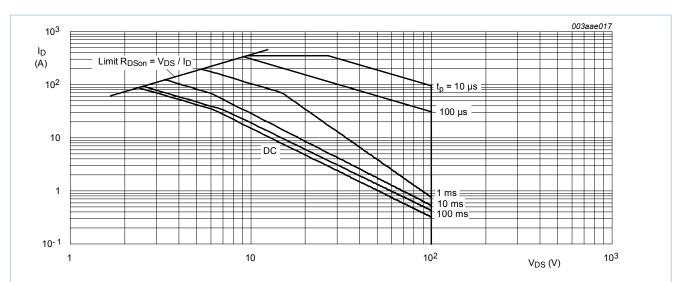


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$$T_{mb} = 25 \,^{\circ}C; I_{DM}$$
is single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	Fig. 4	-	0.38	0.71	K/W

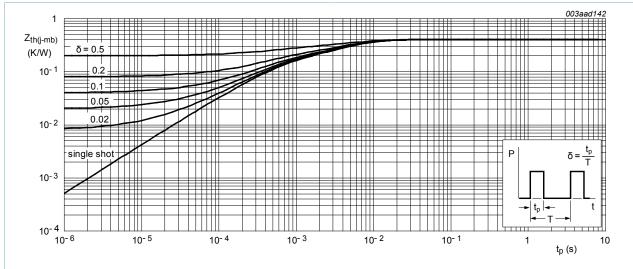


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
V _{(BR)DSS} drain-source		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 ^{\circ}\text{C}$	90	-	-	V
	breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; Fig. 10; Fig. 11	1	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; Fig. 10; Fig. 11	2	3	4	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; Fig. 10; Fig. 11	-	-	4.8	V
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _j = 125 °C	-	-	100	μA
		V _{DS} = 100 V; V _{GS} = 0 V; T _j = 25 °C	-	0.02	4	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	10	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	10	100	nA
R _{DSon} drain-source on-s resistance	drain-source on-state resistance	V _{GS} = 10 V; I _D = 15 A; T _j = 100 °C; Fig. 12	-	-	17.3	mΩ
		V _{GS} = 10 V; I _D = 15 A; T _j = 175 °C; Fig. 12	-	23.5	27.4	mΩ
		V _{GS} = 10 V; I _D = 15 A; T _j = 25 °C; Fig. 13	-	8.16	9.6	mΩ
R_{G}	internal gate resistance (AC)	f = 1 MHz	-	0.7	-	Ω
Dynamic ch	naracteristics		1			
Q _{G(tot)}	total gate charge	I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V; <u>Fig. 14</u>	-	67	-	nC
		I _D = 60 A; V _{DS} = 50 V; V _{GS} = 10 V;	-	82	-	nC
Q_{GS}	gate-source charge	Fig. 14; Fig. 15	-	21	-	nC
Q _{GS(th)}	pre-threshold gate- source charge	I _D = 60 A; V _{DS} = 50 V; V _{GS} = 3 V; Fig. 14	-	13.1	-	nC
Q _{GS(th-pl)}	post-threshold gate- source charge	I _D = 60 A; V _{DS} = 50 V; V _{GS} = 10 V; Fig. 14	-	7.8	-	nC
Q_{GD}	gate-drain charge	I _D = 60 A; V _{DS} = 50 V; V _{GS} = 10 V; Fig. 14; Fig. 15	-	23	-	nC
V _{GS(pI)}	gate-source plateau voltage	V _{DS} = 50 V; <u>Fig. 14</u> ; <u>Fig. 15</u>	-	4.5	-	V
C _{iss}	input capacitance	V _{DS} = 50 V; V _{GS} = 0 V; f = 1 MHz;	-	4454	-	pF
C _{oss}	output capacitance	T _j = 25 °C; <u>Fig. 16</u>	-	302	-	pF

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Symbol	Parameter	Conditions		Min	Тур	Max	Unit
C _{rss}	reverse transfer capacitance			-	185	-	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 50 \text{ V}; R_L = 0.8 \Omega; V_{GS} = 10 \text{ V};$		-	22	-	ns
t _r	rise time	$R_{G(ext)} = 4.7 \Omega; T_j = 25 °C$		-	25.2	-	ns
t _{d(off)}	turn-off delay time			-	52.2	-	ns
t _f	fall time	-		-	22.8	-	ns
Source-dra	ain diode			'			
V_{SD}	source-drain voltage	$I_S = 15 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}; Fig. 17$		-	0.85	1.2	V
t _{rr}	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = 100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$		-	61.5	-	ns
Q _r	recovered charge	V _{DS} = 50 V		-	157	-	nC

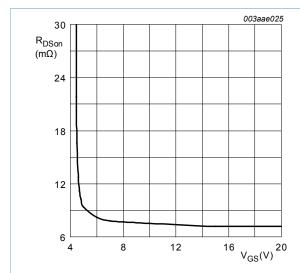


Fig. 5. Drain-source on-state resistance as a function of gate-source voltage; typical values.

$$T_j = 25 \, ^{\circ}C; I_D = 20 \, \text{A}$$

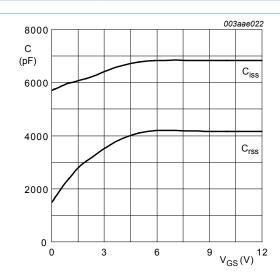


Fig. 6. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

$$V_{DS} = 0V; f = 1MHz$$

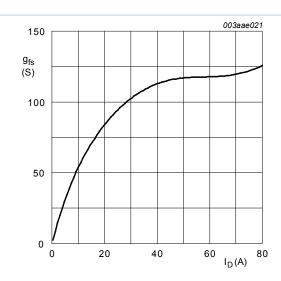


Fig. 7. Forward transconductance as a function of drain current; typical values

$$T_j = 25 \,^{\circ}C; V_{DS} = 25 \,^{\circ}V$$

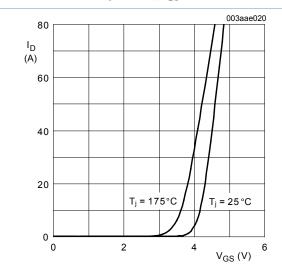


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical valuesvalues

$$V_{DS} > I_D \times R_{DSon}$$

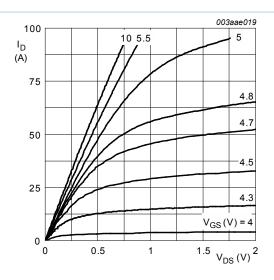


Fig. 8. Output characteristics: drain current as a function of drain-source voltage; typical values

$$T_j = 25 \,^{\circ}C$$

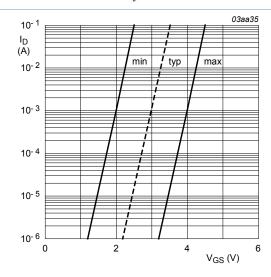


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25 \,^{\circ}C; V_{DS} = 5V$$

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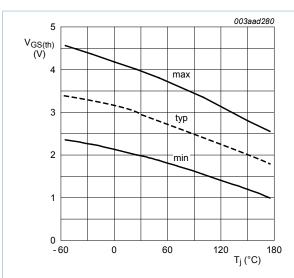


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1 \text{ mA}; \ V_{DS} = V_{GS}$$

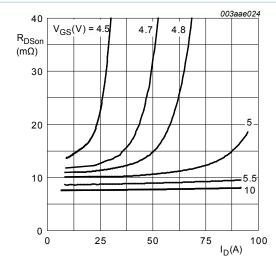


Fig. 13. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25 \,^{\circ}C$$

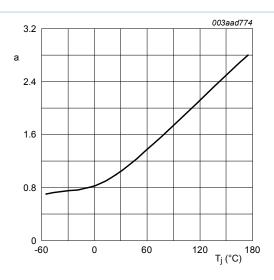


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25 \, ^{\circ}\text{C})}}$$

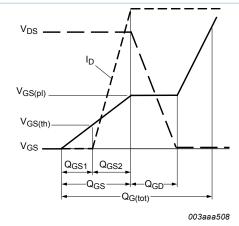


Fig. 14. Gate charge waveform definitions

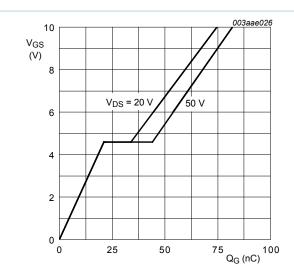


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25$$
 °C; $I_D = 60$ A

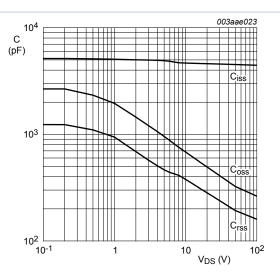


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0 \text{ V; } f = 1 \text{ MHz}$$

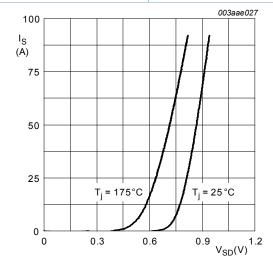
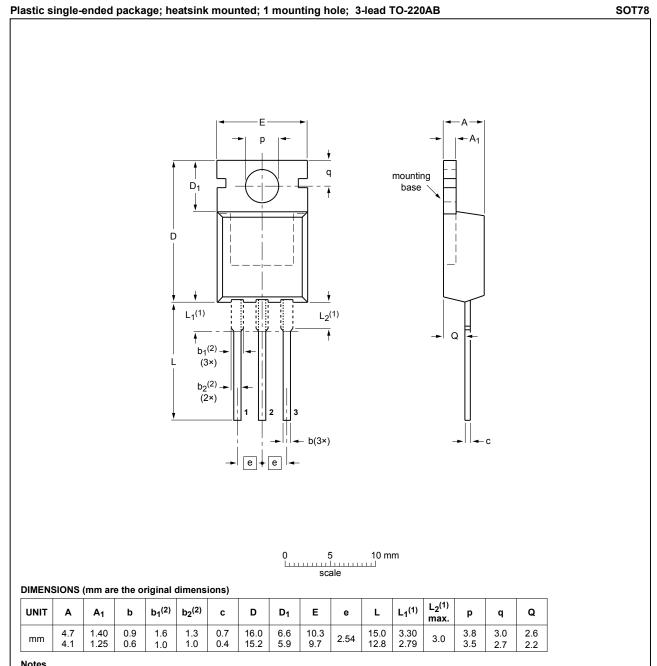


Fig. 17. Source current as a function of source-drain voltage; typical values

$$V_{GS} = 0 V$$

11. Package outline



- 1. Lead shoulder designs may vary.
- 2. Dimension includes excess dambar.

OUTLINE		REFERENCES				ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	1330E DATE
SOT78		3-lead TO-220AB	SC-46			08-04-23 08-06-13

Fig. 18. Package outline TO-220AB (SOT78)

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