



PSMN6R5-80BS

N-channel 80V 6.9mΩ standard level MOSFET in D2PAK

Rev. 2 — 2 March 2012

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in D2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources

1.3 Applications

- DC-to-DC converters
- Motor control
- Load switching
- Server power supplies

1.4 Quick reference data

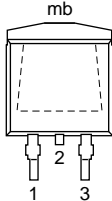
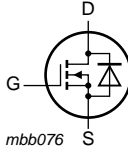
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	80	V
I_D	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see Figure 1	[1]	-	100	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ see Figure 2	-	-	210	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 15\text{ A}; T_j = 25\text{ °C};$ see Figure 13	-	5.9	6.9	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; V_{DS} = 40\text{ V};$ see Figure 14 ; see Figure 15	-	16	-	nC
$Q_{G(tot)}$	total gate charge		-	71	-	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C}; I_D = 49\text{ A}; V_{sup} \leq 80\text{ V}; R_{GS} = 50\text{ Ω};$ unclamped	-	-	700	mJ

[1] Continuous current rating is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain ^[1]		
3	S	source		
mb	D	mounting base; connected to drain		

SOT404 (D2PAK)

[1] It is not possible to make connection to pin 2.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN6R5-80BS	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

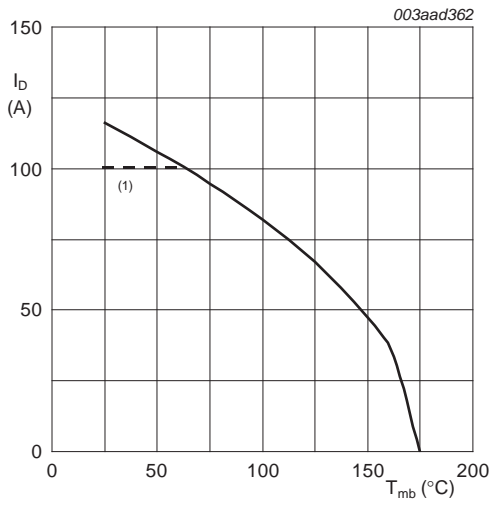
4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

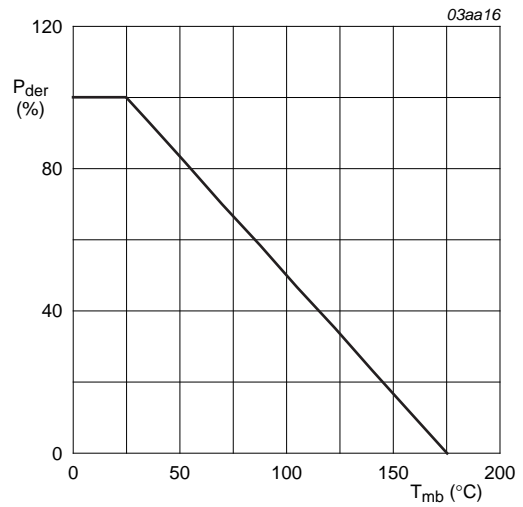
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	80	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	80	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; see Figure 1	-	82	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1	[1]	100	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; see Figure 3	-	470	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	210	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	100	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	470	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 49\text{ A}$; $V_{sup} \leq 80\text{ V}$; $R_{GS} = 50\text{ }\Omega$; unclamped	-	700	mJ

[1] Continuous current rating is limited by package.



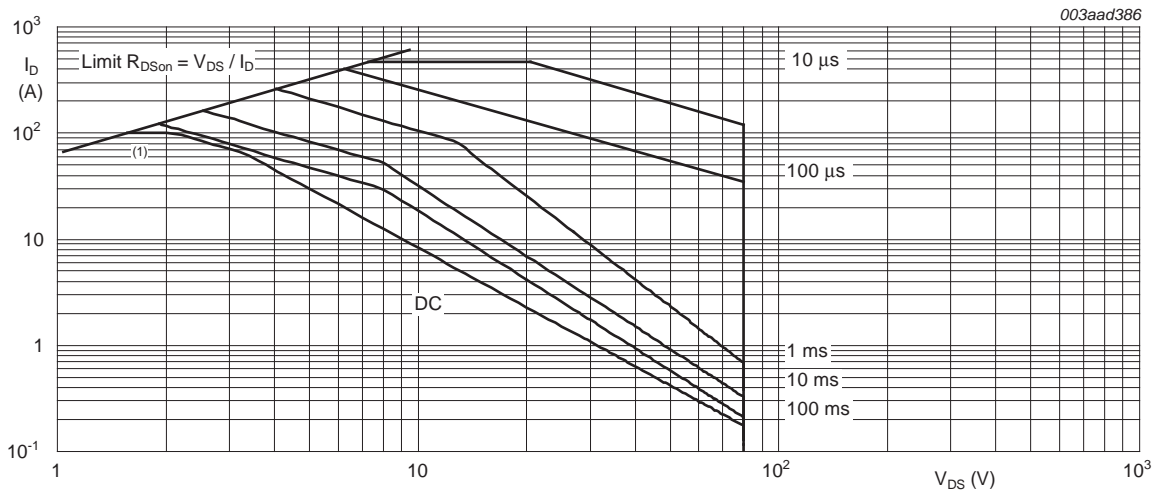
$V_{GS} \geq 10V$
 (1) Capped at 100 A due to package.

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



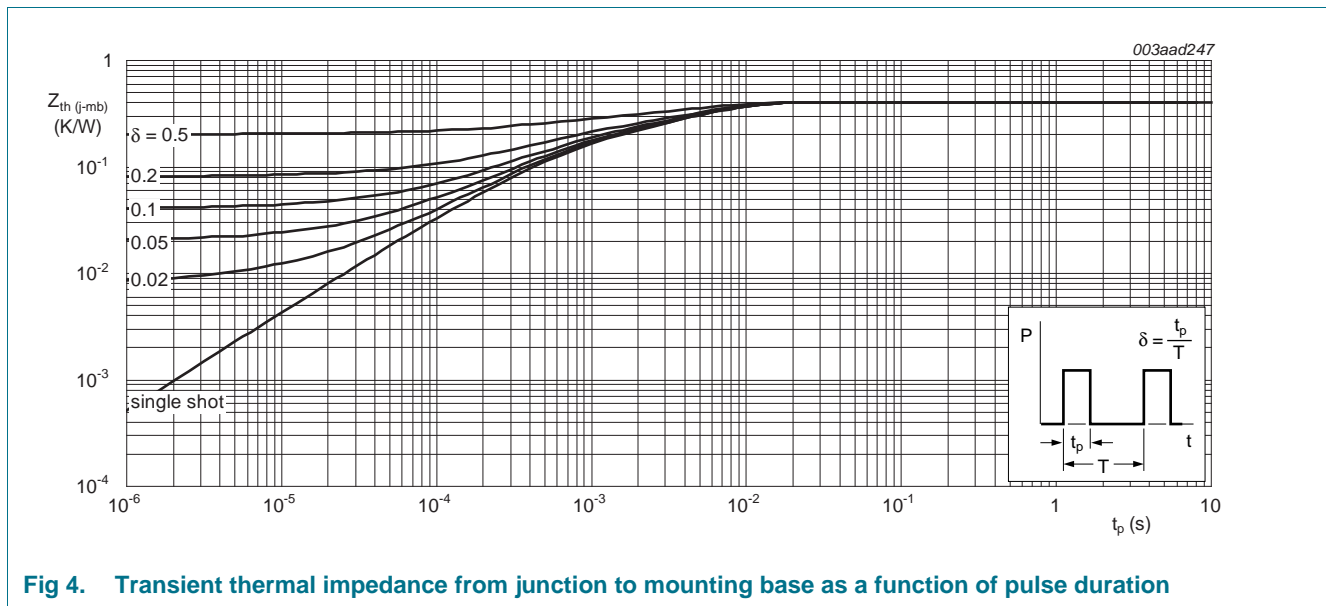
$T_{mb} = 25^\circ C$; I_{DM} is a single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.4	0.7	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	50	-	K/W



6. Characteristics

Table 6. Characteristics

Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	73	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	80	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$; see Figure 10 ; see Figure 11	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$; see Figure 10 ; see Figure 11	-	-	4.6	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$; see Figure 10 ; see Figure 11	2.3	3	4	V
I_{DSS}	drain leakage current	$V_{DS} = 80 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.3	10	μA
		$V_{DS} = 80 V; V_{GS} = 0 V; T_j = 125 \text{ }^\circ C$	-	-	150	μA
I_{GSS}	gate leakage current	$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	10	100	nA
		$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 15 A; T_j = 100 \text{ }^\circ C$; see Figure 12	-	-	11.5	mΩ
		$V_{GS} = 10 V; I_D = 15 A; T_j = 175 \text{ }^\circ C$; see Figure 12	-	-	16.56	mΩ
		$V_{GS} = 10 V; I_D = 15 A; T_j = 25 \text{ }^\circ C$; see Figure 13	-	5.9	6.9	mΩ
R_G	internal gate resistance (AC)	$f = 1 \text{ MHz}$	-	0.75	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$	-	61	-	nC
		$I_D = 25 A; V_{DS} = 40 V; V_{GS} = 10 V$; see Figure 14 ; see Figure 15	-	71	-	nC
Q_{GS}	gate-source charge		-	19	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	13.2	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	5.8	-	nC
Q_{GD}	gate-drain charge		-	16	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 A; V_{DS} = 40 V$; see Figure 15	-	4.3	-	V
C_{iss}	input capacitance	$V_{DS} = 40 V; V_{GS} = 0 V; f = 1 \text{ MHz}$;	-	4461	-	pF
C_{oss}	output capacitance	$T_j = 25 \text{ }^\circ C$; see Figure 16	-	410	-	pF
C_{rss}	reverse transfer capacitance		-	214	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 40 V; R_L = 0.5 \text{ } \Omega; V_{GS} = 10 V$;	-	26	-	ns
t_r	rise time	$R_{G(ext)} = 4.7 \text{ } \Omega$	-	24	-	ns
$t_{d(off)}$	turn-off delay time		-	57	-	ns
t_f	fall time		-	22	-	ns

Table 6. Characteristics ...continued
 Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 15\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; see Figure 17	-	0.79	1.2	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $di_S/dt = 100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	48	-	ns
Q_r	recovered charge	$V_{DS} = 40\text{ V}$	-	82	-	nC

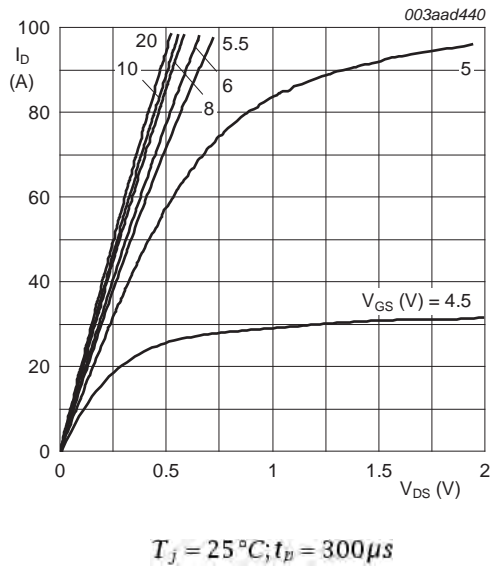


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

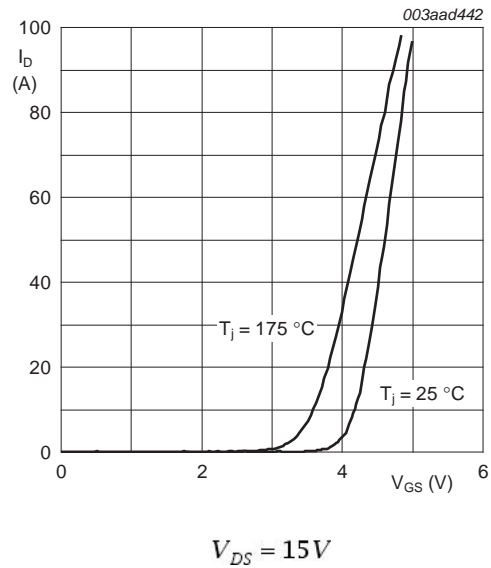


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

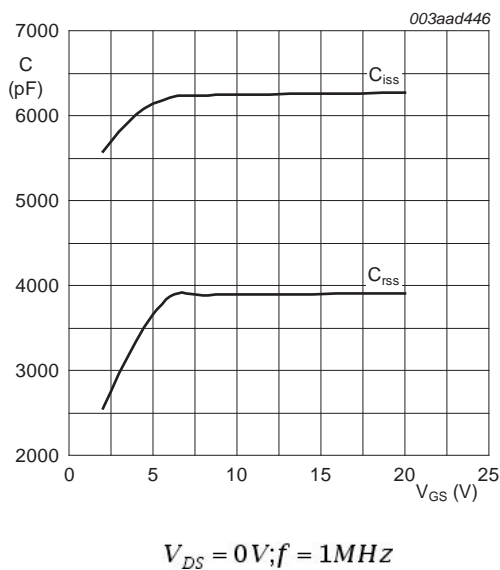


Fig 7. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

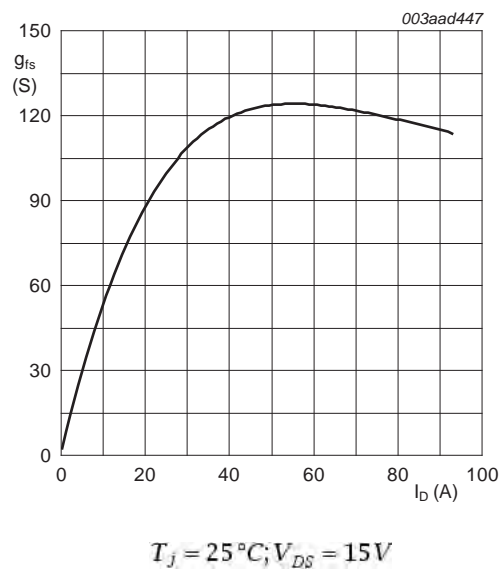
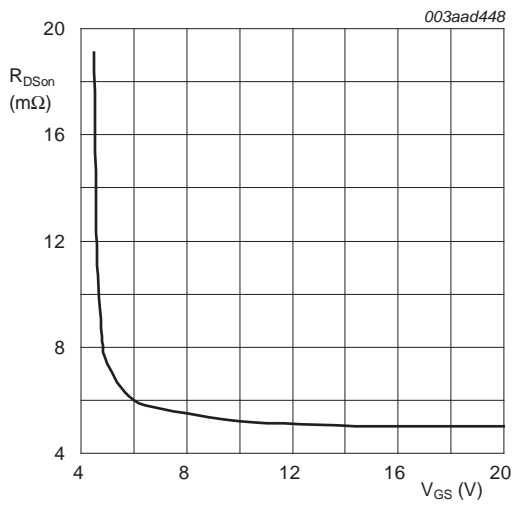
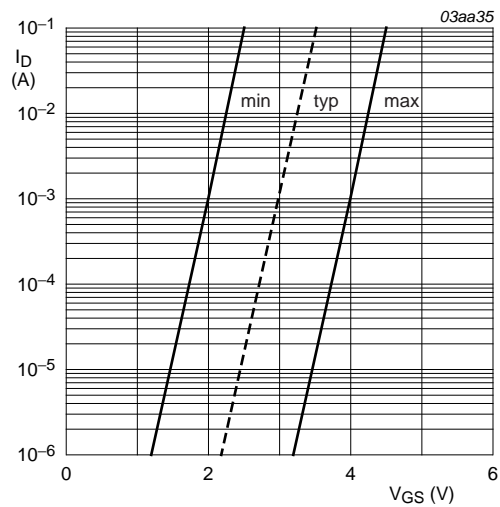


Fig 8. Forward transconductance as a function of drain current; typical values



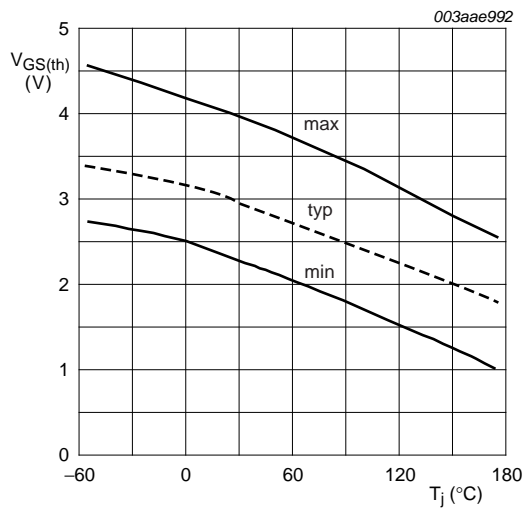
$T_j = 25^\circ\text{C}; I_D = 25\text{A}$

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



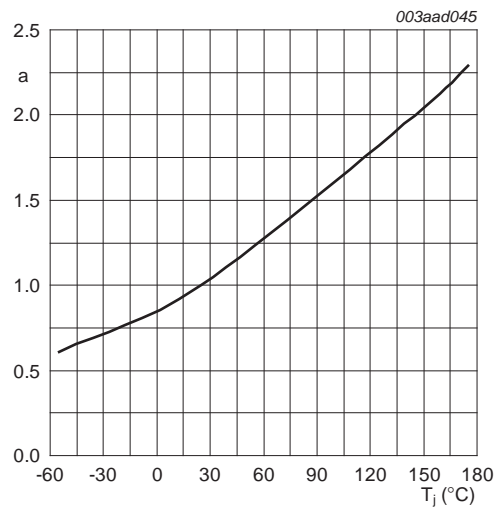
$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



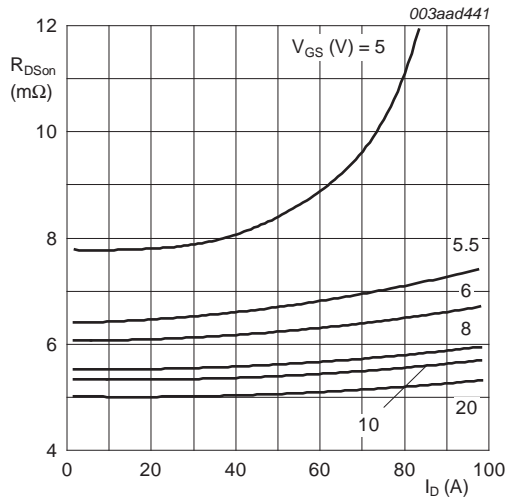
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 11. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DS(on)}}{R_{DS(on)@25^\circ\text{C}}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^\circ C; t_p = 300 \mu s$

Fig 13. Drain-source on-state resistance as a function of drain current; typical values

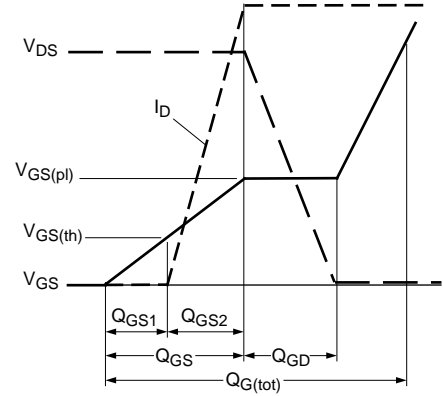
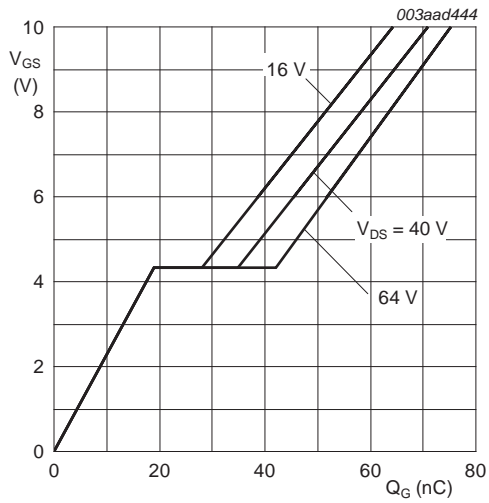
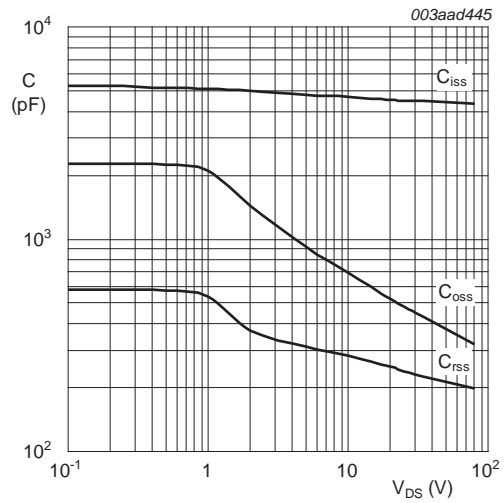


Fig 14. Gate charge waveform definitions



$T_j = 25^\circ C; I_D = 25 A$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0 V; f = 1 MHz$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

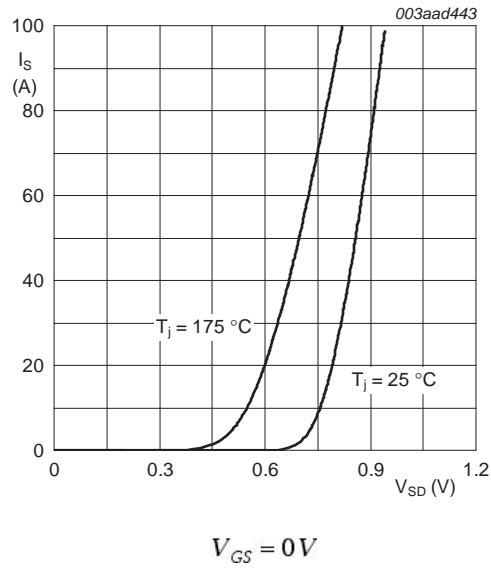


Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

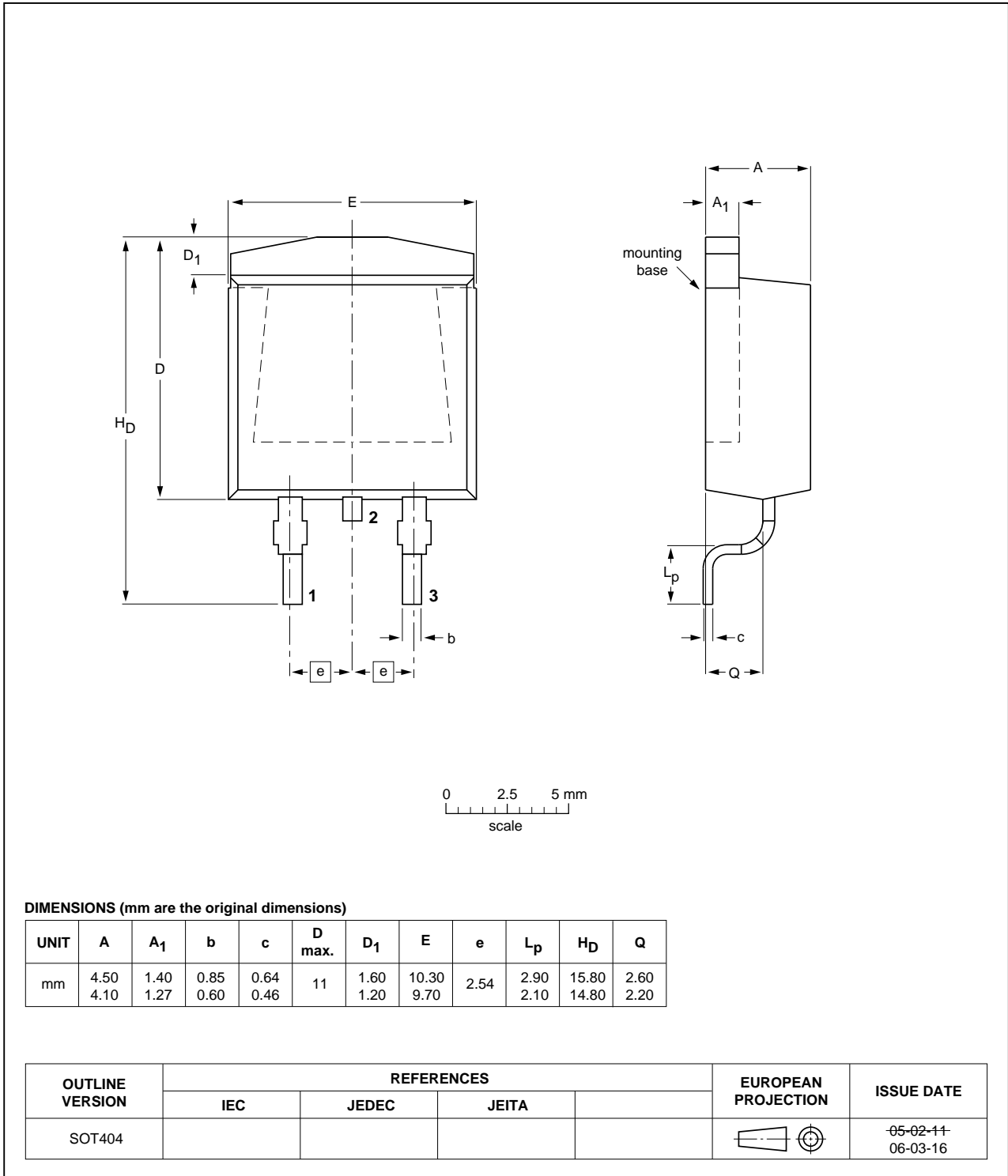


Fig 18. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN6R5-80BS v.2	20120302	Product data sheet	-	PSMN6R5-80BS v.1
Modifications:	<ul style="list-style-type: none">• Status changed from objective to product.• Various changes to content.			
PSMN6R5-80BS v.1	20111021	Objective data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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