

PSMN4R3-30BL

N-channel 30 V 4.1 m Ω logic level MOSFET in D2PAK Rev. 1 — 22 March 2012 Product

Product data sheet

1. **Product profile**

1.1 General description

Logic level N-channel MOSFET in D2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

1.3 Applications

- DC-to-DC converters
- Load switching

- Motor control
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	30	V
I_D	drain current	$T_{mb} = 25 \text{ °C}; V_{GS} = 10 \text{ V}; \text{ see } \frac{\text{Figure 1}}{}$	1 -	-	100	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	-	103	W
Tj	junction temperature		-55	-	175	°C
Static charac	cteristics					
R _{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 15 A; T_j = 100 °C; see <u>Figure 12</u> ; see <u>Figure 13</u>	-	4.9	5.8	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ °C};$ see <u>Figure 13</u>	-	3.5	4.1	mΩ
Dynamic cha	aracteristics					
Q_{GD}	gate-drain charge	$V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A}; V_{DS} = 15 \text{ V};$	-	5	-	nC
Q _{G(tot)}	total gate charge	see <u>Figure 14</u> ; see <u>Figure 15</u>	-	19	-	nC
Avalanche ru	uggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 100 A; $V_{sup} \le$ 30 V; R_{GS} = 50 Ω ; unclamped	-	-	74	mJ

^[1] Continuous current is limited by package.



2. Pinning information

Table 2. Pinning information

I abic 2.	1 111111111	illorination		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		_
2	D	drain[1]	mb	D
3	S	source		
mb	D	mounting base; connected to drain	1 3	mbb076 S
			SOT404 (D2PAK)	

^[1] It is not possible to make connection to pin 2

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN4R3-30BL	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Marking

Table 4. Marking codes

Type number	Marking code
PSMN4R3-30BL	PSMN4R3-30BL

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	30	V
V_{DGR}	drain-gate voltage	$T_j \ge 25$ °C; $T_j \le 175$ °C; $R_{GS} = 20$ kΩ		-	30	V
V_{GS}	gate-source voltage			-20	20	V
I _D	drain current	$V_{GS} = 10 \text{ V}; T_{mb} = 100 \text{ °C}; \text{ see } \frac{\text{Figure 1}}{\text{Model}}$	<u>[1]</u>	-	80	Α
		$V_{GS} = 10 \text{ V}; T_{mb} = 25 \text{ °C}; \text{ see } \frac{\text{Figure 1}}{\text{Model}}$	<u>[1]</u>	-	100	Α
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 \text{ °C}$; see Figure 3		-	465	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>		-	103	W
T _{stg}	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
T _{sld(M)}	peak soldering temperature			-	260	°C
Source-dra	ain diode					
Is	source current	T _{mb} = 25 °C	[1]	-	100	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$		-	465	Α
Avalanche	ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 100 A; $V_{sup} \le$ 30 V; R_{GS} = 50 Ω ; unclamped		-	74	mJ

[1] Continuous current is limited by package.

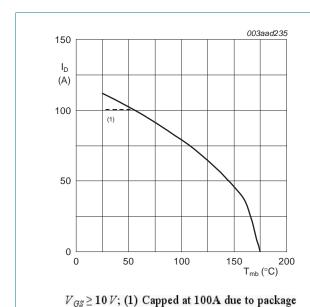


Fig 1. Continuous drain current as a function of mounting base temperature

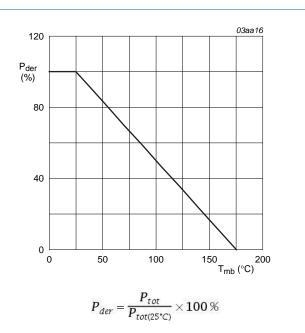


Fig 2. Normalized total power dissipation as a function of mounting base temperature

PSMN4R3-30BL

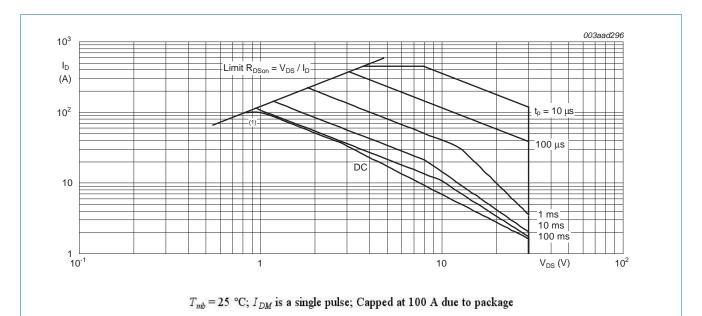


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	1	1.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	50	-	K/W

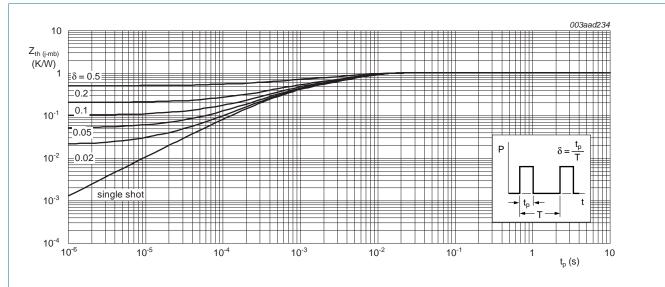


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

7. Characteristics

Table 7. Characteristics

Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static char	racteristics					
V _{(BR)DSS}	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	30	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS} ; T_j = 25 °C; see <u>Figure 10</u> ; see <u>Figure 11</u>	1.3	1.7	2.15	V
		I_D = 1 mA; V_{DS} = V_{GS} ; T_j = 175 °C; see Figure 11	0.5	-	-	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = -55$ °C; see <u>Figure 11</u>	-	-	2.45	V
I _{DSS}	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.02	1	μΑ
	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ °C}$	-	-	40	μΑ	
I_{GSS}	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	10	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	10	100	nA
R _{DSon} drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 175 ^{\circ}\text{C};$ see Figure 12; see Figure 13	-	6.65	7.8	mΩ	
		$V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ °C};$ see Figure 13	-	4.46	5.2	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 100 \text{ °C};$ see Figure 12; see Figure 13	-	4.9	5.8	mΩ
	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ °C};$ see Figure 13	-	3.5	4.1	mΩ	
R _G	gate resistance	f = 1 MHz	-	1	-	Ω
Dynamic c	haracteristics					
$Q_{G(tot)}$	total gate charge	I_D = 15 A; V_{DS} = 15 V; V_{GS} = 4.5 V; see Figure 14; see Figure 15	-	19	-	nC
		$I_D = 15 \text{ A}$; $V_{DS} = 15 \text{ V}$; $V_{GS} = 10 \text{ V}$; see Figure 14; see Figure 15	-	41.5	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	30	-	nC
Q _{GS}	gate-source charge	$I_D = 15 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V};$	-	8	-	nC
Q _{GS(th)}	pre-threshold gate-source charge	see <u>Figure 14</u> ; see <u>Figure 15</u>	-	4	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	4	-	nC
Q_{GD}	gate-drain charge		-	5	-	nC
V _{GS(pl)}	gate-source plateau voltage	$I_D = 15 \text{ A}$; $V_{DS} = 15 \text{ V}$; see <u>Figure 14</u> ; see <u>Figure 15</u>	-	2.7	-	V
C _{iss}	input capacitance	$V_{DS} = 15 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$	-	2400	-	pF
C _{oss}	output capacitance	T _j = 25 °C; see <u>Figure 16</u>	-	500	-	pF
C _{rss}	reverse transfer capacitance		-	240	-	pF

 Table 7.
 Characteristics ...continued

Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t _{d(on)}	turn-on delay time	V_{DS} = 15 V; R_L = 0.5 Ω ; V_{GS} = 10 V; $R_{G(ext)}$ = 5.6 Ω	-	28	-	ns
t _r	rise time		-	58	-	ns
$t_{d(off)}$	turn-off delay time		-	44	-	ns
t _f	fall time		-	21	-	ns
Source-dra	ain diode					
V_{SD}	source-drain voltage	$I_S = 15 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ °C}$; see Figure 17	-	0.81	1.2	V
t _{rr}	reverse recovery time	$I_S = 15 \text{ A}; dI_S/dt = -100 \text{ A}/\mu s;$	-	35	-	ns
Q _r	recovered charge	$V_{GS} = 0 \text{ V}; V_{DS} = 15 \text{ V}$	-	30	-	nC

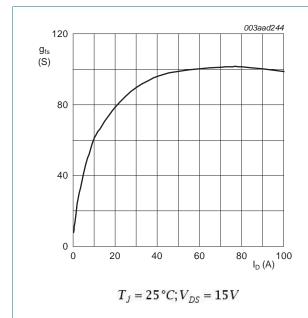


Fig 5. Forward transconductance as a function of drain current; typical values

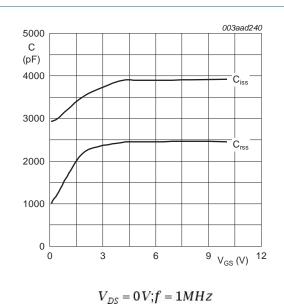


Fig 6. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

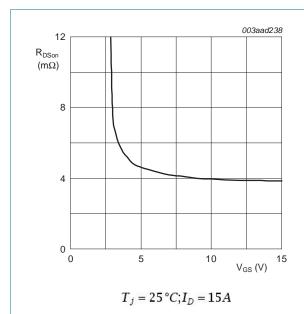


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

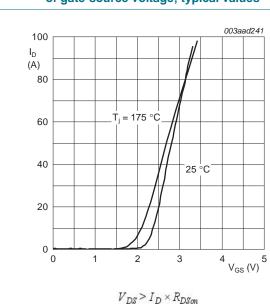


Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

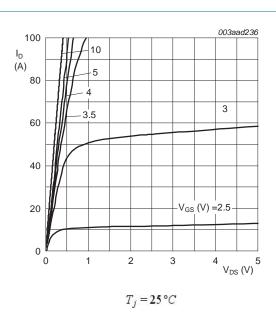
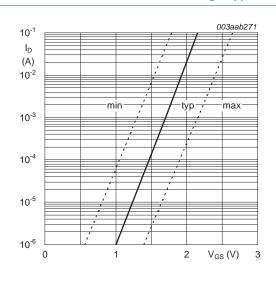


Fig 8. Output characteristics: drain current as a function of drain-source voltage; typical values



 $T_j = 25 \,^{\circ}C; V_{DS} = 5V$

Fig 10. Sub-threshold drain current as a function of gate-source voltage

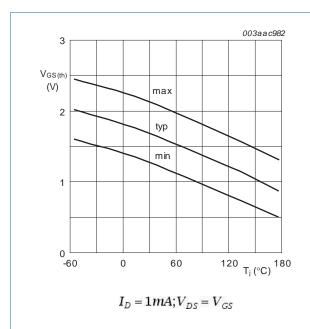


Fig 11. Gate-source threshold voltage as a function of junction temperature

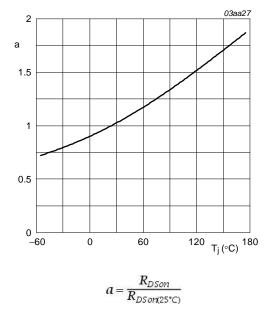


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

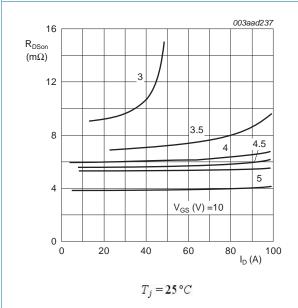


Fig 13. Drain-source on-state resistance as a function of drain current; typical values

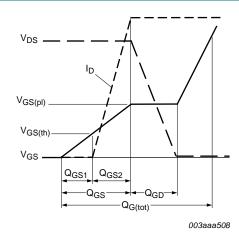


Fig 14. Gate charge waveform definitions

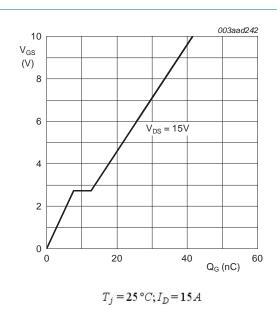
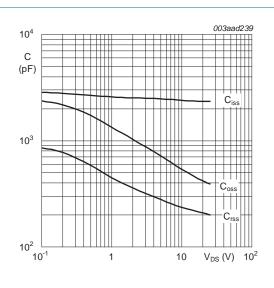
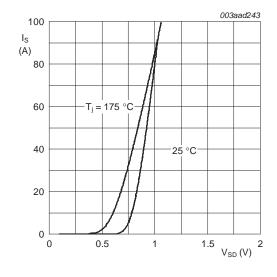


Fig 15. Gate-source voltage as a function of gate charge; typical values



$$V_{GS} = 0V; f = 1MHz$$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



 $V_{GS} = 0 V$

Fig 17. Source current as a function of source-drain voltage; typical values

8. Package outline

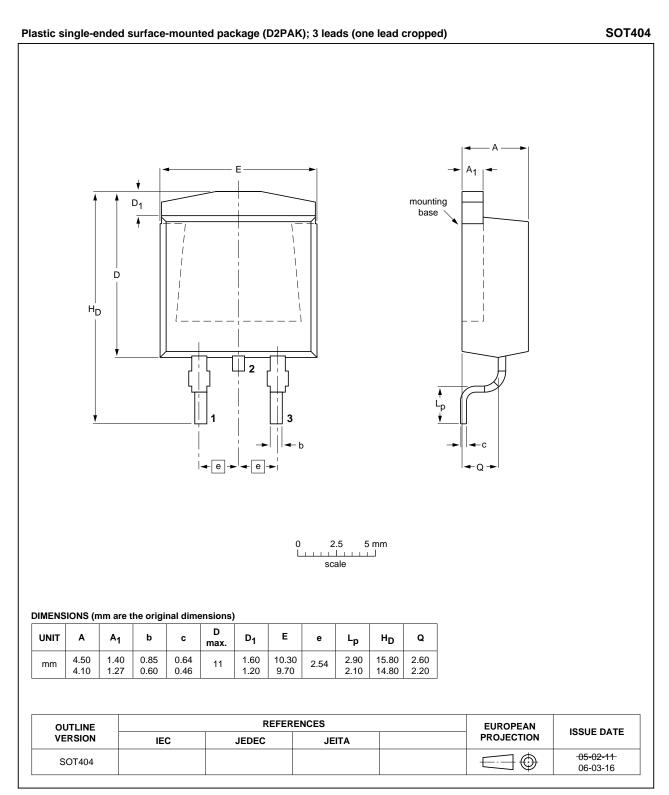


Fig 18. Package outline SOT404 (D2PAK)

9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN4R3-30BL v.1	20120322	Product data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status[1] [2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Nexperia

N-channel 30 V 4.1 mΩ logic level MOSFET in D2PAK

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