1. General description

PNP/PNP matched double transistor in a very small SOT353 (SC-88A) Surface-Mounted Device (SMD) plastic package.

PNP/PNP h_{FE1}/h_{FE2} 0.95 complement: PMP5501G

NPN/NPN complement: PMP4201G

2. Features and benefits

- Current gain matching
- Base-emitter voltage matching
- Common emitter configuration
- Application-optimized pinout
- AEC-Q101 qualified

3. Applications

- Current mirror
- Differential amplifier

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Per transistor						
V _{CEO}	collector-emitter voltage	open base	-	-	-45	V
Ic	collector current		-	-	-100	mA
h _{FE}	DC current gain	V _{CE} = -5 V; I _C = -2 mA; T _{amb} = 25 °C	200	290	450	
Per device			 •			·
h _{FE1} /h _{FE2}	DC current gain matching	$V_{CE} = -5 \text{ V}; I_{C} = -2 \text{ mA}; T_{amb} = 25 ^{\circ}\text{C}$	0.98	1	1.02	
V _{BE1} -V _{BE2}	base-emitter voltage matching		-2	-	2	mV



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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	B1	base TR1	□5 □4	C1 C2
2	E1, E2	common emitter (TR1 and TR2)		TR1 TR2
3	B2	base TR2		
4	C2	collector TR2	∐1 ∐2 ∐3	B1 E1; E2 B2
5	C1	collector TR1	TSSOP5 (SOT353)	006aaa551

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMP5201G		plastic, surface-mounted package; 5 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body	<u>SOT353</u>

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PMP5201G	R5%

^{[1] % =} placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transist	or		•			
V _{CBO}	collector-base voltage	open emitter		-	-50	V
V_{CEO}	collector-emitter voltage	open base		-	-45	V
V_{EBO}	emitter-base voltage	open collector		-	-5	V
I _C	collector current			-	-100	mA
I _{CM}	peak collector current	t _p ≤ 1 ms; single pulse		-	-200	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	200	mW
Per device						
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	300	mW
Tj	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C

^[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

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9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	416	K/W

^[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per transisto	or						
I _{CBO}	collector-base cut-off	V _{CB} = -30 V; I _E = 0 A; T _{amb} = 25 °C		-	-	-15	nA
CL	current	V _{CB} = -30 V; I _E = 0 A; T _j = 150 °C		-	-	-5	μA
I _{EBO}	emitter-base cut-off current	V _{EB} = -5 V; I _C = 0 A; T _{amb} = 25 °C		-	-	-100	nA
h _{FE}	DC current gain	V _{CE} = -5 V; I _C = -10 μA; T _{amb} = 25 °C		-	250	-	
		V_{CE} = -5 V; I_{C} = -2 mA; T_{amb} = 25 °C		200	290	450	
V _{CEsat}	collector-emitter	I_C = -10 mA; I_B = -0.5 mA; T_{amb} = 25 °C		-	-50	-200	mV
	saturation voltage	I_C = -100 mA; I_B = -5 mA; $\delta \le 0.02$; T_{amb} = 25 °C		-	-200	-400	mV
V _{BEsat}	base-emitter saturation	I_C = -10 mA; I_B = -0.5 mA; T_{amb} = 25 °C	[1]	-	-760	-	mV
	voltage	I_C = -100 mA; I_B = -5 mA; T_{amb} = 25 °C	[1]	-	-920	-	mV
V _{BE}	base-emitter voltage	V _{CE} = -5 V; I _C = -2 mA; T _{amb} = 25 °C	[2]	-600	-650	-700	mV
		V _{CE} = -5 V; I _C = -10 mA; T _{amb} = 25 °C	[2]	-	-	-760	mV
C _c	collector capacitance	V _{CB} = -10 V; I _E = 0 A; i _e = 0 A; f = 1 MHz; T _{amb} = 25 °C		-	-	2.2	pF
C _e	emitter capacitance	V_{EB} = -0.5 V; I_{C} = 0 A; i_{c} = 0 A; f = 1 MHz; f_{amb} = 25 °C		-	10	-	pF
f _T	transition frequency	V_{CE} = -5 V; I_{C} = -10 mA; f = 100 MHz; T_{amb} = 25 °C		100	175	-	MHz
NF	noise figure	V_{CE} = -5 V; I_{C} = -0.2 mA; R_{S} = 2 k Ω ; f = 10 Hz to 15.7 kHZ; T_{amb} = 25 °C		-	1.6	-	dB
		V_{CE} = -5 V; I_{C} = -0.2 mA; R_{S} = 2 k Ω ; f = 1 kHz; B = 200 Hz		-	3.1	-	dB
Per device		,			1	1	1
h _{FE1} /h _{FE2}	DC current gain matching	V_{CE} = -5 V; I_{C} = -2 mA; T_{amb} = 25 °C		0.98	1	1.02	
V _{BE1} -V _{BE2}	base-emitter voltage matching			-2	-	2	mV

^[1] V_{BEsat} decreases by about 1.7 mV/K with increasing temperature.

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^[2] V_{BE} decreases by about 2 mV/K with increasing temperature.

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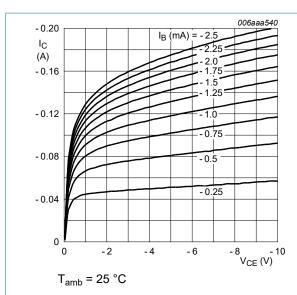
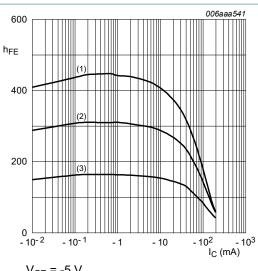


Fig. 1. Per transistor: Collector current as a function of collector-emitter voltage; typical values

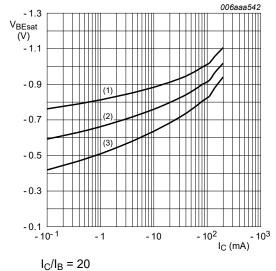


$$V_{CE} = -5 V$$

$$(1) T_{amb} = 100 ° ($$

(2)
$$T_{amb} = 25 \, ^{\circ}C$$

Fig. 2. Per transistor: DC current gain as a function of collector current; typical values



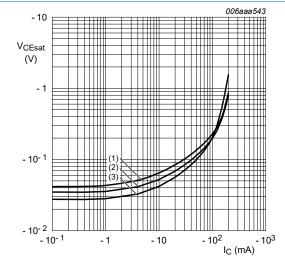
$$I_{\rm C}/I_{\rm B} = 20$$

(1)
$$T_{amb} = -55 \, ^{\circ}C$$

(2)
$$T_{amb} = 25 \, ^{\circ}C$$

(3)
$$T_{amb} = 100 \, ^{\circ}C$$

Fig. 3. Per transistor: Base-emitter saturation voltage as a function of collector current; typical values



$$I_{\rm C}/I_{\rm B} = 20$$

$$(1) T_{amb} = 100 °C$$

(2)
$$T_{amb} = 25 \, ^{\circ}C$$

(3)
$$T_{amb} = -55 \, ^{\circ}C$$

Fig. 4. Per transistor: Collector-emitter saturation voltage as a function of collector current; typical values

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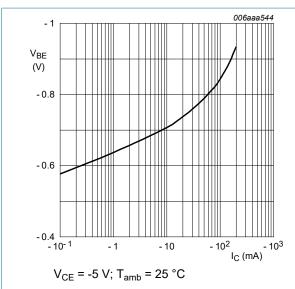


Fig. 5. Per transistor: Base-emitter voltage as a function of collector current; typical values

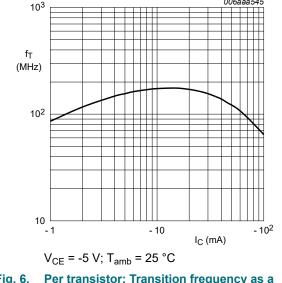


Fig. 6. Per transistor: Transition frequency as a function of collector current; typical values

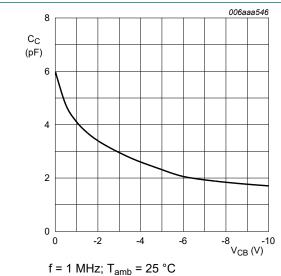


Fig. 7. Per transistor: Collector capacitance as a function of collector-base voltage; typical values

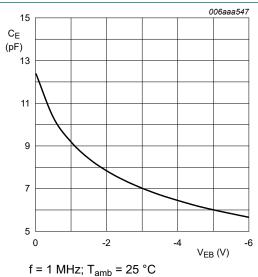
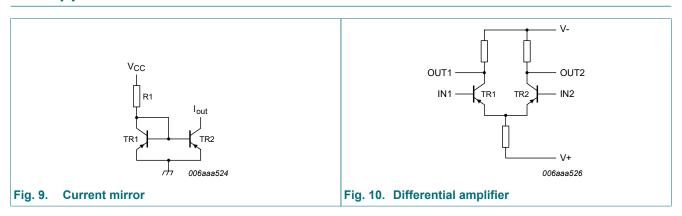


Fig. 8. Per transistor: Emitter capacitance as a function of emitter-base voltage; typical values

11. Application information



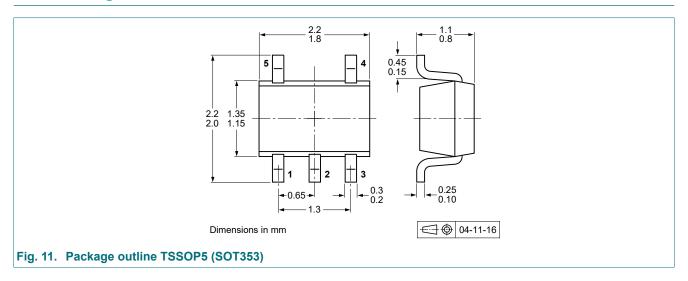
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12. Test information

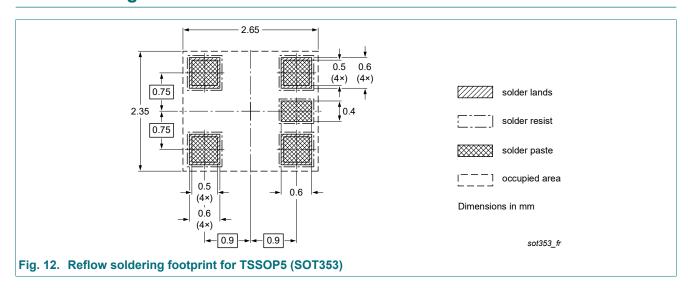
Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

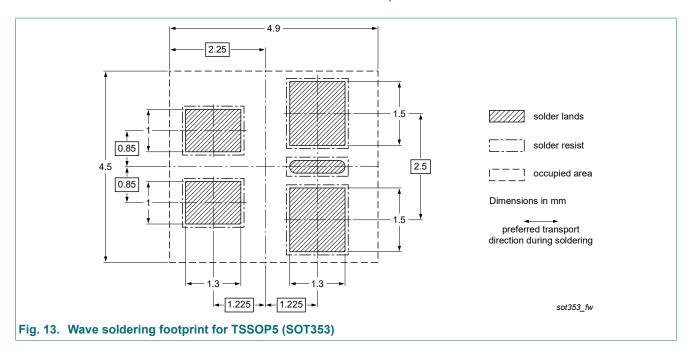
13. Package outline



14. Soldering



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15. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes		
PMP5201G v.4	20221228	Product data sheet	-	PMP5201V_G_Y_3		
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guidelines on Nexperia. Legal texts have been adapted to the new company name where appropriate. Family data sheet splitted to single type data sheets. Packing information removed. 					
PMP5201V_G_Y_3	20090828	Product data sheet	-	PMP5201V_G_Y_2		
PMP5201V_G_Y_2	20060214	Product data sheet	-	PMP5201G_Y_1		
PMP5201G_Y_1	20060214	Product data sheet	-	-		

16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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