



PESD5V0L2UMB-Q

Low capacitance unidirectional double ESD protection array

24 April 2023

Product data sheet

1. General description

Low capacitance unidirectional double ElectroStatic Discharge (ESD) protection array, designed to protect up to two signal lines from the damage caused by ESD and other transients. The device is housed in a leadless ultra small SOT883B Surface-Mounted Device (SMD) plastic package.

2. Features and benefits

- ESD protection of up to two lines
- Low diode capacitance $C_d = 16$ pF
- Low clamping voltage $V_{CL} = 10$ V
- Ultra low leakage current $I_{RM} = 5$ nA
- ESD protection up to 15 kV
- IEC 61000-4-2; level 4 (ESD)
- IEC 61000-4-5 (surge); $I_{PPM} = 2.5$ A
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- Computers and peripherals
- Audio and video equipment
- Cellular handsets and accessories
- Portable electronics
- SIM card protection
- Communication systems

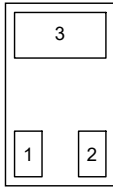
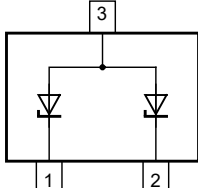
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_{amb} = 25$ °C	-	-	5	V
C_d	diode capacitance	$f = 1$ MHz; $V_R = 0$ V; $T_{amb} = 25$ °C	-	16	19	pF

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 Transparent top view DFN1006B-3 (SOT883B)	 006aac923
2	K2	cathode (diode 2)		
3	CA	common anode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0L2UMB-Q	DFN1006B-3	plastic, leadless ultra small plastic package; 3 solder lands; 0.35 mm pitch; 1.0 mm x 0.6 mm x 0.37 mm body	SOT883B

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD5V0L2UMB-Q	0001 1011

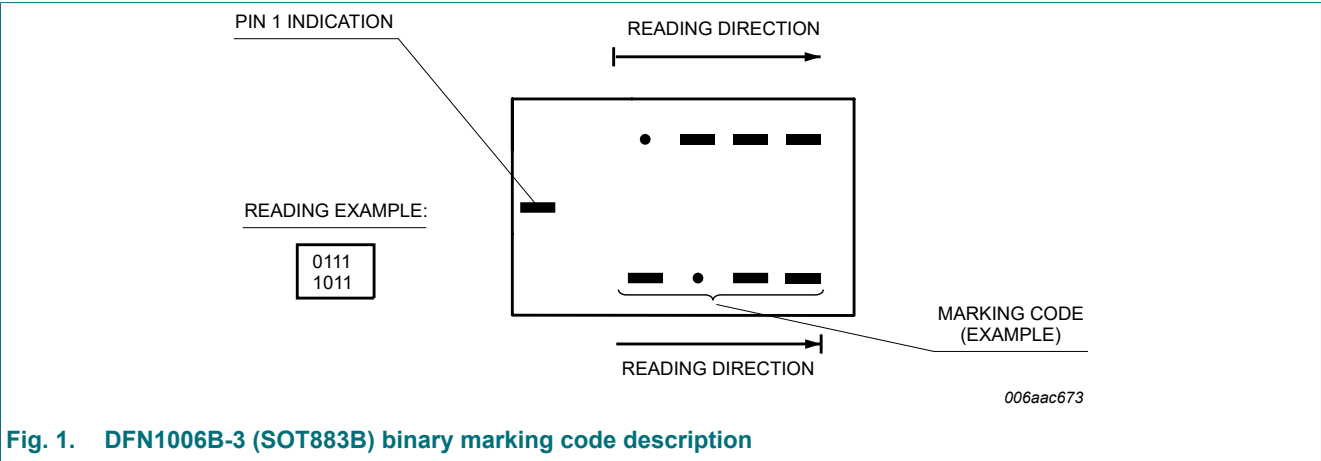


Fig. 1. DFN1006B-3 (SOT883B) binary marking code description

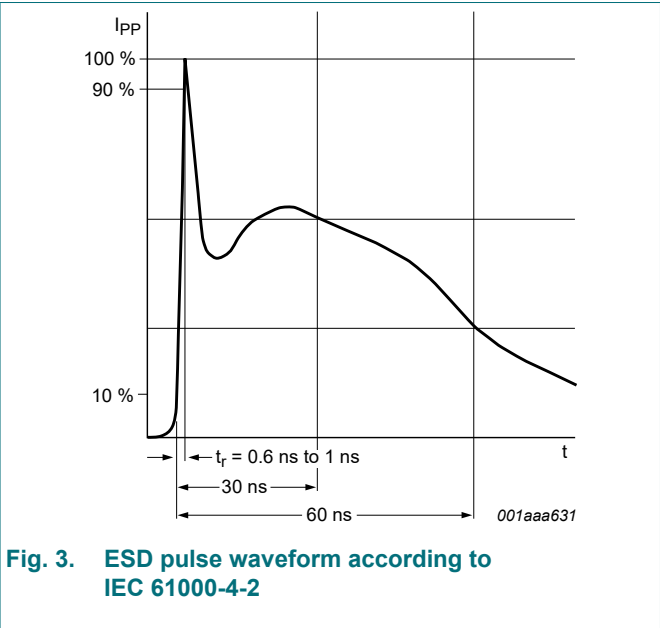
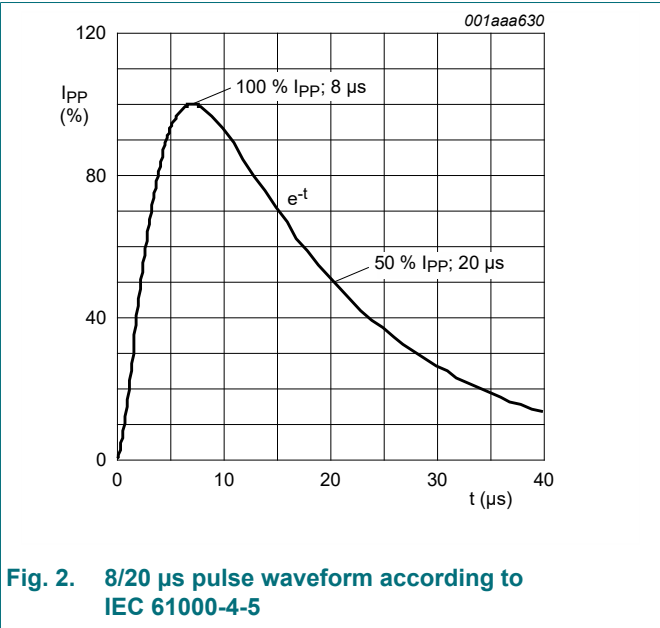
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I _{PPM}	rated peak pulse current	t _p = 8/20 μs	[1] [2]	-	2.5	A
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V _{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[3] [2]	-	15	kV
		machine model	[2]	-	400	V
		MIL-STD-883; human body model (HBM)		-	10	kV

- [1] Device stressed with ten non-repetitive current pulses (8/20 μs exponential decay waveform according to IEC 61000-4-5).
[2] Measured from pin 1 or 2 to 3.
[3] Device stressed with ten non-repetitive ESD pulses.

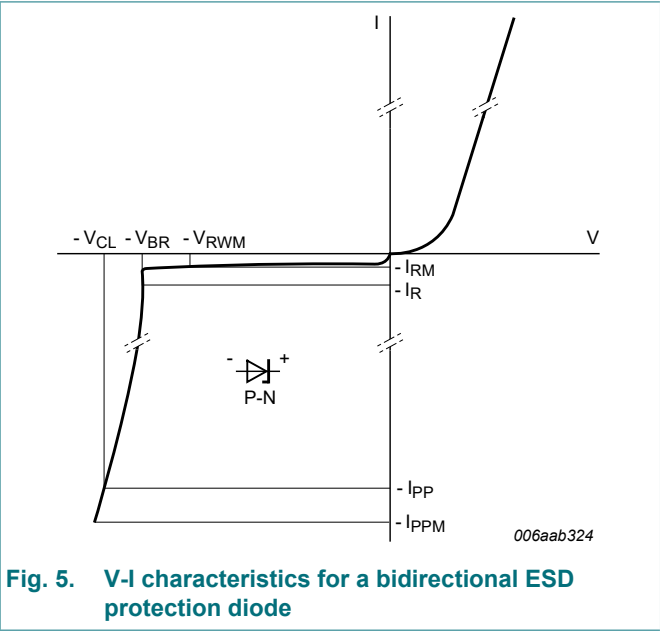
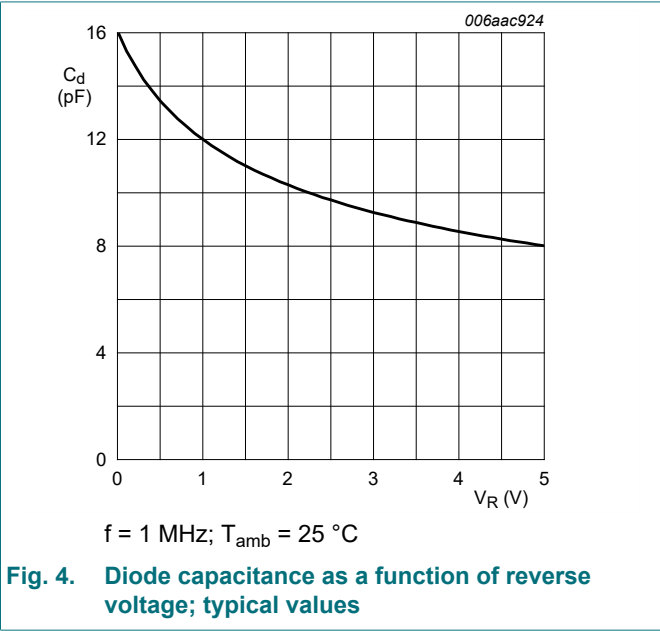


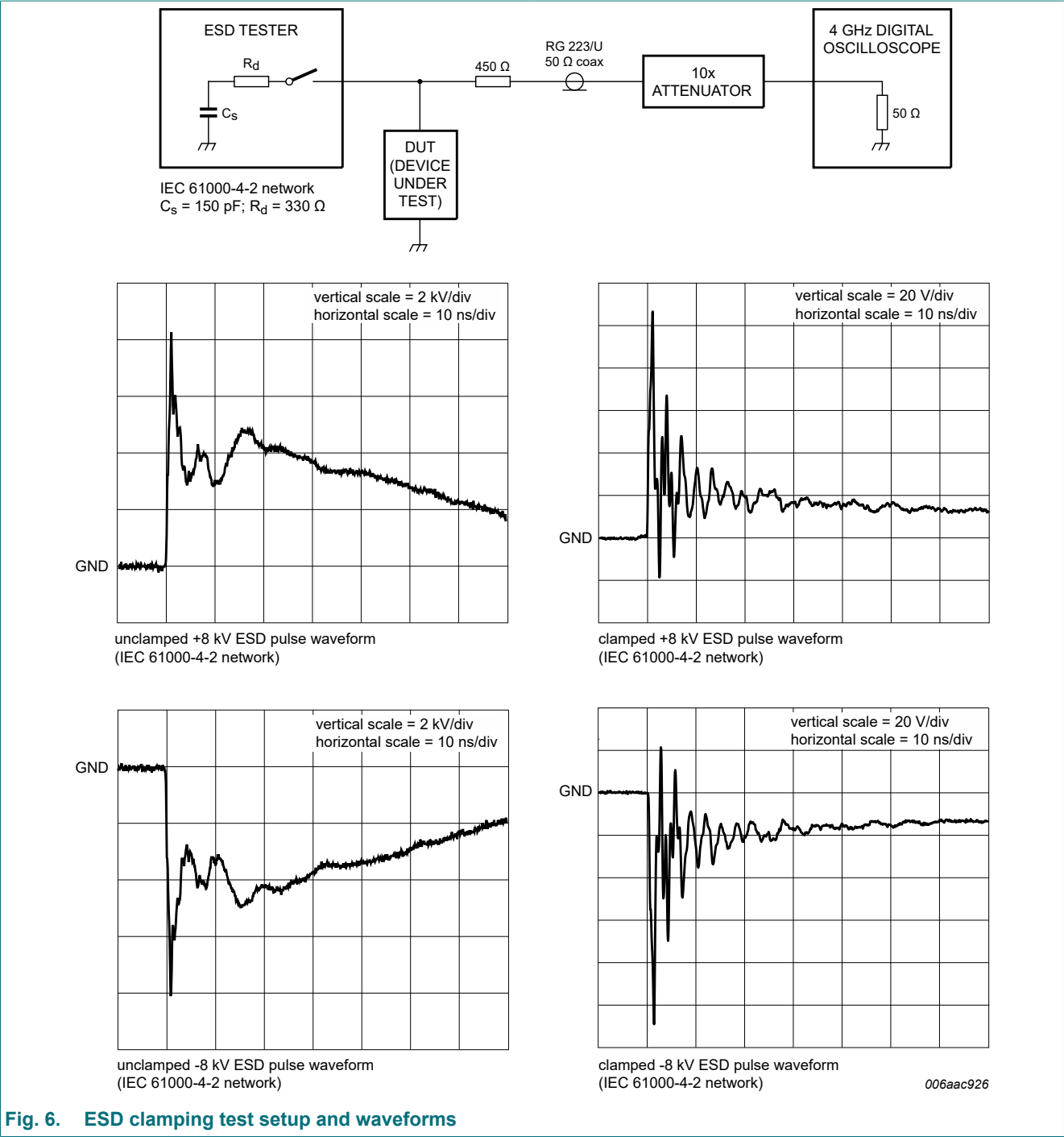
9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_{amb} = 25\text{ }^{\circ}\text{C}$		-	-	5	V
V_{BR}	breakdown voltage	$I_R = 1\text{ mA}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$		6.46	6.8	7.14	V
I_{RM}	reverse leakage current	$V_{RWM} = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$		-	5	25	nA
C_d	diode capacitance	$f = 1\text{ MHz}$; $V_R = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$		-	16	19	pF
		$f = 1\text{ MHz}$; $V_R = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$		-	8	11	pF
V_{CL}	clamping voltage	$I_{PP} = 1\text{ A}$; $t_p = 8/20\text{ }\mu\text{s}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$	[1] [2]	-	-	10	V
			[1] [3]	-	-	11	V
		$I_{PPM} = 2.5\text{ A}$; $t_p = 8/20\text{ }\mu\text{s}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$	[1] [2]	-	-	13	V
			[1] [3]	-	-	15	V
R_{dyn}	dynamic resistance	$I_R = 10\text{ A}$; $t_p = 100\text{ ns}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$	[4]	-	0.9	-	Ω

- [1] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.
[2] Measured from pin 1 or 2 to 3.
[3] Measured from pin 1 to 2.
[4] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008.





10. Application information

The device is designed for the protection of one bidirectional data or signal line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both, positive and negative with respect to ground.

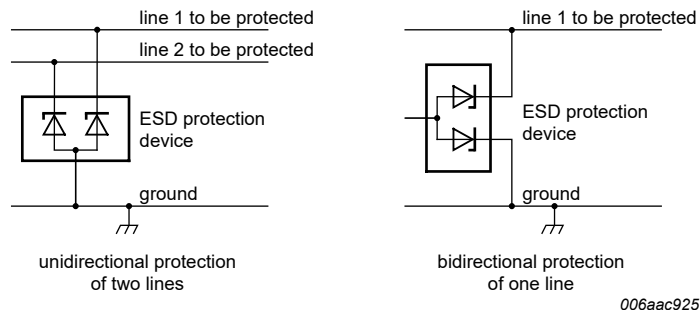


Fig. 7. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

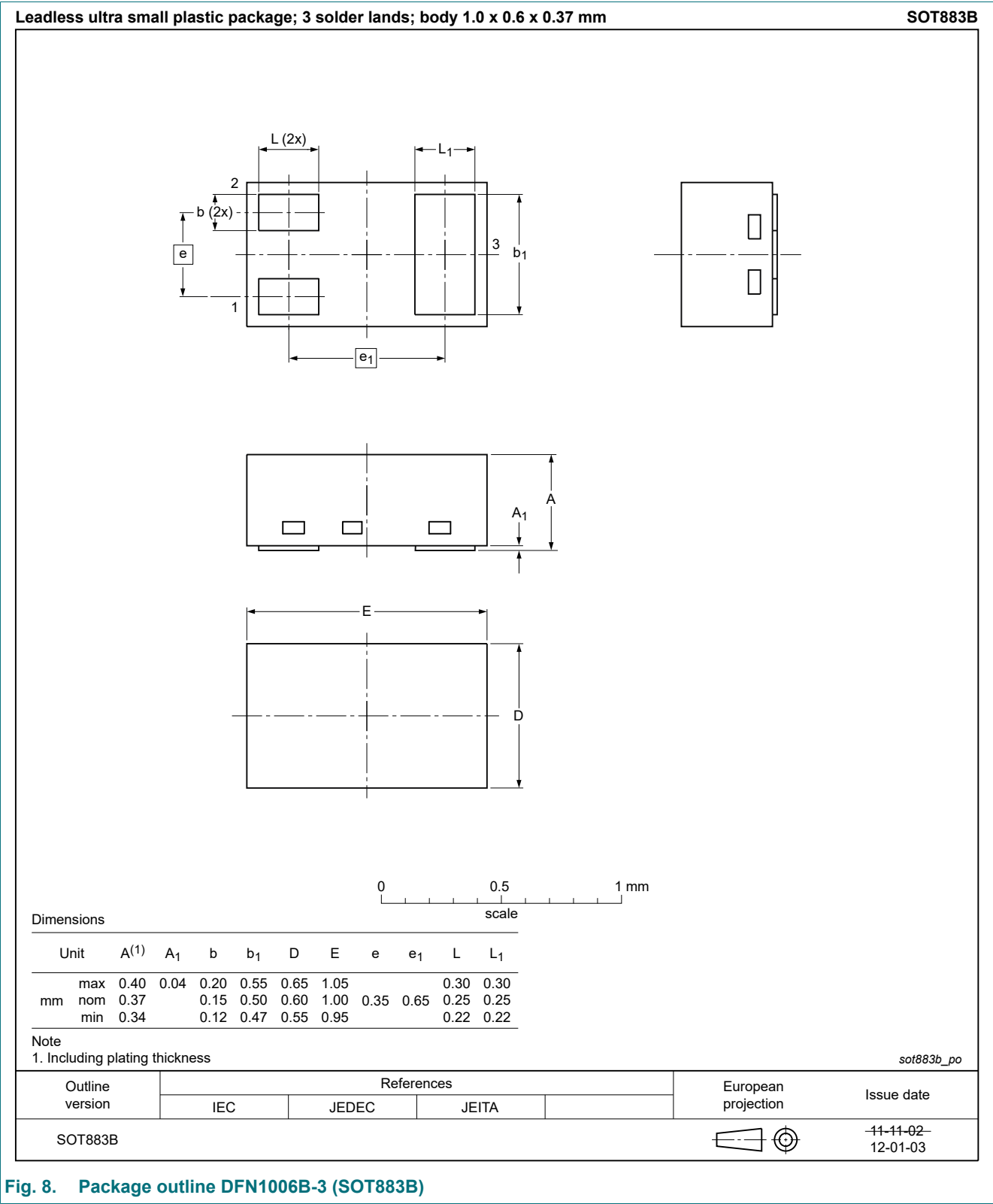
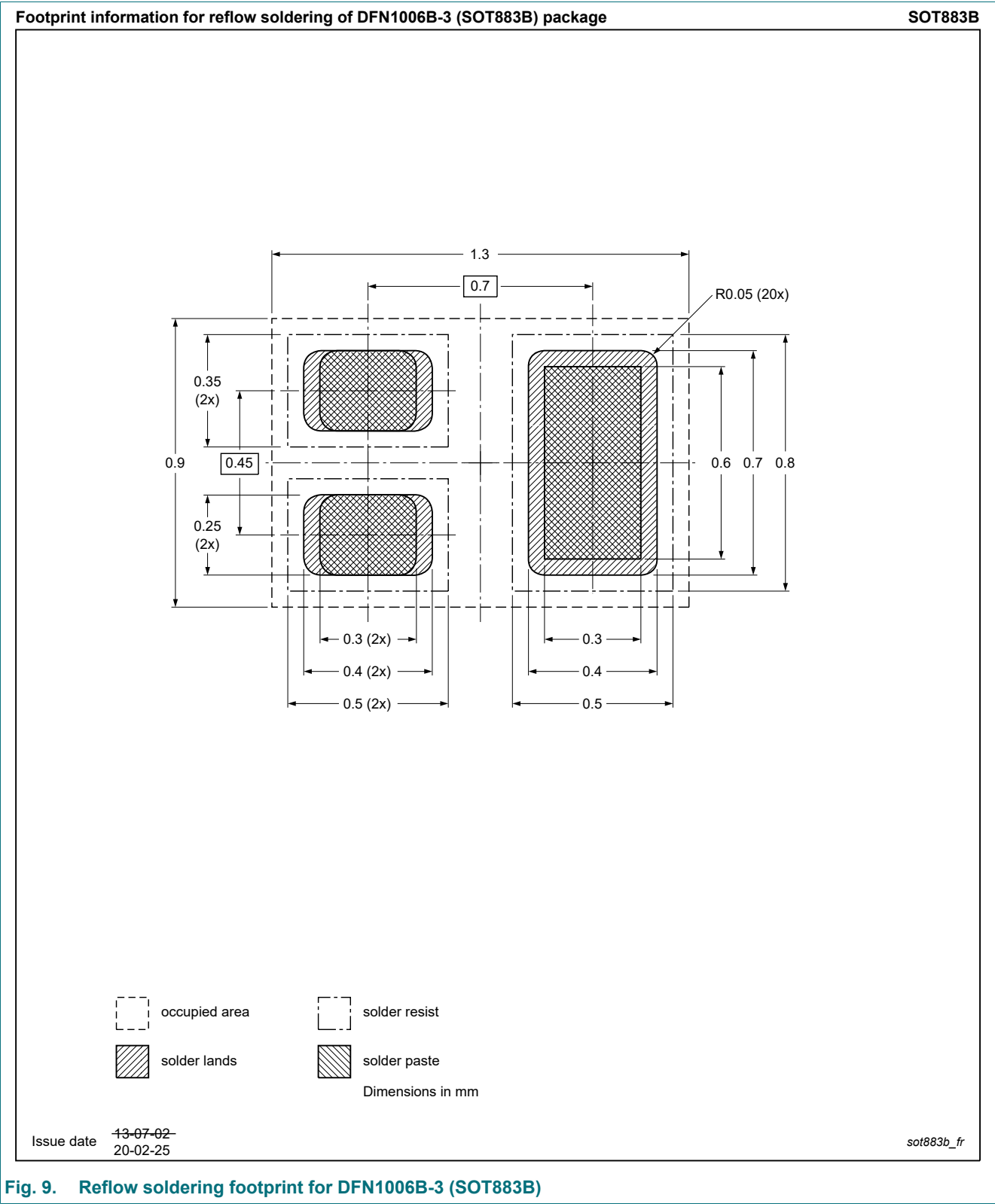


Fig. 8. Package outline DFN1006B-3 (SOT883B)

13. Soldering



14. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0L2UMB-Q v.1	20230424	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 24 April 2023

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