

# 74AVC4T3144

4-bit dual-supply buffer/level translator; 3-state

Rev. 2 — 24 July 2018

Product data sheet

## 1. General description

The 74AVC4T3144 is a 4-bit, dual-supply level translating buffer with 3-state outputs. It features four data inputs (An and B4), four data outputs (YBn and YA4), and an output enable input ( $\overline{OE}$ ). The device is configured to translate three inputs from  $V_{CC(A)}$  to  $V_{CC(B)}$  and one input from  $V_{CC(B)}$  to  $V_{CC(A)}$ .  $\overline{OE}$ , An and YA4 are referenced to  $V_{CC(A)}$  and YBn and B4 are referenced to  $V_{CC(B)}$ . A HIGH on  $\overline{OE}$  causes the outputs to assume a high-impedance OFF-state.

The device is fully specified for partial power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables outputs, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either  $V_{CC(A)}$  or  $V_{CC(B)}$  are at GND level, all outputs are in the high-impedance OFF-state.

## 2. Features and benefits

- Wide supply voltage range:
  - $V_{CC(A)}$ : 0.8 V to 3.6 V
  - $V_{CC(B)}$ : 0.8 V to 3.6 V
- Complies with JEDEC standards:
  - JESD8-12 (0.8 V to 1.3 V)
  - JESD8-11 (0.9 V to 1.65 V)
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8-B (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114E Class 3B exceeds 8000 V
  - CDM JESD22-C101C exceeds 1000 V
- Maximum data rates:
  - 380 Mbit/s ( $\geq 1.8$  V to 3.3 V translation)
  - 200 Mbit/s ( $\geq 1.1$  V to 3.3 V translation)
  - 200 Mbit/s ( $\geq 1.1$  V to 2.5 V translation)
  - 200 Mbit/s ( $\geq 1.1$  V to 1.8 V translation)
  - 150 Mbit/s ( $\geq 1.1$  V to 1.5 V translation)
  - 100 Mbit/s ( $\geq 1.1$  V to 1.2 V translation)
- Suspend mode
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Specified from  $-40$  °C to  $+85$  °C and  $-40$  °C to  $+125$  °C

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74AVC4T3144GU12	-40 °C to +125 °C	XQFN12	plastic, extremely thin quad flat package; no leads; 12 terminals; body 1.70 x 2.0 x 0.50 mm	SOT1174-1

### 4. Marking

Table 2. Marking codes

Type number	Marking code
74AVC4T3144GU12	Bd

### 5. Functional diagram

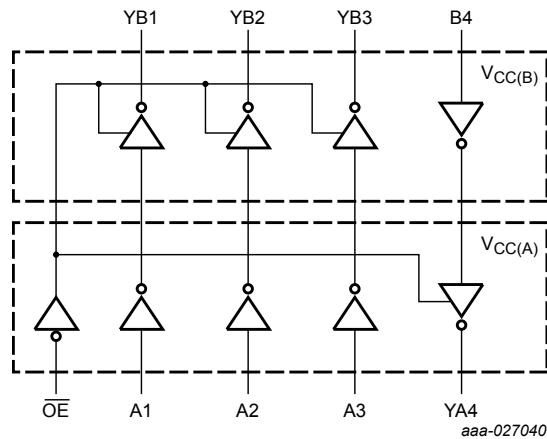


Fig. 1. Logic symbol

## 6. Pinning information

### 6.1. Pinning

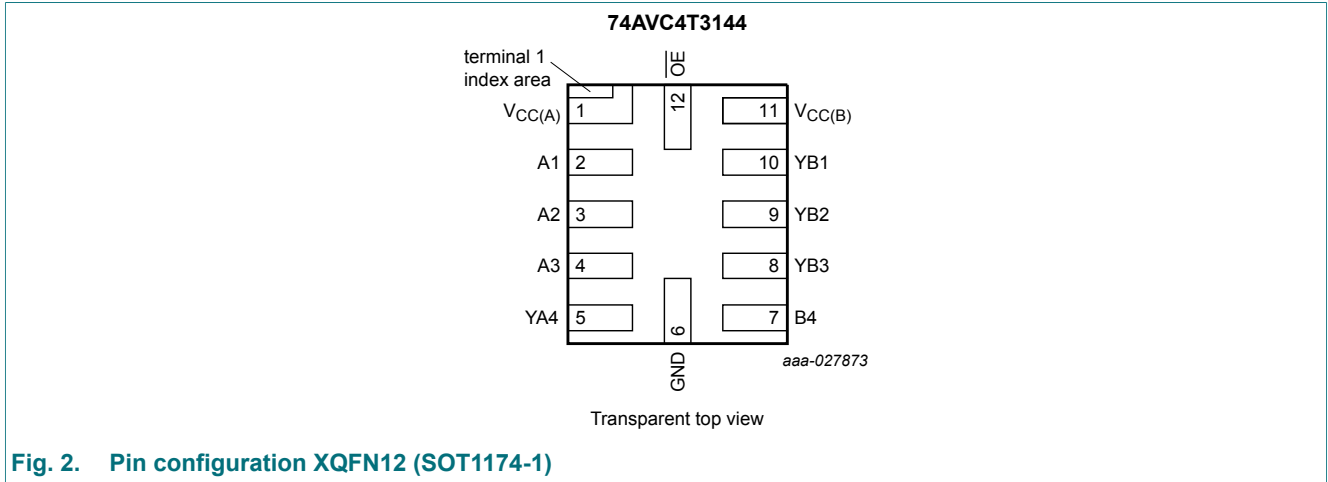


Fig. 2. Pin configuration XQFN12 (SOT1174-1)

### 6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
V <sub>CC(A)</sub>	1	supply voltage A (A1, A2, A3, YA4 and OE pins are referenced to V <sub>CC(A)</sub> )
A1, A2, A3, B4	2, 3, 4, 7	data input
GND	6	ground (0 V)
YB1, YB2, YB3, YA4	10, 9, 8, 5	data output
OE	12	output enable input (active LOW)
V <sub>CC(B)</sub>	11	supply voltage B (YB1, YB2, YB3 and B4 pins are referenced to V <sub>CC(B)</sub> )

## 7. Functional description

Table 4. Function table [1] [2]

Supply voltage	Input	Input	Output
V <sub>CC(A)</sub> , V <sub>CC(B)</sub>	OE	An, B4	YBn, YA4
0.8 V to 3.6 V	L	L	L
0.8 V to 3.6 V	L	H	H
0.8 V to 3.6 V	H	X	Z
GND [3]	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

[2] The A1, A2, A3, YA4 and OE pins are referenced to V<sub>CC(A)</sub>; The YB1, YB2, YB3 and B4 pins are referenced to V<sub>CC(B)</sub>.

[3] If at least one of V<sub>CC(A)</sub> or V<sub>CC(B)</sub> is at GND level, the device goes into suspend mode.

## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		-0.5	+4.6	V
$V_{CC(B)}$	supply voltage B		-0.5	+4.6	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage	[1]	-0.5	+4.6	V
$I_{OK}$	output clamping current	$V_O < 0$ V	-50	-	mA
$V_O$	output voltage	Active mode [1] [2] [3]	-0.5	$V_{CCO} + 0.5$	V
		Suspend or 3-state mode [1]	-0.5	+4.6	V
$I_O$	output current	$V_O = 0$ V to $V_{CCO}$ [2]	-	$\pm 50$	mA
$I_{CC}$	supply current	$I_{CC(A)}$ or $I_{CC(B)}$	-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	-	250	mW

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2]  $V_{CCO}$  is the supply voltage associated with the output port.

[3]  $V_{CCO} + 0.5$  V should not exceed 4.6 V.

## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		0.8	3.6	V
$V_{CC(B)}$	supply voltage B		0.8	3.6	V
$V_I$	input voltage		0	3.6	V
$V_O$	output voltage	Active mode [1]	0	$V_{CCO}$	V
		Suspend or 3-state mode	0	3.6	V
$T_{amb}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CCI} = 0.8$ V to 3.6 V [2]	-	10	ns/V

[1]  $V_{CCO}$  is the supply voltage associated with the output port.

[2]  $V_{CCI}$  is the supply voltage associated with the input port.

## 10. Static characteristics

**Table 7. Typical static characteristics at  $T_{amb} = 25\text{ °C}$  [1] [2]**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -1.5\text{ mA}$ ; $V_{CC(A)} = V_{CC(B)} = 0.8\text{ V}$	-	0.69	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 1.5\text{ mA}$ ; $V_{CC(A)} = V_{CC(B)} = 0.8\text{ V}$	-	0.07	-	V
$I_I$	input leakage current	$\overline{OE}$ input; $V_I = 0\text{ V}$ or $3.6\text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 0.8\text{ V}$ to $3.6\text{ V}$	-	$\pm 0.025$	$\pm 0.25$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	A or B port; $V_O = 0\text{ V}$ or $V_{CCO}$ ; $V_{CC(A)} = V_{CC(B)} = 3.6\text{ V}$	-	$\pm 0.5$	$\pm 2.5$	$\mu\text{A}$
		suspend mode A port; $V_O = 0\text{ V}$ or $V_{CCO}$ ; $V_{CC(A)} = 3.6\text{ V}$ ; $V_{CC(B)} = 0\text{ V}$	-	$\pm 0.5$	$\pm 2.5$	$\mu\text{A}$
		suspend mode B port; $V_O = 0\text{ V}$ or $V_{CCO}$ ; $V_{CC(A)} = 0\text{ V}$ ; $V_{CC(B)} = 3.6\text{ V}$	-	$\pm 0.5$	$\pm 2.5$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	A port; $V_I$ or $V_O = 0\text{ V}$ to $3.6\text{ V}$ ; $V_{CC(A)} = 0\text{ V}$ ; $V_{CC(B)} = 0.8\text{ V}$ to $3.6\text{ V}$	-	$\pm 0.1$	$\pm 1$	$\mu\text{A}$
		B port; $V_I$ or $V_O = 0\text{ V}$ to $3.6\text{ V}$ ; $V_{CC(B)} = 0\text{ V}$ ; $V_{CC(A)} = 0.8\text{ V}$ to $3.6\text{ V}$	-	$\pm 0.1$	$\pm 1$	$\mu\text{A}$
$C_I$	input capacitance	$\overline{OE}$ input; $V_I = 0\text{ V}$ or $3.3\text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 3.3\text{ V}$	-	2.0	-	pF
$C_{I/O}$	input/output capacitance	A and B port; $V_O = 3.3\text{ V}$ or $0\text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 3.3\text{ V}$	-	4.0	-	pF

[1]  $V_{CCO}$  is the supply voltage associated with the output port.

[2]  $V_{CCI}$  is the supply voltage associated with the data input port.

**Table 8. Static characteristics [1] [2]**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	data input					
		$V_{CCI} = 0.8\text{ V}$	$0.70V_{CCI}$	-	$0.70V_{CCI}$	-	V
		$V_{CCI} = 1.1\text{ V}$ to $1.95\text{ V}$	$0.65V_{CCI}$	-	$0.65V_{CCI}$	-	V
		$V_{CCI} = 2.3\text{ V}$ to $2.7\text{ V}$	1.6	-	1.6	-	V
		$V_{CCI} = 3.0\text{ V}$ to $3.6\text{ V}$	2	-	2	-	V
		$\overline{OE}$ input					
		$V_{CC(A)} = 0.8\text{ V}$	$0.70V_{CC(A)}$	-	$0.70V_{CC(A)}$	-	V
		$V_{CC(A)} = 1.1\text{ V}$ to $1.95\text{ V}$	$0.65V_{CC(A)}$	-	$0.65V_{CC(A)}$	-	V
		$V_{CC(A)} = 2.3\text{ V}$ to $2.7\text{ V}$	1.6	-	1.6	-	V
		$V_{CC(A)} = 3.0\text{ V}$ to $3.6\text{ V}$	2	-	2	-	V

## 4-bit dual-supply buffer/level translator; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V <sub>IL</sub>	LOW-level input voltage	data input					
		V <sub>CCI</sub> = 0.8 V	-	0.30V <sub>CCI</sub>	-	0.30V <sub>CCI</sub>	V
		V <sub>CCI</sub> = 1.1 V to 1.95 V	-	0.35V <sub>CCI</sub>	-	0.35V <sub>CCI</sub>	V
		V <sub>CCI</sub> = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		V <sub>CCI</sub> = 3.0 V to 3.6 V	-	0.8	-	0.8	V
		$\overline{OE}$ input					
		V <sub>CC(A)</sub> = 0.8 V	-	0.30V <sub>CC(A)</sub>	-	0.30V <sub>CC(A)</sub>	V
		V <sub>CC(A)</sub> = 1.1 V to 1.95 V	-	0.35V <sub>CC(A)</sub>	-	0.35V <sub>CC(A)</sub>	V
		V <sub>CC(A)</sub> = 2.3 V to 2.7 V	-	0.7	-	0.7	V
V <sub>CC(A)</sub> = 3.0 V to 3.6 V	-	0.8	-	0.8	V		
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>O</sub> = -100 μA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	V <sub>CCO</sub> - 0.1	-	V <sub>CCO</sub> - 0.1	-	V
		I <sub>O</sub> = -3 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.1 V	0.85	-	0.85	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.4 V	1.05	-	1.05	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.65 V	1.2	-	1.2	-	V
		I <sub>O</sub> = -9 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.3 V	1.75	-	1.75	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.0 V	2.3	-	2.3	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>O</sub> = 100 μA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	0.1	-	0.1	V
		I <sub>O</sub> = 3 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.1 V	-	0.25	-	0.25	V
		I <sub>O</sub> = 6 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.4 V	-	0.35	-	0.35	V
		I <sub>O</sub> = 8 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.65 V	-	0.45	-	0.45	V
		I <sub>O</sub> = 9 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.3 V	-	0.55	-	0.55	V
		I <sub>O</sub> = 12 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.0 V	-	0.7	-	0.7	V
I <sub>I</sub>	input leakage current	$\overline{OE}$ input; V <sub>I</sub> = 0 V or 3.6 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	±1	-	±5	μA
I <sub>OZ</sub>	OFF-state output current	A or B port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.6 V	-	±5	-	±30	μA
		suspend mode A port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-	±5	-	±30	μA
		suspend mode B port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 3.6 V	-	±5	-	±30	μA

## 4-bit dual-supply buffer/level translator; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I <sub>OFF</sub>	power-off leakage current	A port; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	±5	-	±30	μA
		B port; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC(B)</sub> = 0 V; V <sub>CC(A)</sub> = 0.8 V to 3.6 V	-	±5	-	±30	μA
I <sub>CC</sub>	supply current	A port; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; I <sub>O</sub> = 0 A					
		V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	10	-	55	μA
		V <sub>CC(A)</sub> = 1.1 V to 3.6 V; V <sub>CC(B)</sub> = 1.1 V to 3.6 V	-	8	-	50	μA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-	8	-	50	μA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 3.6 V	-2	-	-12	-	μA
		B port; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; I <sub>O</sub> = 0 A					
		V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	10	-	55	μA
		V <sub>CC(A)</sub> = 1.1 V to 3.6 V; V <sub>CC(B)</sub> = 1.1 V to 3.6 V	-	8	-	50	μA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-2	-	-12	-	μA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 3.6 V	-	8	-	50	μA
		A plus B port (I <sub>CC(A)</sub> + I <sub>CC(B)</sub> ); I <sub>O</sub> = 0 A; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	20	-	70	μA
		A plus B port (I <sub>CC(A)</sub> + I <sub>CC(B)</sub> ); I <sub>O</sub> = 0 A; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; V <sub>CC(A)</sub> = 1.1 V to 3.6 V; V <sub>CC(B)</sub> = 1.1 V to 3.6 V	-	16	-	65	μA
ΔI <sub>CC</sub>	additional supply current	V <sub>I</sub> = 3.0 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.6 V	-	500	-	650	μA

[1] V<sub>CCO</sub> is the supply voltage associated with the output port.

[2] V<sub>CCI</sub> is the supply voltage associated with the data input port.

**Table 9. Typical total supply current (I<sub>CC(A)</sub> + I<sub>CC(B)</sub>)**

V <sub>CC(A)</sub>	V <sub>CC(B)</sub>							Unit
	0 V	0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	0.1	0.1	0.1	0.1	0.1	0.1	μA
0.8 V	0.1	0.1	0.1	0.1	0.1	0.3	1.6	μA
1.2 V	0.1	0.1	0.1	0.1	0.1	0.1	0.8	μA
1.5 V	0.1	0.1	0.1	0.1	0.1	0.1	0.4	μA
1.8 V	0.1	0.1	0.1	0.1	0.1	0.1	0.2	μA
2.5 V	0.1	0.3	0.1	0.1	0.1	0.1	0.1	μA
3.3 V	0.1	1.6	0.8	0.4	0.2	0.1	0.1	μA

## 11. Dynamic characteristics

**Table 10. Typical power dissipation capacitance at  $V_{CC(A)} = V_{CC(B)}$  and  $T_{amb} = 25\text{ °C}$  [1] [2]**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$V_{CC(A)} = V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$C_{PD}$	power dissipation capacitance	inputs An, B4	0.2	0.2	0.2	0.2	0.3	0.5	pF
		outputs YBn, YA4	9.3	9.5	9.6	9.7	9.9	11.2	pF

[1]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

[2]  $f_i = 10\text{ MHz}$ ;  $V_i = \text{GND to } V_{CC}$ ;  $t_r = t_f = 1\text{ ns}$ ;  $C_L = 0\text{ pF}$ ;  $R_L = \infty\ \Omega$ .

**Table 11. Typical dynamic characteristics at  $V_{CC(A)} = 0.8\text{ V}$  and  $T_{amb} = 25\text{ °C}$  [1]**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5; for wave forms see Fig. 3 and Fig. 4

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$t_{pd}$	propagation delay	An to YBn	14.5	7.3	6.5	6.2	5.9	6.0	ns
		B4 to YA4	14.5	12.7	12.4	12.3	12.1	12.0	ns
$t_{dis}$	disable time	$\overline{OE}$ to YBn	14.3	14.3	14.3	14.3	14.3	14.3	ns
		$\overline{OE}$ to YA4	17.0	9.9	9.0	9.4	9.0	9.7	ns
$t_{en}$	enable time	$\overline{OE}$ to YBn	18.2	18.2	18.2	18.2	18.2	18.2	ns
		$\overline{OE}$ to YA4	19.2	10.7	9.8	9.6	9.7	10.2	ns

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .

**Table 12. Typical dynamic characteristics at  $V_{CC(B)} = 0.8\text{ V}$  and  $T_{amb} = 25\text{ °C}$  [1]**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5; for wave forms see Fig. 3 and Fig. 4

Symbol	Parameter	Conditions	$V_{CC(A)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$t_{pd}$	propagation delay	An to YBn	14.5	12.7	12.4	12.3	12.1	12.0	ns
		B4 to YA4	14.5	7.3	6.5	6.2	5.9	6.0	ns
$t_{dis}$	disable time	$\overline{OE}$ to YBn	14.3	5.5	4.1	4.0	3.0	3.5	ns
		$\overline{OE}$ to YA4	17.0	13.8	13.4	13.1	12.9	12.7	ns
$t_{en}$	enable time	$\overline{OE}$ to YBn	18.2	5.6	4.0	3.2	2.4	2.2	ns
		$\overline{OE}$ to YA4	19.2	14.6	14.1	13.9	13.7	13.6	ns

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .



Table 13. Dynamic characteristics for temperature range -40 °C to +85 °C [1]

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5; for wave forms see Fig. 3 and Fig. 4

Symbol	Parameter	Conditions	V <sub>CC(B)</sub>										Unit
			1.2 V ±0.1 V		1.5 V ±0.1 V		1.8 V ±0.15 V		2.5 V ±0.2 V		3.3 V ±0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
<b>V<sub>CC(A)</sub> = 1.1 V to 1.3 V</b>													
t <sub>pd</sub>	propagation delay	An to YBn	2.0	10.5	1.3	7.8	1.2	6.9	1.0	5.9	0.8	5.7	ns
		B4 to YA4	2.0	10.5	1.5	9.9	1.5	9.7	1.4	9.4	1.4	9.3	ns
t <sub>dis</sub>	disable time	$\overline{OE}$ to YBn	2.0	10.0	2.0	10.0	2.0	10.0	2.0	10.0	2.0	10.0	ns
		$\overline{OE}$ to YA4	2.0	11.1	2.0	8.6	1.0	8.0	0.7	7.0	1.0	8.0	ns
t <sub>en</sub>	enable time	$\overline{OE}$ to YBn	2.0	13.5	2.0	13.5	2.0	13.5	2.0	13.5	2.0	13.5	ns
		$\overline{OE}$ to YA4	2.0	15.0	2.0	11.0	2.0	9.4	1.0	7.8	1.0	7.4	ns
<b>V<sub>CC(A)</sub> = 1.4 V to 1.6 V</b>													
t <sub>pd</sub>	propagation delay	An to YBn	1.5	9.9	1.0	7.1	1.0	6.0	0.5	4.8	0.5	4.3	ns
		B4 to YA4	1.3	7.8	1.0	7.1	0.9	6.9	0.8	6.6	0.6	6.5	ns
t <sub>dis</sub>	disable time	$\overline{OE}$ to YBn	1.0	6.0	1.0	6.0	1.0	6.0	1.0	6.0	1.0	6.0	ns
		$\overline{OE}$ to YA4	2.0	10.2	1.5	7.5	0.9	7.2	0.4	6.2	0.4	6.1	ns
t <sub>en</sub>	enable time	$\overline{OE}$ to YBn	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	ns
		$\overline{OE}$ to YA4	2.0	14.4	1.4	7.9	1.3	7.7	1.1	6.4	1.1	5.6	ns
<b>V<sub>CC(A)</sub> = 1.65 V to 1.95 V</b>													
t <sub>pd</sub>	propagation delay	An to YBn	1.5	9.7	0.9	6.9	0.8	5.7	0.5	4.5	0.3	4.0	ns
		B4 to YA4	1.2	6.9	1.0	6.0	0.8	5.7	0.5	5.5	0.5	5.3	ns
t <sub>dis</sub>	disable time	$\overline{OE}$ to YBn	0.5	5.7	0.5	5.7	0.5	5.7	0.5	5.7	0.5	5.7	ns
		$\overline{OE}$ to YA4	2.0	9.9	1.5	7.0	0.8	6.9	0.2	5.8	0.2	5.9	ns
t <sub>en</sub>	enable time	$\overline{OE}$ to YBn	1.0	6.7	1.0	6.7	1.0	6.7	1.0	6.7	1.0	6.7	ns
		$\overline{OE}$ to YA4	1.5	13.9	1.2	7.2	1.2	6.9	0.8	5.4	0.6	5.0	ns
<b>V<sub>CC(A)</sub> = 2.3 V to 2.7 V</b>													
t <sub>pd</sub>	propagation delay	An to YBn	1.4	9.4	0.8	6.6	0.5	5.5	0.4	4.2	0.2	3.7	ns
		B4 to YA4	1.0	5.9	0.5	4.8	0.5	4.5	0.4	4.2	0.3	3.9	ns
t <sub>dis</sub>	disable time	$\overline{OE}$ to YBn	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	ns
		$\overline{OE}$ to YA4	2.0	9.3	1.5	6.7	0.7	6.3	0.2	5.0	0.2	5.7	ns
t <sub>en</sub>	enable time	$\overline{OE}$ to YBn	0.6	4.5	0.6	4.5	0.6	4.5	0.6	4.5	0.6	4.5	ns
		$\overline{OE}$ to YA4	1.5	13.6	1.0	6.8	1.0	6.0	0.8	4.6	0.6	4.2	ns
<b>V<sub>CC(A)</sub> = 3.0 V to 3.6 V</b>													
t <sub>pd</sub>	propagation delay	An to YBn	1.4	9.3	0.6	6.5	0.5	5.3	0.3	3.9	0.2	3.5	ns
		B4 to YA4	0.8	5.7	0.5	4.3	0.3	4.0	0.2	3.7	0.2	3.5	ns
t <sub>dis</sub>	disable time	$\overline{OE}$ to YBn	0.2	4.5	0.2	4.5	0.2	4.5	0.2	4.5	0.2	4.5	ns
		$\overline{OE}$ to YA4	2.0	9.0	1.5	6.4	0.7	6.1	0.2	4.8	0.2	5.6	ns
t <sub>en</sub>	enable time	$\overline{OE}$ to YBn	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	ns
		$\overline{OE}$ to YA4	1.5	13.4	1.0	6.7	1.0	5.9	0.7	4.4	0.5	4.0	ns

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>; t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.

Table 14. Dynamic characteristics for temperature range -40 °C to +125 °C [1]

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5; for wave forms see Fig. 3 and Fig. 4

Symbol	Parameter	Conditions	$V_{CC(B)}$										Unit
			1.2 V $\pm 0.1$ V		1.5 V $\pm 0.1$ V		1.8 V $\pm 0.15$ V		2.5 V $\pm 0.2$ V		3.3 V $\pm 0.3$ V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
<b><math>V_{CC(A)} = 1.1</math> V to <math>1.3</math> V</b>													
$t_{pd}$	propagation delay	An to YBn	2.0	12.1	1.3	9.0	1.2	8.0	1.0	6.8	0.8	6.6	ns
		B4 to YA4	2.0	12.1	1.5	11.4	1.5	11.2	1.4	10.9	1.4	10.7	ns
$t_{dis}$	disable time	$\overline{OE}$ to YBn	2.0	11.5	2.0	11.5	2.0	11.5	2.0	11.5	2.0	11.5	ns
		$\overline{OE}$ to YA4	2.0	12.8	2.0	9.9	1.0	9.2	0.7	8.1	1.0	9.2	ns
$t_{en}$	enable time	$\overline{OE}$ to YBn	2.0	15.6	2.0	15.6	2.0	15.6	2.0	15.6	2.0	15.6	ns
		$\overline{OE}$ to YA4	2.0	17.3	2.0	12.7	2.0	10.9	1.0	9.0	1.0	8.6	ns
<b><math>V_{CC(A)} = 1.4</math> V to <math>1.6</math> V</b>													
$t_{pd}$	propagation delay	An to YBn	1.5	11.4	1.0	8.2	1.0	6.9	0.5	5.6	0.5	5.0	ns
		B4 to YA4	1.3	9.0	1.0	8.2	0.9	8.0	0.8	7.6	0.6	7.5	ns
$t_{dis}$	disable time	$\overline{OE}$ to YBn	1.0	6.9	1.0	6.9	1.0	6.9	1.0	6.9	1.0	6.9	ns
		$\overline{OE}$ to YA4	2.0	11.8	1.5	8.7	0.9	8.3	0.4	7.2	0.4	7.1	ns
$t_{en}$	enable time	$\overline{OE}$ to YBn	1.0	8.7	1.0	8.7	1.0	8.7	1.0	8.7	1.0	8.7	ns
		$\overline{OE}$ to YA4	2.0	16.6	1.4	9.1	1.3	8.9	1.1	7.4	1.1	6.5	ns
<b><math>V_{CC(A)} = 1.65</math> V to <math>1.95</math> V</b>													
$t_{pd}$	propagation delay	An to YBn	1.5	11.2	0.9	8.0	0.8	6.6	0.5	5.2	0.3	4.6	ns
		B4 to YA4	1.2	8.0	1.0	6.9	0.8	6.6	0.5	6.4	0.5	6.1	ns
$t_{dis}$	disable time	$\overline{OE}$ to YBn	0.5	6.6	0.5	6.6	0.5	6.6	0.5	6.6	0.5	6.6	ns
		$\overline{OE}$ to YA4	2.0	11.4	1.5	8.1	0.8	8.0	0.2	6.7	0.2	6.8	ns
$t_{en}$	enable time	$\overline{OE}$ to YBn	1.0	7.8	1.0	7.8	1.0	7.8	1.0	7.8	1.0	7.8	ns
		$\overline{OE}$ to YA4	1.5	16.0	1.2	8.3	1.2	8.0	0.8	6.3	0.6	5.8	ns
<b><math>V_{CC(A)} = 2.3</math> V to <math>2.7</math> V</b>													
$t_{pd}$	propagation delay	An to YBn	1.4	10.9	0.8	7.6	0.5	6.4	0.4	4.9	0.2	4.3	ns
		B4 to YA4	1.0	6.8	0.5	5.6	0.5	5.2	0.4	4.9	0.3	4.5	ns
$t_{dis}$	disable time	$\overline{OE}$ to YBn	0.2	4.6	0.2	4.6	0.2	4.6	0.2	4.6	0.2	4.6	ns
		$\overline{OE}$ to YA4	2.0	10.7	1.5	7.8	0.7	7.3	0.2	5.8	0.2	6.6	ns
$t_{en}$	enable time	$\overline{OE}$ to YBn	0.6	5.2	0.6	5.2	0.6	5.2	0.6	5.2	0.6	5.2	ns
		$\overline{OE}$ to YA4	1.5	15.7	1.0	7.9	1.0	6.9	0.8	5.3	0.6	4.9	ns
<b><math>V_{CC(A)} = 3.0</math> V to <math>3.6</math> V</b>													
$t_{pd}$	propagation delay	An to YBn	1.4	10.7	0.6	7.5	0.5	6.1	0.3	4.5	0.2	4.1	ns
		B4 to YA4	0.8	6.6	0.5	5.0	0.3	4.6	0.2	4.3	0.2	4.1	ns
$t_{dis}$	disable time	$\overline{OE}$ to YBn	0.2	5.2	0.2	5.2	0.2	5.2	0.2	5.2	0.2	5.2	ns
		$\overline{OE}$ to YA4	2.0	10.4	1.5	7.4	0.7	7.1	0.2	5.6	0.2	6.5	ns
$t_{en}$	enable time	$\overline{OE}$ to YBn	0.5	4.6	0.5	4.6	0.5	4.6	0.5	4.6	0.5	4.6	ns
		$\overline{OE}$ to YA4	1.5	15.5	1.0	7.8	1.0	6.8	0.7	5.1	0.5	4.6	ns

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .

11.1. Waveforms and test circuit

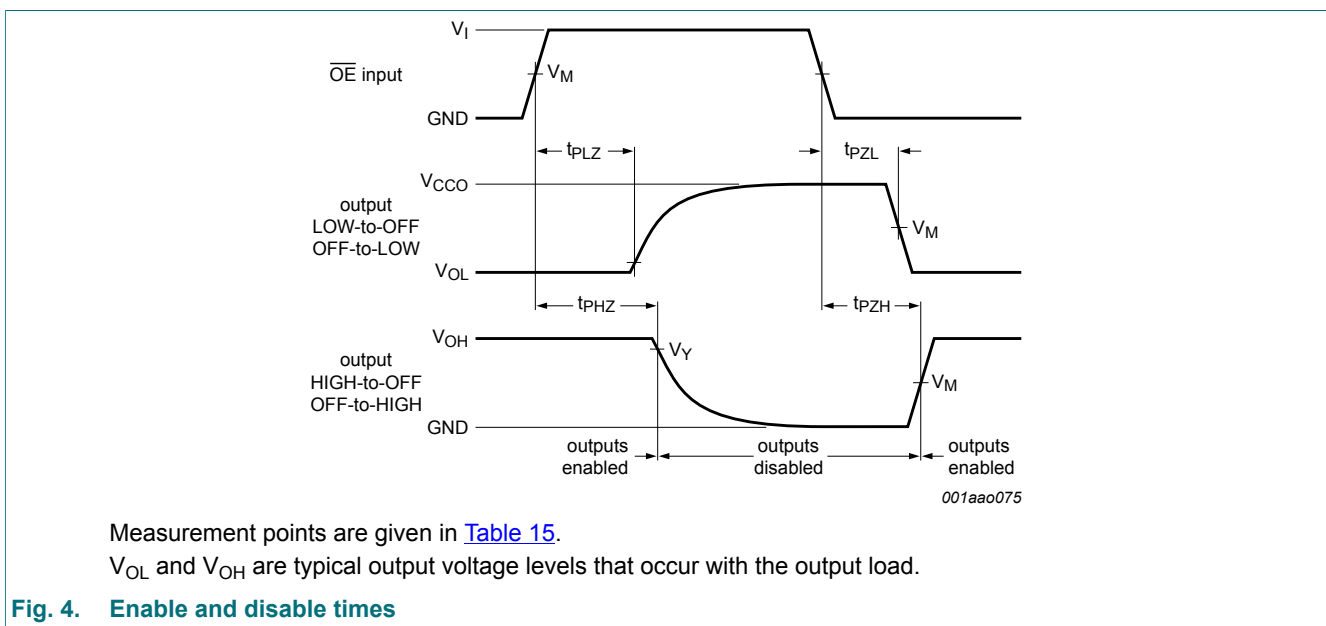
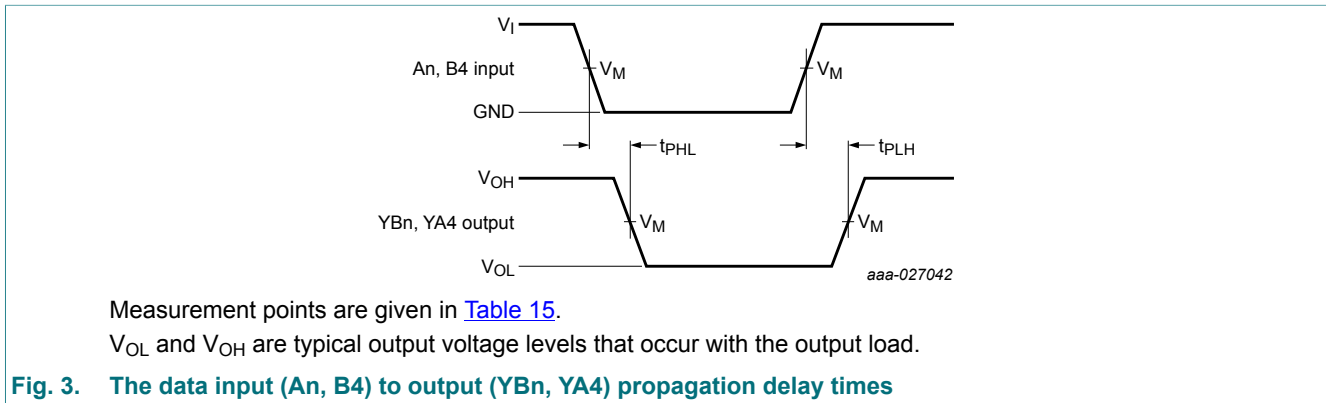
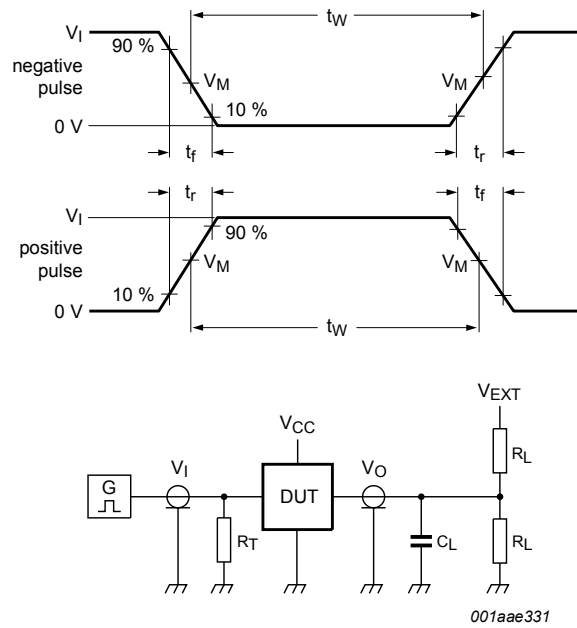


Table 15. Measurement points

Supply voltage	Input [1]	Output [2]		
$V_{CC(A)}, V_{CC(B)}$	$V_M$	$V_M$	$V_X$	$V_Y$
0.8 V to 1.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.1\text{ V}$	$V_{OH} - 0.1\text{ V}$
1.65 V to 2.7 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
3.0 V to 3.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$

[1]  $V_{CCI}$  is the supply voltage associated with the data input port.  
 [2]  $V_{CCO}$  is the supply voltage associated with the output port.



Test data is given in [Table 16](#) .

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig. 5. Test circuit for measuring switching times**

**Table 16. Test data**

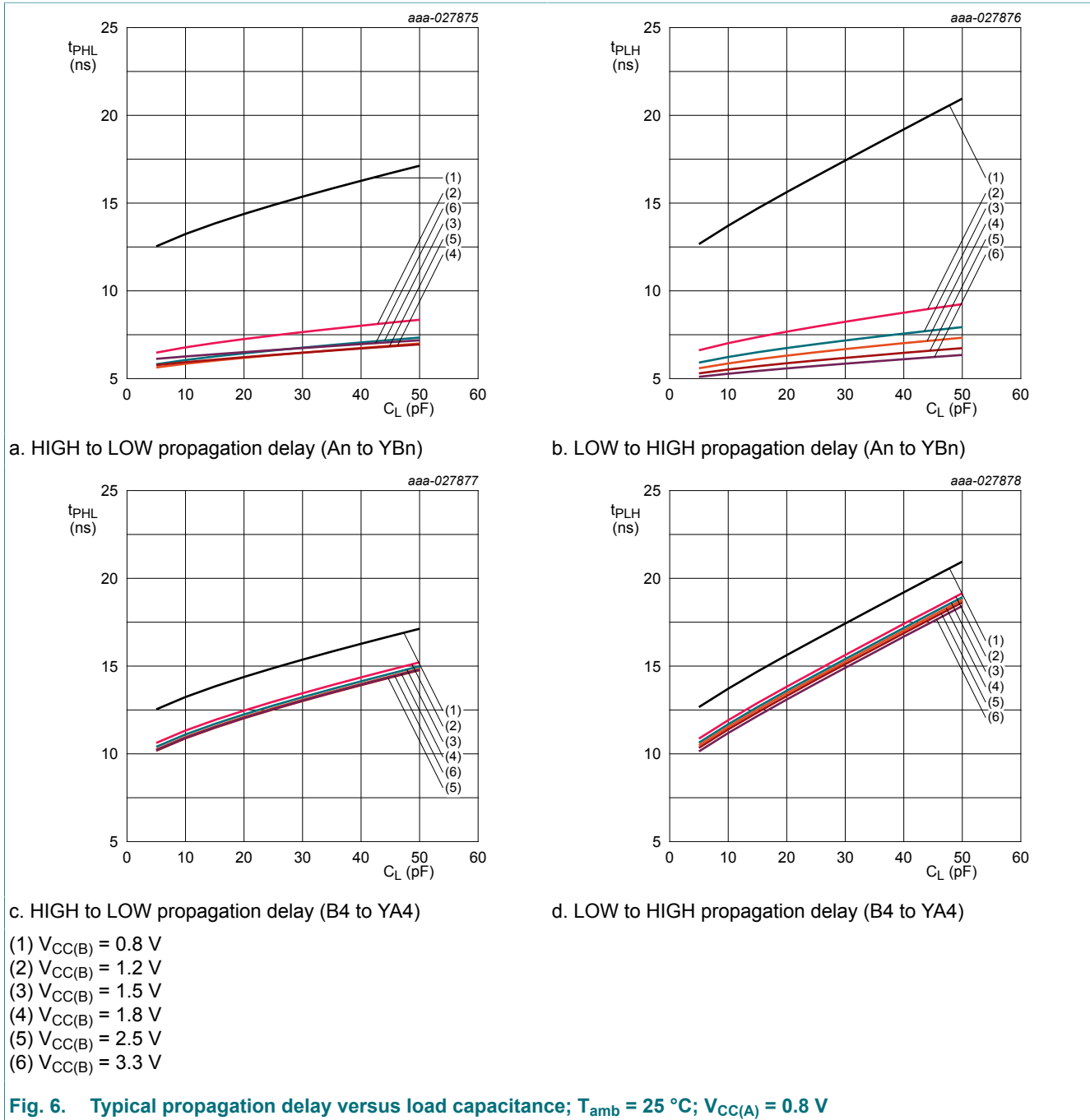
Supply voltage	Input		Load		$V_{EXT}$		
$V_{CC(A)}, V_{CC(B)}$	$V_I$ [1]	$\Delta t/\Delta V$ [2]	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$ [3]
0.8 V to 1.6 V	$V_{CCI}$	$\leq 1.0$ ns/V	15 pF	2 k $\Omega$	open	GND	$2V_{CCO}$
1.65 V to 2.7 V	$V_{CCI}$	$\leq 1.0$ ns/V	15 pF	2 k $\Omega$	open	GND	$2V_{CCO}$
3.0 V to 3.6 V	$V_{CCI}$	$\leq 1.0$ ns/V	15 pF	2 k $\Omega$	open	GND	$2V_{CCO}$

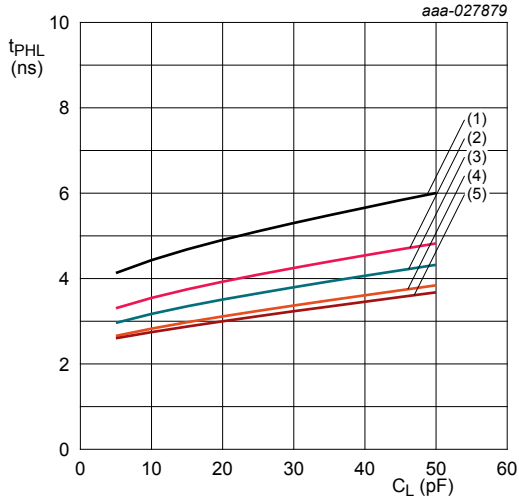
[1]  $V_{CCI}$  is the supply voltage associated with the data input port.

[2]  $dV/dt \geq 1.0$  V/ns

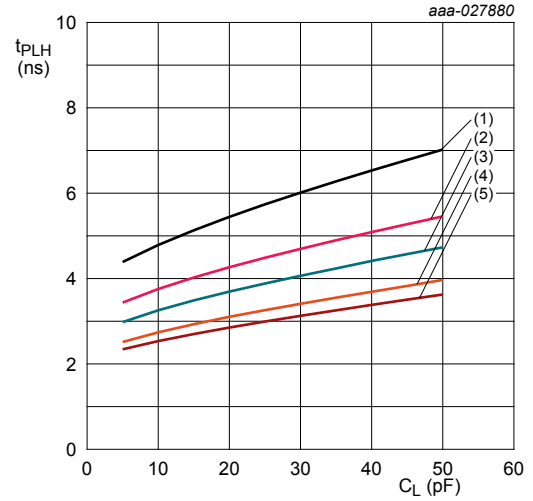
[3]  $V_{CCO}$  is the supply voltage associated with the output port.

11.2. Typical propagation delay characteristics

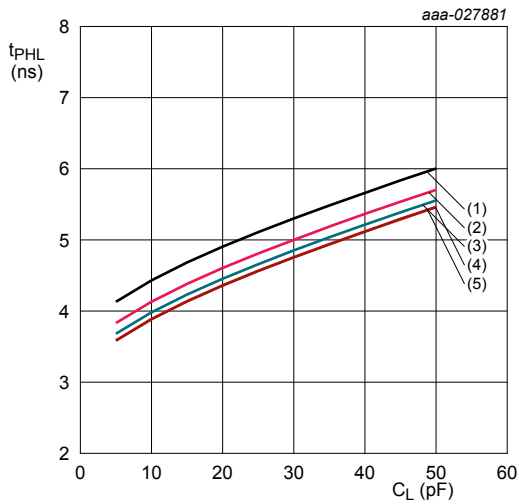




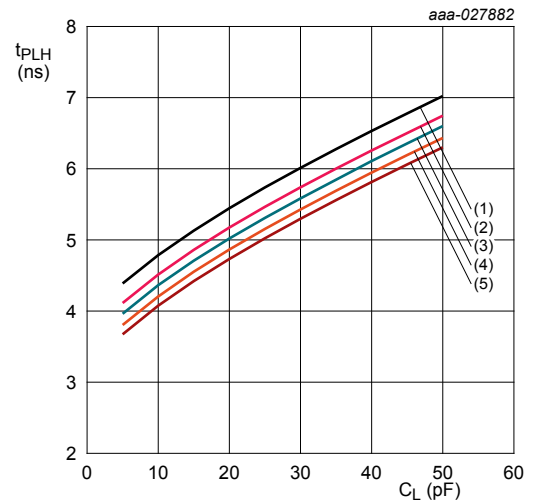
a. HIGH to LOW propagation delay (An to YBn)



b. LOW to HIGH propagation delay (An to YBn)



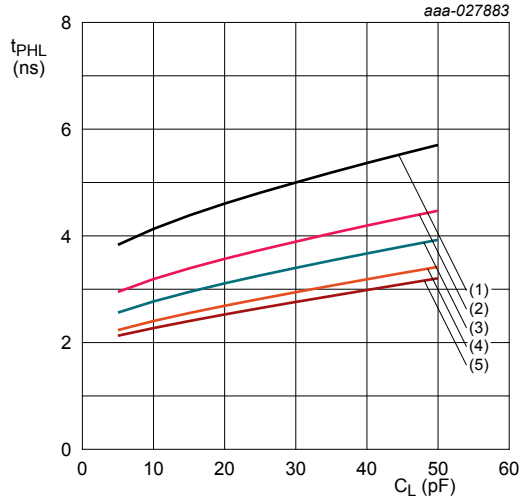
c. HIGH to LOW propagation delay (B4 to YA4)



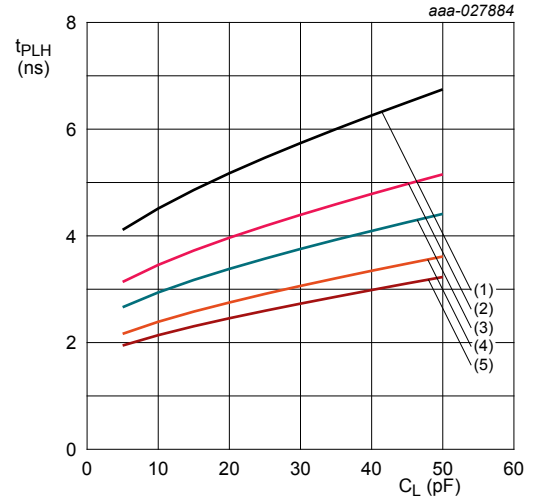
d. LOW to HIGH propagation delay (B4 to YA4)

- (1)  $V_{CC(B)} = 1.2\text{ V}$
- (2)  $V_{CC(B)} = 1.5\text{ V}$
- (3)  $V_{CC(B)} = 1.8\text{ V}$
- (4)  $V_{CC(B)} = 2.5\text{ V}$
- (5)  $V_{CC(B)} = 3.3\text{ V}$

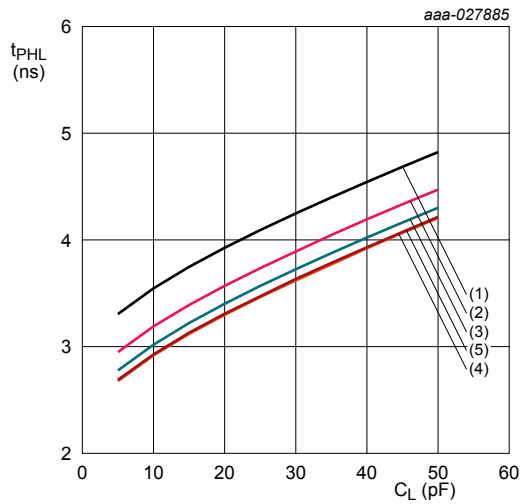
Fig. 7. Typical propagation delay versus load capacitance;  $T_{amb} = 25\text{ }^\circ\text{C}$ ;  $V_{CC(A)} = 1.2\text{ V}$



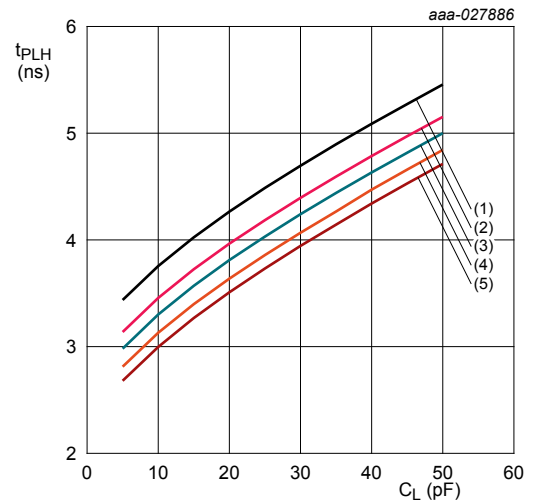
a. HIGH to LOW propagation delay (An to YBn)



b. LOW to HIGH propagation delay (An to YBn)



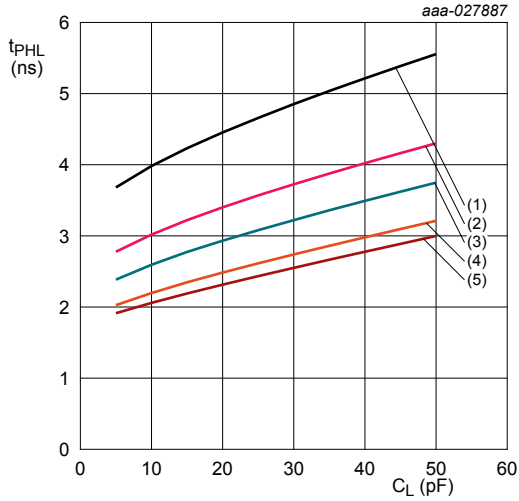
c. HIGH to LOW propagation delay (B4 to YA4)



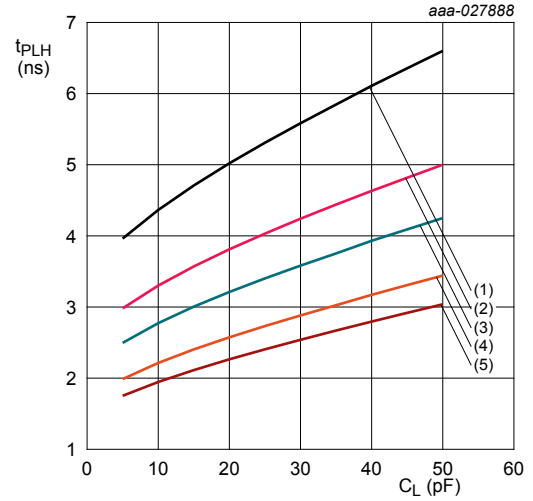
d. LOW to HIGH propagation delay (B4 to YA4)

- (1)  $V_{CC(B)} = 1.2\text{ V}$
- (2)  $V_{CC(B)} = 1.5\text{ V}$
- (3)  $V_{CC(B)} = 1.8\text{ V}$
- (4)  $V_{CC(B)} = 2.5\text{ V}$
- (5)  $V_{CC(B)} = 3.3\text{ V}$

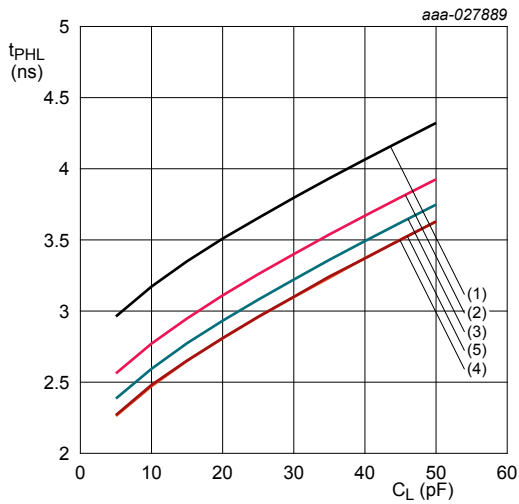
Fig. 8. Typical propagation delay versus load capacitance;  $T_{amb} = 25\text{ }^\circ\text{C}$ ;  $V_{CC(A)} = 1.5\text{ V}$



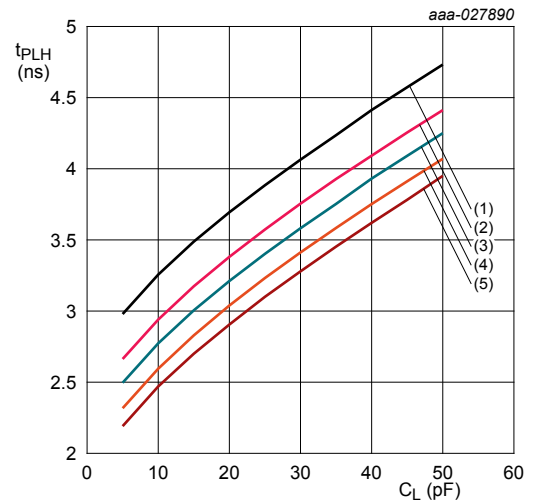
a. HIGH to LOW propagation delay (An to YBn)



b. LOW to HIGH propagation delay (An to YBn)



c. HIGH to LOW propagation delay (B4 to YA4)

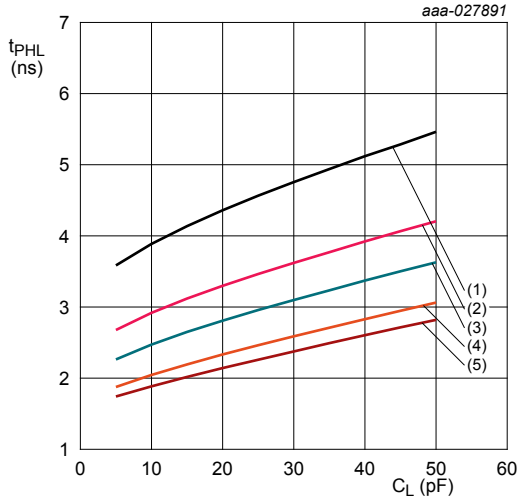


d. LOW to HIGH propagation delay (B4 to YA4)

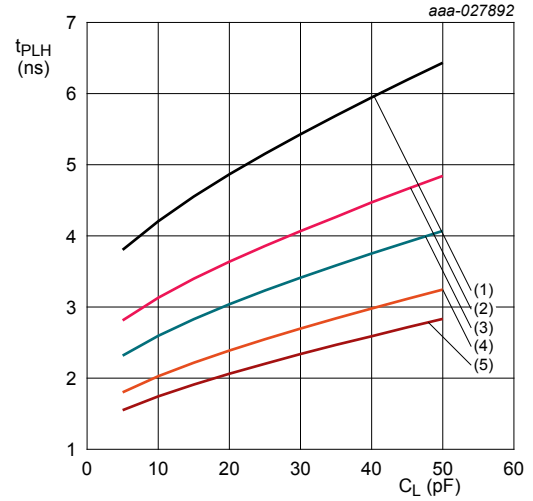
- (1)  $V_{CC(B)} = 1.2$  V
- (2)  $V_{CC(B)} = 1.5$  V
- (3)  $V_{CC(B)} = 1.8$  V
- (4)  $V_{CC(B)} = 2.5$  V
- (5)  $V_{CC(B)} = 3.3$  V

Fig. 9. Typical propagation delay versus load capacitance;  $T_{amb} = 25$  °C;  $V_{CC(A)} = 1.8$  V

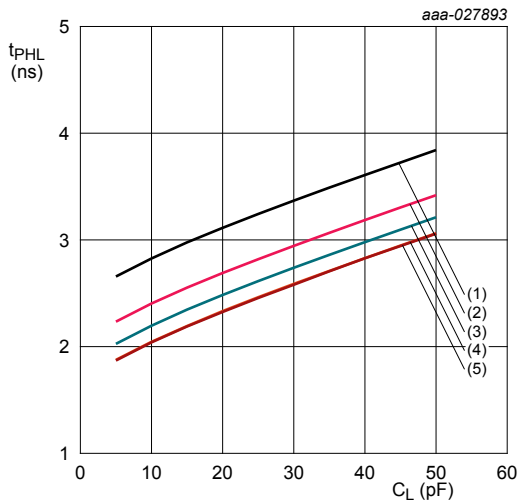




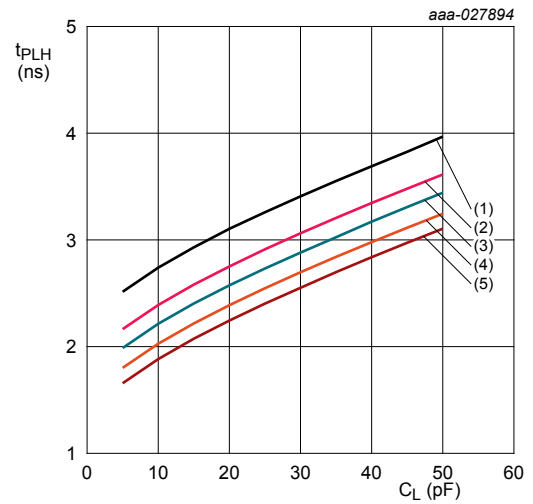
a. HIGH to LOW propagation delay (An to YBn)



b. LOW to HIGH propagation delay (An to YBn)



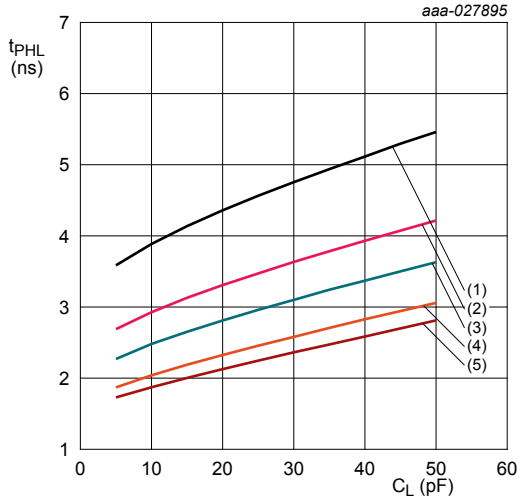
c. HIGH to LOW propagation delay (B4 to YA4)



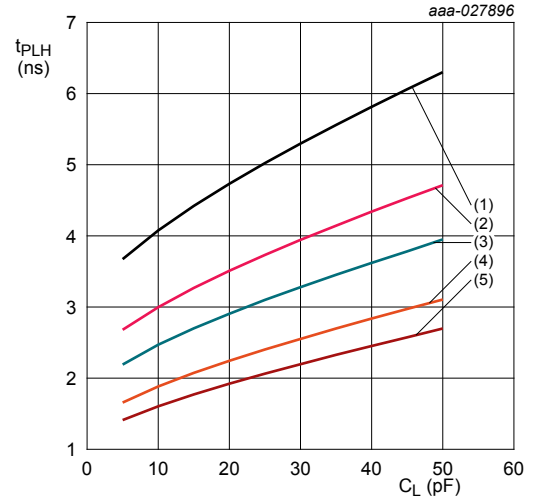
d. LOW to HIGH propagation delay (B4 to YA4)

- (1)  $V_{CC(B)} = 1.2\text{ V}$
- (2)  $V_{CC(B)} = 1.5\text{ V}$
- (3)  $V_{CC(B)} = 1.8\text{ V}$
- (4)  $V_{CC(B)} = 2.5\text{ V}$
- (5)  $V_{CC(B)} = 3.3\text{ V}$

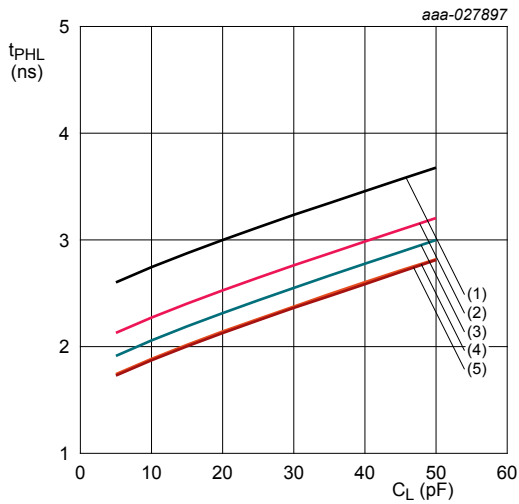
Fig. 10. Typical propagation delay versus load capacitance;  $T_{amb} = 25\text{ }^\circ\text{C}$ ;  $V_{CC(A)} = 2.5\text{ V}$



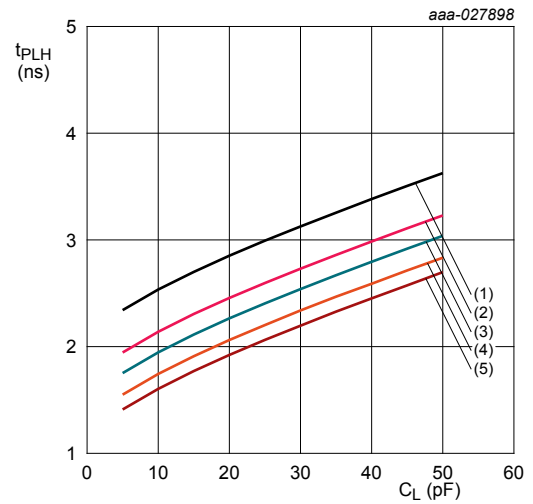
a. HIGH to LOW propagation delay (An to YBn)



b. LOW to HIGH propagation delay (An to YBn)



c. HIGH to LOW propagation delay (B4 to YA4)



d. LOW to HIGH propagation delay (B4 to YA4)

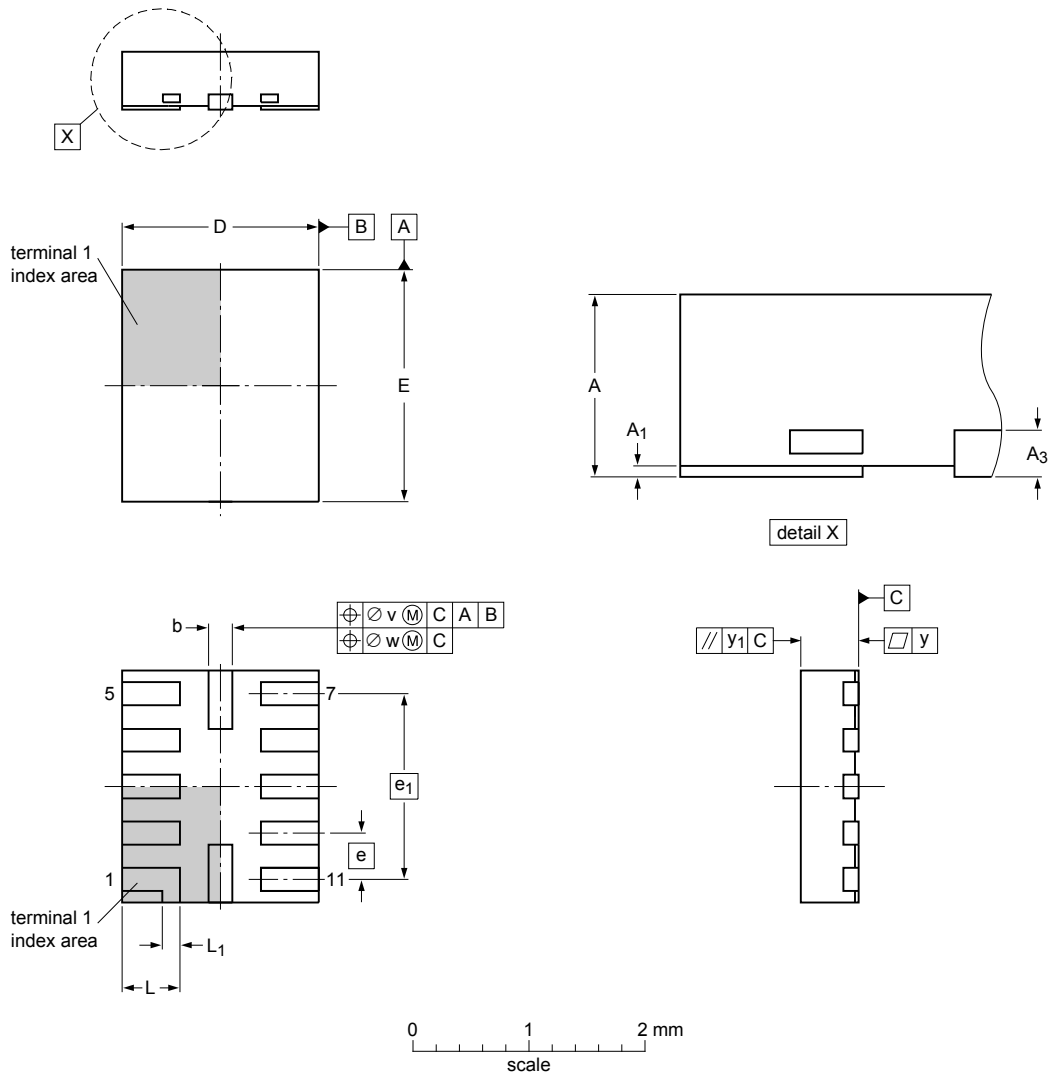
- (1)  $V_{CC(B)} = 1.2\text{ V}$
- (2)  $V_{CC(B)} = 1.5\text{ V}$
- (3)  $V_{CC(B)} = 1.8\text{ V}$
- (4)  $V_{CC(B)} = 2.5\text{ V}$
- (5)  $V_{CC(B)} = 3.3\text{ V}$

Fig. 11. Typical propagation delay versus load capacitance;  $T_{amb} = 25\text{ }^\circ\text{C}$ ;  $V_{CC(A)} = 3.3\text{ V}$

## 12. Package outline

**XQFN12: plastic, extremely thin quad flat package; no leads; 12 terminals; body 1.70 x 2.00 x 0.50 mm**

SOT1174-1



**Dimensions**

Unit <sup>(1)</sup>	A	A <sub>1</sub>	A <sub>3</sub>	b	D	E	e	e <sub>1</sub>	L	L <sub>1</sub>	v	w	y	y <sub>1</sub>
max	0.5	0.05		0.25	1.8	2.1			0.55					
nom			0.127	0.20	1.7	2.0	0.4	1.6	0.50	0.15	0.1	0.05	0.05	0.05
min		0.00		0.15	1.6	1.9			0.45					

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1174-1\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1174-1	---	MO-288	---		10-04-07 10-04-21

**Fig. 12. Package outline SOT1174-1 (XQFN12)**

## 13. Abbreviations

Table 17. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

## 14. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AVC4T3144 v.2	20180724	Product data sheet	-	74AVC4T3144 v.1
Modifications:	• <a href="#">Table 3</a> : pin number corrected for GND pin.			
74AVC4T3144 v.1	20171218	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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