

# PTRA087008NB

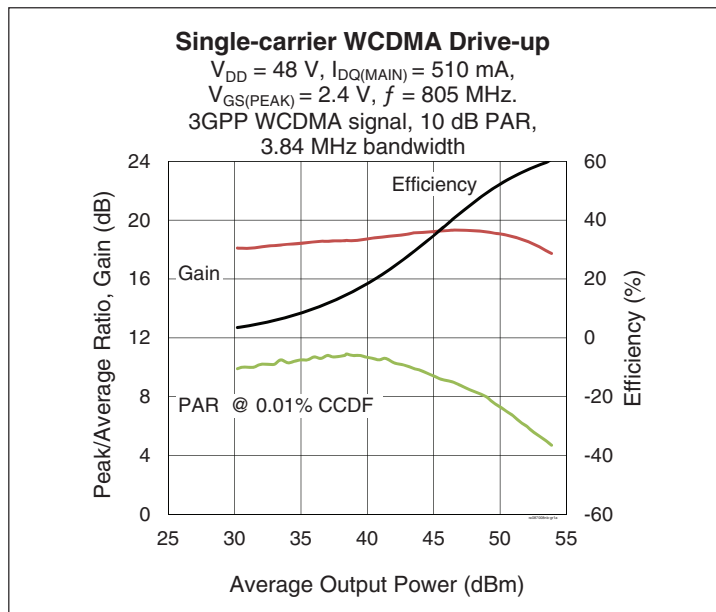
## Thermally-Enhanced High Power RF LDMOS FET 650 W, 48 V, 755 – 805 MHz

### Description

The PTRA087008NB is a 650-watt LDMOS FET. It is designed for use in multi-standard cellular power amplifier applications from 755 MHz to 805 MHz. Manufactured with Wolfspeed's advanced LDMOS process, this device provides excellent thermal performance and superior reliability.



PTRA087008NB  
Package PG-HB2SOF-6-1



### Features

- Broadband internal input and output matching
- Asymmetric design
  - Main:  $P_{1dB} = 245\text{ W Typ}$
  - Peak:  $P_{1dB} = 380\text{ W Typ}$
- Typical pulsed CW performance, 805 MHz, 48 V, Doherty configuration
  - Output power at  $P_{3dB} = 650\text{ W}$
  - Efficiency = 52%
  - Gain = 19.5 dB
- Capable of handling 10:1 VSWR @48 V, 30 W (WCDMA) output power
- Human Body Model Class 2 (per ANSI/ESDA/JEDEC JS-001)
- Integrated ESD protection
- Low thermal resistance
- RoHS-compliant

### RF Characteristics

#### Single-carrier WCDMA Specifications (tested in Wolfspeed Doherty test fixture)

$V_{DD} = 48\text{ V}$ ,  $I_{DQ} = 510\text{ mA}$ ,  $P_{OUT} = 107\text{ W avg}$ ,  $V_{GS(PEAK)} = 2.4\text{ V}$ ,  $f = 805\text{ MHz}$ , 3GPP, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	$G_{ps}$	17.5	18.5	—	dB
Drain Efficiency	$\eta_D$	48.5	52	—	%
Adjacent Channel Power Ratio	ACPR	—	-31	-28	dBc
Output PAR @ 0.01% CCDF	OPAR	6.7	-7.2	—	dB

All published data at  $T_{CASE} = 25^\circ\text{C}$  unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!



**DC Characteristics** (each side)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_{DS} = 10\text{ mA}$	$V_{(BR)DSS}$	105	—	—	V
Drain Leakage Current	$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}$	$I_{DSS}$	—	—	1	$\mu\text{A}$
	$V_{DS} = 105\text{ V}, V_{GS} = 0\text{ V}$	$I_{DSS}$	—	—	10	$\mu\text{A}$
Gate Leakage Current	$V_{GS} = 10\text{ V}, V_{DS} = 0\text{ V}$	$I_{GSS}$	—	—	1	$\mu\text{A}$
On-State Resistance	(Main) $V_{GS} = 10\text{ V}, V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	0.07	—	$\Omega$
	(Peak) $V_{GS} = 10\text{ V}, V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	0.05	—	$\Omega$
Operating Gate Voltage	(Main) $V_{DS} = 48\text{ V}, I_{DQ} = 0.2\text{ A}$	$V_{GS}$	3.0	3.5	4.0	V
	(Peak) $V_{DS} = 48\text{ V}, I_{DQ} = 0\text{ A}$	$V_{GS}$	—	2.4	—	V

**Maximum Ratings**

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	105	V
Gate-Source Voltage	$V_{GS}$	-6 to +12	V
Operating Voltage	$V_{DD}$	0 to +55	V
Junction Temperature	$T_J$	225	$^{\circ}\text{C}$
Storage Temperature Range	$T_{STG}$	-65 to +150	$^{\circ}\text{C}$

1. Operation above the maximum values listed here may cause permanent damage. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the component. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For reliable continuous operation, the device should be operated within the operating voltage range ( $V_{DD}$ ) specified above.

2. Parameters values can be affected by end application and product usage. Values may change over time.

**Thermal Characteristics**

$V_{DD} = 48\text{ V}, I_{DQ} = 500\text{ mA}, 780\text{ MHz}$

Parameter	Symbol	Value	Unit	
Thermal Resistance (Main)	$T_{CASE} = 70^{\circ}\text{C}, P_{OUT} = 107\text{ W CW}$	$R_{\theta JC}$	0.70	$^{\circ}\text{C/W}$

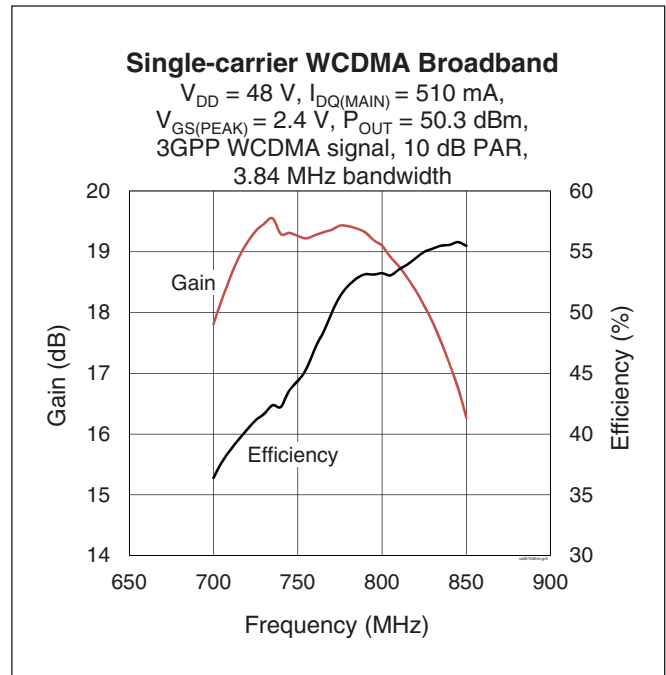
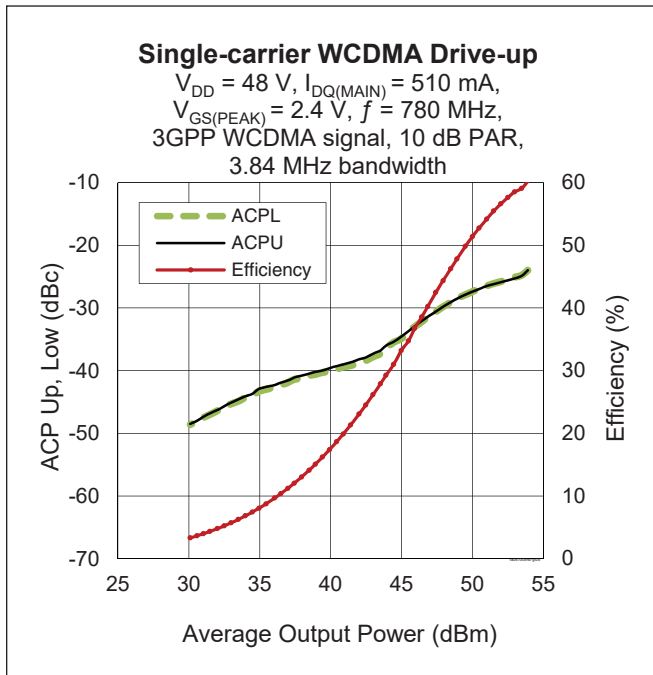
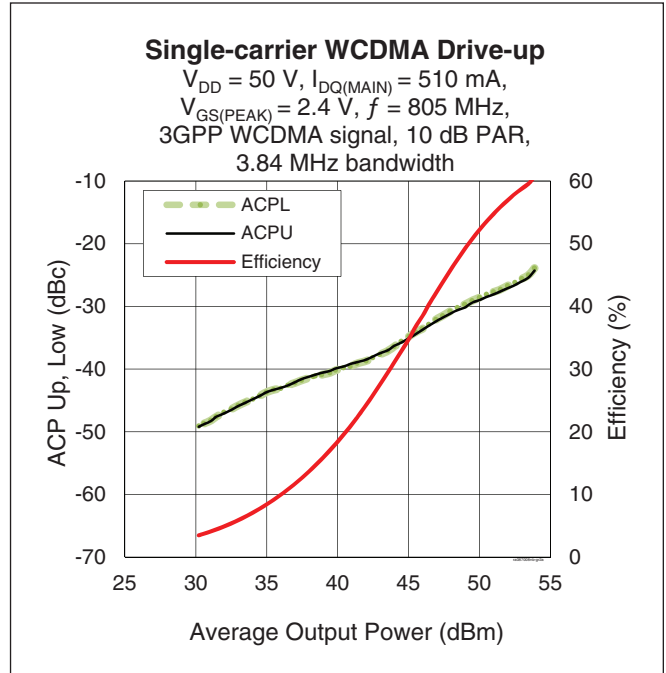
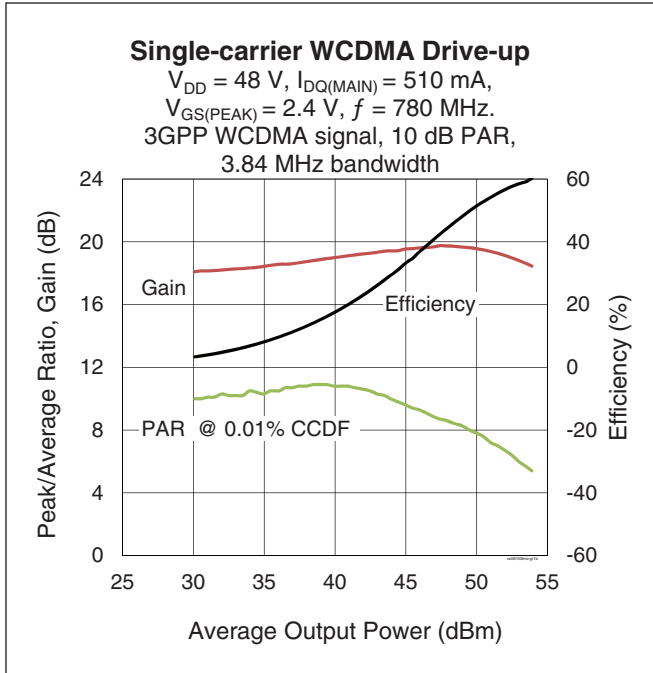
**Moisture Sensitivity Level**

Level	Test Signal	Package Temperature	Unit
3	IPC/JEDEC J-STD-020	260	$^{\circ}\text{C}$

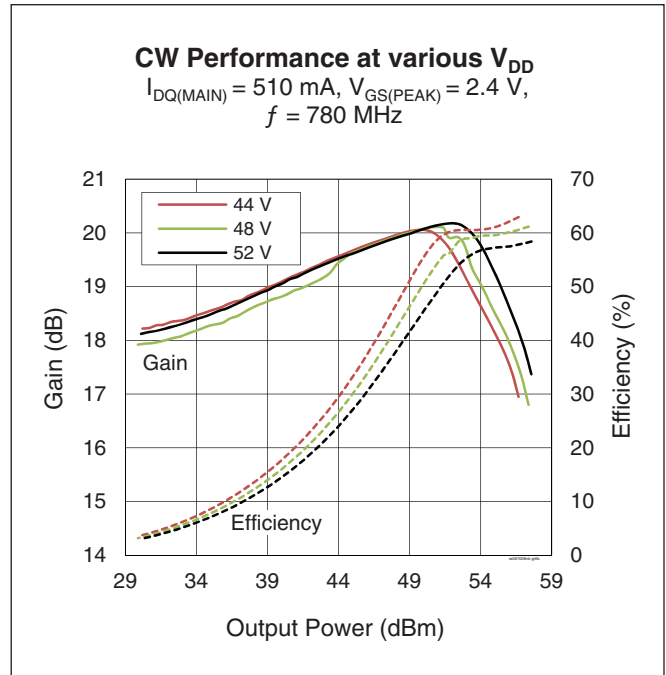
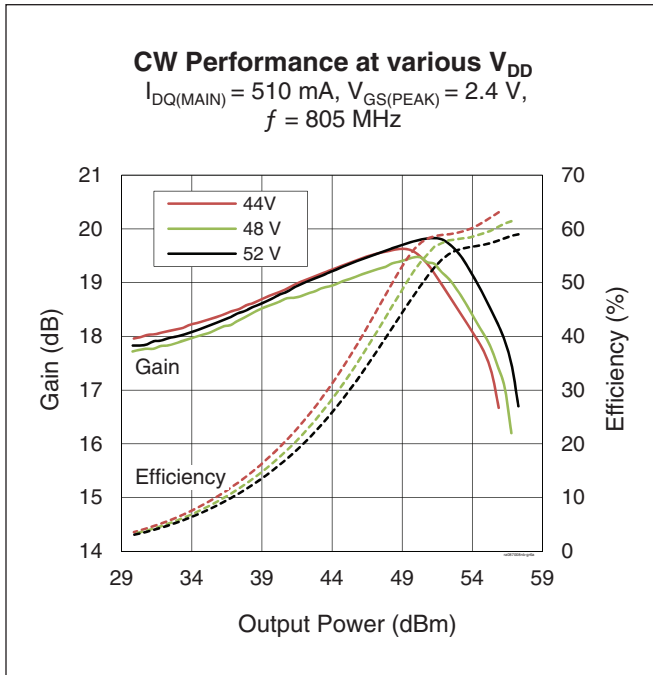
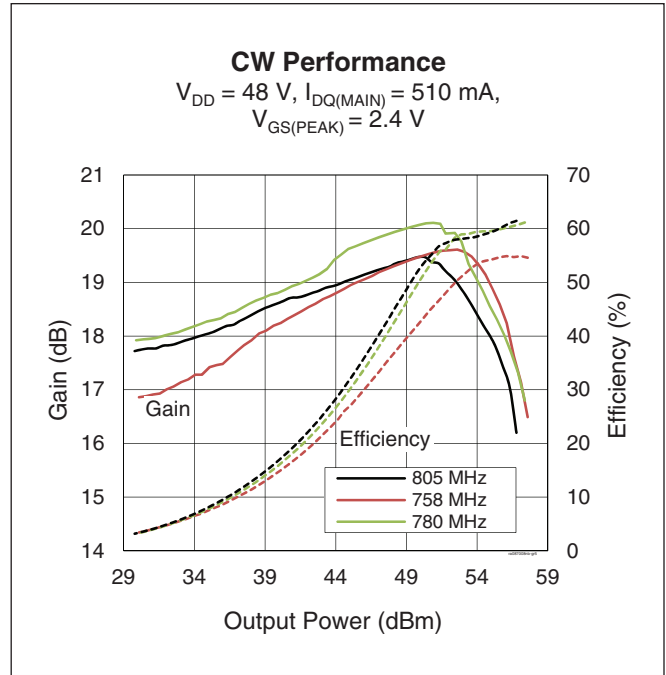
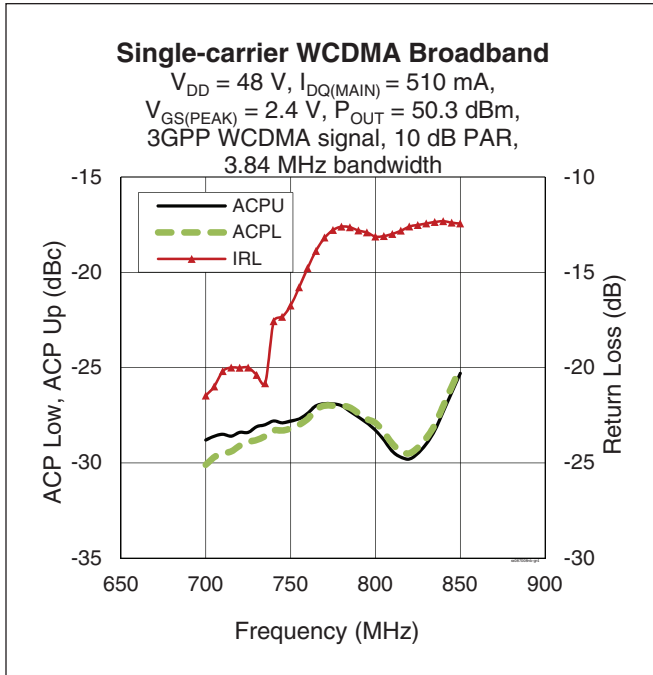
**Ordering Information**

Type and Version	Order Code	Package and Description	Shipping
PTRA087008NB V1 R2	PTRA087008NB-V1-R2	PG-HB2SOF-6-1, overmold	Tape & Reel, 250 pcs

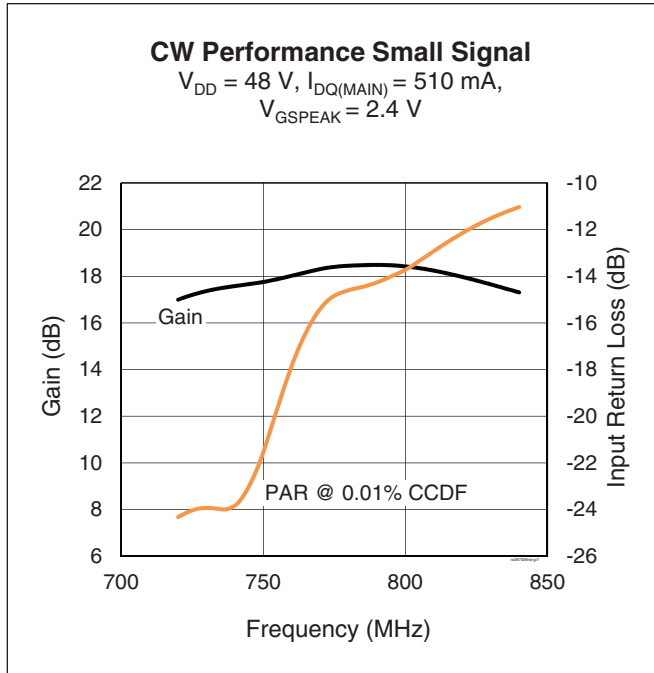
**Typical Performance** (data taken in a production test fixture)



**Typical Performance** (cont.)



**Typical Performance** (cont.)



**See Load Pull Performance, next page**



### Load Pull Performance

**Main side**

Pulsed CW signal: 10  $\mu$ sec, 10% duty cycle,  $V_{DD} = 48$  V,  $I_{DQ} = 510$  mA, class AB

		P <sub>1dB</sub>									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Z <sub>s</sub> [ $\Omega$ ]	Z <sub>l</sub> [ $\Omega$ ]	Gain [dB]	P <sub>OUT</sub> [dBm]	P <sub>OUT</sub> [W]	$\eta_D$ [%]	Z <sub>l</sub> [ $\Omega$ ]	Gain [dB]	P <sub>OUT</sub> [dBm]	P <sub>OUT</sub> [W]	$\eta_D$ [%]
760	0.6 - j1.9	1.3 - j0.5	21.41	54.81	303	59.5	2.7 + j1.1	23.40	52.50	178	71.7
780	0.6 - j2.0	1.3 - j0.5	21.45	54.73	297	59.0	2.5 + j2.0	23.55	52.42	175	71.4
805	0.6 - j2.3	1.2 - j0.3	21.39	54.66	292	58.5	2.3 + j1.2	23.58	52.50	178	71.1

		P <sub>3dB</sub>									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Z <sub>s</sub> [ $\Omega$ ]	Z <sub>l</sub> [ $\Omega$ ]	Gain [dB]	P <sub>OUT</sub> [dBm]	P <sub>OUT</sub> [W]	$\eta_D$ [%]	Z <sub>l</sub> [ $\Omega$ ]	Gain [dB]	P <sub>OUT</sub> [dBm]	P <sub>OUT</sub> [W]	$\eta_D$ [%]
760	0.6 - j1.9	1.4 - j0.6	19.53	55.56	360	62.9	2.3 + j0.6	21.02	53.91	246	72.5
780	0.6 - j2.0	1.3 - j0.6	19.52	55.49	354	61.7	2.3 + j0.6	21.24	53.92	247	72.3
805	0.6 - j2.3	1.3 - j0.6	19.62	55.44	350	61.7	2.0 + j0.5	21.13	54.15	260	71.0

**Peak side**

Pulsed CW signal: 10  $\mu$ sec, 10% duty cycle,  $V_{DD} = 48$  V,  $V_{GS(PEAK)} = 2.4$  V, class B

		P <sub>1dB</sub>									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Z <sub>s</sub> [ $\Omega$ ]	Z <sub>l</sub> [ $\Omega$ ]	Gain [dB]	P <sub>OUT</sub> [dBm]	P <sub>OUT</sub> [W]	$\eta_D$ [%]	Z <sub>l</sub> [ $\Omega$ ]	Gain [dB]	P <sub>OUT</sub> [dBm]	P <sub>OUT</sub> [W]	$\eta_D$ [%]
760	0.3 - j2.1	0.7 - j0.6	19.78	56.85	484	60.1	1.2 + j0.4	21.46	54.72	296	73.2
780	0.5 - j2.3	0.8 - j0.4	20.13	56.75	473	61.0	1.3 + j0.6	21.40	54.56	286	73.0
805	0.7 - j2.8	0.8 - j0.3	19.91	56.65	462	61.1	1.4 + j0.8	21.40	54.12	258	72.2

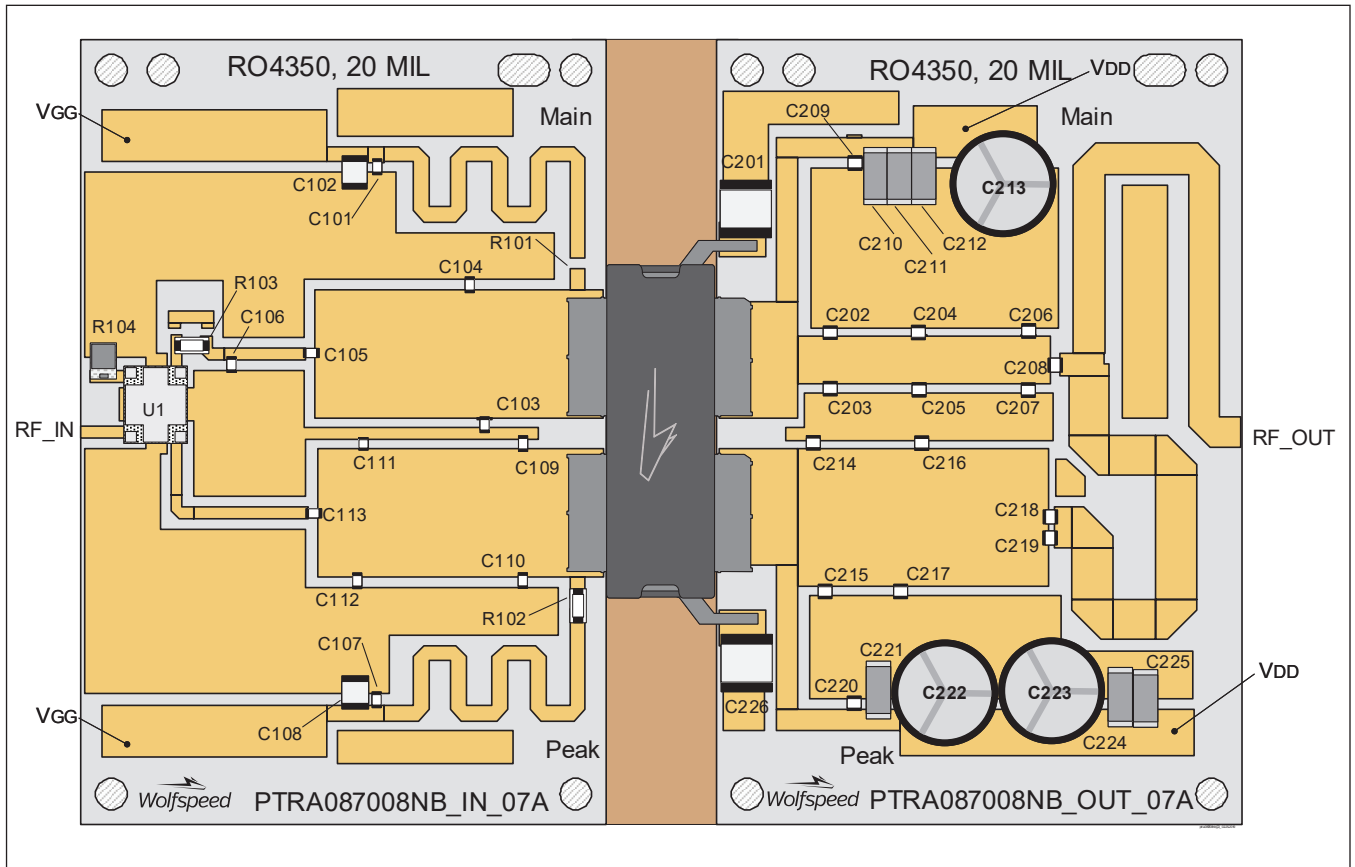
		P <sub>3dB</sub>									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Z <sub>s</sub> [ $\Omega$ ]	Z <sub>l</sub> [ $\Omega$ ]	Gain [dB]	P <sub>OUT</sub> [dBm]	P <sub>OUT</sub> [W]	$\eta_D$ [%]	Z <sub>l</sub> [ $\Omega$ ]	Gain [dB]	P <sub>OUT</sub> [dBm]	P <sub>OUT</sub> [W]	$\eta_D$ [%]
760	0.3 - j2.1	0.8 - j0.7	17.86	57.63	579	62.8	1.2 + j0.2	19.35	55.84	384	74.3
780	0.5 - j2.3	0.8 - j0.5	18.16	57.45	556	62.4	1.3 + j0.4	19.39	55.49	354	73.3
805	0.7 - j2.8	0.8 - j0.3	17.90	57.34	542	62.4	1.1 + j0.5	19.13	55.50	355	72.7



**Reference Circuit, tuned for 755 to 805 MHz**

**Reference Circuit Assembly**

DUT	PTRA087008NB-V1
Reference Circuit Part No.	LTA/PTRA087008NB-V1
PCB	Rogers 4360, 0.508 mm [0.020"] thick, 2 oz. copper, $\epsilon_r = 3.66$
Find Gerber files for this test fixture on the Wolfspeed Web site at <a href="http://www.wolfspeed.com/RF">www.wolfspeed.com/RF</a>	



Reference circuit assembly diagram (not to scale)

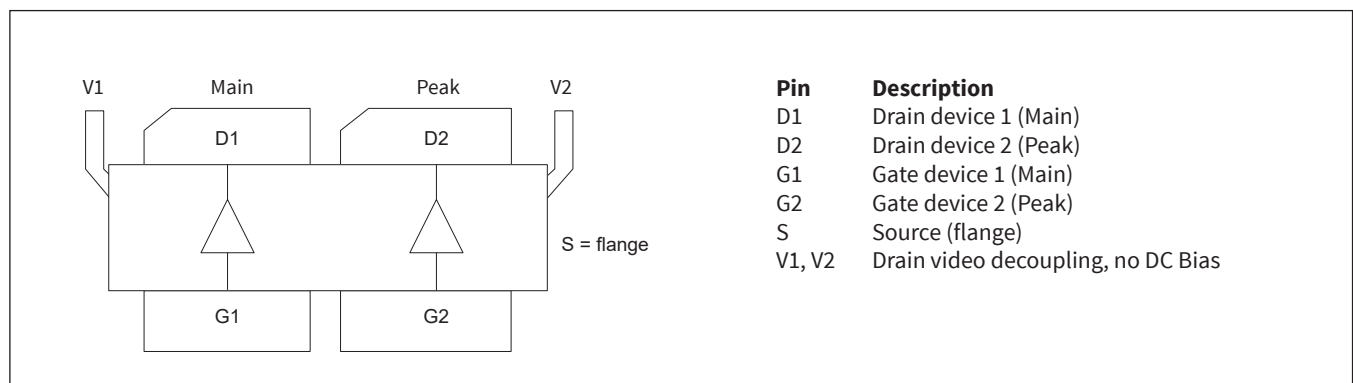


**Reference Circuit** (cont.)

**Components Information**

Component	Description	Manufacturer	P/N
<b>Input</b>			
C101, C105, C107, C113	Capacitor, 43 pF	ATC	ATC600F430JW250T
C102, C108	Capacitor, 10 μF	Taiyo Yuden	UMK325C7106MM-T
C103	Capacitor, 6.8 pF	ATC	ATC600F6R8JW250T
C104	Capacitor, 7.5 pF	ATC	ATC600F7R5JW250T
C106	Capacitor, 3.0 pF	ATC	ATC600F3R0CT250T
C109, C111, C112	Capacitor, 2.0 pF	ATC	ATC600F2R0CW250T
C110	Capacitor, 9.1 pF	ATC	ATC600F9R1JW250T
R101, R102	Resistor, 6.2 ohms	Panasonic	P6.2ECT-ND
R103	Resistor, 5.1 ohms	Panasonic	P5.1ETR-ND
R104	Resistor, 50 ohms	Anaren	C8A50Z4A
U1	Hybrid coupler	Anaren	X3C09P1-03S
<b>Output</b>			
C201, C210, C211, C212, C221, C224, C225, C226	Capacitor, 10 μF, 100 V	TDK Corporation	C5750X7S2A106M230KB
C202	Capacitor, 9.1 pF	ATC	ATC600F9R1JW250T
C203	Capacitor, 8.2 pF	ATC	ATC600F8R2JW250T
C204	Capacitor, 3.0 pF	ATC	ATC600F3R0CW250T
C205	Capacitor, 2.2 pF	ATC	ATC600F2R2CW250T
C206, C207	Capacitor, 0.6 pF	ATC	ATC600F0R6CW250T
C208, C214, C215	Capacitor, 10 pF	ATC	ATC600F100JW250T
C209, C218, C219, C220	Capacitor, 43 pF	ATC	ATC600F430JW250T
C213, C222, C223	Capacitor, 100 μF, 63 V	Panasonic	EEE-FK1J101P
C216, C217	Capacitor, 6.2 pF	ATC	ATC600F6R2JW250T

**Pinout Diagram** (top view)



Lead connections for PTRA087008NB



Package Outline Specifications

Package PG-HB2SOF-6-1 (top and side views)

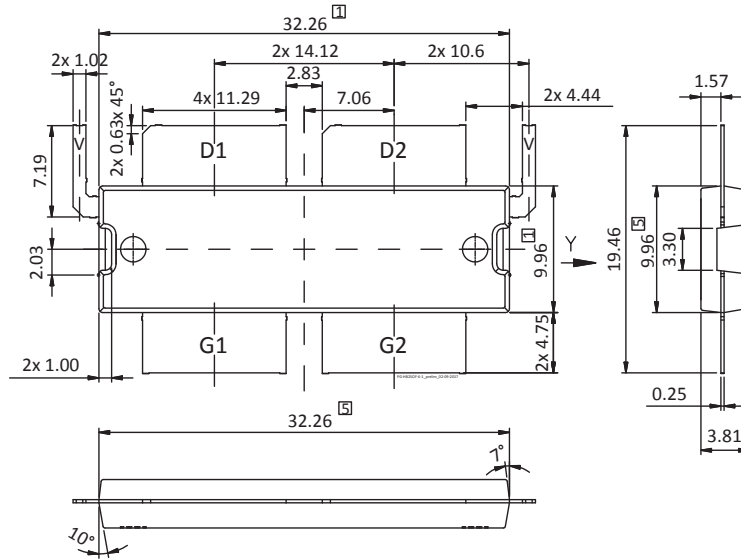


Diagram Notes—unless otherwise specified:

1. Mold/dam bar/metal protrusion of 0.30 mm max per side not included.
2. Fillets and radii: all radii are 0.3 mm max.
3. Interpret dimensions and tolerances per ISO 8015.
4. Dimensions are mm.
5. Does not include mold/dam bar and metal protrusion.
6. All tolerances  $\pm 0.1$  mm unless specified otherwise.
7. All metal surfaces tin pre-plated, except area of cut.
8. Lead thickness: 0.25 mm.
9. Pins: D1, D2 – drain; G1, G2 – gate; S – source;  
V – drain video decoupling, no DC bias

**Package Outline Specifications**

**Package PG-HB2SOF-6-1 (bottom view)**

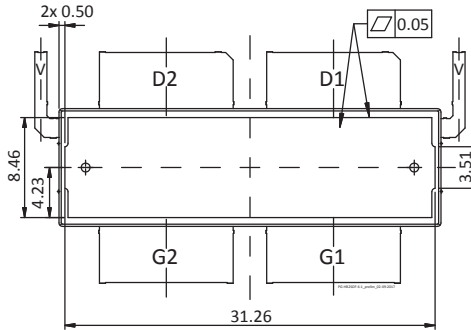


Diagram Notes—unless otherwise specified:

1. Mold/dam bar/metal protrusion of 0.30 mm max per side not included.
2. Fillets and radii: all radii are 0.3 mm max.
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V – drain video decoupling, no DC bias

## Revision History

Revision	Date	Data Sheet Type	Page	Subjects (major changes at each revision)
01	2016-07-14	Advance	All	Data Sheet reflects advance specification for product development
01.1	2017-08-15	Advance	1, 2	Updated features, RF Characteristics, Max Ratings table and Pinout Diagram
02	2018-06-20	Preliminary	All	Update specifications tables (pg 1-2), and graphs.
03	2018-06-26	Production	All	Final specifications for Production-released product, including updates to Thermal Characteristics table (p1) and circuit BOM (p8).
03.1	2018-07-12	Production	1	Revised title to 650W, removed R0 ordering information
03.2	2019-02-25	Production	2	Added MSL table
03.3	2020-10-12	Production	7	Corrected package in Ref circuit

For more information, please contact:

4600 Silicon Drive  
 Durham, North Carolina, USA 27703  
[www.wolfspeed.com/rf](http://www.wolfspeed.com/rf)

Sales Contact  
[rfsales@cree.com](mailto:rfsales@cree.com)

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