TECHNICAL REFERENCE NOTE

ARTESYN AIF04ZPFC SERIES

1600 Watts Full Brick PFC Converter

PRODUCT DESCRIPTION

Advanced Energy's Artesyn AIF04ZPFC series full-brick power factor correction module accepts a wide 85 to 264Vac or 120 to370Vdc input and presents a unity power factor. Rated at 1600 watts, the module has a high conversion efficiency of 95% and provides a nominal non-isolated output voltage of 380Vdc. Featuring an industry-standard 2.4 x 4.6 in full-brick form factor and a height of only 0.5 in, they have a power density of 290 W/in^3.

AT A GLANCE

Total Power

1000 to 1600 Watts

Input Voltage

85 to 264 Vac

120 to 370 Vdc

# of Outputs

Single

RoHS

SPECIAL FEATURES

- Unity power factor
- Configurable DC input
- High efficiency up to 95%
- Universal input voltage and frequency range
- Up to 1600W output power
- Parallelable with current sharing
- < 10% harmonic distortion conforming to IEC1000-3-2
- 100^{O}C baseplate operating temperature
- Power fail warning signal
- Enable output to control DC-DC Converter
- High reliability - over 1 million hours MTBF with baseplate temperature 50^{O}C
- EEPROM data storage via I2C interface
- Switching Frequency 125KHz
- Power density up to 290W/in^3
- Two-year warranty

SAFETY

- TUV EN62368-1
- UL+CUL UL62368-1
- CE Mark
- UKCA Mark

TYPICAL APPLICATIONS

- Industrial

MODEL NUMBERS

Standard	Input Voltage	Output Voltage	Minimum Load	Maximum Load	Efficiency
AIF04ZPFC-01L	85-264Vac	380Vdc	0A	4.2A	95%
AIF04ZPFC-02L	85-264Vac	380Vdc	0A	4.2A	95%

Order Information

AIF	04	ZPFC	-	01	N	NT	L
①	②	③		④	⑤	⑥	⑦

①	Model series	Full brick size unit
②	Output current	4.2A rated output current
③	Output voltage	Power factor correction module, the output is 380Vdc
④	Model variant	01: parallel / stand-alone configuration, total input current must be <16A 02: parallel / stand-alone configuration, designed for parallel operation where the total input current >16A, requires external negative rail input rectifiers
⑤	Remote on/off logic	Blank: Positive enable. N: Negative enable
⑥	Structure	Blank is default with M3 thread. NT: Non-Threaded-inserts for mounting
⑦	RoHS status	L: RoHS R6

Options

None

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Stress in excess of those listed in the "Absolute Maximum Ratings" may cause permanent damage to the power supply. These are stress ratings only and functional operation of the unit is not implied at these or any other conditions above those given in the operational sections of this TRN. Exposure to any absolute maximum rated condition for extended periods may adversely affect the power supply's reliability.

Table 1. Absolute Maximum Ratings

Parameter	Model	Symbol	Min	Typ	Max	Unit
Input Voltage						
Operating Continuous	All modules	$V_{IN,AC}$	85	-	264	Vac
		$V_{IN,DC}$	120	-	370	Vdc
Surge Voltage (1 Sec)		$V_{IN,AC}$	-	-	290	Vac
Input Frequency	All modules	-	47	50/60	63	Hz
Maximum Output Power						
$85Vac \le V_{IN,AC} \le 120Vac$	All modules	$P_{O,max}$	-	-	1000	W
$120Vac < V_{IN,AC} < 220Vac$[1]			-	-	-	-
$V_{IN,AC} \ge 220Vac$			-	-	1600	W
Isolation						
Input to Baseplate	All modules		-	-	2700	V
Output to Baseplate			-	-	2700	V
Baseplate Capacitance			-	-	1300	pF
Operating Case Temperature	All modules	$T_{\_BP}$	-20	-	100	^{O}C
Startup Case Temperature	All modules	$T_{\_BP}$	-40	-	100	^{O}C
Storage Temperature	All modules	T_{STG}	-40	-	110	^{O}C
Humidity						
Operating	All modules	-	-	-	95	%
MTBF[2]	All modules	-	-	450	-	KHrs

Note 1 - Refer Maximum Output Power Vs Input Voltage diagram on page 27.
Note 2 - Under the condition of output current of 2.6A, baseplate temperature is 40°C, compliance with MIL-217FN2.
Note 3 - Unless otherwise indicated, specifications applied over all operating input voltage and temperature conditions. Standard test condition on a single unit.

$T_{Ambient}$:	25°C
L1:	115Vac, 220Vac
L2:	Return pin for L1
PF Enable:	Open
+Vout1:	Connect to load
- Vout1:	Connect to load (return)
LD Enable:	Use for load control
Vrim (Vadj):	Connect to S GND
Output Cap:	470uF x 2

Note of caution

Please note that AIF06ZPFC is a non-isolated product between input and output terminals. Only the baseplate and mounting inserts can be considered as isolated from input and output. Please be cautioned that high voltage differential scope probe (500V or 1KV) or isolated oscilloscope should be used for any waveform monitoring or measurement due to safety consideration. Failure to observe this instruction can cause either incorrect measurements, or as a worst case, irreparable damage.

ELECTRICAL SPECIFICATIONS

Input Specifications

Table 2. Input Specifications

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Operating Input Voltage, AC	All	$V_{IN,AC}$	85	-	264	Vac
Operating Input Voltage, DC	All	$V_{IN,DC}$	120	-	370	Vdc
Input AC Frequency	All	$f_{IN,AC}$	47	50/60	63	Hz
Maximum Input Current[1] ($I_O = I_{O,max}$)	$V_{IN,AC}$ = 115Vac	$I_{IN,max}$	-	-	10	A
No Load Input Current (V_O On, I_O = 0A)	All	I_{IN,no_load}	-	-	0.3	A_{RMS}
No Load Input Power (V_O On, I_O = 0A)	$V_{IN,AC}$ = 230Vac	P_{IN,no_load}	-	-	3.8	W
Harmonic Line Currents	All	THD	IEC1000-3-2 Less than 10%			
Power Factor	$P_O \geq 500W$ $P_O \geq 1000W$	PF	0.96 0.98	0.97 0.99	- -	
Startup Surge Current (Inrush)[2]	All	$I_{IN,surge}$	-	-	20	A
Input AC Low Line Start-up Voltage	$I_O = I_{O,max}$	$V_{IN,AC}$	79	-	84.5	Vac
Input AC Undervoltage Lockout Voltage	$I_O = I_{O,max}$	$V_{IN,AC}$	57	-	62	Vac
Efficiency	$V_{IN,AC}$ = 115Vac(1000W) $V_{IN,AC}$ = 230Vac(1000W) $V_{IN,AC}$ = 230Vac(1600W)	η	90 92 92	92 94 95	- - -	% % %
Turn On Delay Time	$V_{IN,AC}$ = 115Vac $V_{IN,AC}$ = 230Vac	T_{on_delay}	0.5 0.5	2.5 2.5	4.0 3.5	Sec Sec

Note 1 - For AIF04ZPFC-01, total input current for modules connected in parallel must not exceed 16A; For AIF04ZPFC-02, negative rail input rectifier must be provided by external circuitry, refer page 27.

Note 2 - Need external inrush limiting circuit; Half cycle surge current due to input transient surge must be limited to 20A peak or less; The PFC's LD ENABLE signal is recommended to be used to enable the load in case of initial surge load condition.

ELECTRICAL SPECIFICATIONS

Output Specifications

Table 3. Output Specifications

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Output Voltage	I_O = 4.2A / V_{IN} >180Vac I_O = 0	V_O	370 -	380 393	- 400	Vdc Vdc
Maximum Output Power[1]	85Vac ≤ $V_{IN,AC}$ ≤ 120Vac 120Vac < $V_{IN,AC}$ <220Vac[1] $V_{IN,AC}$ ≥ 220Vac	P_O	- - -	- - -	1000 - 1600	W W W
V_O Load Capacitance	All	-	470	-	3000	uF
Output Voltage Adjustment Range	All	V_O	76	-	100	%
Output Voltage Ripple, pk-pk	$V_{IN,AC}$ = 115Vac I_O = 2.6A, V_O = 380Vdc	$V_{O,ripple}$	11	-	-	V_{PK-PK}
Output Current, continuous	All	I_O	0	-	4.2	A
Over Voltage Protection[2]	All	Vo	420	-	430	Vdc
Over Temperature Protection[3]	All	T	105	-	120	°C
Number of Parallel Units[4]	"C SHARE" connected	-	-	-	10	Units
V_O Current Share Accuracy[4]	"C SHARE" connected	±%V_O	-	3	10	%
C Mon	I_O = 4.2A	$I_{C\ Mon}$	0.9	1.0	1.1	mA
	I_O = 20 to 100% $I_{O,max}$	$I_O/I_{C\ Mon}$	-	4.2	-	A/mA
TEMP MON $V_{TEMP\ MON}$ Sensitivity Source impedance	All	- -	9.8 -	10.0 16.0	10.2 -	mV/°C KΩ
CLKOUT- Clock Output	CLKIN open	$V_{CLK\ OUT}$	-	5.00	-	V_{PK-PK}
	Clock frequency	f	0.97	1.00	1.03	MHz
CLK IN - Clock Input	All	$V_{CLK\ IN}$	4.5	-	6.0	V_{PK-PK}
	All	f	0.95	1.00	1.05	MHz
PFW ADJ - Power Fail Warning Adjust	0 to 2.8 V 3.2 V 3.4 V	V_{PFW}	265 305 325	280 320 340	295 335 355	Vdc Vdc Vdc
PFW ADJ Current Source	All	I_{PFW}	-	1	-	mA
PFW - Power Fail Warning[5]	Input Power OK I_{PFW} = 0	V_{PFW}	12	13.7	15	V
	Input Power Fail I_{PFW} = 15mA	V_{PFW}	0	0.2	0.4	V
	PFW short to S_GND	I_{PFW}	-	2.9	-	mA

Note 1 - Refer Maximum Output Power Vs Input Voltage diagram on page 26.
Note 2 - Latch mode.
Note 3 - Baseplate temperature.
Note 4 - For AIF04ZPFC-01, total input current of all the modules should not exceed 16Arms.
Note 5 - Only apply on primary side.

ELECTRICAL SPECIFICATIONS

Output Specifications Con't

Table 3. Output Specifications

Parameter	Condition	Symbol	Min	Typ	Max	Unit
LD ENABLE - Load Enable	Load enabled, I_{LD} = 0	V_{LD}	12.0	13.7	15.0	V
	Load disabled I_{LD} = 15mA	V_{LD}	0	0.2	0.4	V
	LD ENABLE short to S_GND	I_{LD}	-	2.9	-	mA
PF ENABLE - Module Enable[1] Negative Enable	Module enabled	V_{PF}	0	-	0.8	V
	Module disabled	V_{PF}	2.2	-	5.0	V
PF ENABLE - Module Enable[1] Positive Enable	Module enabled	V_{PF}	2.2	-	5.0	V
	Module disabled	V_{PF}	0	-	0.8	V
PF ENABLE Current Source	V_{Enable} = 0.8V	I_{PF}	-	400	-	uA
PV_AUX[1]	I_{PV_AUX} = 0A I_{PV_AUX} = 20mA	V_{PV}	- 8	- -	11 9	V V

Note 1 - Only apply on primary side.

WARNING - LD ENABLE must be used to start the unit, otherwise the inrush resistor inside the module will be damaged or overstressed.

ELECTRICAL SPECIFICATIONS

AIF04ZPFC-01L Performance Curves

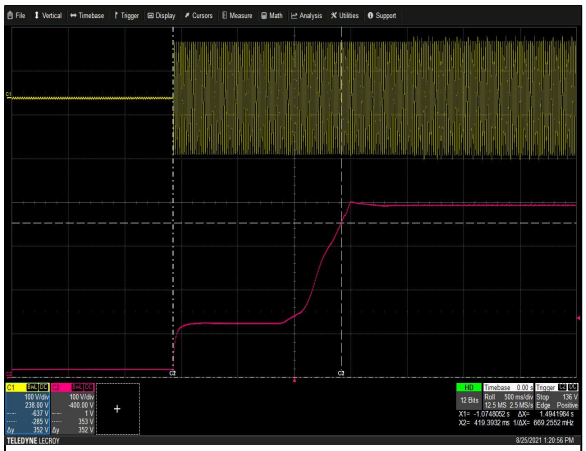


Figure 1: AIF04ZPFC-01L Turn-on delay via AC mains
Vin = 90Vac Load: Io = 0A Co = 470uF
Ch 1: Vin Ch 2: Vo

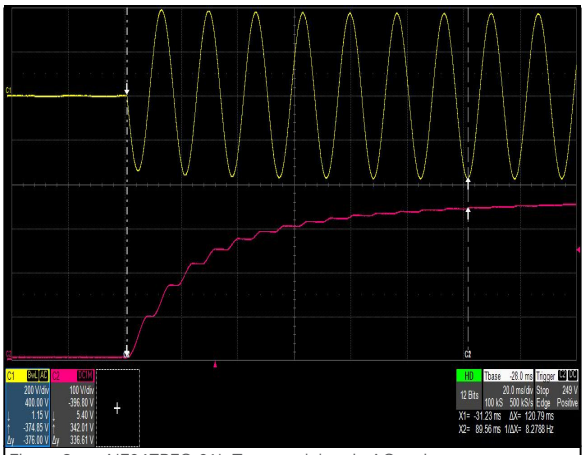


Figure 2: AIF04ZPFC-01L Turn-on delay via AC mains
Vin = 264Vac Load: Io = 0A Co = 470uF
Ch 1: Vin Ch 2: Vo

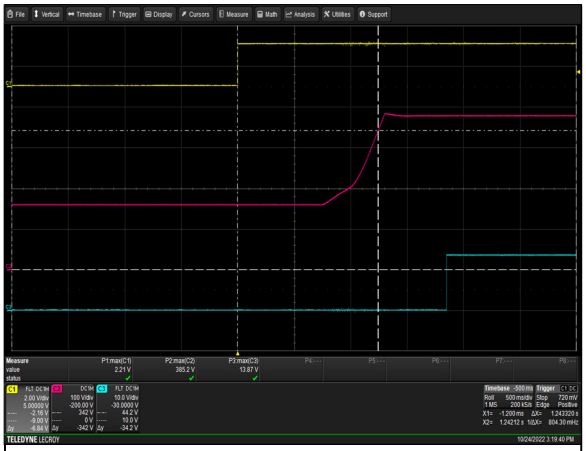


Figure 3: AIF04ZPFC-01L Turn-on delay via PF ENABLE
Vin = 115Vac Load: Io = 0A Co = 470uF
Ch 1: PF ENABLE Ch 2: Vo Ch 3: LD ENABLE

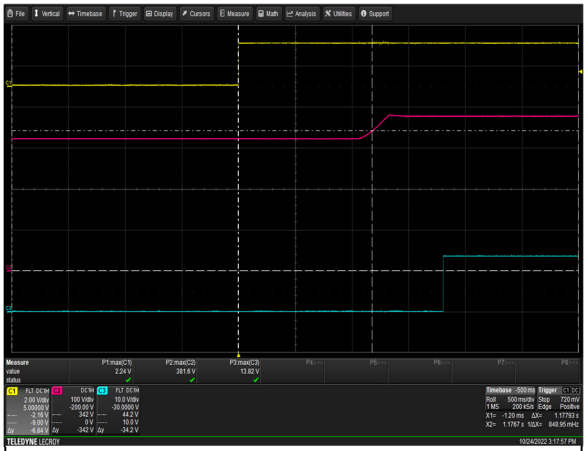


Figure 4: AIF04ZPFC-01L Turn-on delay via PF ENABLE
Vin = 230Vac Load: Io = 0A Co = 470uF
Ch 1: PF ENABLE Ch 2: Vo Ch 3: LD ENABLE

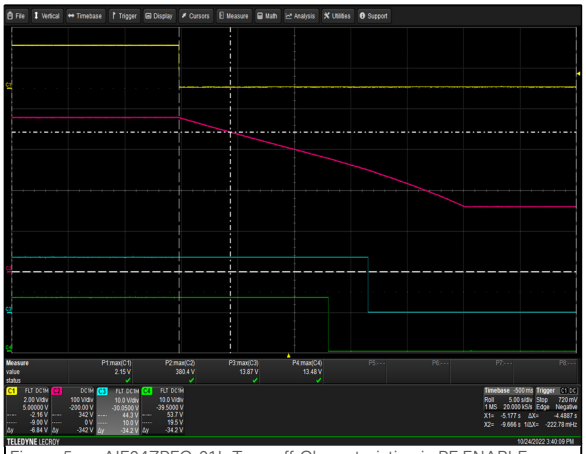


Figure 5: AIF04ZPFC-01L Turn-off Characteristic via PF ENABLE
Vin = 115Vac Load: Io = 0A Co = 470uF
Ch 1: PF ENABLE Ch 2: Vo Ch 3: LD ENABLE Ch 4: PFW

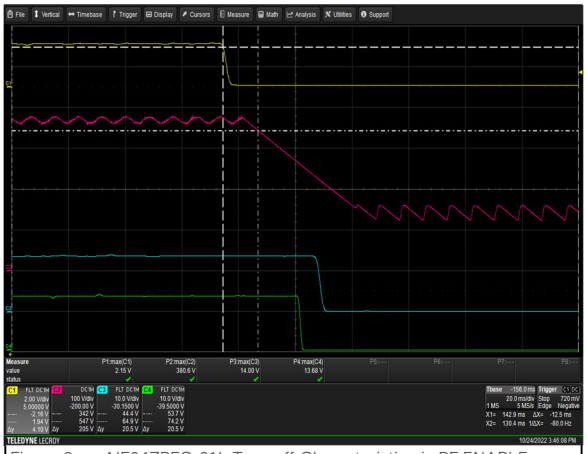


Figure 6: AIF04ZPFC-01L Turn-off Characteristic via PF ENABLE
Vin = 115Vac Load: Io = 2.6A Co = 470uF
Ch 1: PF ENABLE Ch 2: Vo Ch 3: LD ENABLE Ch 4: PFW

ELECTRICAL SPECIFICATIONS

AIF04ZPFC-01L Performance Curves

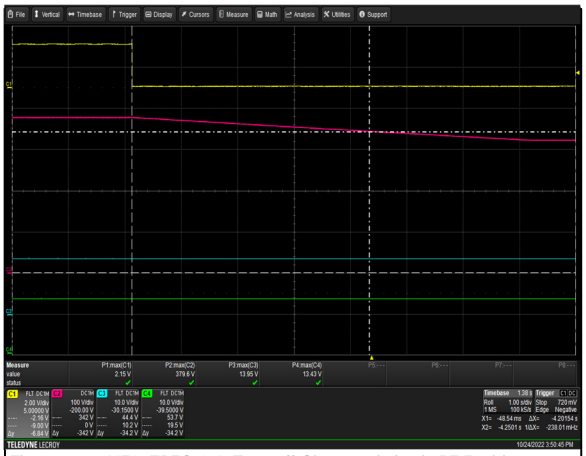


Figure 7: AIF04ZPFC-01L Turn-off Characteristic via PF Enable
Vin = 230Vac Load: Io = 0A Co = 470uF
Ch 1: PF Enable Ch 2: Vo Ch 3: LD Enable Ch 4：PFW

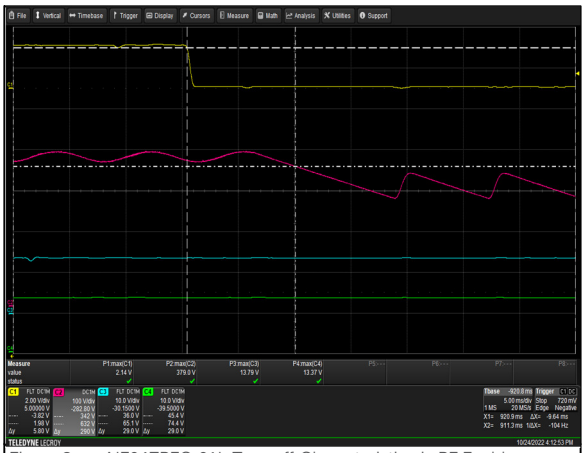


Figure 8: AIF04ZPFC-01L Turn-off Characteristic via PF Enable
Vin = 230Vac Load: Io = 4.2A Co = 470uF
Ch 1: PF Enable Ch 2: Vo Ch 3: LD Enable Ch 4：PFW

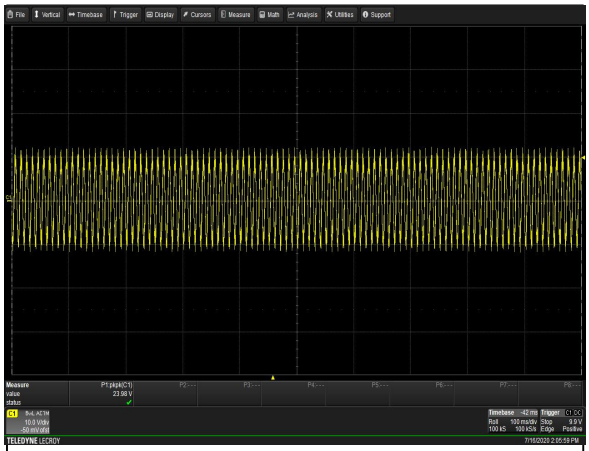


Figure 9: AIF04ZPFC-01L Ripple and Noise Measurement
Vin = 115Vac Load: Io = 2.6A Co = 470uF
Ch 1: Vo

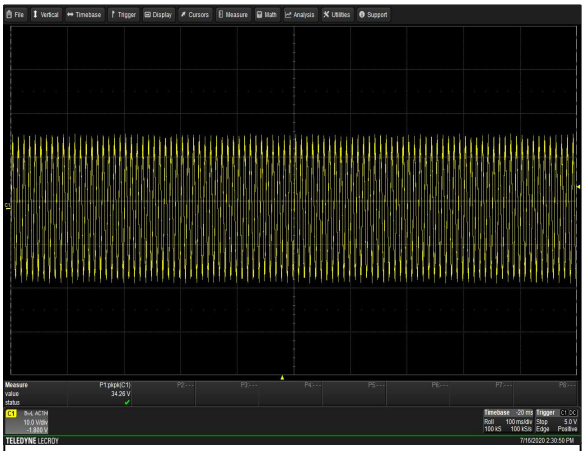


Figure 10: AIF04ZPFC-01L Ripple and Noise Measurement
Vin = 230Vac Load: Io = 4.2A Co = 470uF
Ch 1: Vo

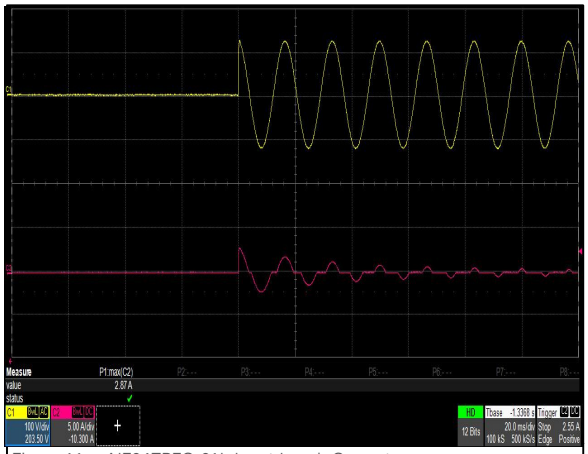


Figure 11: AIF04ZPFC-01L Input Inrush Current
Vin = 85Vac Load: Io = 0A Co = 470uF
Ch 1: Vin Ch 2: Iin

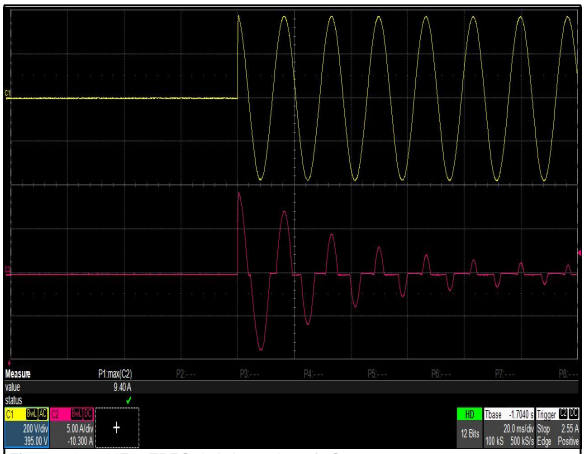


Figure 12: AIF04ZPFC-01L Input Inrush Current
Vin = 264Vac Load: Io = 0A Co = 470uF
Ch 1: Vin Ch 2: Iin

ELECTRICAL SPECIFICATIONS

AIF04ZPFC-01L Performance Curves

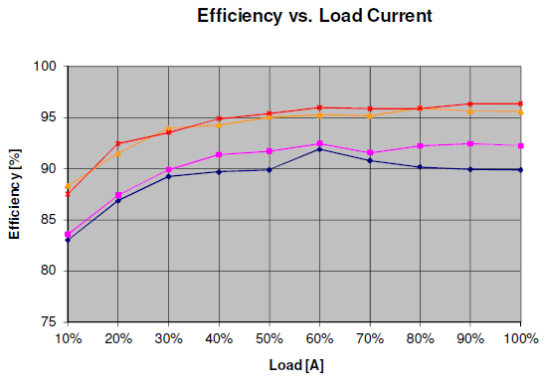


Figure 13: AIF04ZPFC-01L Turn-off Characteristic via PF Enable

85Vac 110Vac 230Vac 264Vac

Loading: I_O = 10%$I_{O,max}$ increment to 100%$I_{O,max}$

ELECTRICAL SPECIFICATIONS

Protection Function Specifications

Input Fuse

The AIF04ZPFC series module do not have an in-line fuse fitted internally. In order to comply with CSA, VDE and UL safety regulations, it is recommended that a fuse of 250Vac, 15A fast type be fitted at the module's input.

Input Undervoltage Protection

An input undervoltage protection circuit protects the module under low input voltage conditions. Hysteresis is built into the PFC series module to allow for high levels of variation on the input supply voltage without causing the module to cycle on and off. PFC modules will operate when the input exceeds 85Vac and turn off when input below 63Vac.

Over Voltage Protection (OVP)

The maximum over voltage point is 430Vdc. The power supply latches off during output over voltage with the AC line recycled to reset the latch.

Parameter	Min	Typ	Max	Unit
V_O Output Overvoltage	420	/	430	Vdc

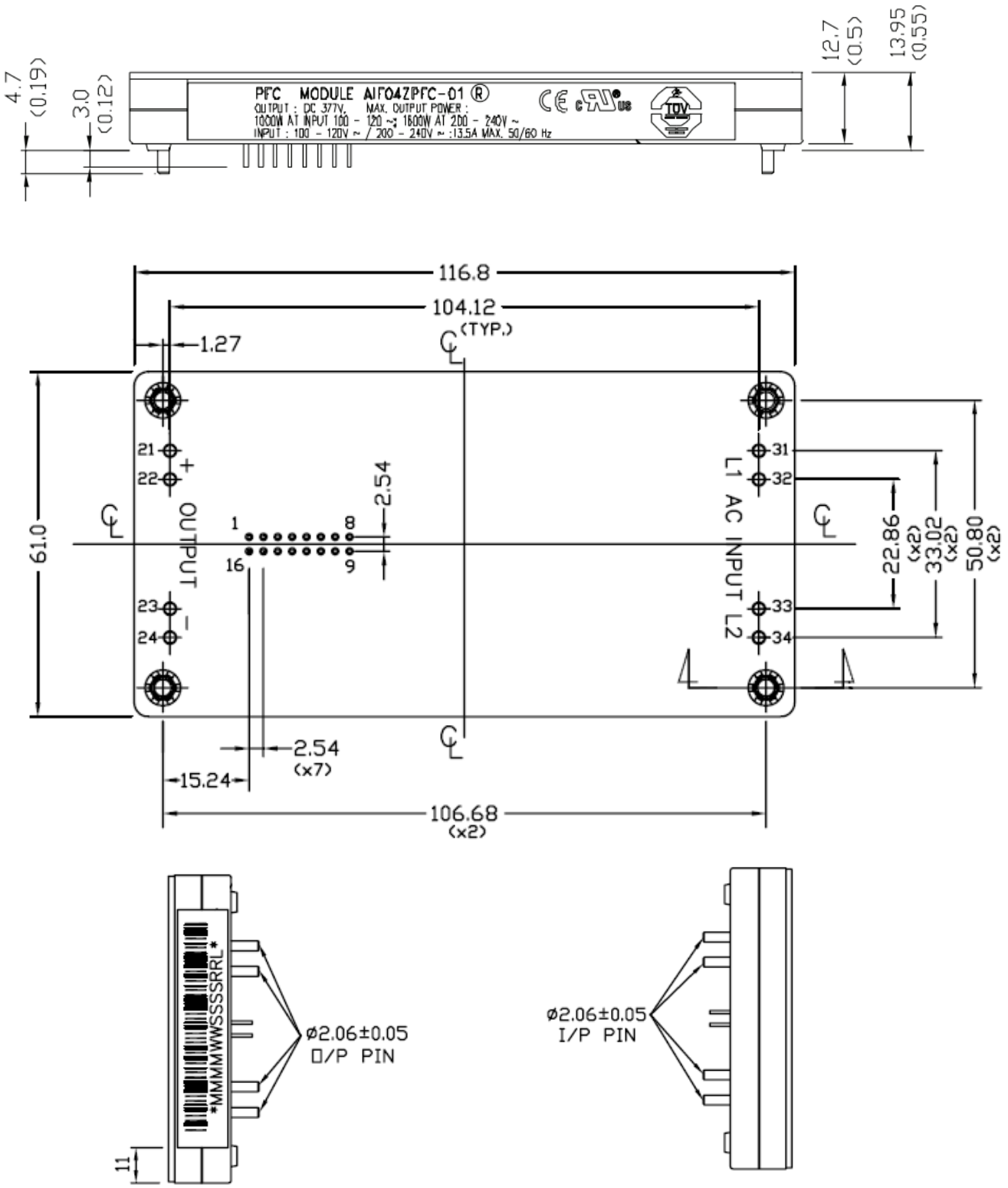
Over Temperature Protection (OTP)

The power supply have a thermal sensor to monitor its internal temperature. If the module's internal temperature exceeds 105^{O}C (typical), the module will shut down itself.

Parameter	Min	Typ	Max	Unit
Over Temperature	105	/	120	^{O}C

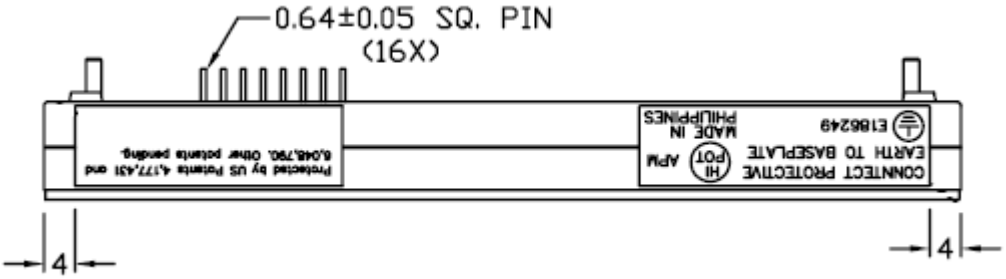
MECHANICAL SPECIFICATIONS

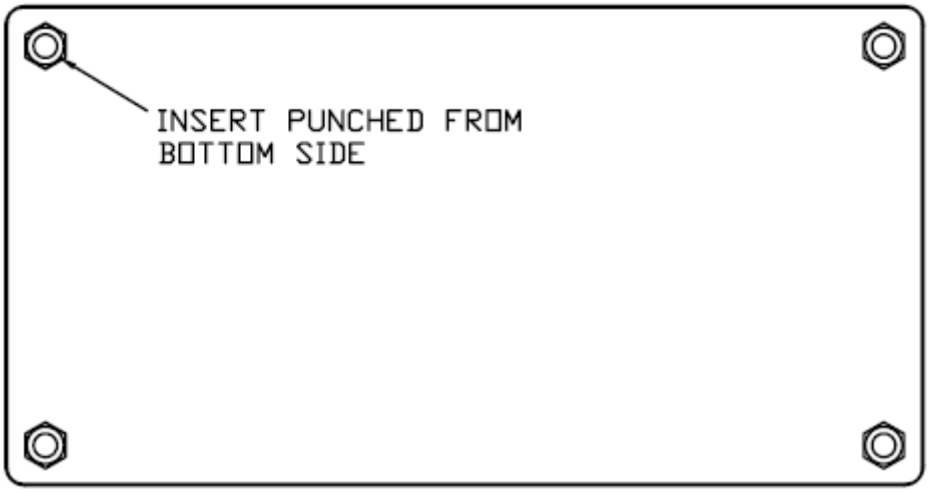
Mechanical Outlines (unit: mm)

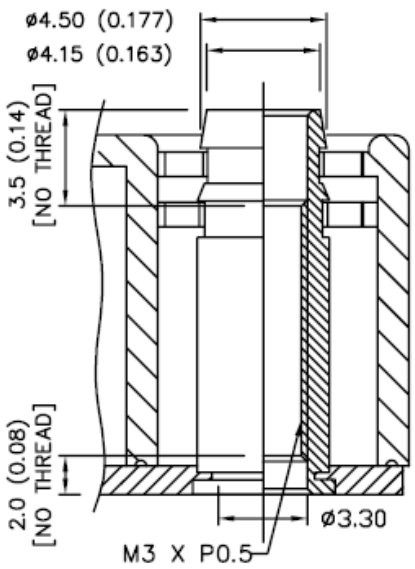


MECHANICAL SPECIFICATIONS

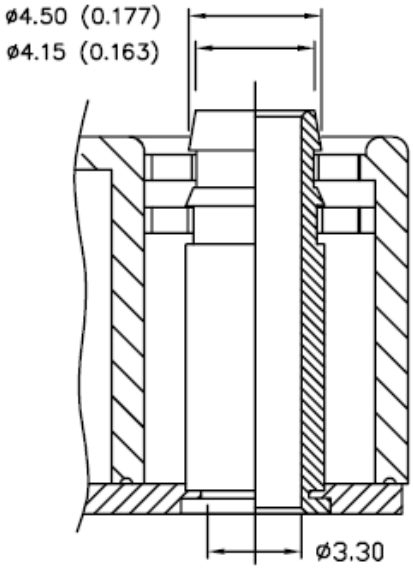
Mechanical Outlines (unit: mm)







THREADED INSERT



NO THREADED INSERT

MECHANICAL SPECIFICATIONS

Mechanical Outlines

Model Number	Stand off options
AIF04ZPFC-02NTL	3.3mm Hole, No thread
AIF04ZPFC-01NTL	3.3mm Hole, No thread
AIF04ZPFC-02L	M3 X P0.5 thread
AIF04ZPFC-01L	M3 X P0.5 thread

NOTES:

Surface flatness : Concave inwards: 0.12mm MAX

Convex outwards: 0.38mm MAX

Unless otherwise specified: Tolerance as below:

Whole Number	Decimal	Angle
+/-1	.X +/- 0.5	+/- 0.5^{O}
	.XX +/- 0.25	

MECHANICAL SPECIFICATIONS

Pin Assignments

Pin Assignments		
Input (AC)	Output (DC)	Control Pin
31. L1	21. Vout+	1. PV AUX-
32. L1	22. Vout+	2. TEMP MON
33. L2	23. Vout-	3. C MON
34. L2	24. Vout-	4. C SHARE
		5. CLK OUT
		6. CLK IN
		7. PV AUX+
		8. SDA
		9. SCL
		10. DC ENABLE
		11. V ADJ
		12. PFW ADJ
		13. S GND
		14. PFW
		15. LD ENABLE
		16. PF ENABLE

MECHANICAL SPECIFICATIONS

Weight

The AIF04ZPFC series module weight is 9.6oz / 300g typical.

ENIVIRONMENTAL SPECIFICATIONS

Safety Certifications

The AIF04ZPFC series module is intended for inclusion in other equipment and the installer must ensure that it is in compliance with all the requirements of the end application. This product is only for inclusion by professional installers within other equipment and must not be operated as a stand alone product.

Table 4. Safety Certifications for AIF04ZPFC power supply

Standard	Agency	Description
UL 62368-1, 2nd Ed, 2014-12-01, CAN/CSA C22.2 No. 62368-1-14, 2nd Ed	UL+CUL	US and Canada Requirements
EN 62368-1:2014/A11:2017	TUV	Europe Requirements
EN 62368-1:2014/A11:2017	CE	CE marking by internal verification/certificate
UKCA Mark		UK Requirements

ENIVIRONMENTAL SPECIFICATIONS

EMI Emissions

The AIF04ZPFC series module will require additional EMI filtering to enable the system to meet relevant EMI standards. PFC modules have an effective input to ground (baseplate) capacitance of 1600pF. This should be accounted for when calculating the maximum EMI 'Y' capacitance to meet ground leakage current specifications. An example filter circuit is shown below.

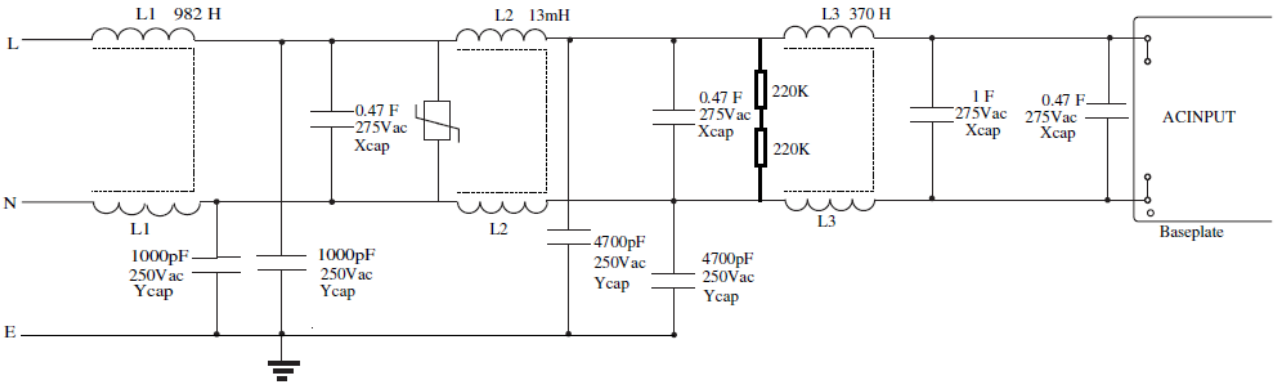


Figure 14: Reference EMI Filter Circuit (Single AIF04ZPFC series module)

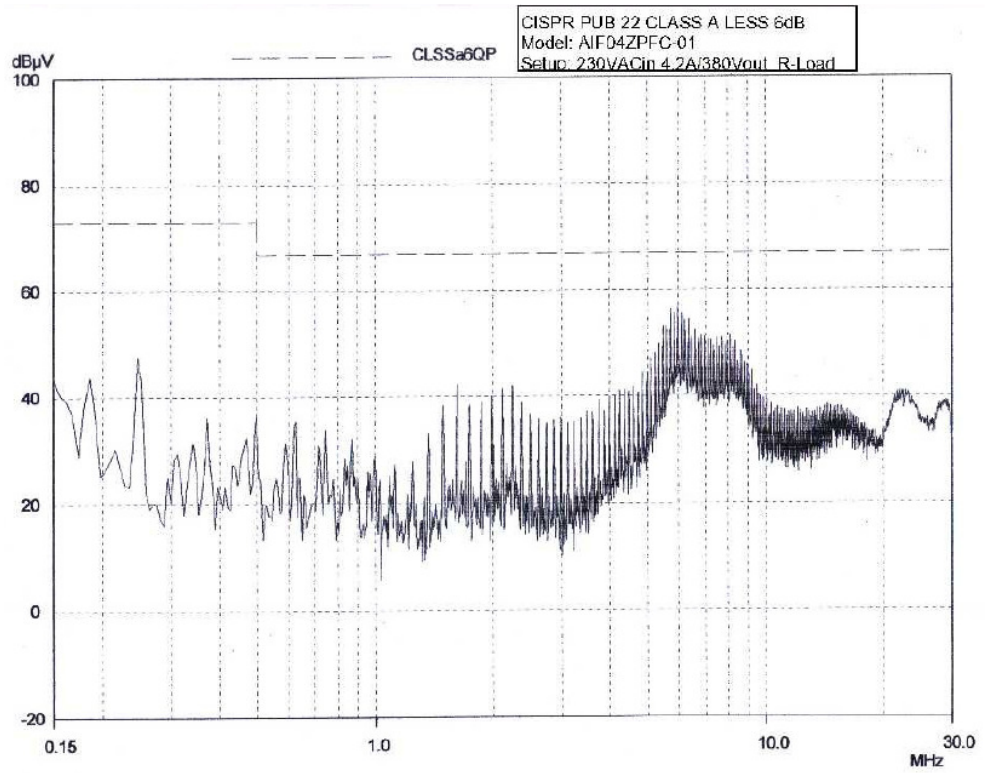


Figure 15: Conducted Emissions (Single AIF04ZPFC series module @ Vin=230Vac)

ENIVIRONMENTAL SPECIFICATIONS

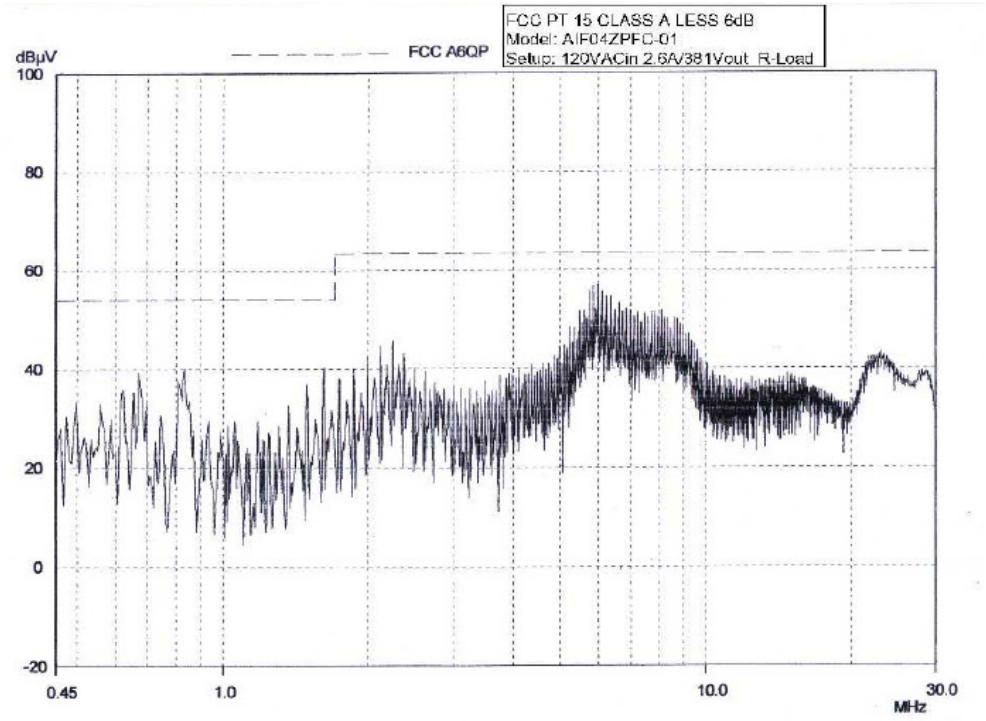


Figure 16: Conducted Emissions (Single AIF04ZPFC series module @ Vin=120Vac)

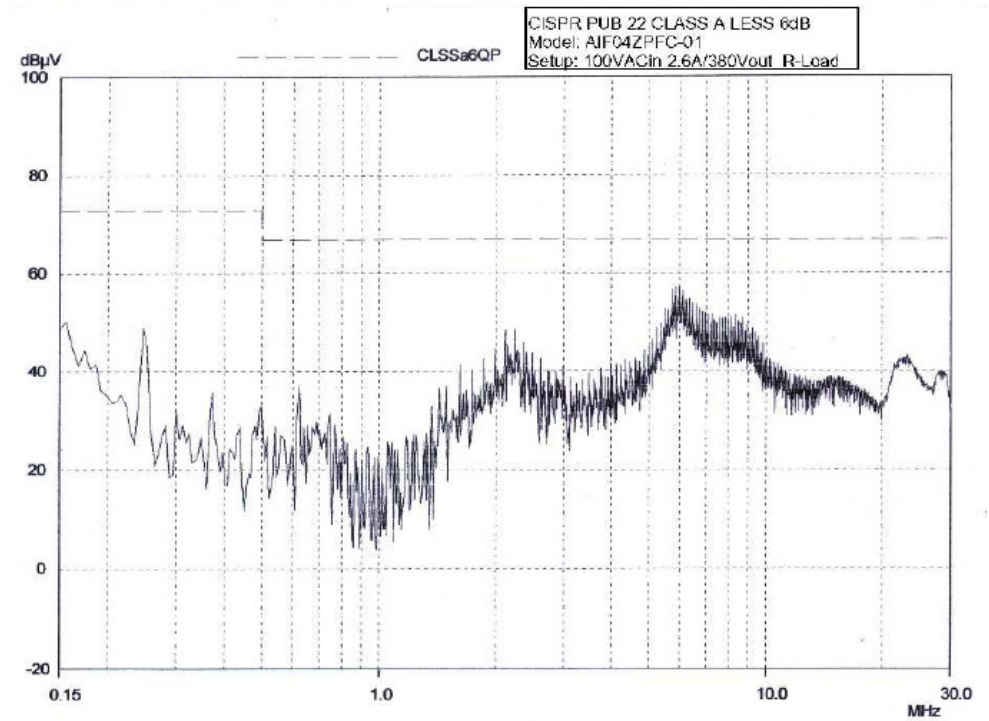


Figure 17: Conducted Emissions (Single AIF04ZPFC series module @ Vin=100Vac)

ENIVIRONMENTAL SPECIFICATIONS

Storage and Shipping Temperature

The AIF04ZPFC series module can be stored or shipped at temperatures between -40^{O}C to +110^{O}C and relative humidity from 0 to 95%, non-condensing.

Humidity

The AIF04ZPFC series power supply can be operated/stored in a relative humidity from 0 to 95% non-condensing.

POWER AND CONTROL SIGNAL DESCRIPTIONS

AC Input Pin

These pins provide the AC Mains to the AIF04ZPFC series module.

Pin 31 - AC Input Line / Return
Pin 32 - AC Input Line / Return
Pin 33 - AC Input Return / Line
Pin 34 - AC Input Return / Line

DC Output Pin

These pins provide the main output for the AIF04ZPFC series module. The "+" and the "-"pins are the output positive and output negative rails. The output (V_O) pins are electrically isolated from the power supply chassis.

Pin 21 - (+) Output (Vo)
Pin 22 - (+) Output (Vo)
Pin 23 - (-) Output (Vo Return)
Pin 24 - (-) Output (Vo Return)

Control Signals

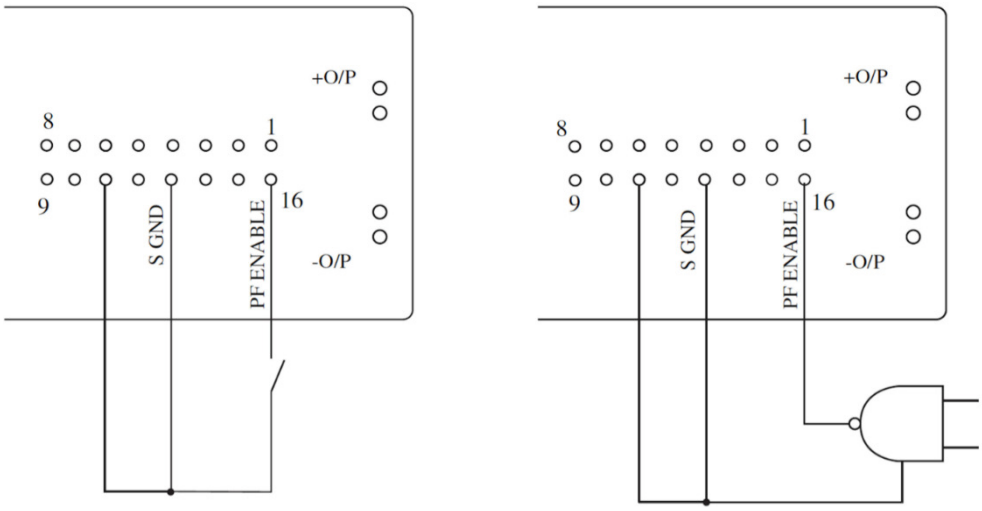
The AIF04ZPFC series module contains a 16 pins control signal header providing an analogue control interface, temperature monitor and PFC module status warning interface, all signals are on primary side.

PF ENABLE - (pin 16)

The PF ENABLE pin is a TTL compatible input used to turn the output of the module on or off.

For module with no suffix, the output is enabled when the PF ENABLE is open or driven to a logic high > 2.2V. The output is disabled when the PF ENABLE is connected to S GND or driven to a logic low of < 0.8V (but not negative).

For module with suffix "N", the output is enabled when the PF ENABLE is connected to S GND or driven to a logic low < 0.8V (but not negative). The output is disabled when the PF ENABLE is open or driven to a logic high > 2.2V.



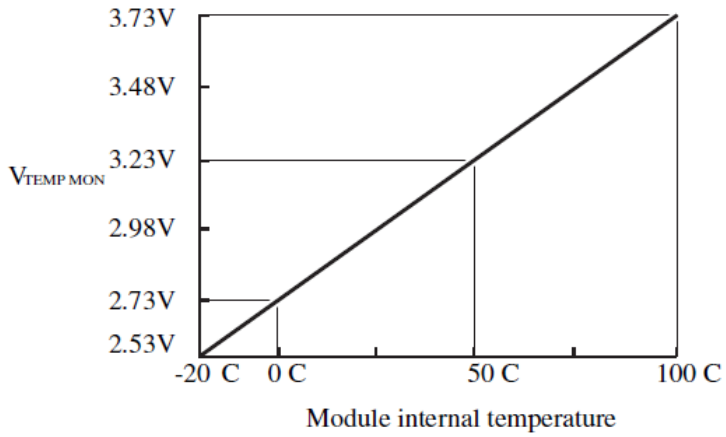
POWER AND CONTROL SIGNAL DESCRIPTIONS

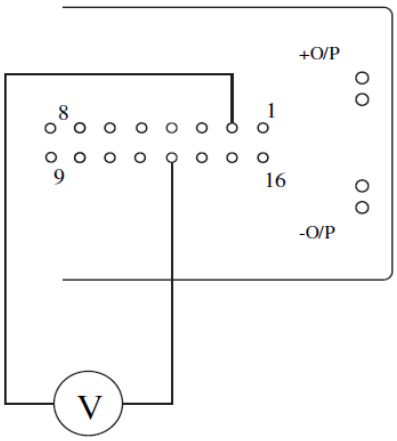
TEMP MON - (pin 2)

The TEMP MON pin provides an indication of the module's internal temperature. The voltage at the TEMP MON pin is proportional to the temperature of the module baseplate at 10mV per ^{O}C. Where:

Module temperature (^{O}C) = ($V_{TEMP\ MON}$ x 100) - 273

The temperature monitor signal can be used by thermal management systems (e.g. to control a variable speed fan). It can also be used for over temperature warning circuits and for thermal design verification of prototype power supplies and heatsink.



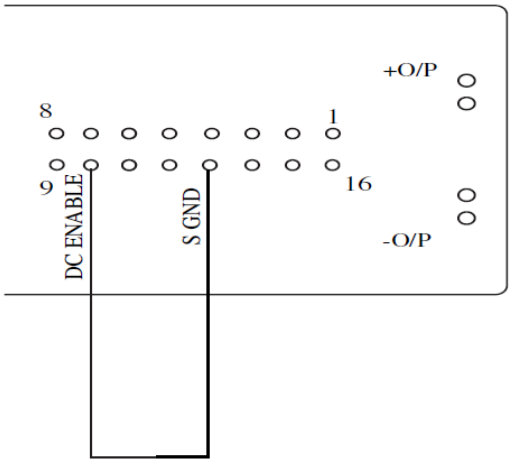


PV AUX- / PV AUX+ - (pins 1,7)

It supports 10V 20mA logic driving. PV AUX+ and PV AUX- are isolated with power rail & signal ground, and the isolated voltage is 800V max. It can't support current share, and PV AUXs from different PFC modules cannot be directly tied together. External Oring diode connection method could be used to support PV AUX redundant application.

DC ENABLE - (pin 10)

For using DC input, connect the DC ENABLE pin to S GND



POWER AND CONTROL SIGNAL DESCRIPTIONS

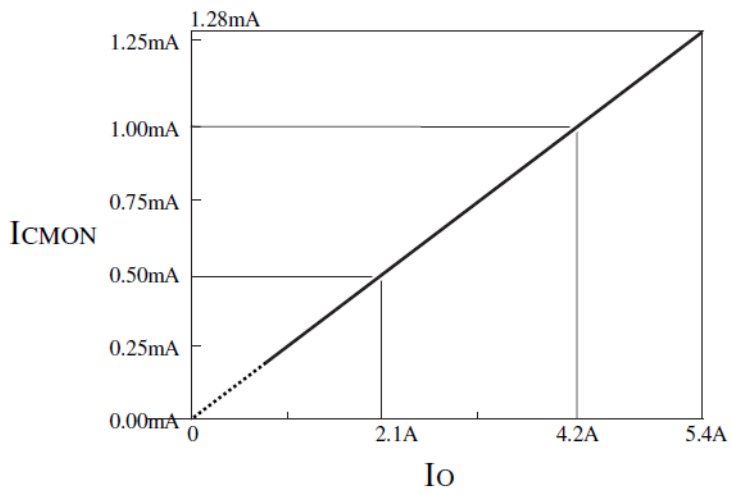
C MON - (pin 3)

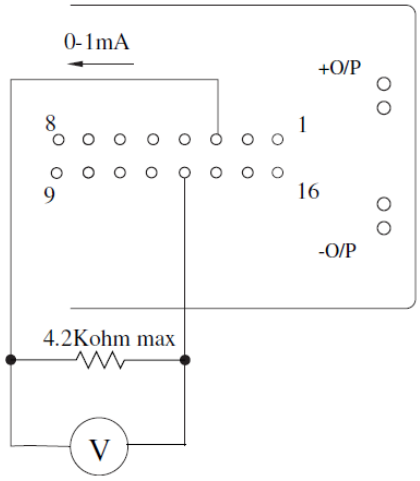
The C MON pin provides an indication of the amount of current supplied by the module. The output of the C MON pin is a voltage source proportional to the output current of the module,

where Io / $I_{C\ MON}$ = 4.2A/1mA

If a 4.2K ohm resistor is connected then the voltage in Volts on the C MON pin is directly equivalent to the current supplied by the module in Amps.

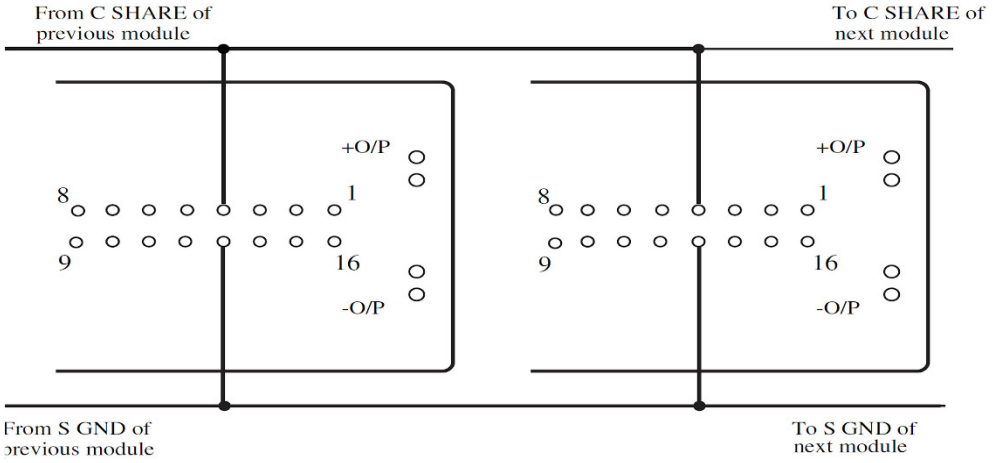
Maximum voltage on C MON is 6V.





C SHARE - (pin 4)

The C SHARE pins and S GND pins on each of the sharing group modules shall be connected together to ensure all modules in a parallel system accurately share current. Current flow to S GND must less than 25 mA.



The voltage on the C SHARE pins represents the average load current per module. Each module compares this average with its own current and adjusts its output voltage to correct the error. In this way the module maintains accurate current sharing even under variable or light load conditions.

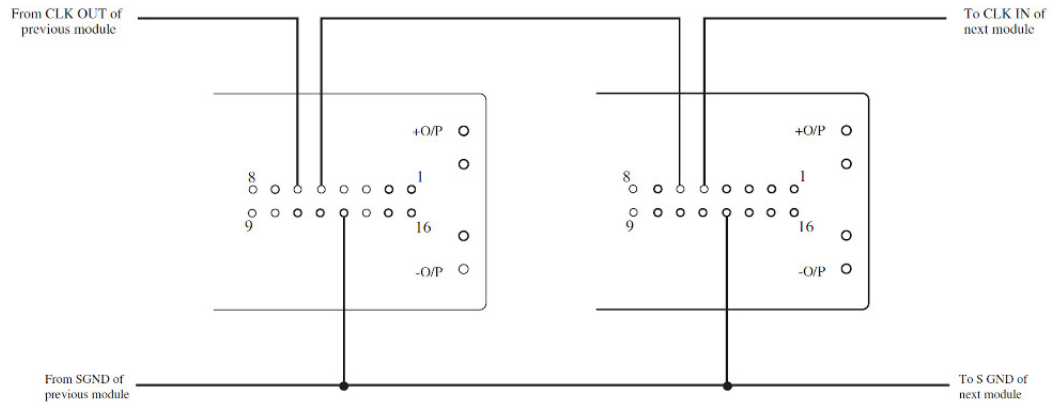
In multi-module paralleled systems, all modules will share current to within ± 10% of the average load current per module when the C SHARE pins of each module are connected together.

POWER AND CONTROL SIGNAL DESCRIPTIONS

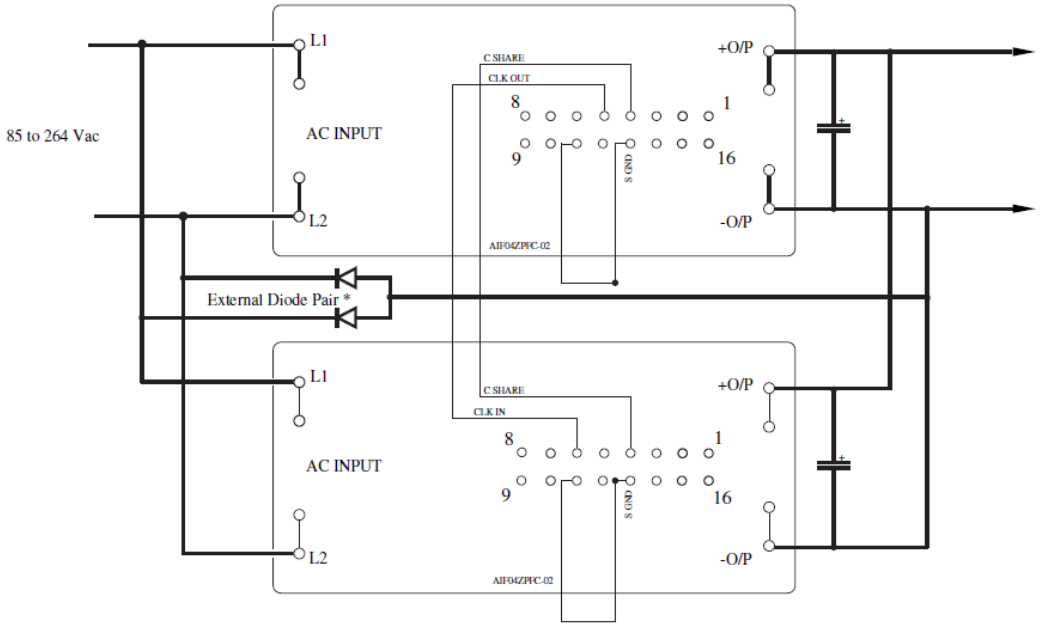
CLK OUT, CLK IN - (pins 5, 6)

The PFC's internal clock is accurate and stable over its full operating range and synchronization is not normally required but it can reduce noise & have better EMI performance in paralleled systems.

Clock signals can be wired in series (the CLK OUT pin of one module to the CLK IN pin of the next etc) in which case all the modules will be synchronized with the first module in the chain. Alternatively, an external clock signal of TTL signal of TTL level at 1MHz ±10% can be connected to the CLK IN pins of all the modules.



Modules are synchronized by connecting the CLK OUT pin of one module to the CLK IN of the next module in an open daisy chain configuration. If the clock input to a module fails, it will automatically revert to its internal clock and continue to operate at full power. The CLK IN and CLK OUT signals are AC coupled.

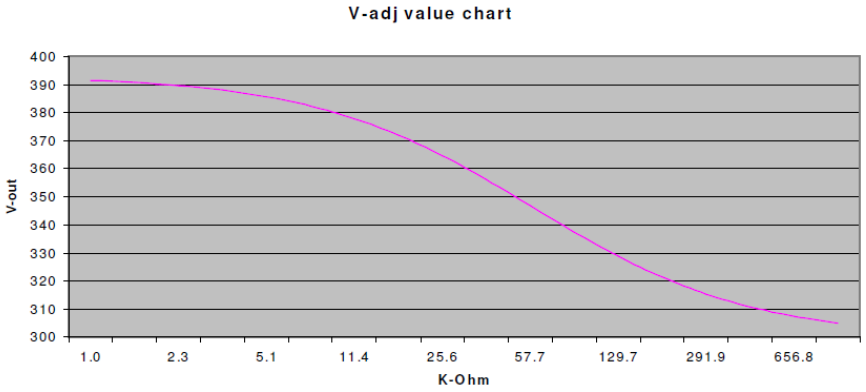


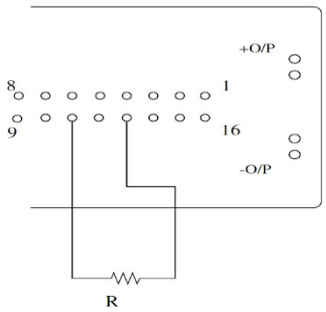
The current rating requirement of external rectifier for each line is 20A x number of units in parallel. For example, if there are 3 pieces of AIF04ZPFC-02 in parallel, customer will need to put 60A (20A x 3) external rectifier for each line.

POWER AND CONTROL SIGNAL DESCRIPTIONS

V ADJ - (pin 11)

The output voltage of the module can be accurately adjusted from 76% to 100% of the normal output voltage. Adjustment can be made using a resistor connected as below





Vout = Vr x (1+Rh x (1 / (Rj + R) + 1 / Rw)) + 10.94

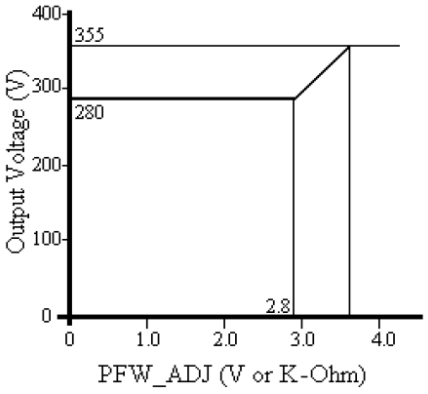
Where:
R is the resistor connected between the V ADJ pin to S_GND (units in Kohm)

Vr = 5.029
Rh = 1084
Rw = 19.2
Rj = 58.5

PFW ADJ (Power Fail Warning Adjust) - (pin 12)

The level at which a Power Fail Warning occurs can be programmed using the PFW adjust input(pin 12). If the pin is left unconnected then the PFW operates at the default factory set value.

The output from the PFW ADJ pin is a 1mA current source. To adjust the PFW threshold, a voltage source (0 - 4V) or a programming resistance (0 - 4Kohm) referenced to S GND (pin 13) should be connected. This allows adjustment of the PFW threshold from 280V up to 340V. The value of resistance or voltage required can be read from the graph of below.



POWER AND CONTROL SIGNAL DESCRIPTIONS

S GND - (pin 13)

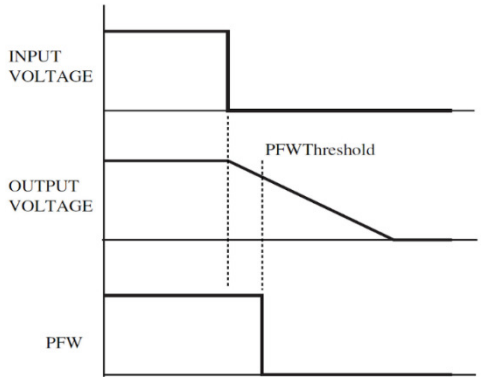
The S GND pin internally connected to the common ground of the module, it's also internally connected to the -O/P terminals.

When connecting S GND to external circuitry care must be taken to ensure that the current flowing through this pin is kept below 25mA.

PFW - (pin 14)

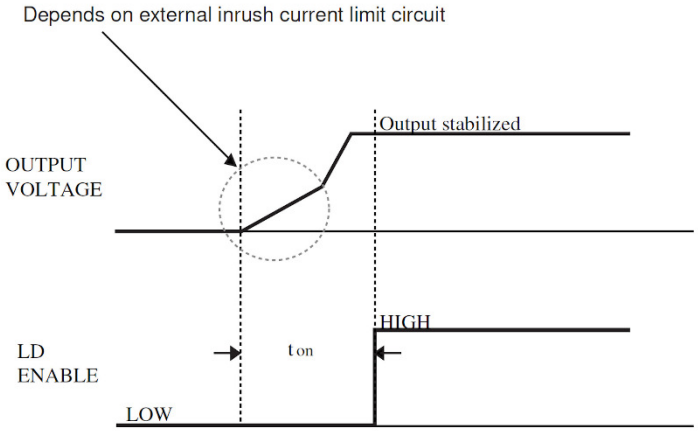
If output voltage can not be maintained at the pre-programmed PFW threshold voltage, the PFW (pin 14) will go from HIGH to LOW.

The output of the PFW signal can drive an opto-coupler to provide an isolated signal from primary side to the secondary side. The nominal factory set PFW threshold is set at 340V.



LD ENABLE - (pin 15)

After the PFC power up sequence, the power to the load can be enabled, and the PFC can automatically enable the load using the LD ENABLE signal.

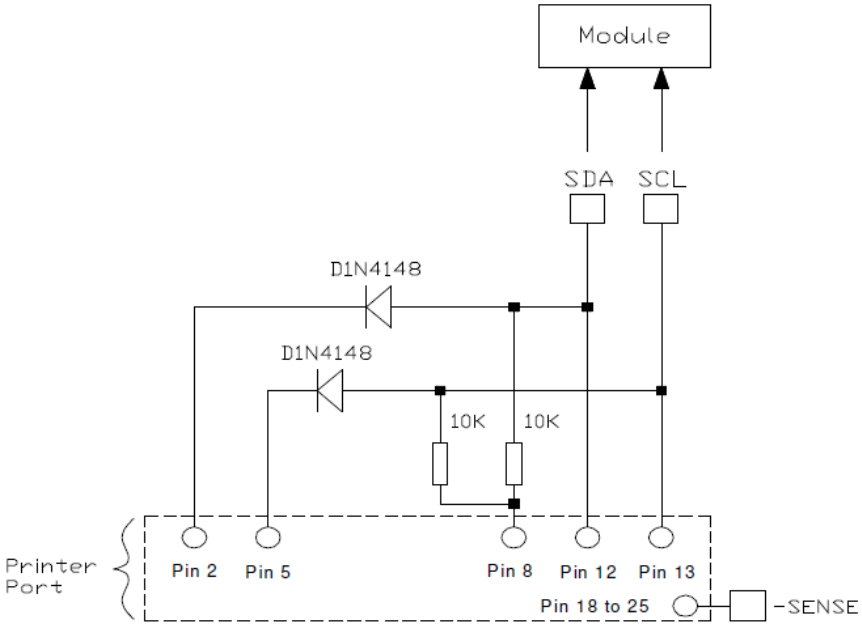


Initially the load is disabled and the LD ENABLE (pin 15) is at 0.4V (LOW). When the PFC power up sequence has completed, the LD ENABLE voltage goes HIGH. And the LD ENABLE will stay high as long as Vin is above 175Vac or Vout is above 250V, even if PF_ENABLE is in disable mode. The LD ENABLE pin is capable of delivering 2.7mA at 1.5V when HIGH.

POWER AND CONTROL SIGNAL DESCRIPTIONS

I2C EEPROM Content Programing - SDA&SCL - (pin 8 & pin 9)

This function is provided for product information storage, template as per customer define. Connect RS232 (Printer Port) from PC to test unit at 300Vdc in and test with Read/Write capability of the I2C EEPROM.



MCU Internal Flash Memory

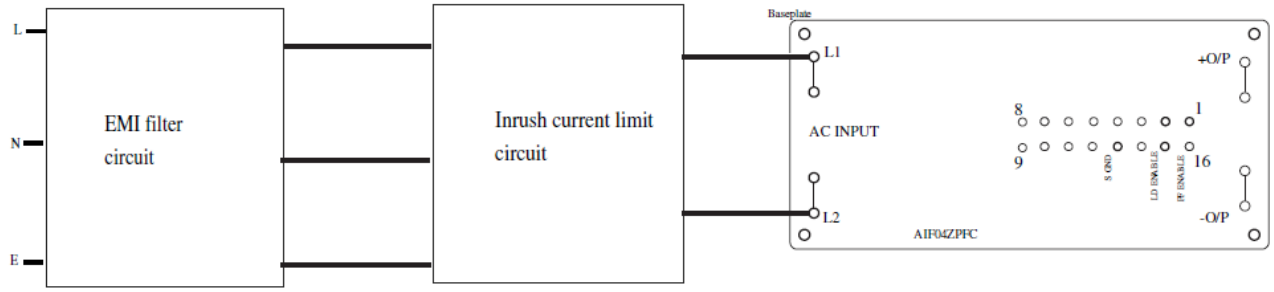
The module is equipped with a 256 Kbyte flash memory. This device will be programmed during the manufacturing process. The EEPROM content will include the following information:

- Manufacturer name string “ Artesyn”
- Product name and product number
- Serial number assigned by manufacturer
- Max output power

APPLICATION NOTES

PFC Module Input Connection Diagram

Below block diagram is the application connection of the AIF04ZPFC series module.



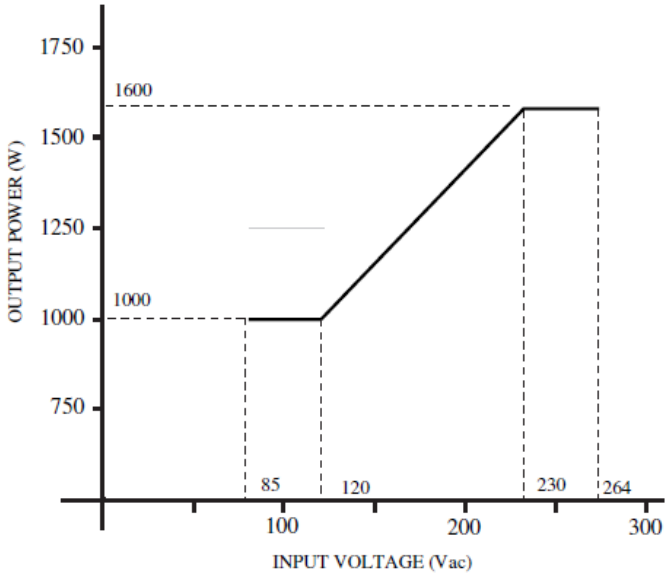
AIF04ZPFC-02 Parallel Operation

The AIF04ZPFC-02 has been specifically designed for paralleling applications where the total input current exceeds 16Arms. For stand-alone applications or those where the total input current does not exceed 16Arms, the AIF04ZPFC-01 is recommended.

The AIF04ZPFC-02 requires external negative rail rectifiers to be implemented at the input to the system. It is possible to operate the AIF04ZPFC-02 as a stand-alone configuration although the external negative rail rectifiers must still be provided.

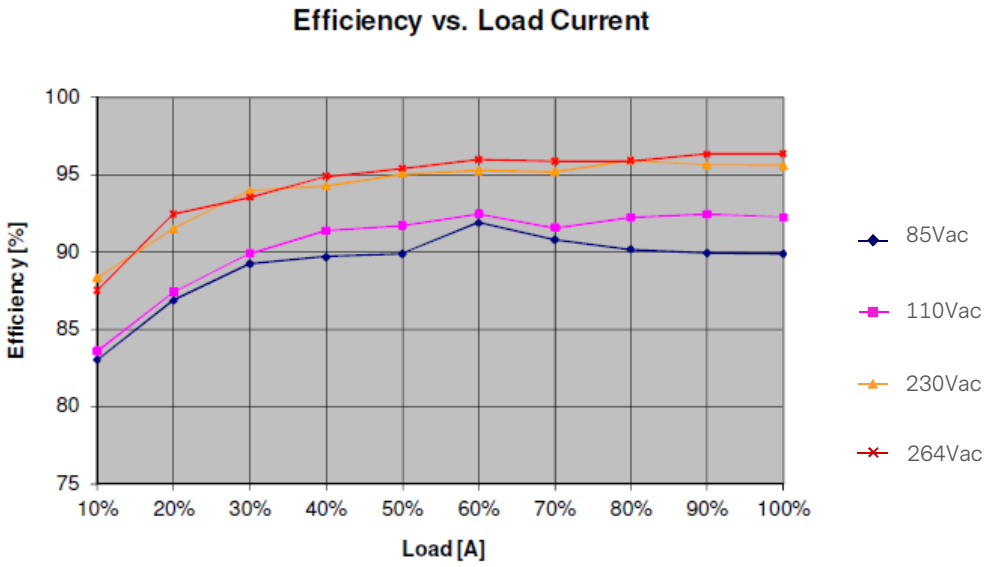
Maximum Output Power Vs Input Voltage

The maximum output power available varies with the input voltage as shown below.



APPLICATION NOTES

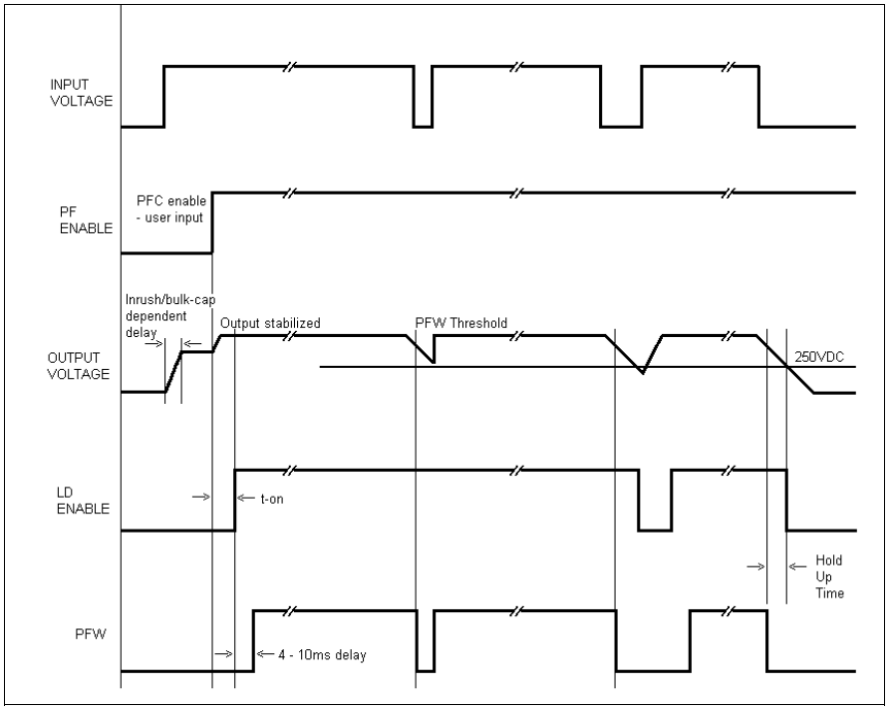
Efficiency Vs Input Voltage and Output Power



PF & Load Enable Connections and Timing

The PFC module must be supplied with a PF ENABLE signal to initiate the start-up sequence. The output of the LD ENABLE pin goes HIGH (ON) once the PFC has completed the start-up sequence.

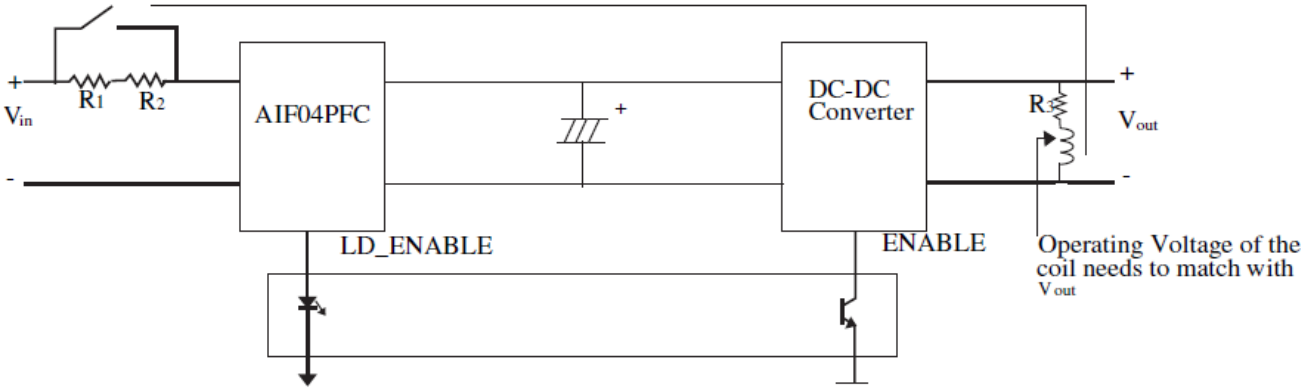
It is recommended that the LD ENABLE signals is always used to enable the load, however, if the load is to be enabled manually it is essential that the ton time has expired before enabling occurs.



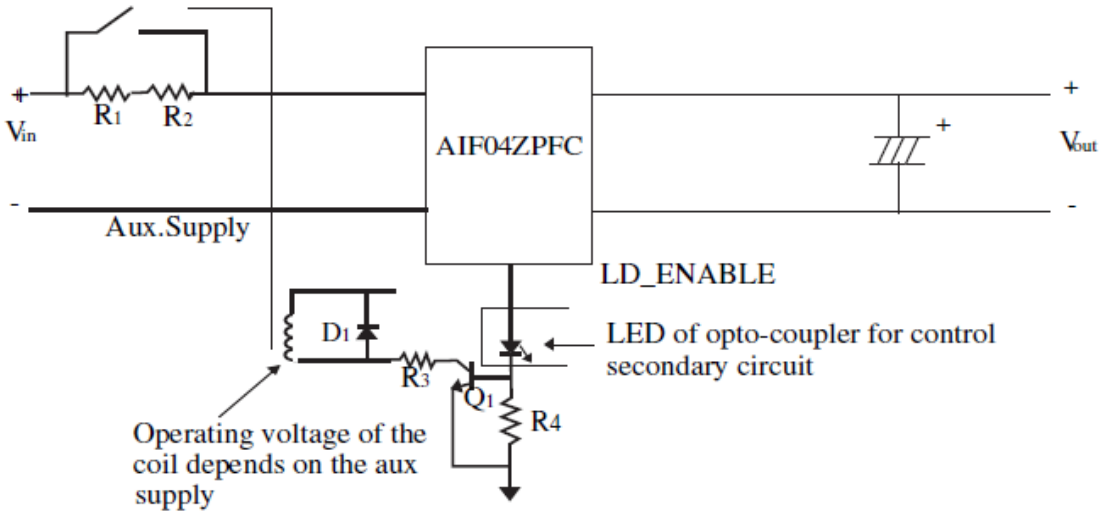
APPLICATION NOTES

Recommend external Inrush Current Limit circuit

Using relay controlled from secondary side.



Using relay controlled by Auxiliary supply on primary side.



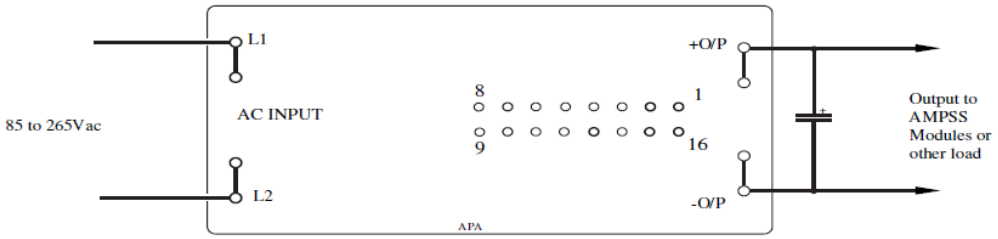
Inrush Limit for PFC Series

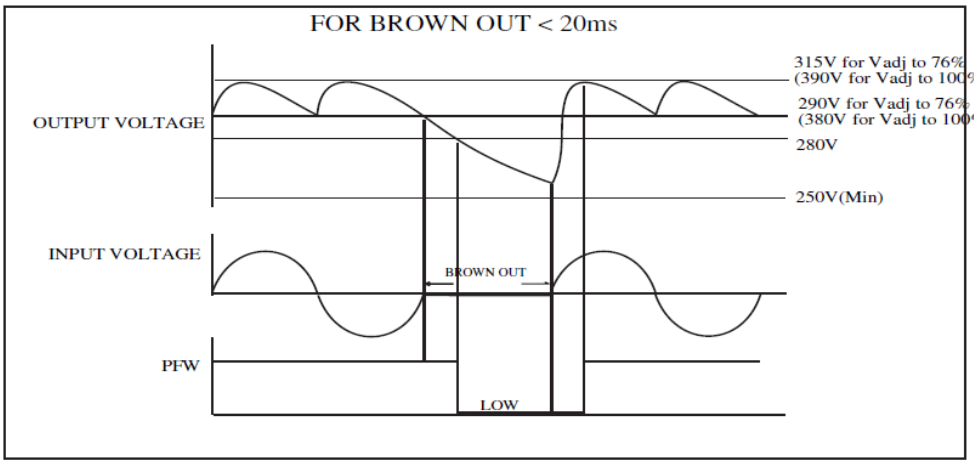
APPLICATION NOTES

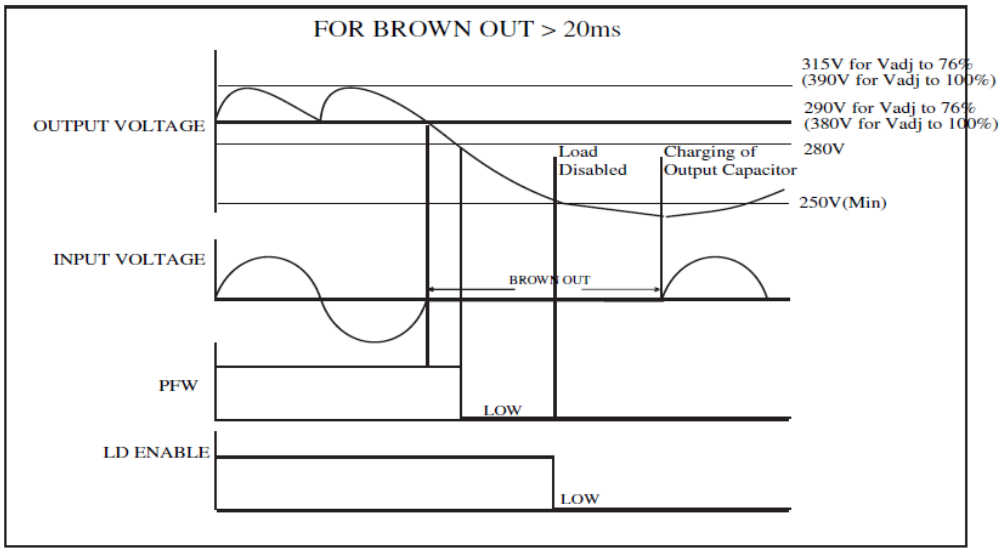
Brown Out Ride Through

Brown Out conditions occurs when there is a transient break in input voltage. During this period the external output bulk capacitor holds up the voltage to the load until input current is restored. When the input voltage is restored the PFC module will continue delivering power to the load.

After a Brown Out condition where the output voltage has not dropped below 250Vdc, the module will recover when input power is restored. The PFW signal can be used to monitor input power loss.





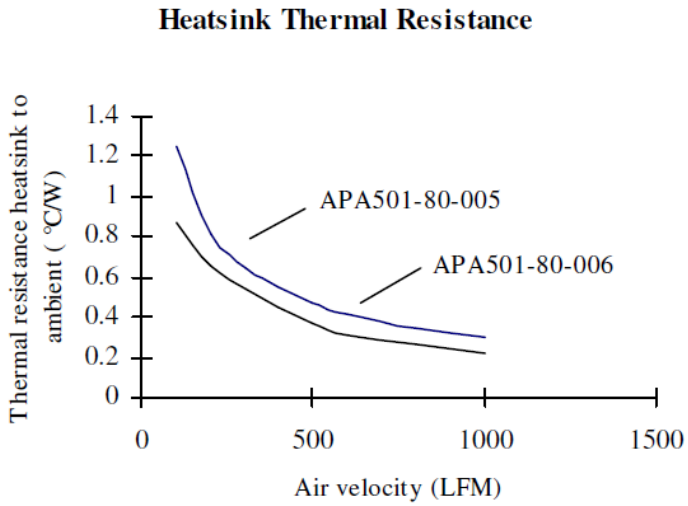


APPLICATION NOTES

Thermal Data

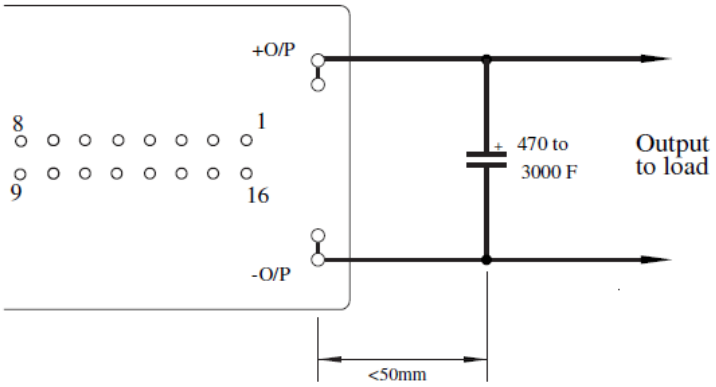
Natural convection thermal impedance of the PFC package without a heatsink is approximately 4°C/W.

A standard horizontal fin heatsink available from Artesyn (part number APA501-80-006) with 37mm fins and 8.8mm pitch, will reduce module thermal impedance to 0.4°C/W with a forced air flow of 2.5m/s (500LFM) when mounted with a thermal pad (Artesyn P/N APA502-80-001) between heatsink and module.



Output Capacitor

The PFC requires an output hold-up capacitor of between 470uF and 3000uF to prevent the module from disabling due to fluctuations in output voltage. Ideally the capacitor should be connected directly to the PFC output pins. If this is not possible, the connection is recommended less than 50mm from the output pins.



Selecting an External Output Capacitor

The output capacitor value is determined by the following factors:
1. RMS ripple current.
2. Peak-to-peak output ripple voltage.
3. Hold-up time.
4. Expected lifetime of the capacitor.

APPLICATION NOTES

RMS Ripple Current

The maximum permissible RMS ripple current for the output capacitor should be greater than the RMS ripple current for the application. The ripple current for the PFC module can be approximated as

$$I_{rms} = (P_O / Eff) \times 1V (V_O \times V_{rms})$$

where :

P_O = output power (W)
Eff = efficiency (%)
V_O = output voltage (V)
Vrms = input rms voltage (V)

This gives the ripple current at 125KHz. The maximum ripple current for capacitors is usually specified at 120Hz. To convert from 125KHz to 120Hz the Irms figure should be divided by 1.3.

Peak to Peak Output Ripple Voltage

The ac input causes a ripple on the output voltage. The size of the ripple is inversely proportional to the size of the capacitor. Therefore the maximum allowable ripple voltage should be decided in order to calculate the size of capacitor required. This may be calculated using the following equation:

$$C_O = P_O / (2\pi f \times Eff \times V_O \times V_{rms})$$

where :

C_O = output capacitance (F)
Eff = efficiency (%)
f = input voltage frequency (Hz)
V_O = output voltage (V)
V_{ripple} = output ripple voltage (V)

Hold-Up Time Requirement

The output capacitor value is different for different hold-up time requirements. The minimum capacitance corresponding to the required hold-up time of a system comprised of AE DC/DC power modules and an AIF04ZPFC series module can be calculated as follows:

$$C_{O,min} = (2 \times P_O \times T_{hold})/[(V_O - V_{ripple})^2 - (V_{min})^2]$$

Where :

$C_{O,min}$ = output capacitance (F)
P_O = output power (W)
T_{hold} = hold up time (sec)
V_O = output voltage (V)
V_{ripple} = output ripple voltage (V)
V_{min} = 290V of LD Enable OFF level (or minimum input voltage for DC/DC module if the setting is higher than 290V)

For example:

A PFC module driving 3pcs of AIF80A300 400W modules @ 5Vo. Efficiency of the AIF80A300 module is 88%, the minimum input voltage is 250V, the output voltage of the PFC is 380V, the required hold-up time is 20mS and the peak-to-peak voltage V_{ripple} is chosen to be 16V.

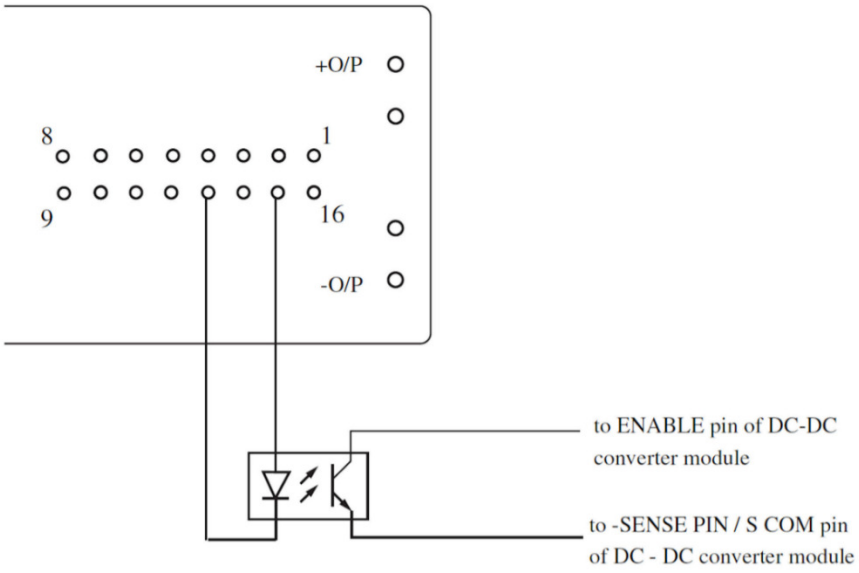
$$C_{O,min} = \frac{2 \times (3 \times 400/0.88) \times 0.02}{[(380-16)^2-250^2]} = 780\mu F$$

This figure is the minimum capacitance. To allow for capacitor tolerances and aging effects the actual value is recommended more than 1.5 times

APPLICATION NOTES

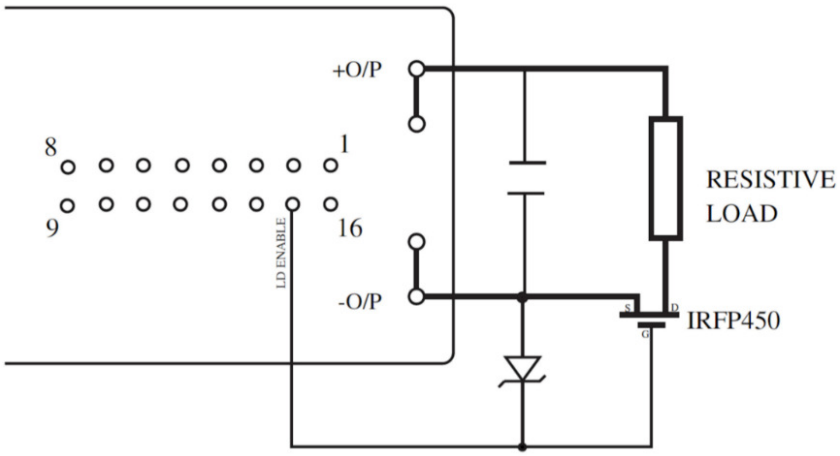
Connections to enable DC-DC converters

The output from the AIF04ZPFC's LD ENABLE (pin 13) can directly drive an opto-coupler to provide an isolated signal to enable the power output of one or more AE DC-DC converter modules.



General Connections to Enable a Resistive Load

For enabling resistive loads other than AE DC-DC converters the following circuit can be used. The LD ENABLE pin can directly drive a MOSFET with a 15V zener clamping the gate voltage.

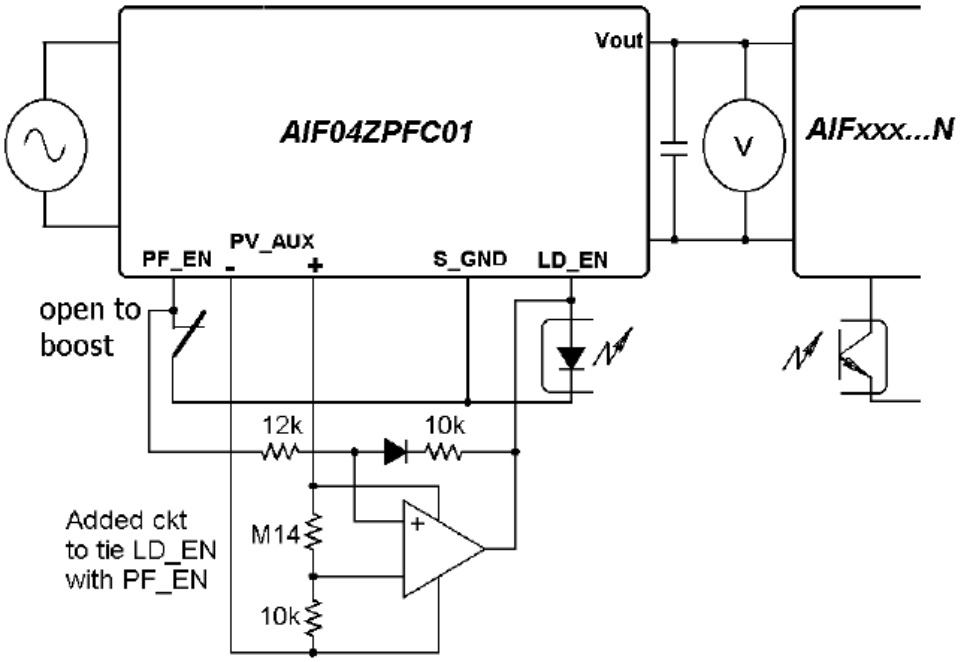


APPLICATION NOTES

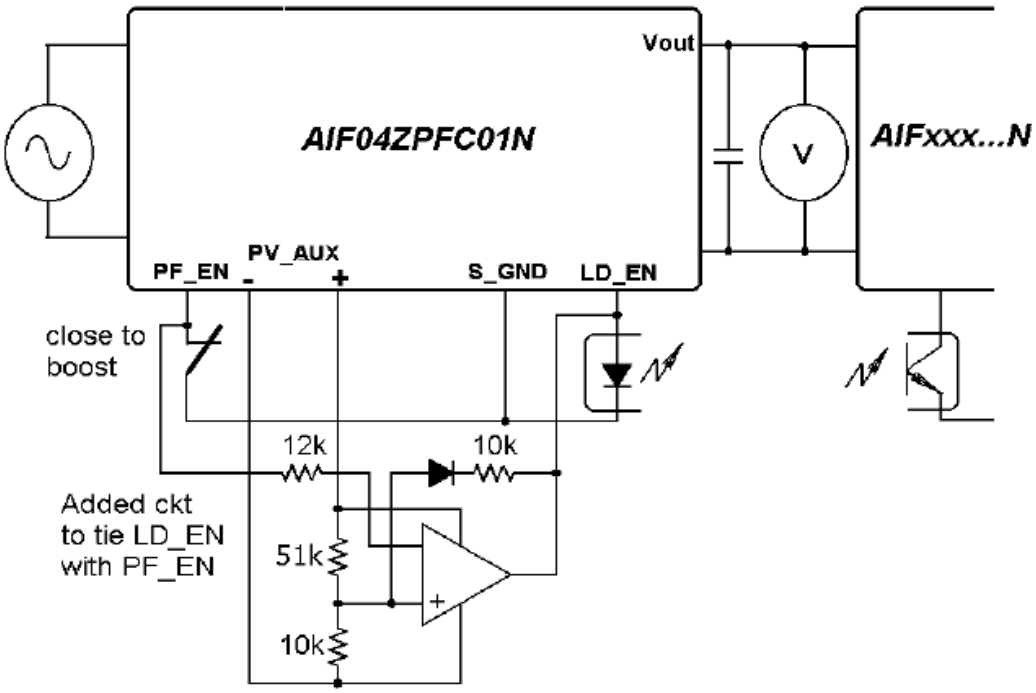
Interlock circuit between LD ENABLE and PF ENABLE

For the application needs the LD_EN goes low when the PF_EN is disable, please use the following interlock circuitry.

LD_EN goes low when PF_EN is set low (AIF04ZPFC-01).



LD_EN goes low when PF_EN is set high (AIF04ZPFC-01N).

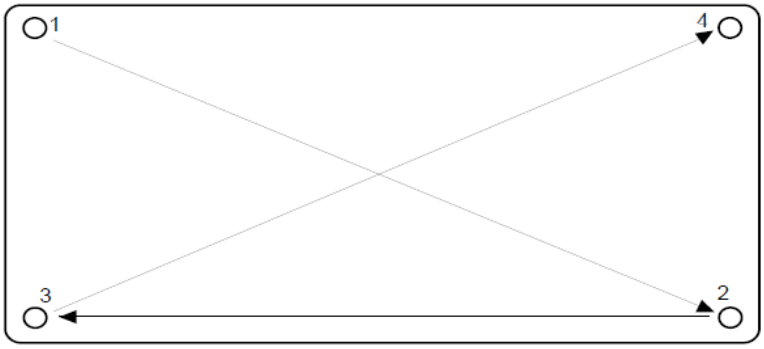


APPLICATION NOTES

Mounting Recommendations

Recommended torque setting and sequence for PFC M3 Mounting Screws.

Screw Size	Torque
M3	4-6kg-cm (3.5-5.2lb-in)



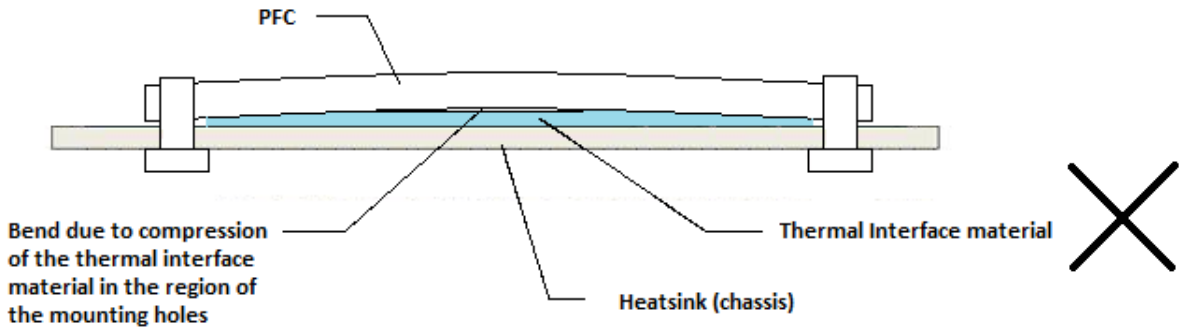
Heatsink Torquing Sequence

Recommended Flatness Spec for PFC Heatsink:

To provide optimal thermal contact between heatsink and module, it is recommended that the mating surface of the heatsink should have a surface flatness of no greater than 0.1mm.

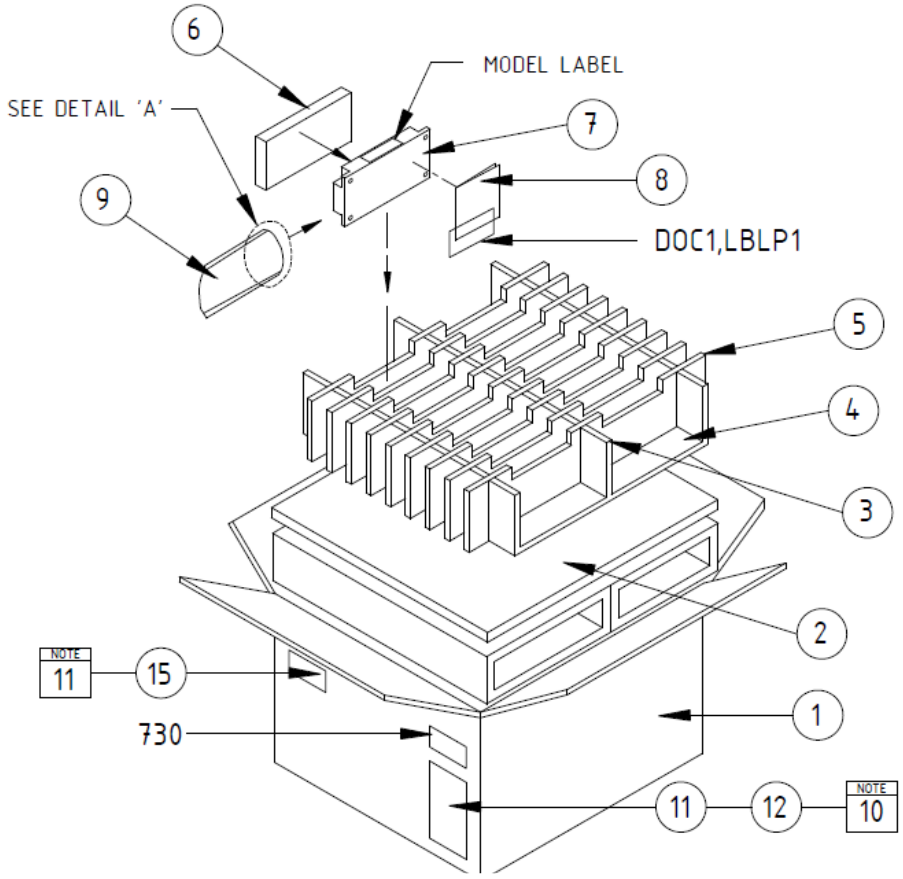
Recommended PFC Thermal Interface Material:

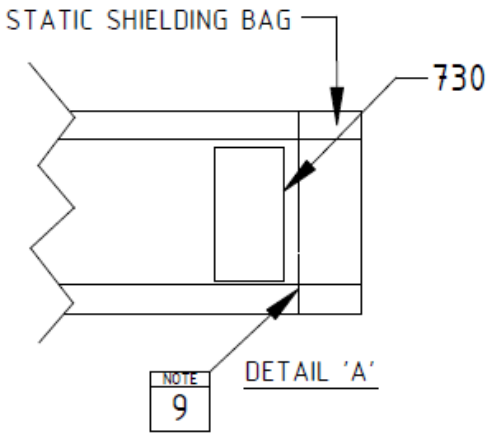
The use of a thermal pad or a thin layer of thermal grease is recommended. If a thermal pad is used, its thickness should be 0.5mm or less, to avoid bending the PFC baseplate due to compression of the interface material in the region of the mounting holes (see below illustration):

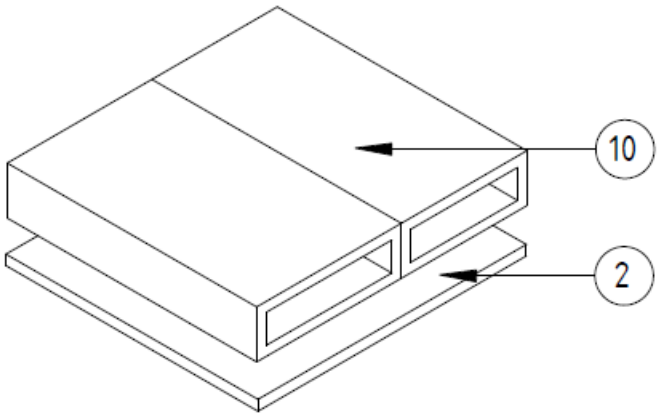


APPLICATION NOTES

Packaging Information







APPLICATION NOTES

Note:

1. Parts to be oriented as shown.
2. Each shipping carton contain 2 layers.
3. Each layer contain 16 units.
4. Carton O. D. Dimension 406mm(L) x 335mm(W) * 266mm(H)
5. For pallet packing please refer to 659-000272-0xxxx.
6. 32 units/ shipping carton.

   9 shipping carton/pallet layer

   3 pallet layers/ pallet

7. ref. weight approx.20g.

8. Gross weigt approx. 20LBS.

9. The opening OS static shielding bag must be heat sealed after a module with PE foam sheet and instruction sheet have been put inside the bag.

10. Print barcode information of LBLP11.(Refer to LBLD12)

Put LBLP11 - barcode label on the lower right hand side corner of the side shown. (I.E. the smallest side of carton BOX)

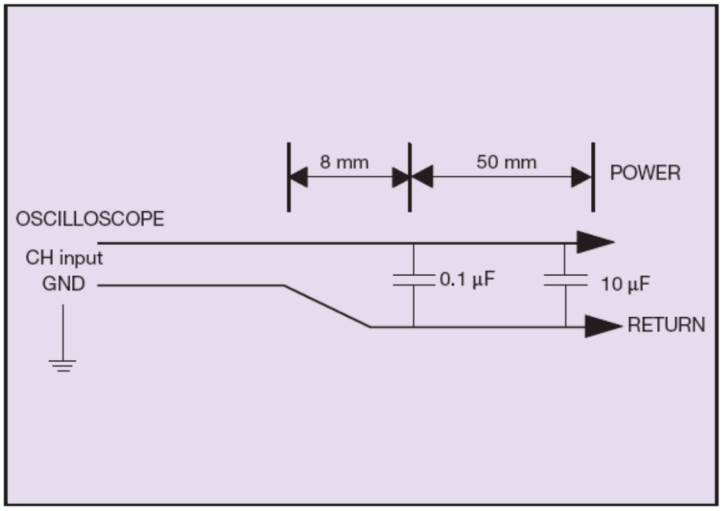
11. LBLP15 is to be place on the upper left corner of the smallest surface of the box and is applicable only for units to be shipped to Avnet. Please refer to LBLD16 for printing format details.

Ref.	DESIG	Remarks
PACK	①	Under package BOM
PACK	②	Under package BOM
PACK	③	Under package BOM
PACK	④	Under package BOM
PACK	⑤	Under package BOM
PACK	⑥	Under package BOM
----	⑦	AMPSS 80
----	⑧	INSTRUCTION SHEET REF. LOCATION ONLY, SEE BOM FOR AVAILABILITY
PACK	⑨	Under package BOM
PACK	⑩	Under package BOM
LBLP	⑪	Under package BOM
LBLD	⑫	Under package BOM
730	⑬	Under TLA
Doc1,LBLP1	⑭	Under TLA
LBLP	⑮	
LBLP	⑯	Under package BOM

APPLICATION NOTES

Output Ripple and Noise Measurement

The setup outlined in the diagram below has been used for output voltage ripple and noise measurements on the AIF04ZPFC series module. When measuring output ripple and noise, a scope jack in parallel with a 0.1uF ceramic chip capacitor, and a 10uF aluminum electrolytic capacitor should be used. Oscilloscope should be set to 20MHz bandwidth for this measurement.



Record of Revision and Changes

Issue	Date	Description	Originators
1.0	02.16.2022	First Issue	K. Ma
1.1	10.24.2022	Update LD Enable related Performance Curves	K. Ma
1.2	08.29.2023	Add warning for LD ENABLE	K. Ma

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Advanced Energy (AE) has devoted more than three decades to perfecting power for its global customers. AE designs and manufactures highly engineered, precision power conversion, measurement and control solutions for mission-critical applications and processes.

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AIF04PFC - Rev.08.29.23_#1.2

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