SY21199C

High Efficiency 1MHz, 600mA Step-Up Regulator

General Description

The SY21199C high efficiency step-up regulator is targeted at general applications and can deliver 600mA current over a wide input voltage range from 3V to 25V. It integrates an N-channel MOSFET with low 150mΩ $R_{DS(ON)}$ to minimize conduction loss.

The 1MHz switching frequency and internal compensation reduce external inductor and capacitor sizes.

The SY21199C is available in a compact SOT23-6 package.

Features

- 3V to 25V Bias Input Range, 25$V_{OUT,MAX}$
- Up to 600mA Output Current
- Low $R_{DS(ON)}$ for Internal N-Channel MOSFET: 150mΩ
- 1MHz Switching Frequency
- Minimum On-Time: 100ns Typical
- Minimum Off-Time: 100ns Typical
- Internal Soft-Start Limits Inrush Current
- ±2% 0.6V Reference
- RoHS-Compliant and Halogen-Free
- Compact SOT23-6 Package

Applications

- WLED Drivers
- Networking Cards Powered From PCI Or PCI-Express Slots

Typical Application

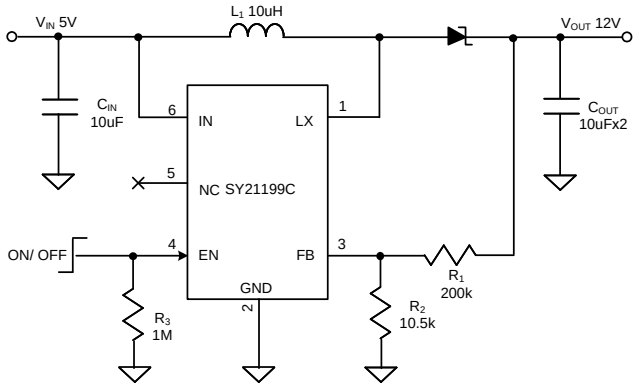


Figure 1. Typical Application Circuit

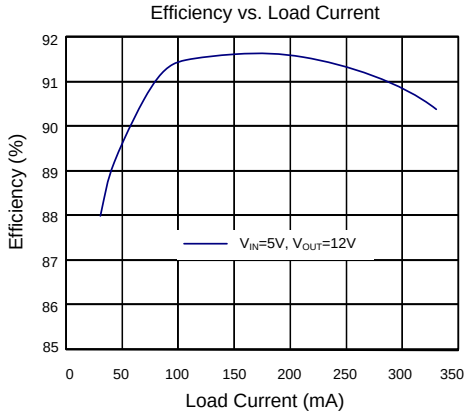


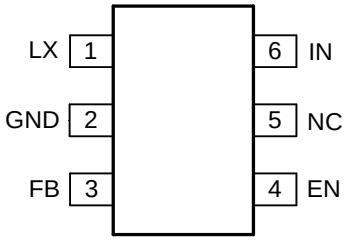
Figure 2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package type	Top Mark
SY21199CABC	SOT23-6 RoHS-Compliant and Halogen-Free	**JU*xyz***

x = year code, y = week code, z = lot number code

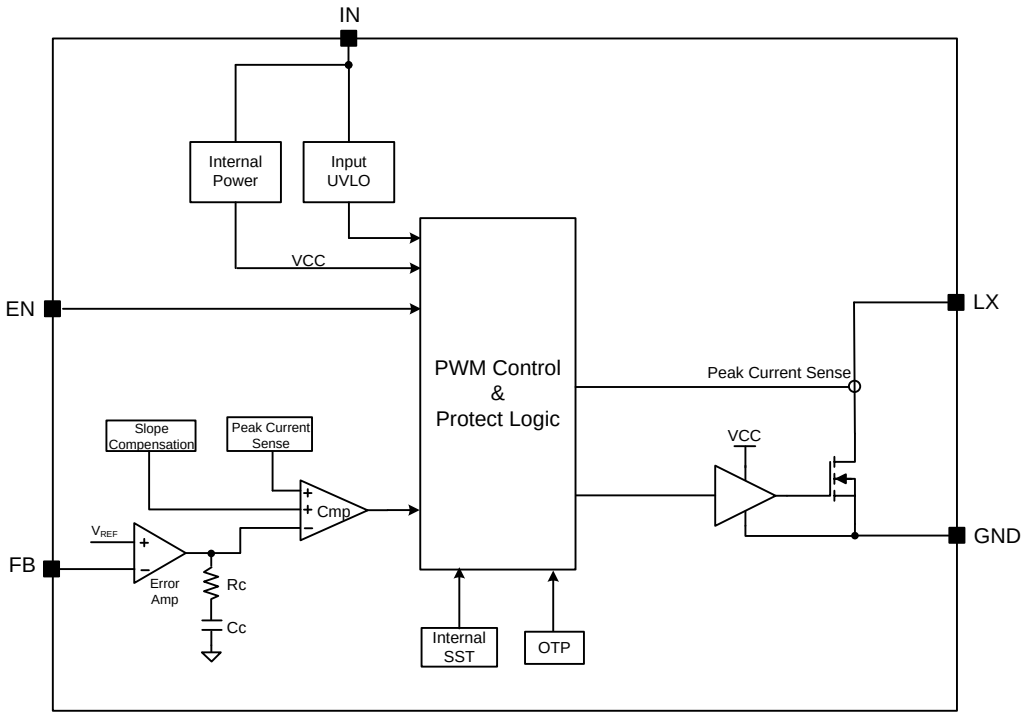
Pinout (top view)



Pin Description

Pin Number	Pin Name	Pin Description
1	LX	Inductor node. Connect an inductor between the IN and LX pins.
2	GND	Ground pin
3	FB	Feedback pin. Connect a resistor R1 between V_{OUT} and FB, and a resistor R2 between FB and GND to program the output voltage: V_{OUT} = 0.6V × (R1/R2+1).
4	EN	Enable pin. Pull low to disable the device, pull high to enable. Do not leave this pin floating.
5	NC	No connection.
6	IN	Input pin. Decouple this pin to the GND pin with a 1μF ceramic capacitor.

Block Diagram



Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
LX, IN, EN	-0.3	26	V
FB	-0.3	3.6	
LX Voltage, 50ns Duration	-3	30	
LX Voltage, 500ns Duration	-1	28	
Lead Temperature (Soldering, 10 sec.)		260	°C
Junction Temperature, Operating	-40	125	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	161	°C/W
θ_{JC} Junction-to-case Thermal Resistance	130	
P_D Power Dissipation T_A=25°C	0.6	W

Recommended Operating Conditions

Parameter (Note3)	Min	Max	Unit
IN	3	25	V
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 100mA, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		3		25	V
Quiescent Current	I_Q	V_{FB} = 0.66V		100		μA
Shutdown Current	I_{SHDN}	EN = 0		1	5	μA
Low Side Main FET R_{ON}	$R_{DS(ON)}$			150		mΩ
Main FET Current Limit	I_{LIM1}		600			mA
Switching Frequency	f_{SW}		0.8	1	1.2	MHz
Feedback Reference Voltage	V_{REF}		0.588	0.6	0.612	V
IN UVLO Rising Threshold	$V_{IN,UVLO}$				2.3	V
UVLO Hysteresis	$U_{VLO,HYS}$			0.1		V
Thermal Shutdown Temperature	T_{SD}			150		°C
EN Rising Threshold	V_{ENH}		2			V
EN Falling Threshold	V_{ENL}				0.4	V
EN Pin Input Current	I_{EN}		0		100	nA

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2” x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

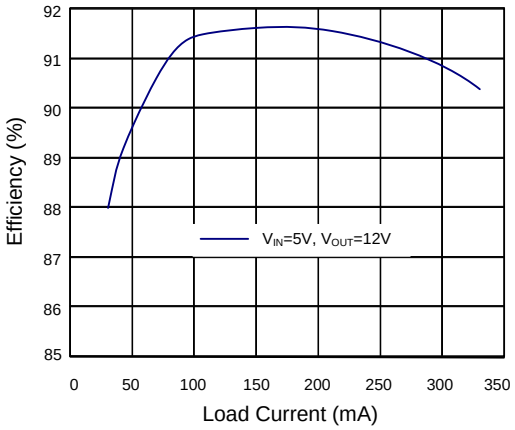
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: The IC could start up at 2.7V.

Typical Performance Characteristics

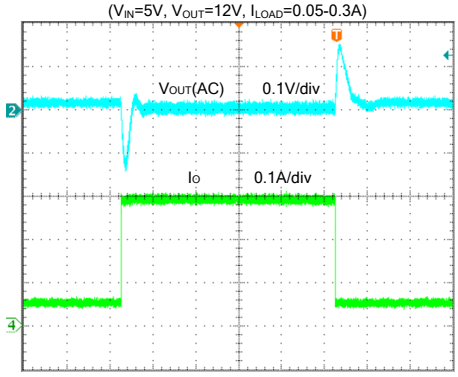
(T_A= 25℃, V_{IN}=5V, V_{OUT} = 12V, L = 10μH, C_{OUT}= 20μF, unless otherwise specified.)

Efficiency vs. Load Current



Load Transient

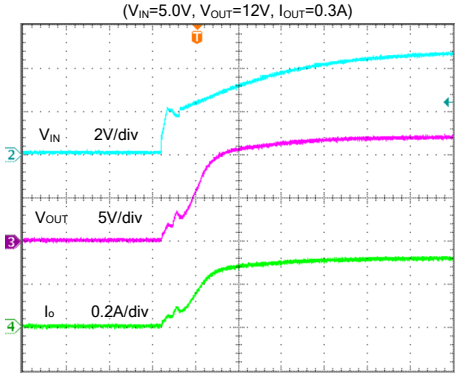
(V_{IN}=5V, V_{OUT}=12V, I_{LOAD}=0.05-0.3A)



Time (100μs/div)

Startup from V_{IN}

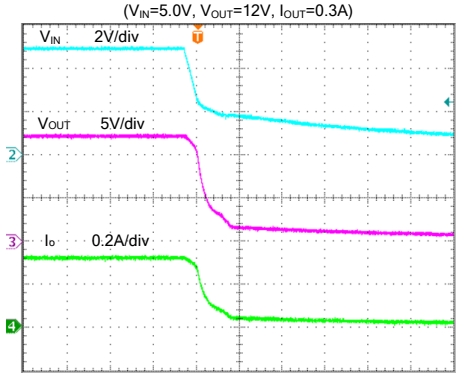
(V_{IN}=5.0V, V_{OUT}=12V, I_{OUT}=0.3A)



Time (1ms/div)

Shutdown from V_{IN}

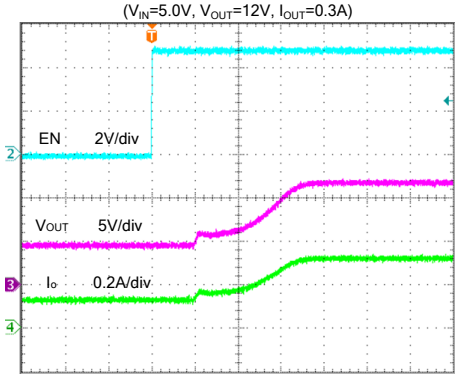
(V_{IN}=5.0V, V_{OUT}=12V, I_{OUT}=0.3A)



Time (2ms/div)

Startup from Enable

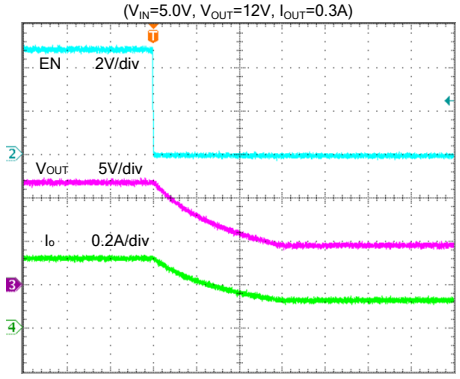
(V_{IN}=5.0V, V_{OUT}=12V, I_{OUT}=0.3A)



Time (200μs/div)

Shutdown from Enable

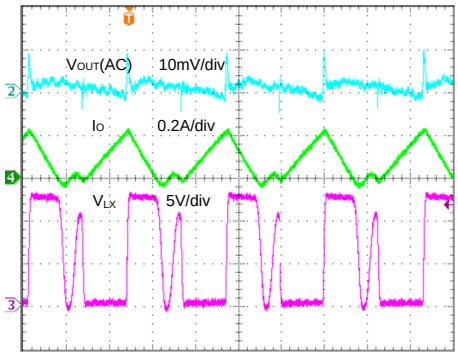
(V_{IN}=5.0V, V_{OUT}=12V, I_{OUT}=0.3A)



Time (100μs/div)

Output Ripple

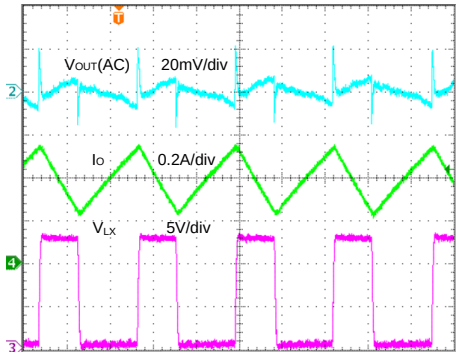
(V_{IN}=5.0V, V_{OUT}=12V, I_{OUT}=20mA)



Time (400ns/div)

Output Ripple

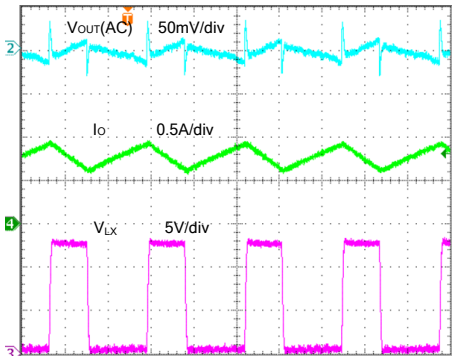
(V_{IN}=5.0V, V_{OUT}=12V, I_{OUT}=150mA)



Time (400ns/div)

Output Ripple

(V_{IN}=5.0V, V_{OUT}=12V, I_{OUT}=300mA)



Time (400ns/div)

Detailed Description

The SY21199C high efficiency step-up regulator is targeted at general applications and can deliver 600mA current over a wide input voltage range from 3V to 25V. It integrates an N-channel MOSFET with low 150mΩ $R_{DS(ON)}$ to minimize conduction loss.

The 1MHz switching frequency and internal compensation reduce external inductor and capacitor sizes.

The SY21199C is available in a compact SOT23-6 package.

Enable Operation

Driving the EN pin high (>2V) enables normal operation. Driving the EN pin low (<0.4V) will shut down the device. During shutdown mode, the SY21199C shutdown current drops to less than 5μA.

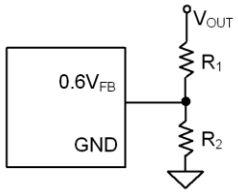
Application Information

The following paragraphs describe the selection process for the feedback resistors (R1 and R2), input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L, and diode D.

Feedback Resistor-Divider R1 and R2

Choose R1 and R2 to program the proper output voltage. Choose large resistance values between 10kΩ and 1MΩ for both R1 and R2 to minimize power consumption under light loads. If a value of 200kΩ is chosen for R1, then R2 can be calculated as:

$$R2 = \frac{0.6\text{V}}{V_{OUT}\text{-}0.6\text{V}} R1$$



Input Capacitor C_{IN}:

For the best performance, select a typical X7R or better grade ceramic capacitor. The component should be placed as close as possible to the module, while also minimizing the loop area formed by C_{IN} and the IN/GND pins. When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply.

In situations where the input rail is supplied through long wires, it is recommended to add some bulk capacitance using electrolytic, tantalum or polymer type capacitors to reduce the overshoot and ringing caused by the added parasitic inductance.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2\sqrt{3} \times L\, f_{SW} \times V_{OUT}}$$

Output Capacitor C_{OUT}:

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting the component. For the best performance, use an X7R or better grade ceramic capacitor with a 25V rating, and capacitance greater than 10μF.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed:

The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, both should be considered.

$$V_{RIPPLE,ESR1} = I_{LREAK} \times ESR$$

$$V_{RIPPLE,ESR2} = I_{LVALLEY} \times ESR$$

$$V_{RIPPLE,CAP} = \frac{I_{OUT} \times (1 - D)}{C_{OUT} \times f_{SW}}$$

The capacitive ripple might be higher because the effective capacitance for ceramic capacitors decreases with the voltage across the terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Inductor L

Consider the following when choosing this inductor:

- Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \times \frac{V_{OUT} - V_{IN}}{f_{sw} \times I_{OUT,MAX} \times 0.4}$$

  where f_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

  The SY21199C has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

- The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > \frac{V_{OUT}}{V_{IN}} \times I_{OUT,MAX} + \frac{V_{IN}(V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}}$$

- The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Choose an inductor with DCR greater than 50mΩ to achieve a good overall efficiency.

The maximum current that the converter can provide to the load depends on the output voltage / input voltage ratio.

Use the following formulas to evaluate an approximate max current that the converter can deliver when driving the load.

Estimate the maximum output current:

$$I_{MAXOUT} = (IL_{MIN} - \frac{\Delta IL}{2}) \times \frac{\eta \times V_{IN(MIN)}}{V_{OUT}}$$

Where: $V_{IN(MIN)}$ is the minimum voltage at the boost input in the application, IL_{MIN} is the minimum device current datasheet limit (0.6A for SY21199C), ΔIL is the current ripple and η is the efficiency, which can be substituted with a value of 0.8 for simplicity.

For example, when $V_{IN(MIN)}$ = 5V and V_{OUT} = 12V and a value of 40% is used for the ripple current, the calculated I_{MAXOUT} is shown below:

$$I_{MAXOUT}(\text{mA}) = (600 - \frac{600 \times 0.4}{2}) \times \frac{0.8 \times 5}{12}$$
$$= 160$$

Rectifier Diode

For high efficiency, choose a Schottky diode with low forward voltage drop and fast reverse recovery. The average diode current is equal to the output current: I_{AVG} = I_{OUT}.

The diode reverse voltage is equal to the output voltage. The reverse breakdown voltage of the Schottky diode should be greater than the output voltage.

Applications with Large Bulk Capacitance

In applications with large capacitance present on the output, a very high inrush current could flow through the inductor during power-on. In order to limit the current flowing into the device and prevent damage, a Zener diode connected from the power input to the output or an RC delay circuit added on the EN pin are recommended, as shown in Figure 3.

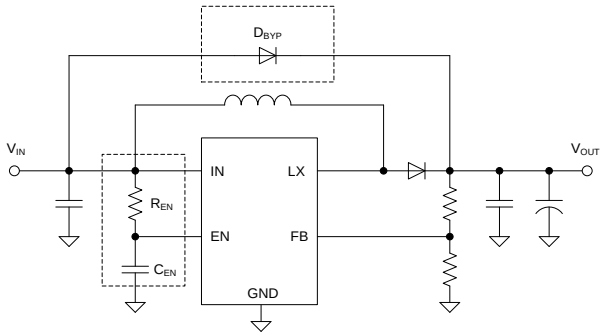


Figure 3. Inrush Current Limiting

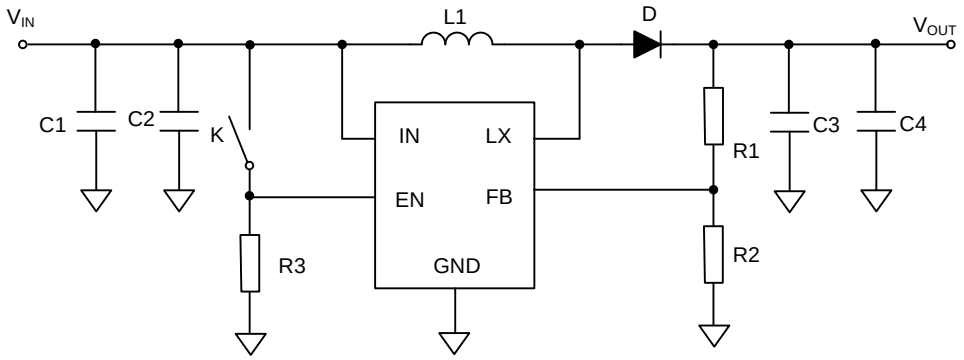
Thermal Protection

The SY21199C includes over temperature protection circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. When the junction temperature cools down by approximately 15°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the thermal protection threshold.

Over Current Protection

The SY21199C provides a cycle-by-cycle overcurrent protection and turns off the main power MOSFET once the inductor current reaches the overcurrent limit threshold. During the overcurrent protection, the output voltage drops as a function of the load. If the output voltage drops below the input voltage, the current will directly flow through L and rectifier diode. In this case the current is only limited by the DC resistance in the path during the event. As soon as the overload condition is removed, the converter resumes operation.

Application Schematic



Design Specifications

Input Voltage (V)	Output Voltage(V)	Input Current (A)
5	12	0.8

BOM List

Reference Designator	Description	Part Number	Manufacturer
U1	1MHz Boost (SOT23-6)	SY21199CABC	
L1	10μH/2.5A	VLC6045-100M	TDK
D	3A/40V, Schottky		
C1	47μF/50V (electronic capacitor)		
C2, C3, C4	10μF/25V,1206, X7R	GRM31CR71E106KA12L	MuRata
R1	200kΩ, 1%, 0603		
R2	10.5kΩ, 1%, 0603		
R3	1M Ω, 1%, 0603		

Recommend Components for Typical Applications

V_{OUT}(V)	R1(kΩ)	R2(kΩ)	L(μH)	C3
12	200	10.5	10	2×10μF/25V/X7R,1206
24	200	5.1	15	2×10μF/50V/X7R,1206

Layout Design

To achieve optimal design, follow these PCB layout considerations:

- Place C_{IN}, L, R1, and R2 close to the IC
- To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if board space allows.
- C_{IN} must be close to pins IN and GND. Minimize the loop area formed by C_{IN} and GND.
- To reduce the switching noise, minimize the PCB copper area connected to the LX pin.
- In order to reduce crosstalk, R1, R2, and the trace connected to the FB pin must not be adjacent to the LX net on the PCB layout.
- If the system chip interfacing with the EN pin has a high impedance state during shutdown mode, and the IN pin is connected directly to a power source such as a Li-ion battery, add a 1MΩ pulldown resistor between the EN and GND pins to prevent noise from falsely triggering the regulator during shutdown mode.

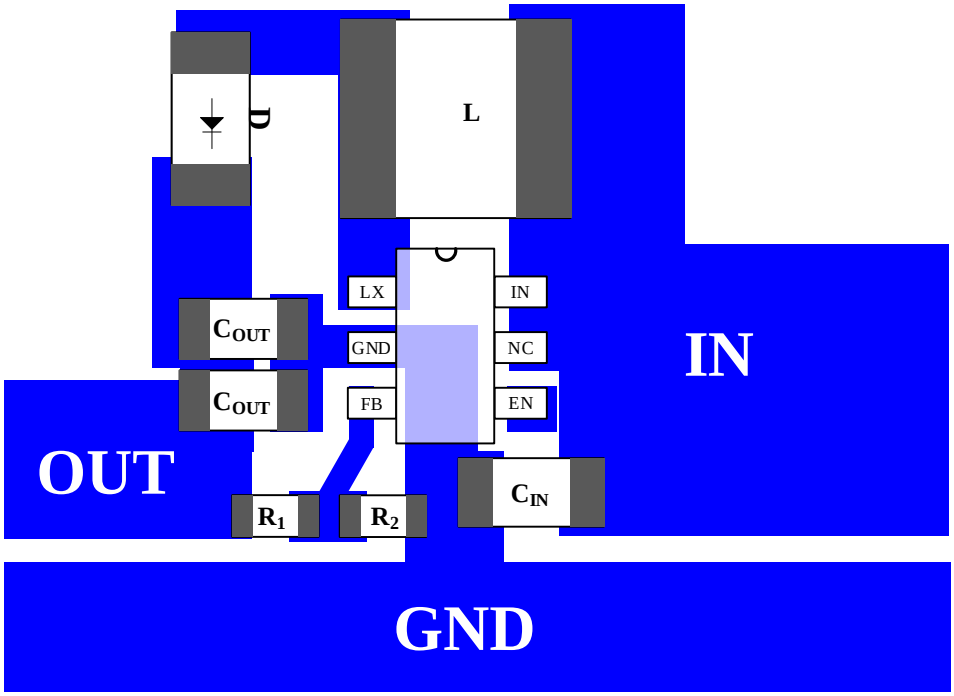
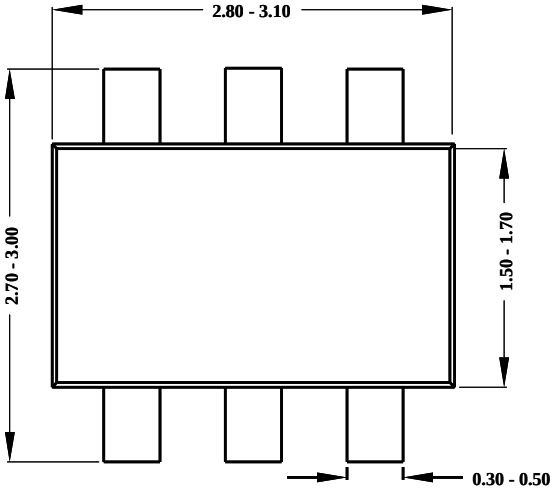
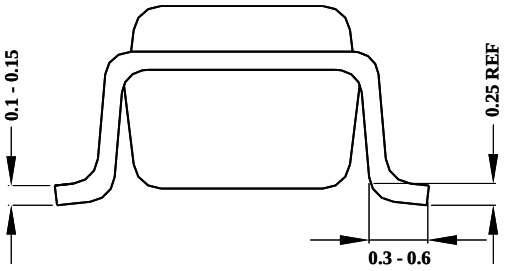


Figure 4. Suggested PCB Layout

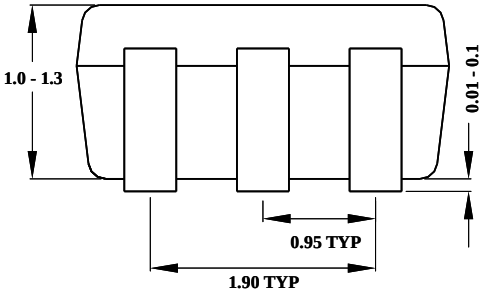
SOT23-6 Package Outline and PCB Layout



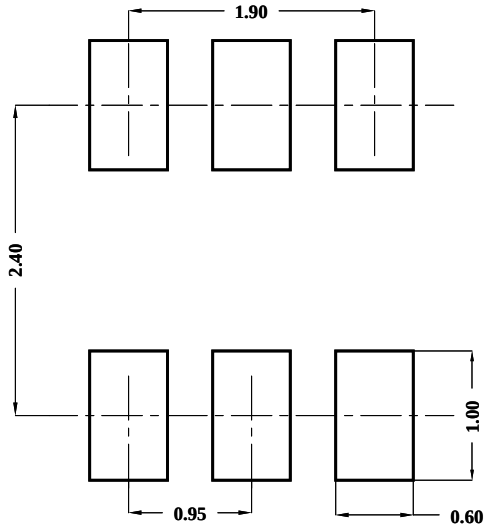
Top view



Side view



Side view

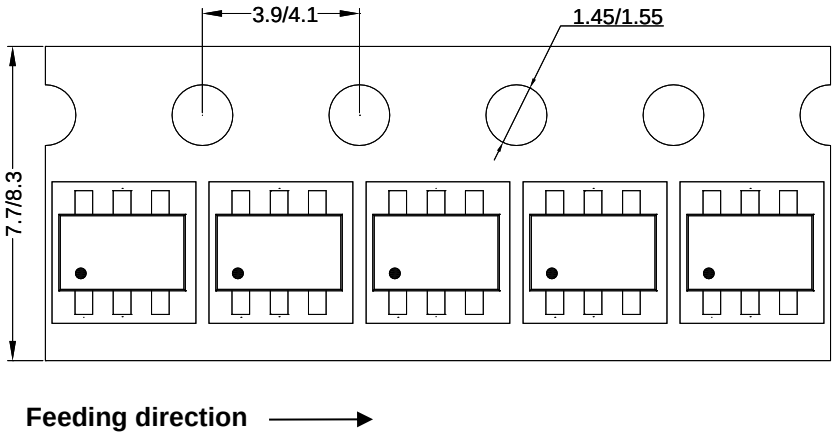


Recommended pad layout
(reference only)

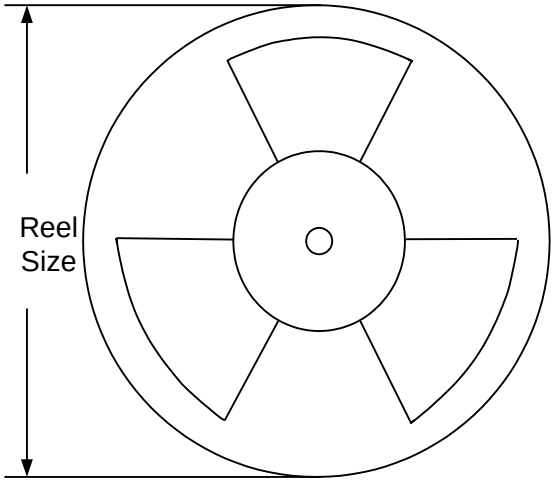
Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

Taping and Reel Specification

SOT23-6 taping orientation



Carrier tape and reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-6	**8**	**4**	**7"**	**280**	**160**	**3000**

Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
June.09, 2023	Revision 1.0	Language improvements for clarity
Nov.29, 2022	Revision 0.9B	Add Dynamic LX Voltage in Absolute Maximum Ratings
Sep. 27, 2017	Revision 0.9A	Modify the formula in "Output Inductor L" (page 6) From $I_{SAT,\,MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT,\,MAX} + \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L}$ To $I_{SAT,\,MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT,\,MAX} + \frac{V_{IN}(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L \times V_{OUT}}$
July 30, 2012	Revision 0.9	Initial Release

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