SY21153A

High-Efficiency, Fast-Response, 40V Input, 3A Synchronous Step-Down Regulator

General Description

The SY21153A high-efficiency synchronous step-down DC/DC converter operates using a peak-current-mode control architecture and can deliver 3A load current over a wide input voltage range from 4.5V to 40V. It integrates a main switch and a synchronous switch with low $R_{DS(ON)}$ to minimize conduction loss.

The switching frequency is adjustable from 500kHz to 2.5MHz using an external resistor. The SY21153A also features very low 19µA quiescent current to achieve high efficiency under light load, and internal soft-start to limit inrush current during power-on.

The SY21153A is available in a compact TSOT23-8 package.

Features

- 4.5 to 40V Input Voltage Range
- 3A Output Current Capability
- Low $R_{DS(ON)}$ for Internal Switches: 110mΩ Top, 70mΩ Bottom
- Adjustable Switching Frequency Range: 500kHz to 2.5MHz
- 1.5% 0.6V Reference Voltage
- Low 19µA Quiescent Current
- Internal Compensation
- Internal 1ms Soft-Start Limits Inrush Current
- Cycle-by-Cycle Peak-Current Limit
- Hiccup Mode Short-Circuit Protection
- Thermal Shutdown and Auto-Recovery
- RoHS-Compliant and Halogen-Free
- Compact Package: TSOT23-8

Applications

- LCD-TV
- Set-Top Box
- Notebook
- Storage
- High-Power AP Router
- Networking

Typical Applications

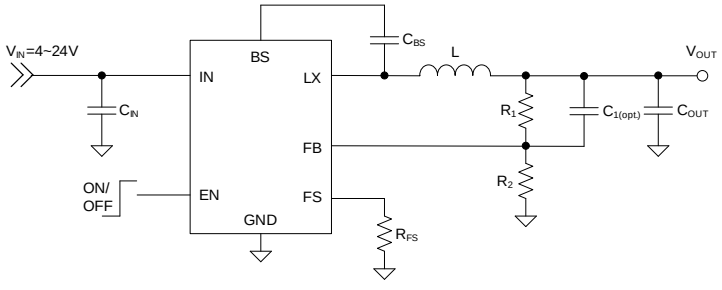


Figure 1. Schematic Diagram

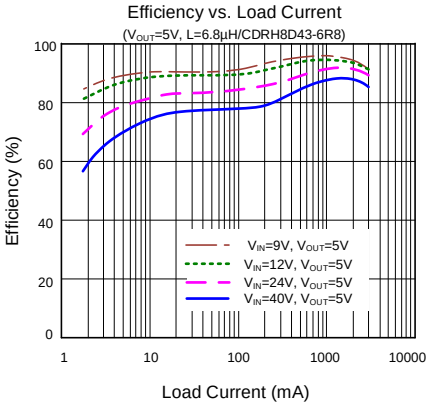


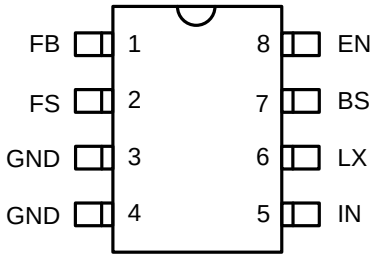
Figure 2. Efficiency vs. Load Current

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY21153AAIC	TSOT23-8 RoHS-Compliant and Halogen-Free	**bQ*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	FB	Output feedback pin. Connect this pin to the center point of the output resistor-divider (as shown in Figure 1) to program the output voltage: V_{OUT}=0.6 × (1+R1/R2)
2	FS	Frequency programming pin. Connect a resistor to ground to program a switching frequency between 500kHz to 2.5MHz. The switching frequency can be configured as: fsw(kHz) =10^5/R_{FS}(kΩ).
8	EN	Enable control. Pull high to turn on. Do not leave floating.
3, 4	GND	Ground pin.
5	IN	Input pin. Decouple this pin to GND pin with at least a 4.7μF ceramic capacitor.
6	LX	Inductor pin. Connect this pin to the switching node of the inductor.
7	BS	Bootstrap pin. Supply for the high-side gate driver. Connect a 0.1μF ceramic capacitor between the BS and the LX pin.

Block Diagram

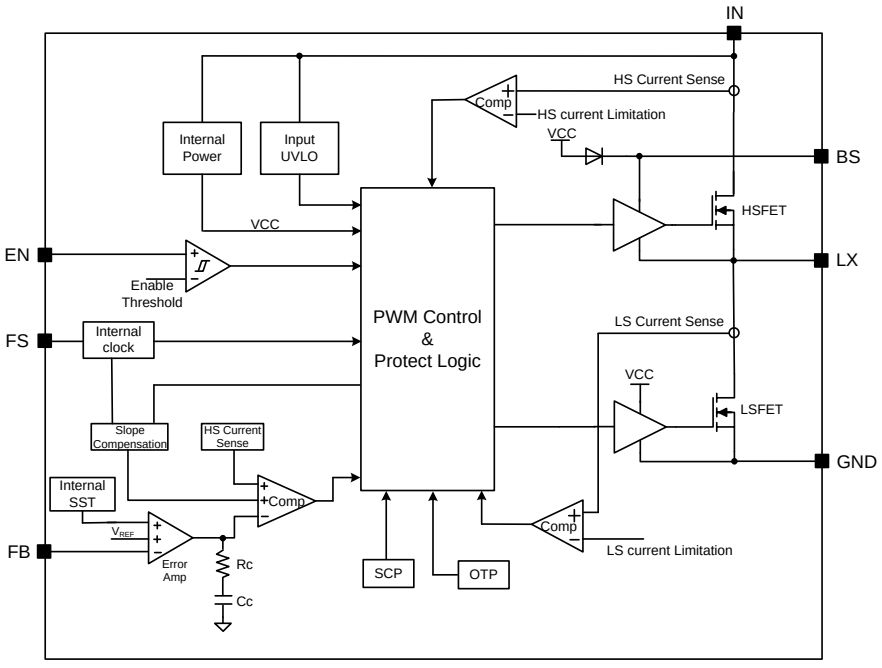


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	40	V
LX, FB, EN, FS to GND	-0.3	40	
BS-LX	-0.3	4	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	60.2	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	11.2	
P_D Power Dissipation T_A = 25°C	2	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	4.5	40	V
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{IN} = 12V, V_{OUT} = 5V, C_{OUT} = 47μF, T_A = 25°C, I_{OUT} = 1A unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Input Voltage Range	V_{IN}		4.5		40	V
	Quiescent Current	I_Q	I_{OUT} = 0, V_{FB} = V_{REF} × 105%			19	μA
	Shutdown Current	I_{SHDN}	EN = 0		1	2	μA
	Input UVLO Threshold	V_{UVLO}				4.35	V
	UVLO Hysteresis	V_{HYS}			0.3		V
Output	Feedback Reference Voltage	V_{REF}		0.591	0.6	0.609	V
	FB Input Current	I_{FB}	V_{FB} = V_{CC}	-50		50	nA
	Soft-Start Time	t_{SS}			1		ms
MOSFET	Top FET R_{ON}	$R_{DS(ON)1}$			110		mΩ
	Bottom FET R_{ON}	$R_{DS(ON)2}$			70		mΩ
	Top FET Current Limit	$I_{LIM,TOP}$		4		6.8	A
Enable (EN)	EN Low Threshold	V_{ENL}		0.5			V
	EN High Threshold	V_{ENH}				1.5	V
Frequency	Oscillator Frequency Program Range	F_{OSC}	R_{FS} = 40k–200k	0.5		2.5	MHz
	Oscillator Frequency Accuracy		R_{FS} = 200k	425	500	575	kHz
	Min On-Time				80		ns
	Min Off-Time				120		ns
OTP	Thermal Shutdown Temperature	T_{SD}			150		°C
	Thermal Shutdown Hysteresis	$T_{SD,HYS}$			15		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective 4-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Pin 2 of TSOT-23-8 packages is the case position for θ_{JC} measurement.

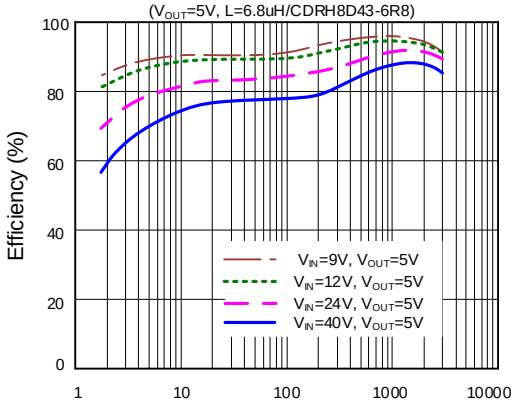
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

(T_A = 25℃, V_{IN} = 12V, V_{OUT} = 5V, L = 6.8μH, C_{OUT} = 44μF, unless otherwise noted)

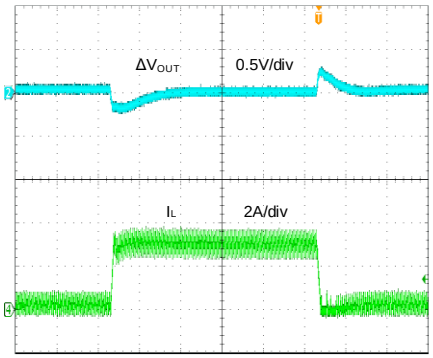
Efficiency vs. Load Current

(V_{OUT}=5V, L=6.8uH/CDRH8D43-6R8)



Load Transient

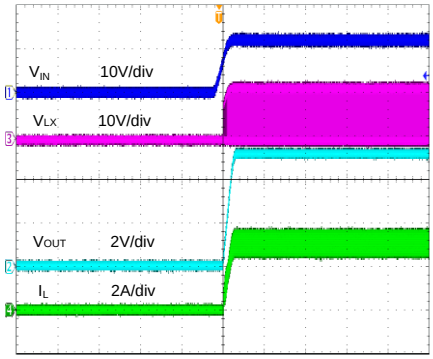
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0.3A ~ 3A)



Time (40μs/div)

Startup from V_{IN}

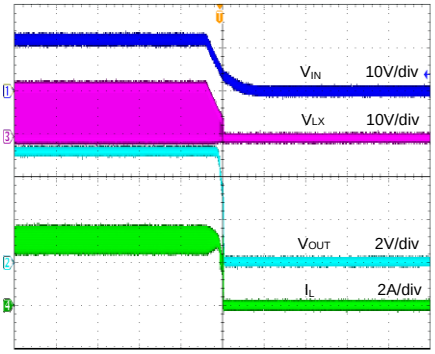
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A)



Time (4ms/div)

Shutdown from V_{IN}

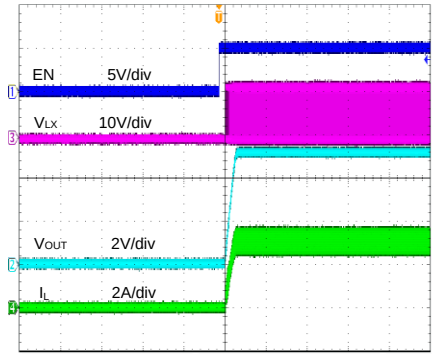
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A)



Time (20ms/div)

Startup from Enable

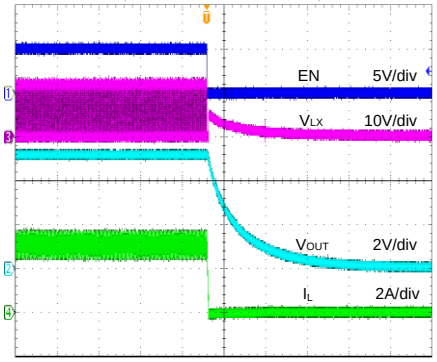
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A)



Time (4ms/div)

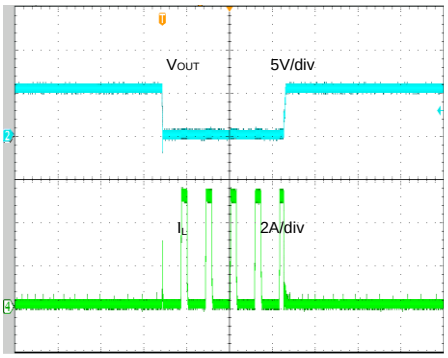
Shutdown from Enable

(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A)



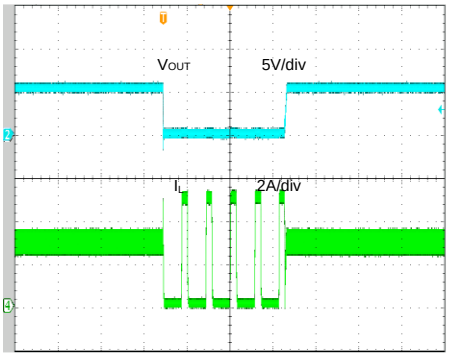
Time (100μs/div)

Short Circuit Protection
(V_{IN}=12V, V_{OUT}=5V, 0A to Short)



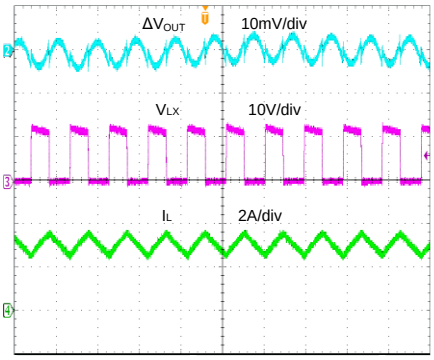
Time (10ms/div)

Short Circuit Protection
(V_{IN}=12V, V_{OUT}=5V, 3A to Short)



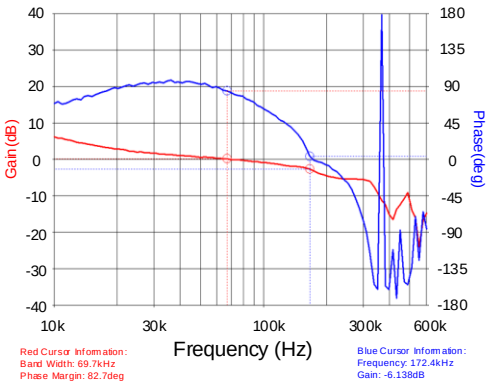
Time (10ms/div)

Output Ripple
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}= 3A)

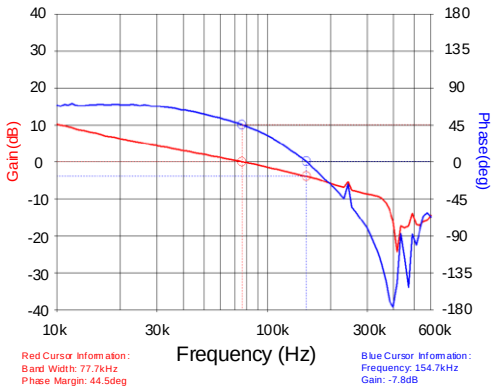


Time (2μs/div)

Bode Plot
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=1A)



Bode Plot
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=1A)



Detailed Description

General Features

Peak Current and Clock Control Architecture

The SY21153A high-efficiency synchronous step-down DC/DC converter can deliver up to 3A load current over a wide input voltage range from 4.5V to 40V. It integrates a main switch and a synchronous switch with low $R_{DS(ON)}$ to minimize conduction loss.

The SY21153A uses a clock-control and peak-current-mode control architecture. When the top FET's current-sense signal reaches internal V_{COMP}, the top FET turns off and the bottom FET turns on for a fixed period of time (constant t_{OFF}).

Input Undervoltage Lockout (UVLO)

To prevent operation before all internal circuitry is ready, and to ensure that the power and synchronous rectifier switches work reliably, the Instant-PWM™ architecture incorporates input undervoltage lockout protection. The SY21153A remains in a low-current state and all switching actions are inhibited until V_{IN} exceeds the UVLO (rising) threshold. At that time, if EN is enabled, the device will start up by initiating a soft-start ramp. If V_{IN} falls below V_{UVLO} by more than the input UVLO hysteresis, switching actions will again be suppressed.

If required, increasing the default input UVLO threshold is possible by connecting a resistor-divider to the EN pin as shown in Figure 5.

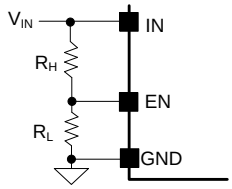


Figure 5. UVLO Adjustment

Enable Control

The EN input is a high-voltage capable input with logic-compatible threshold. When EN is driven above 1.4V, normal device operation is enabled. When driven to less than 1V, the device enters shutdown mode.

It is not recommended to connect EN and IN directly. Use a resistor with a value between 10kΩ and 1MΩ if EN is pulled high to V_{IN}.

Startup and Shutdown

The SY21153A incorporates an internal soft-start circuit to smoothly ramp the output to the desired voltage whenever the device is enabled. Internally, the soft-start circuit clamps the output at a low voltage and then allows the output to rise to the desired voltage over approximately 1ms, which avoids high current flow and transients during startup. The startup and shutdown sequences are shown in Figure 6.

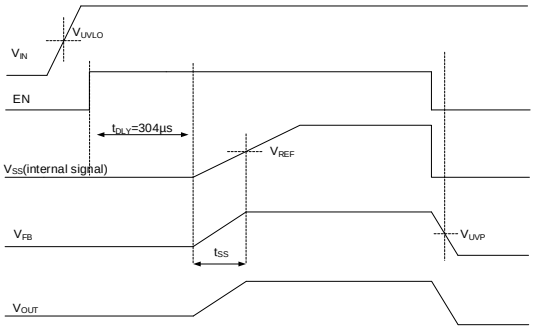


Figure 6. Startup and Shutdown Sequence

Output Discharge

The SY21153A discharges the output voltage when the converter shuts down from V_{IN} or EN, or due to thermal shutdown, so that output voltage can be discharged in a minimal amount of time, even if the output load current is zero. The discharge FET in parallel with the low-side synchronous rectifier will turn on after the low-side synchronous rectifier turns off when shutdown logic is triggered. The output discharge current is typically 55mA when LX voltage is 5V. Note that the discharge FET is not active outside these shutdown conditions.

External Bootstrap Capacitor Connection

The SY21153A integrates a floating power supply for the gate driver that operates the high-side power switch. Proper operation requires a 0.1μF low-ESR ceramic capacitor to be connected between the BS and LX pins, which provides the gate-driver supply voltage for the high-side N-channel MOSFET power switch, as shown in Figure 7.

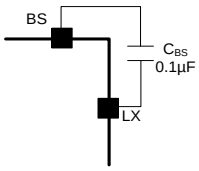


Figure 7. Bootstrap Capacitor Connection

Switching Frequency Selection

Connect a resistor from the FS pin to GND to adjust the switching frequency. The switching frequency is adjustable from 500kHz to 2.5MHz as calculated by the following equation:

$$f_{SW}(kHz) = \frac{10^5}{R_{FS}(k\Omega)}$$

Fault-Protection Modes

Output Current Limit

The SY21153A incorporates a cycle-by-cycle peak current limit (top-FET current limit). The high-side power-switch current is monitored during t_{ON} time. If the monitored current exceeds the top-FET current limit, the MOSFET is turned off, the low-side synchronous rectifier is turned on, and t_{ON} is inhibited.

Output Undervoltage Protection (UVP)

If V_{OUT} is less than approximately 33% of the target output voltage for approximately 15µs when the output short circuits or the load current is much higher than the maximum current capacity, the output undervoltage protection (UVP) will be triggered, and the device will enter into hiccup protection mode. The hiccup on-time is 1.5ms, and the hiccup off-time is 4.5ms. If the output fault conditions are removed, the device will return to normal operation in the subsequent hiccup on-time, as shown in Figure 8.

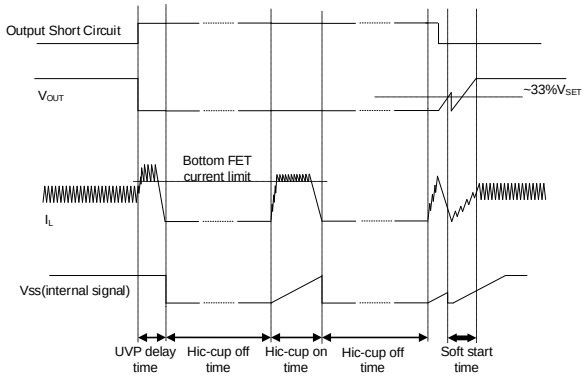


Figure 8. Output Undervoltage Protection

To avoid output overshoot, the internal soft-start circuit voltage V_{SS} is pulled low temporarily when V_{FB} exceeds the UVP threshold if the output fault conditions are removed during hiccup on-time, and then the V_{SS} rises smoothly to ramp the output to the desired voltage during a new soft-start cycle.

Overtemperature Protection (OTP)

The device includes overtemperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C, as shown in Figure 9. Once the junction temperature cools by approximately 15°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the OTP threshold.

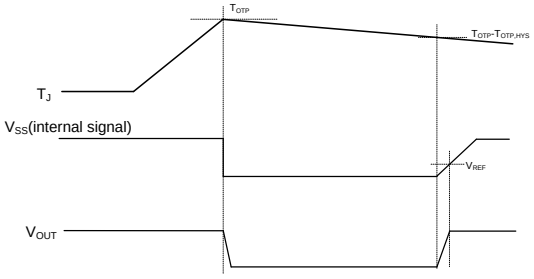


Figure 9. Overtemperature Protection

Application Information

The selection process for the input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L, and feedback resistors (R1 and R2) is described in the following sections.

Feedback Resistor-Divider R1 and R2

Choose R1 and R2 to program the proper output voltage. A value between 10kΩ and 1MΩ is recommended for both resistors to minimize power consumption under light loads. For example, if V_{SET} is 5V and R1= 100kΩ, then R2 can be calculated using the following equation:

$$R_2 = \frac{0.6V}{V_{SET} - 0.6V} \times R_1$$

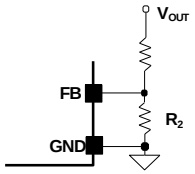


Figure 10. Feedback Resistor Selection

With a calculated value of 13.7kΩ for R2, a standard 1% 13.7kΩ resistor is selected.

Input Capacitor Selection

Input filter capacitors reduce the ripple voltage on the input, filter the switched current drawn from the input supply, and reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating higher than the system requirements. X5R series ceramic capacitors are most often selected due to their small size, low cost, surge-current capability, and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum, or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1-D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 10µF X5R capacitor is sufficient in most applications.

Inductor Selection

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage.

Instant-PWM™ operates well over a wide range of inductor values. This flexibility allows for optimization to find the best trade-off of efficiency, cost, and size for a particular application. Selecting a low inductor value will help reduce size and cost, and enhance transient response, but will increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low-value inductors may help reduce DC losses and increase efficiency. Higher inductor values tend to have higher DCR and will slow transient response.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting a ripple current (ΔI_L) approximately 20–50% of the desired full output load current. Start calculating the approximate inductor value by selecting the input and output voltages, the operating frequency (f_{SW}), the maximum output current ($I_{OUT,MAX}$), and estimated ΔI_L as a percentage of that current:

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current (ΔI_L) and required peak-current inductor current $I_{L,PEAK}$.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L_1}$$

$$I_{L,PEAK} = I_{OUT,MAX} \times \frac{\Delta I_L}{2}$$

Select an inductor with a saturation current and thermal rating in excess of $I_{L,PEAK}$.

For maximum efficiency, select an inductor with a low DCR that meets the inductance, size, and cost targets. Low-loss ferrite materials should be considered.

Inductor Design Example

Consider a typical design for a device providing $5V_{OUT}$ at 3A from $24V_{IN}$, operating at 500kHz and using target inductor ripple current (ΔI_L) of 40% or 1.2A. First determine the approximate inductance value:

$$L_1 = \frac{5V \times (24V - 5V)}{24V \times 500kHz \times 1.2A} = 6.597\mu H$$

Next, select the nearest standard inductance value (in this case 6.8µH) and calculate the resulting inductor ripple current (ΔI_L):

$$\Delta I_L = \frac{5V \times (24V - 5V)}{24V \times 500kHz \times 6.8\mu H} = 1.164A$$

$$I_{L,PEAK} = 3A + \frac{1.164A}{2} = 3.582A$$

The resulting 1.164A ripple current is approximately 38.8% (1.164A/3A), which is within the 20–40% target.

$$I_{L,PEAK,RVS} = \frac{1.164A}{2} = 0.582A$$

Finally, select an available inductor with a saturation current higher than the resulting $I_{L,PEAK}$ of 3.582A.

Output Capacitor Selection

Instant-PWM™ provides excellent performance with a wide variety of output capacitor types. Ceramic and POS types are most often selected due to their small size and low cost. Total capacitance is determined by the transient response and output voltage ripple requirements of the system.

Output Ripple

Output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitors ESR (ESR ripple), as well as the stored charge (capacitive ripple). When considering total ripple, both should be considered.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Consider a typical application with ΔI_L = 0.291A using two 22µF ceramic capacitors, each with an ESR of approximately 4mΩ for a parallel total of 44µF and 2mΩ ESR.

$$V_{RIPPLE,ESR} = 1.164A \times 2m\Omega = 2.328mV$$

$$V_{RIPPLE,CAP} = \frac{1.164A}{8 \times 44\mu F \times 500kHz} = 6.614mV$$

Total ripple = 8.942mV. The actual capacitive ripple may be higher than the calculated value because the capacitance decreases with the voltage on the capacitor. Using a 150µF 40mΩ POS capacitor, the result is as follows:

$$V_{RIPPLE,ESR} = 1.164A \times 40m\Omega = 46.56mV$$

$$V_{RIPPLE,CAP} = \frac{1.164A}{8 \times 150\mu F \times 500kHz} = 1.94mV$$

Total ripple = 48.50mV.

Output Transient Undershoot/Overshoot

If very fast load transients must be supported, consider the effect of the output capacitor on the output transient undershoot and overshoot. Instant-PWM™ responds quickly to changing load conditions, but some considerations are still required, especially when using small ceramic capacitors. These capacitors have low capacitance, which results in insufficient stored energy for load transients. Output-transient undershoot and overshoot have two causes: voltage changes caused by the ESR of the output capacitor, and voltage changes caused by the output capacitance and inductor current slew rate.

ESR undershoot or overshoot may be calculated as $V_{ESR} = \Delta I_{OUT} \times ESR$. Using the ceramic capacitor example above and a fast load transient of ± 1.5A, V_{ESR} = ±1.5A × 2mΩ = ±3mV. The POS capacitor result with the same load transient is V_{ESR} = ±1.5A × 40mΩ = ±60mV.

Capacitive undershoot (load increasing) is a function of the output capacitance, load step, inductor value, input-output voltage difference, and maximum duty factor. During a fast load transient, the maximum duty factor of instant-PWM™ is a function of t_{ON} and the minimum t_{OFF}, as the control scheme is designed to rapidly ramp the inductor current by grouping together many t_{ON} pulses in this case. The maximum duty factor D_{MAX} may be calculated as:

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF,MIN}}$$

Given this, the capacitive undershoot may be calculated as:

$$V_{UNDERSHOOT,CAP} = -\frac{L_1 \times \Delta I_{OUT}^2}{2 \times C_{OUT} \times (V_{IN,MIN} \times D_{MAX} - V_{OUT})}$$

Consider a 1.5A load increase using the ceramic capacitors above when V_{IN} = 24V. At V_{OUT} = 5V, the result is t_{ON} = 417ns, $t_{OFF,MIN}$ = 120ns, D_{MAX} = 417 / (417+ 120) = 0.777, and:

$$V_{UNDERSHOOT,CAP} = -\frac{6.8\mu H \times (3A)^2}{2 \times 44\mu F \times (24V \times 0.777 - 5V)} = -50.96mV$$

Using the POS capacitor, the result changes to :

$$V_{UNDERSHOOT,CAP} = -\frac{6.8\mu H \times (3A)^2}{2 \times 150\mu F \times (24V \times 0.510 - 5V)} = -14.95mV$$

Capacitive overshoot (load decreasing) is a function of the output capacitance, inductor value, and output voltage.

$$V_{OVERSHOOT,CAP} = \frac{L_1 \times \Delta I_{OUT}^2}{2 \times C_{OUT} \times V_{OUT}}$$

Consider a 1.5A load decrease using the ceramic capacitors above. At V_{OUT} = 5V the result is:

$$V_{OVERSHOOT,CAP} = \frac{6.8\mu H \times (1.5A)^2}{2 \times 44\mu F \times 5V} = 34.77mV$$

Using the POS capacitor, the above result is:

$$V_{OVERSHOOT,CAP} = \frac{6.8\mu H \times (1.5A)^2}{2 \times 150\mu F \times 5V} = 10.2mV$$

Combine the ESR and capacitive undershoot and overshoot to calculate the total overshoot and undershoot for a given application.

Load-Transient Considerations

The SY21153A uses the instant-PWM architecture to achieve good stability and fast transient responses. In applications with high step-load current, adding an RC feed-forward compensation network R_{FF} and C_{FF} may further speed up the load-transient responses. R_{FF} = 1kΩ and C_{FF} = 100pF have been shown to perform well in most applications. Increasing C_{FF} will speed up the load-transient response if there is no stability issue.

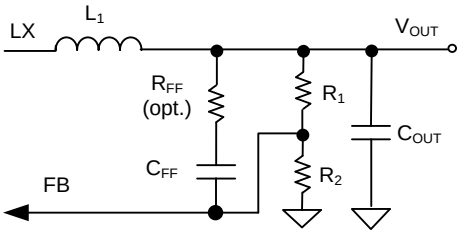


Figure 11. Feed-Forward Network

Note that when C_{OUT} > 500µF and minimum load current is low, using the feed-forward values R_{FF} = 1kΩ and C_{FF} = 2.2nF is recommended to provide sufficient ripple to the FB node for reliable operation.

Thermal Design Considerations

The maximum power dissipation depends on multiple factors: PCB layout, IC package thermal resistance, local airflow, and the junction temperature relative to ambient. The maximum power dissipation may be calculated as:

$$P_{D,MAX} = \frac{(T_{J,MAX} - T_A)}{\theta_{JA}}$$

Where $T_{J,MAX}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

To comply with the recommended operating conditions, the maximum junction temperature is 125℃. The junction-to-ambient thermal resistance θ_{JA} is layout-dependent. For the TSOT23-8 package, the thermal resistance θ_{JA} is 60.2℃/W when measured on a standard Silergy four-layer thermal test board. These standard thermal test layouts have a very large area with long 2oz. copper traces connected to each IC pin and very large, unbroken 1oz. internal power and ground planes.

Meeting the performance of the standard thermal test board in a typical evaluation board area requires wide copper traces well-connected to the IC's backside pads leading to exposed copper areas on the component side of the board as well as good thermal vias from the exposed pad connecting to a wide middle-layer ground plane and, perhaps, to an exposed copper area on the board's bottom side.

The maximum power dissipation at T_A = 25°C may be calculated using the following formula:

$$P_{D,MAX} = \frac{(125°C - 25°C)}{(60.2°C/W)} = 1.66W$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J,MAX}$ and thermal resistance θ_{JA}. Use the derating curve in figure below to calculate the effect of rising ambient temperature on the maximum power dissipation.

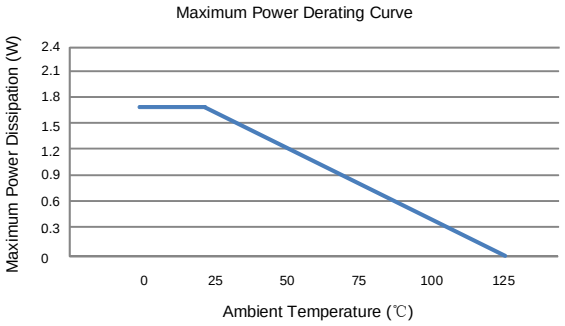
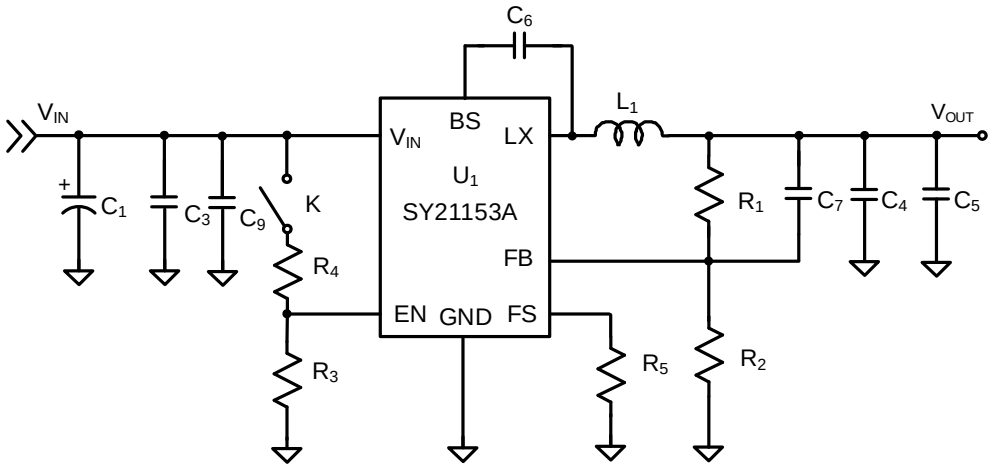


Figure 12. Maximum Power Dissipation

Application Schematic (V_{OUT} = 5V)



BOM List

Designator	Description	Part Number	Manufacturer
U1		SY21153AAIC	Silergy
L1	inductor 6.8uH /4.4A	CDRH8D43-6R8NC	Sumida
C1	47μF/50V Electrolytic Cap		
C3	10μF/50V/X5R, 1206	GRM31CR61H106KA12L	Murata
C4, C5	22μF/16V/X5R, 1206	GRM31CR61C226ME15L	Murata
C6, C9	0.1μF/50V/X7R, 0603	GRM188R71H104KA93D	Murata
C7	100pF/50V/C0G, 0603	C1608C0G1H101J	TDK
R1	100kΩ, 1%, 0603		
R2	13.7kΩ, 1%, 0603		
R3	1MΩ, 1%, 0603		
R4	10kΩ, 1%, 0603		
R5	200kΩ, 1%, 0603		
R6	null		

Recommended Components for Typical Applications

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C13 (pF)	L_1/Part Number
1.2	100	100	100	2.2μH/VLP6045-2R2M
1.8	100	50	100	3.3μH/VLP6045-3R3M
3.3	100	22.1	100	4.7μH/ CDRH8D43-4R7
5	100	13.7	100	6.8μH/CDRH8D43-6R8

Layout Design

To achieve optimal performance, follow these PCB layout considerations:

- Place C_{IN}, L, R1, and R2 close to the IC
- To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground copper pour is highly recommended if board space allows it.
- Minimize the loop area formed by C_{IN}, IN, LX, and the rectifier.
- Minimize the PCB copper area connected to the LX pin.
- R1, R2, and the trace connected to the FB pin must not be adjacent to the LX net on the PCB layout.
- If the system chip interfacing with the EN pin has a high impedance state during shutdown mode, and the IN pin is connected directly to a power source such as a Li-ion battery, add a 1MΩ pulldown resistor between the EN and GND pins to prevent noise from falsely triggering the regulator during shutdown mode.

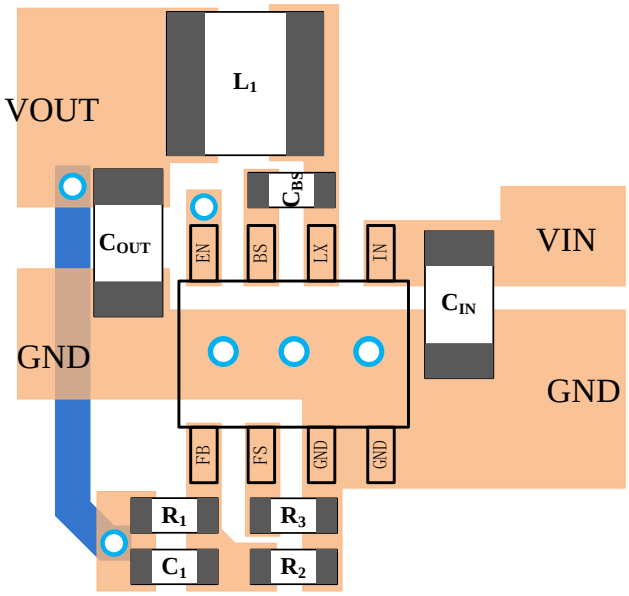
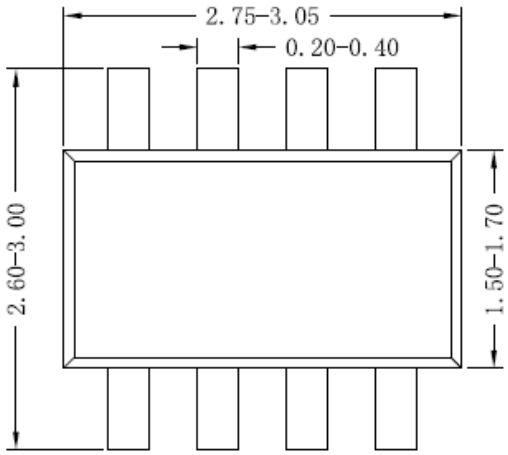
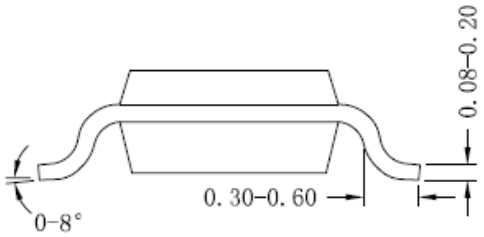


Figure 13. Suggested PCB Layout

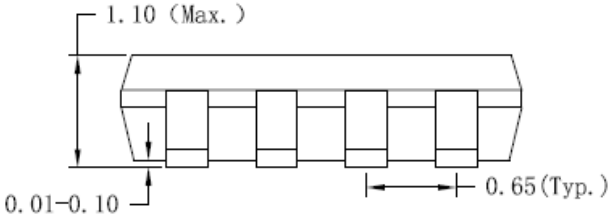
TSOT23-8 Package Outline Drawing



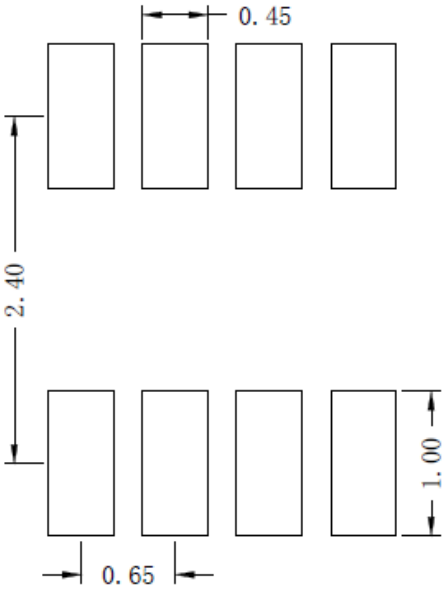
Top view



Side view A



Side view B

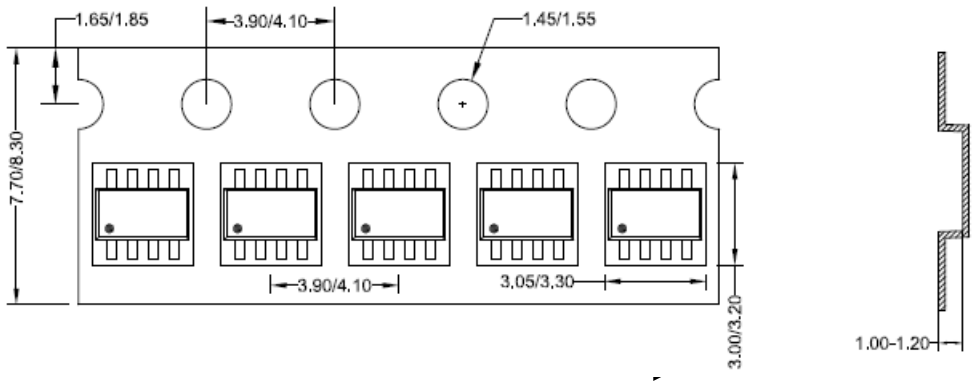


Recommended PCB layout
(Reference only)

Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

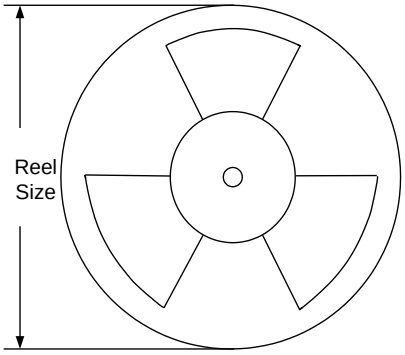
Taping and Reel Specification

TSOT23-8 taping orientation



Feeding direction ⟶

Carrier tape and reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
TSOT23-8	**8**	**4**	**7**	**400**	**160**	**3000**

Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Aug.30, 2023	Revision 1.0	Language improvements for clarity.
Mar.02, 2019	Revision 0.9B	1. Update the BS-LX Voltage in Absolute Maximum Ratings (page3) 2. Add “Junction Temperature Range" and ”Ambient Temperature Range" in Recommended Operating Conditions
Oct.12, 2017	Revision 0.9A	Fix the typo in the datasheet
July 10, 2017	Revision 0.9	Initial Release

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