

## General Description

SY205226DWC is a low-capacitance transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With a typical capacitance of 0.4pF, SY205226DWC is designed to protect against over-voltage and over-current transient events. It complies with IEC61000-4-2 (ESD) ( $\pm 30\text{kV}$  air,  $\pm 30\text{kV}$  contact discharge), IEC61000-4-5 (Surge) (6A, 8/20 $\mu\text{s}$ ).

Each SY205226DWC device can protect one data line. The SY205226DWC is available in a small DFN1.0x0.6-2 package.

## Features

- Protects One Data, Control, or Power Line
- Low Capacitance: 0.4pF (Typical)
- Low Leakage Current: 0.01 $\mu\text{A}$  @  $V_{\text{RWM}}$  (Typical)
- Low Clamping Voltage
- For Operating Voltage of 3.3V and Below
- Transient Protection for High-Speed Data Lines
  - IEC 61000-4-2 (ESD)  $\pm 30\text{kV}$  (Air)  $\pm 30\text{kV}$  (Contact)
  - IEC 61000-4-5 (Surge) 6A (8/20  $\mu\text{s}$ )
- Package Optimized for High-Speed Lines
- Ultra-Small Package: DFN1.0x0.6-2
- Each I/O pin can withstand over 1000 ESD strikes for  $\pm 8\text{kV}$  contact discharge.

## Applications

- Serial ATA
- PCI Express
- Desktops, Servers, and Notebooks
- MDDI Ports
- USB2.0, 3.0, and 3.1
- Display Ports
- HDMI 1.3, 1.4, 2.0, and 2.1
- Digital Visual Interfaces (DVI)

## Mechanical Characteristics

- Package: DFN1.0x0.6-2
- Marking: Device Code, Date Code
- Packaging: Tape and Reel

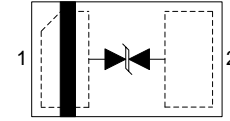
## Circuit Diagram



## Ordering Information

Part Number	Package Type	Top Mark
SY205226DWC	DFN1.0x0.6-2 RoHS Compliant and Halogen Free	fM

## Pinout (Top View)



## Marking Codes



**Note 1:** "f" is device code, fixed.

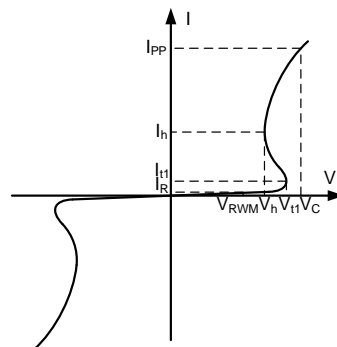
**Note 2:** "M" is date code.

Absolute Maximum Rating				
Parameter	Symbol	Min	Max	Unit
Maximum Peak Pulse Current (8/20μs)	$I_{PP}$		6	A
Maximum Peak Pulse Power (8/20μs)	$P_{PK}$		48	W
ESD per IEC 61000-4-2 (Air)	$V_{ESD}$	-30	30	kV
ESD per IEC 61000-4-2 (Contact)				
Operating Temperature	$T_{OPT}$	-40	+125	°C
Storage Temperature	$T_{STG}$	-55	+150	°C

Electrical Characteristics $T_A = 25^\circ\text{C}$						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal Reverse Working Voltage	$V_{RWM}$		-3.3		3.3	V
Reverse Leakage Current @ $V_{RWM}$	$I_R$	$V_{RWM} = 3.6\text{V}, T_A = 25^\circ\text{C}$		0.01	0.1	μA
Triggering Voltage @ $I_{t1}$	$V_{t1} (1)$	$I_{t1} = 1\mu\text{A}$	3.7			V
Holding Voltage @ $I_h$	$V_h$	$I_h = 100\text{mA}$	3.3		6.0	V
Clamping Voltage @ $I_{PP}$	$V_C (1)$	$I_{PP} = 6\text{A}, t_p = 8/20\mu\text{s}$		8.0		V
Clamping Voltage @ $I_{PP}$	$V_C (1)$	$I_{PP} = 16\text{A}, t_p = 10/100\text{ns}$		8.5		V
Dynamic Resistance	$R_{DYN(1,2)}$	$t_p = 10/100\text{ns}$		0.25		Ω
Parasitic Capacitance	$C_{ESD(1)}$	$V_R = 1.65\text{V}, f = 1\text{MHz}$		0.40	0.50	pF

**Note 1:** Guaranteed by design and not subject to production test.

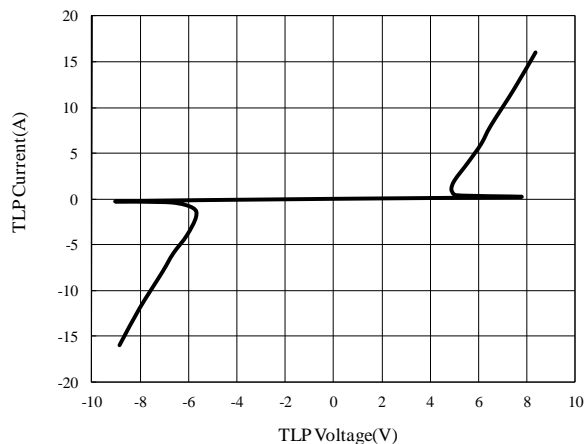
**Note 2:**  $R_{DYN}$  calculated based on  $I_{PP}=8\text{A}$  to  $I_{PP}=16\text{A}$ ,  $t_p = 10/100\text{ns}$ .



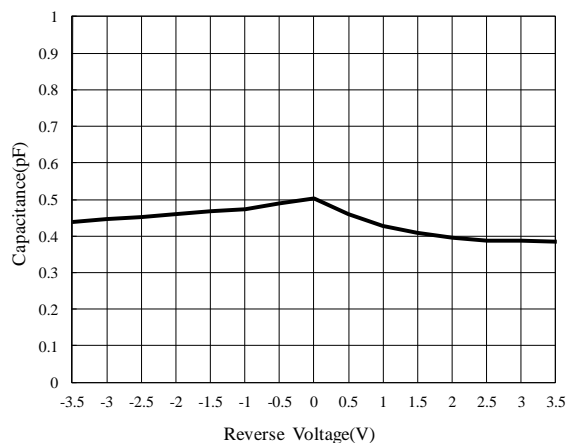
**Figure 1. Bi-directional TVS**

## Typical Characteristics

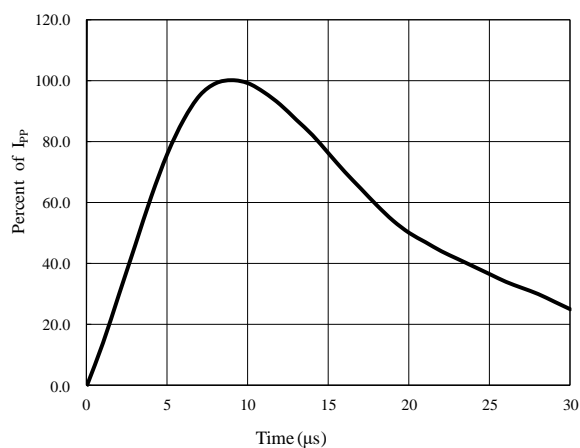
### TLP Measurement



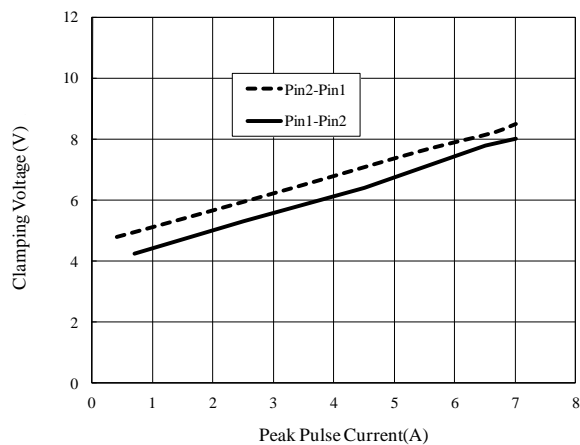
### Capacitance vs. Voltage



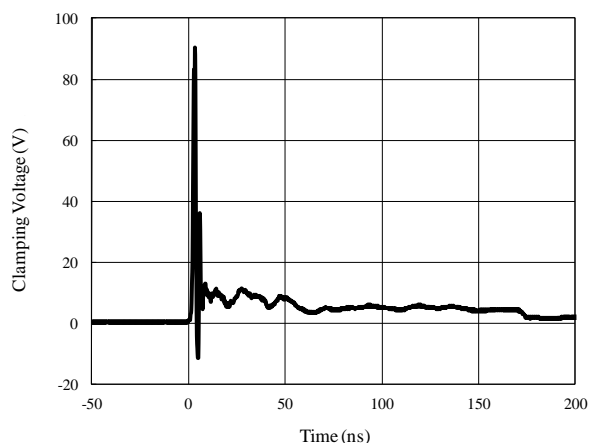
### Pulse Waveform



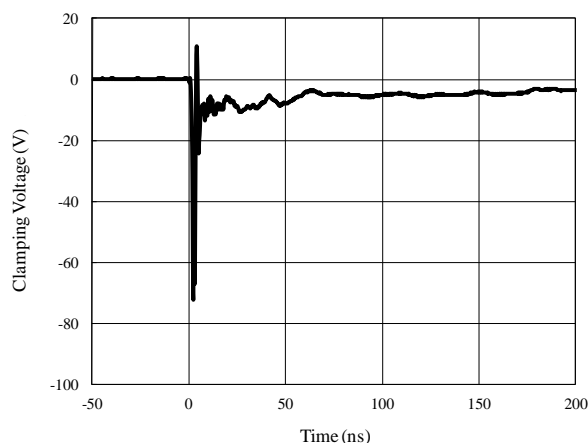
### Clamping Voltage vs. Peak Pulse Current



### ESD Clamping of I/O\_1 to I/O\_2 (+8kV Contact per IEC 61000-4-2)



### ESD Clamping of I/O\_1 to I/O\_2 (-8kV Contact per IEC 61000-4-2)



## Eye Diagram Measurement for HDMI2.1

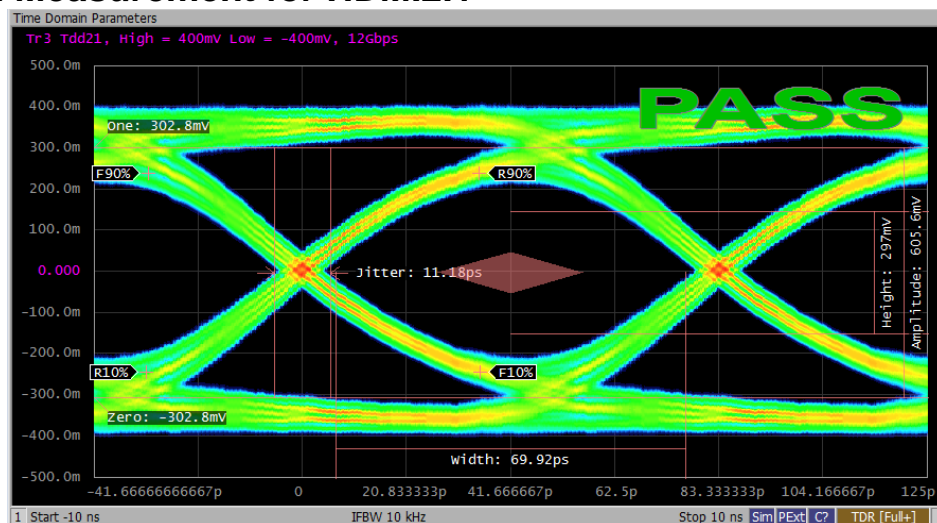


Figure 2. Data Rate 12Gb/s  
HDMI 2.1 Eye Diagram without SY205226DWC

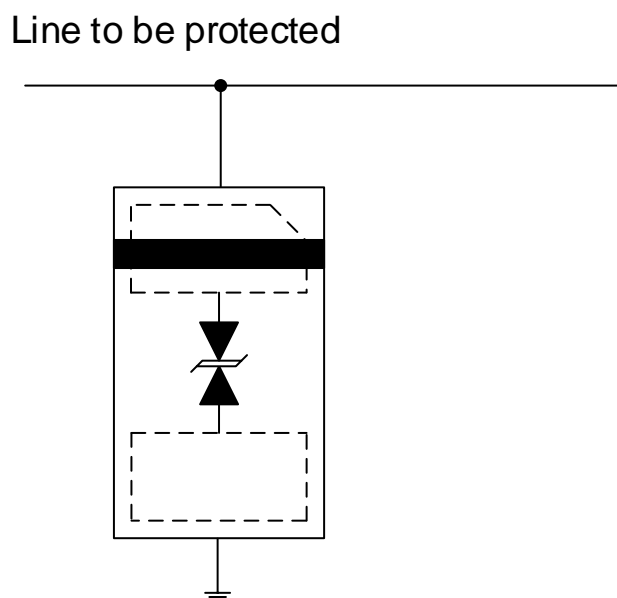


Figure 3. Data Rate 12Gb/s  
HDMI 2.1 Eye Diagram with SY205226DWC

## Application Information

SY205226DWC is designed to protect one bi-directional data line against over-voltage and over-current transient events by clamping it to an acceptable reference.

The SY205226DWC pin connections are shown in Figure 4. The protected line is connected to Pin1. Pin2 is connected to the GND, which should connect to a ground plane on the board. All path lengths connected to pins of SY205226DWC should be as short as possible to minimize the parasitic inductance.



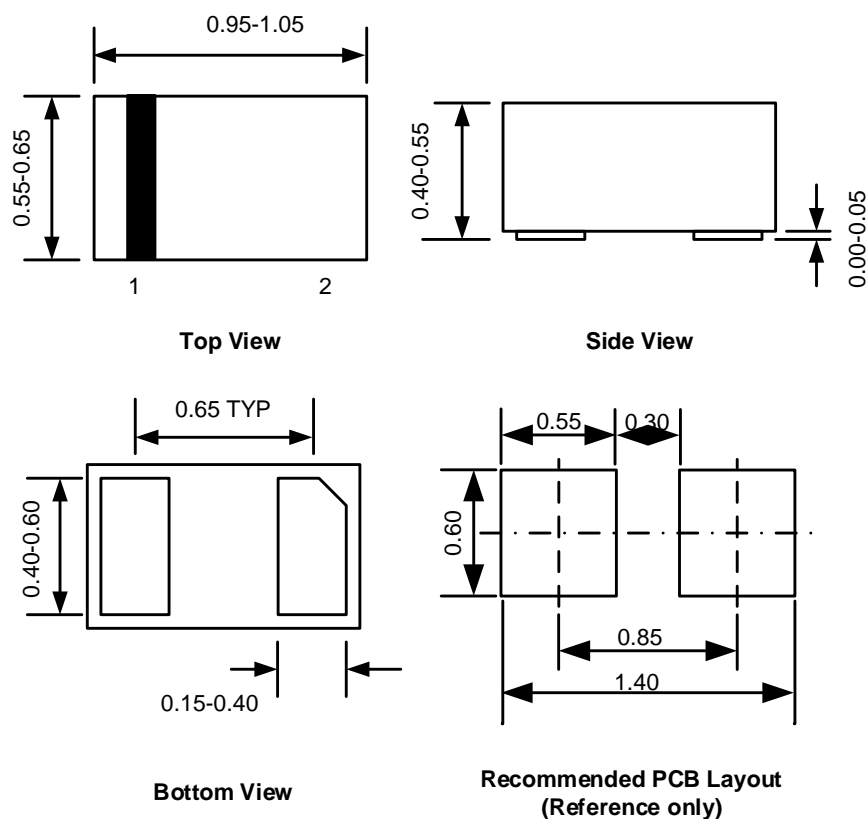
**Figure 4. ESD/Surge Protection Circuit**

## PCB Layout Guidelines

For optimum ESD protection and circuit performance, the following PCB layout guidelines are recommended:

- Place SY205226DWC as close to the connector port as possible.
- Use a large via to connect the SY205226DWC pin to the ground.
- Avoid running signals near board edges.
- The distance between the SY205226DWC ground pin and the GND reference path should be as short as possible.

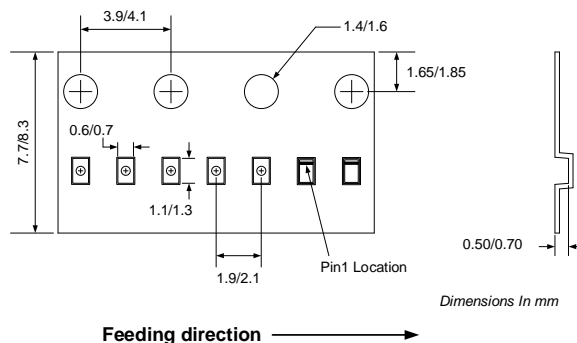
## DFN1.0x0.6-2 Package Outline



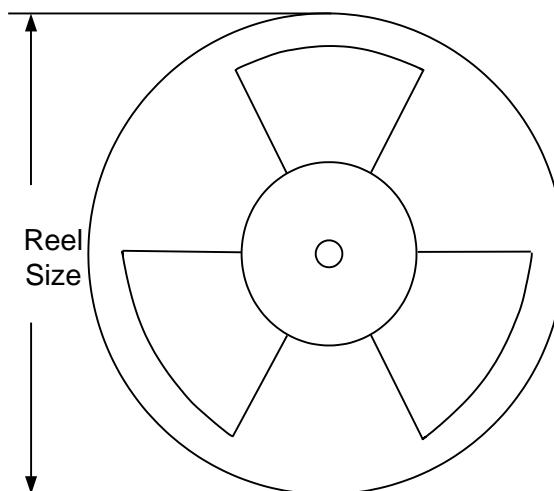
**Note:** All dimensions are in millimeters and exclude mold flash and metal burr.

## Tape and Reel Specification

### DFN1.0x0.6-2 Taping Orientation



### Carrier Tape & Reel Specification for Packages



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Qty per Reel(pcs)
DFN1.0x0.6-2	8	2	7"	10000



## Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
0.9	09/04/2020	Initial Release	
1.0	09/04/2021	Production Release	



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