

### General Description

The SY205216DWC is a low-capacitance transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With a typical capacitance of 12pF, the SY205216DWC is designed to protect against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD) ( $\pm 30\text{kV}$  air,  $\pm 30\text{kV}$  contact discharge), IEC 61000-4-5 (surge) (4A, 8/20 $\mu\text{s}$ ).

Each SY205216DWC device can protect one data line.

The SY205216DWC is available in a small DFN1.0 $\times$ 0.6-2 package.

### Features

- Transient Protection for High-speed Data Lines
  - IEC 61000-4-2 (ESD)  $\pm 30\text{kV}$  (Air)  $\pm 30\text{kV}$  (Contact)
  - IEC 61000-4-5 (Surge) 4A (8/20 $\mu\text{s}$ )
- Package Optimized for High-Speed Lines
- Ultra-Small Package (1.0mm $\times$ 0.6mm $\times$ 0.55mm)
- Protects One Data, Control, or Power Line
- Low Capacitance: 12pF (Typical)
- Low Leakage Current: 0.01 $\mu\text{A}$  @  $V_{\text{RWM}}$  (Typical)
- Low Clamping Voltage
- Each I/O pin can withstand over 1000 ESD strikes for  $\pm 8\text{kV}$  contact discharge.

### Applications

- Desktops, Servers, and Notebooks
- Cellular Phones
- Digital Camera Ports

### Mechanical Characteristics

- DFN1.0 $\times$ 0.6-2 Package
- Marking: Part Number
- Packaging: Tape and Reel

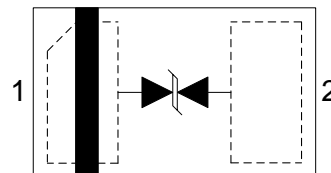
### Circuit Diagram



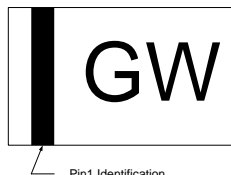
## Ordering Information

## Pinout (Top View)

Part Number	Package Type	Top Mark
SY205216DWC	DFN1.0x0.6-2 RoHS Compliant and Halogen Free	GW



## Marking Codes



**Note 1:** "G" is device code, fixed.

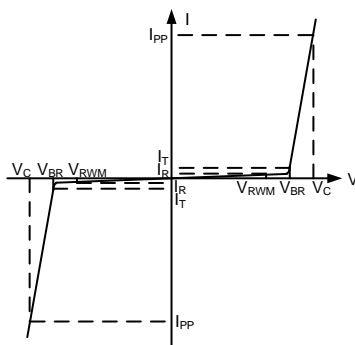
**Note 2:** "W" is date code.

Absolute Maximum Rating				
Parameter	Symbol	Min	Max	Unit
Maximum Peak Pulse Current (8/20μs)	I <sub>PP</sub>		4	A
Maximum Peak Pulse Power (8/20μs)	P <sub>PK</sub>		180	W
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V <sub>ESD</sub>	-30	30	kV
Operating Temperature	T <sub>OPT</sub>	-40	+125	°C
Storage Temperature	T <sub>STG</sub>	-55	+150	°C

Electrical Characteristics T <sub>A</sub> = 25°C						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal Reverse Working Voltage	V <sub>RWM</sub>				24	V
Reverse Leakage Current @ V <sub>RWM</sub>	I <sub>R</sub>	V <sub>RWM</sub> = 24V, T = 25°C Between I/O_1 and I/O_2		0.01	0.1	μA
Reverse Breakdown Voltage @ I <sub>T</sub>	V <sub>BR</sub>	I <sub>T</sub> = 1mA Between I/O_1 and I/O_2	26.5		33	V
Clamping Voltage @ I <sub>PP</sub>	V <sub>C</sub> (1)	I <sub>PP</sub> = 1A, t <sub>p</sub> = 8/20μs Between I/O_1 and I/O_2			36	V
Clamping Voltage @ I <sub>PP</sub>	V <sub>C</sub> (1)	I <sub>PP</sub> = 4A, t <sub>p</sub> = 8/20μs Between I/O_1 and I/O_2			42	V
Clamping Voltage @ I <sub>PP</sub>	V <sub>C</sub> (1)	I <sub>PP</sub> = 16A, t <sub>p</sub> = 10/100ns Between I/O_1 and I/O_2		35		V
Dynamic Resistance	R <sub>DYN</sub> (1,2)	t <sub>p</sub> = 10/100ns Between I/O_1 and I/O_2		0.3		Ω
Parasitic Capacitance	C <sub>ESD</sub> (1)	V <sub>R</sub> = 0V, f = 1MHz Between I/O_1 and I/O_2		12	15	pF

**Note 1:** Guaranteed by design and not subject to production test.

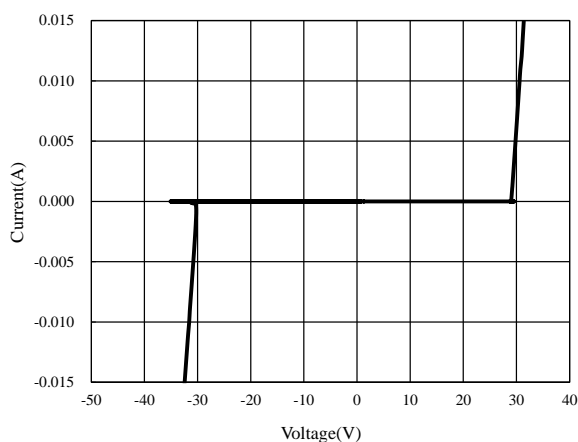
**Note 2:** R<sub>DYN</sub> calculated based on I<sub>PP</sub> = 8A to I<sub>PP</sub> = 16A, t<sub>p</sub> = 10/100ns.



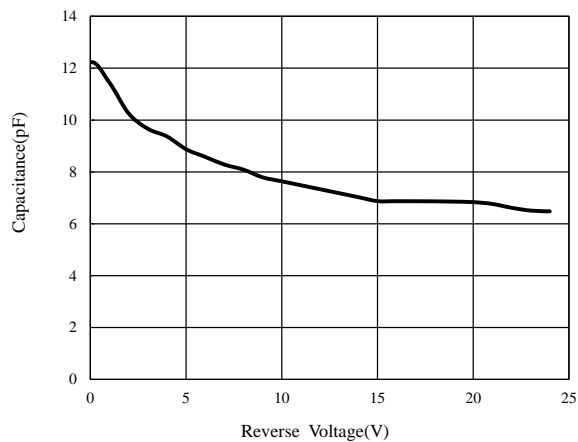
**Figure 1. Bi-directional TVS**

## Typical Characteristics

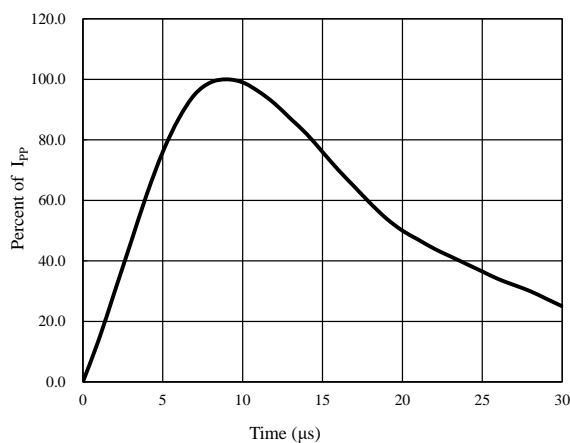
### Voltage Sweeping of I/O\_1 to I/O\_2



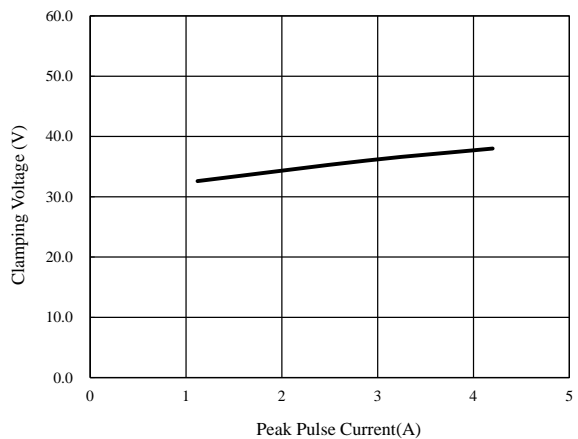
### Capacitance vs. Voltage



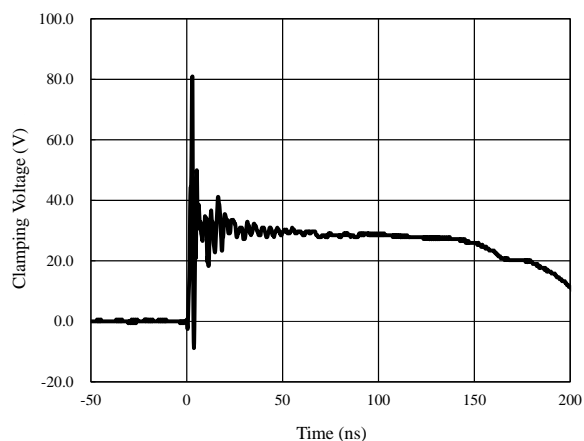
### Pulse Waveform



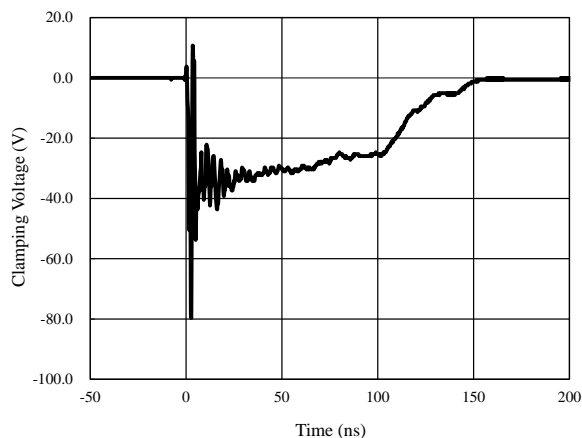
### Clamping Voltage vs. Peak Pulse Current



### ESD Clamping of I/O\_1 to I/O\_2 (+8kV Contact per IEC 61000-4-2)



### ESD Clamping of I/O\_1 to I/O\_2 (-8kV Contact per IEC 61000-4-2)



## Application Information

The SY205216DWC protects one bidirectional data line against over-voltage and over-current transient events by clamping it to an acceptable reference.

The SY205216DWC pin connections are shown in Figure 2. The protected line is connected at Pin1, while Pin2 is connected to the GND, which should connect to a ground plane on the board. All path lengths connected to pins of SY205216DWC should be as short as possible to minimize the parasitic inductance.

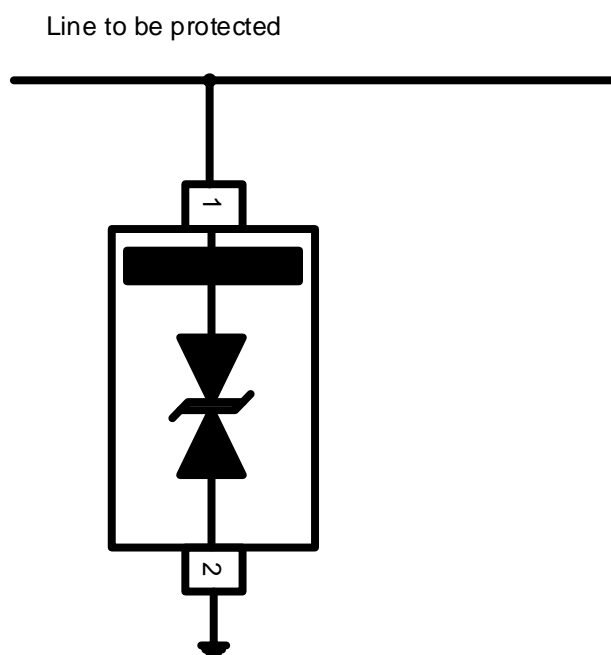


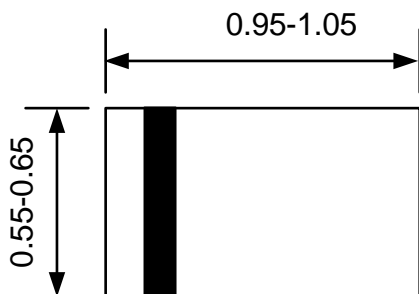
Figure 2. ESD/Surge Protection Circuit

## PCB Layout Guidelines

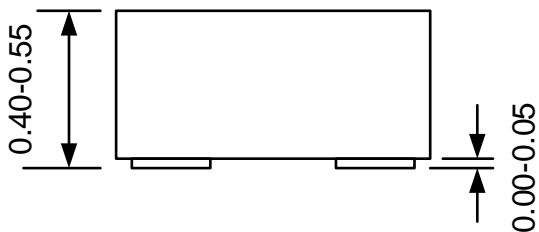
For optimum ESD protection and circuit performance, the following circuit board guidelines are recommended:

- Place SY205216DWC as close to the connector or terminal ports as possible.
- Use a large via to connect the SY205216DWC pin to the ground.
- Avoid running signals near board edges.
- The SY205216DWC should be placed near the protected line.
- The distance between the SY205216DWC ground pin and the GND reference path should be as short as possible.

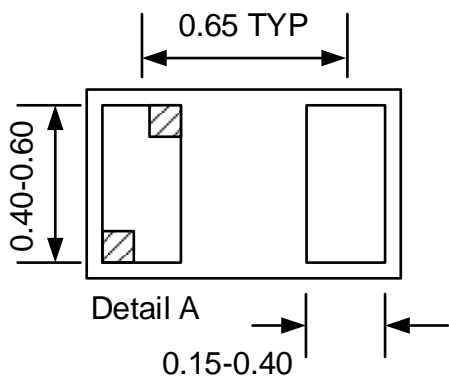
## DFN1.0x0.6-2 Package Outline



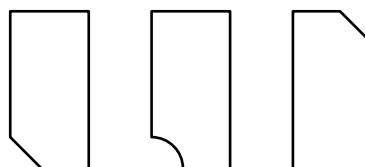
Top View



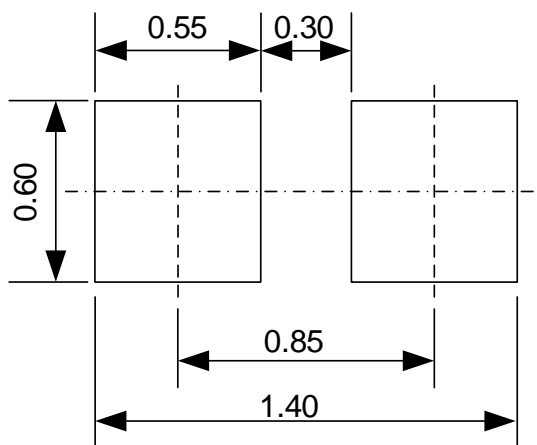
Side View



Bottom View



Detail A

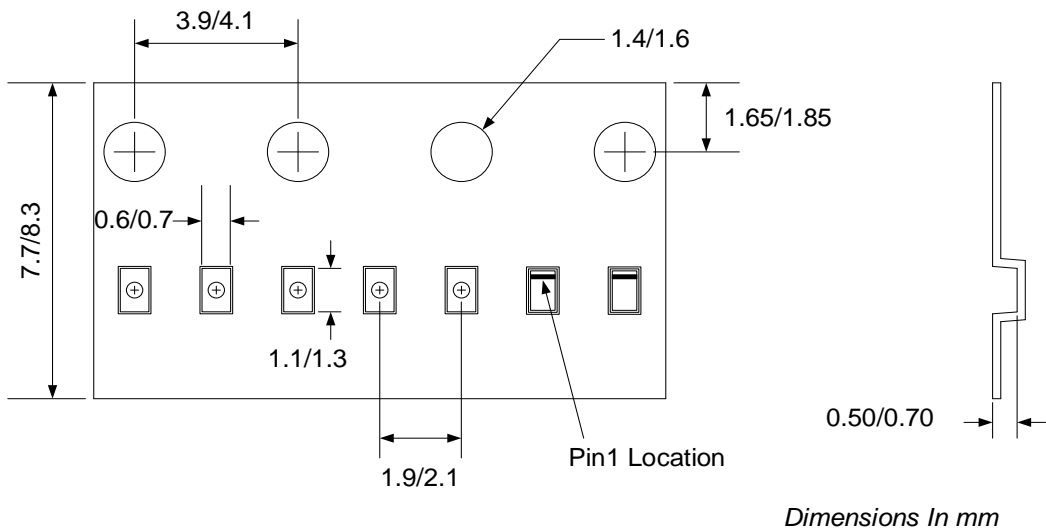


Recommended PCB Layout  
(Reference only)

**Note:** All dimensions are in millimeters and exclude mold flash and metal burr.

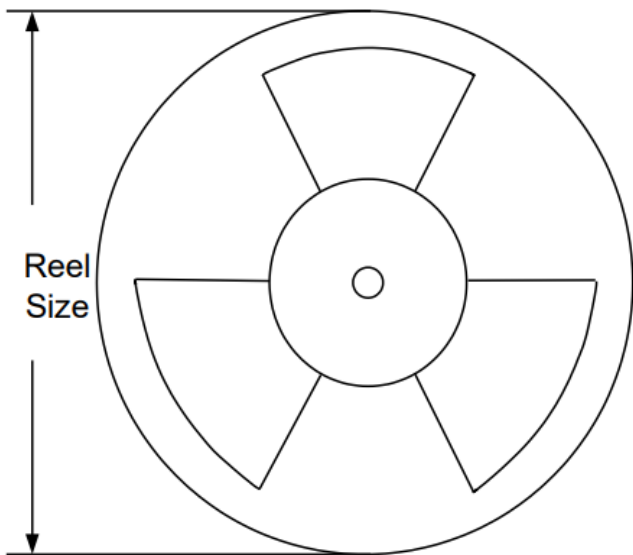
### Tape and Reel Specification

#### DFN1.0x0.6-2 Taping Orientation



Feeding direction →

#### Carrier Tape & Reel Specification for Packages



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Trailer * Length(mm)	Leader * Length (mm)	Qty per Reel (pcs)
DFN1.0x0.6-2	8	2	7"	400	400	10000



## Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
0.9	10/16/2018	Initial Release	
1.0	10/16/2019	Production Release	



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