# SY20122A1

## High Efficiency, 1.5MHz, 5.5V, 2A Synchronous Buck Regulator

## General Description

The SY20122A1 high efficiency and low quiescent current synchronous Buck regulator operates over a wide input voltage range of 2.5V to 5.5V, and can deliver an output current up to 2A. It integrates a top FET and a bottom FET with very low $R_{DS(ON)}$ to minimize conduction loss. The 1.5MHz pseudo-constant switching frequency enables using small external inductor and capacitor values.

The SY20122A1 employs constant off-time and peak current mode control strategy to achieve fast transient response and high efficiency at light loads. It also provides cycle-by-cycle current limiting and over temperature protection.

The SY20122A1 is highly integrated, so only the input and output capacitors, inductor, and feedback network components need to be selected for the targeted application specifications.

The SY20122A1 is available in a space-saving, low-profile SOT23-6 package.

## Features

- Low $R_{DS(ON)}$ for Internal Switches: 130mΩ Top, 85mΩ Bottom
- 2.5V ~ 5.5V Input Voltage Range
- Up to 2A Output Current
- 50μA Low Quiescent Current
- 1.5MHz High Switching Frequency Minimizes Required External Components
- Constant Off-Time and Peak Current Mode Control
- Internal Soft-Start Limits Inrush Current
- 100% Dropout Operation
- Power-Good Indicator
- Hiccup Mode for Short-Circuit Protection
- Output Auto-Discharge Function
- Input Under Voltage Lockout (UVLO)
- RoHS-Compliant and Halogen-Free
- Compact SOT23-6 Package

## Applications

- Set-Top Box
- USB Dongle
- Media Player
- Smartphone

## Typical Application

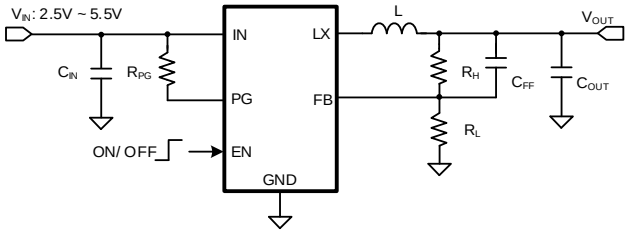



*Figure 1. Schematic Diagram*

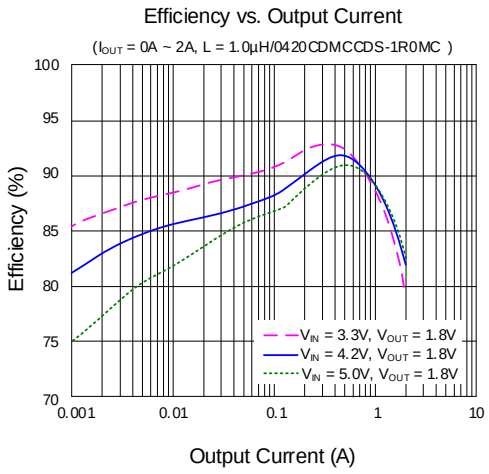


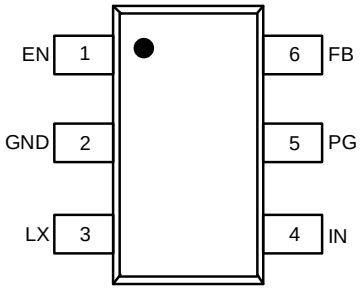

*Figure 2. Efficiency vs. Output Current*

## Ordering Information

| Ordering Part Number | Package Type | Top Mark |
|---|---|---|
| SY20122A1ABC | SOT23-6<br>RoHS-Compliant, Halogen-Free | **rB*xyz*** |

***x = year code, y = week code, z = lot number code***

## Pinout (top view)




## Pin Description

| Pin No | Pin Name | Pin Description |
|---|---|---|
| 1 | EN | Enable pin. Pull low to disable the Buck regulator, pull high to enable the Buck regulator. Do not leave this pin floating. |
| 2 | GND | Ground pin. |
| 3 | LX | Inductor pin. Connect this pin to the switching node of the inductor. |
| 4 | IN | Input pin. Decouple this pin to the GND pin with at least a 10µF ceramic capacitor. |
| 5 | PG | Power-good Indicator. PG pin should be connected to $V_{IN}$ or another voltage source through a resistor (e.g., 10kΩ–100kΩ). This pin becomes low if the $V_{FB}$ < 90%$V_{REF}$ or $V_{FB}$ > 120%$V_{REF}$; this pin becomes high otherwise. |
| 6 | FB | Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT} = 0.6 \times (1 + R_H/R_L)$. |

## Block Diagram

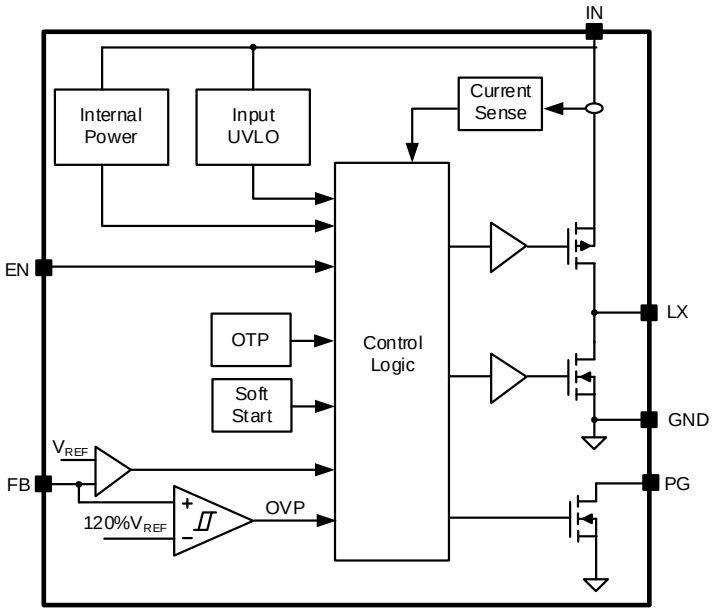



*Figure 3. Block Diagram*

## Absolute Maximum Ratings

| Parameter (Note 1) | Min | Max | Unit |
|---|---|---|---|
| IN | -0.3 | 6 | V |
| EN, FB, PG | -0.3 | IN + 0.6 | |
| LX | -0.3 | 6 | |
| LX, 40ns duration | -3 | 7 | |
| Junction Temperature, Operating | -40 | 150 | °C |
| Lead Temperature (Soldering,10s) | | 260 | |
| Storage Temperature | -65 | 150 | |

## Thermal Information

| Parameter (Note 2) | Typ | Unit |
|---|---|---|
| $\theta_{JA}$ Junction-to-Ambient Thermal Resistance | 120 | °C/W |
| $\theta_{JC}$ Junction-to-Case Thermal Resistance | 20 | |
| $P_D$ Power Dissipation $T_A$ = 25°C | 0.83 | W |

## Recommended Operating Conditions

| Parameter (Note 3) | Min | Max | Unit |
|---|---|---|---|
| IN | 2.5 | 5.5 | V |
| Output Voltage | 0.6 | 5.5 | |
| Output Current | | 2 | A |
| Junction Temperature | -40 | 125 | °C |

## Electrical Characteristics

($V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, L =1μH, $C_{OUT}$ = 10μF, $T_J$ = 25°C, unless otherwise specified)

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Input | Voltage | $V_{IN}$ | | 2.5 | | 5.5 | V |
| | UVLO Rising Threshold | $V_{IN,UVLO}$ | | | | 2.5 | |
| | UVLO Hysteresis | $V_{IN,HYS}$ | | | 150 | | mV |
| | Quiescent Current | $I_Q$ | $V_{FB}$ = 105% × $V_{REF}$ | | 50 | 70 | μA |
| | Shutdown Current | $I_{SHDN}$ | $V_{EN}$ = 0V | | 0.1 | 1 | |
| Output | Reference Voltage | $V_{REF}$ | $I_{OUT}$ = 0.5A, CCM | 0.591 | 0.6 | 0.609 | V |
| | Turn On Delay Time | $t_{ON,DLY}$ | From EN high to LX starts switching (Note 4) | | 0.5 | | ms |
| | Soft-Start Time | $t_{SS}$ | $V_{OUT}$ from 0% to 100% (Note 4) | | 1 | | |
| | Discharge on Resistance | $R_{DIS}$ | | | 50 | | Ω |
| MOSFET | Top FET $R_{DS(ON)}$ | $R_{DS(ON)1}$ | | | 130 | | mΩ |
| | Bottom FET $R_{DS(ON)}$ | $R_{DS(ON)2}$ | | | 85 | | |
| | Top FET Current Limit Threshold | $I_{LMT,TOP}$ | | 3.5 | | | A |
| Enable (EN) | Input Voltage High | $V_{EN,H}$ | | 1.2 | | | V |
| | Input Voltage Low | $V_{EN,L}$ | | | | 0.4 | |
| Power-Good | Thresholds | $V_{PG,UVP}$ | PG threshold for under voltage detection | | 90 | | %$V_{REF}$ |
| | | $V_{PG,OVP}$ | PG threshold for over voltage detection | | 120 | | |
| | Delay | $t_{PG,UVP}$ | PG low delay time for under voltage detection (Note 4) | | 20 | | μs |
| | | $t_{PG,OVP}$ | PG low delay time for over voltage detection (Note 4) | | 20 | | |
| COT | Switching Frequency | $f_{SW}$ | $I_{OUT}$ = 0.5A, CCM | | 1.5 | | MHz |
| | Minimum On-Time | $t_{ON,MIN}$ | (Note 4) | | 60 | | ns |
| | Maximum Duty Cycle | $D_{MAX}$ | (Note 4) | 100 | | | % |
| OTP | Temperature | $T_{OTP}$ | (Note 4) | | 160 | | °C |
| | Temperature Hysteresis | $T_{HYS}$ | (Note 4) | | 20 | | |

**Note 1**: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:** $\theta_{JA}$ of SY20122A1ABC is measured in the natural convection at $T_A$ = 25°C on a 2oz two-layer Silergy evaluation board. Pin 3 is the case position for SY20122A1ABC $\theta_{JC}$ measurement.

**Note 3:** The device is not guaranteed to function outside its operating conditions.

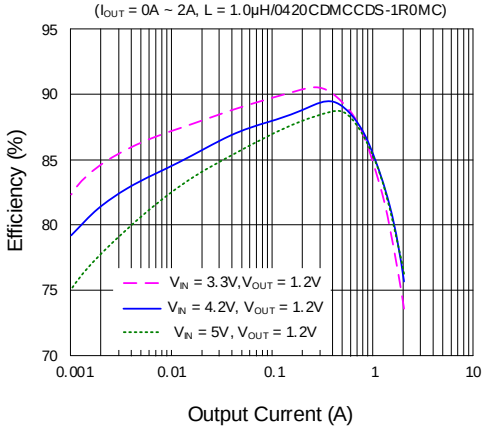
**Note 4:** Guaranteed by design.

## Typical Performance Characteristics

($T_A$ = 25°C, $V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, L = 1μH, $C_{OUT}$ = 10μF, unless otherwise noted)

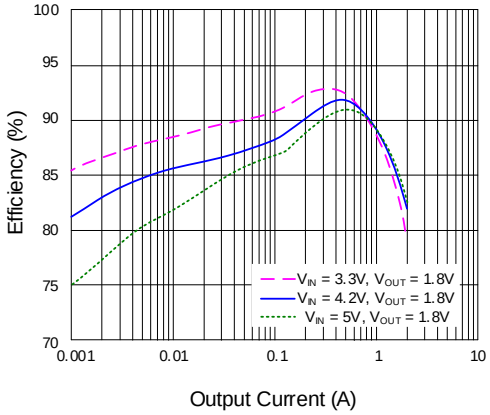
Efficiency vs. Output Current

($I_{OUT}$ = 0A ~ 2A, L = 1.0μH/0420CDMCCDS-1R0MC)



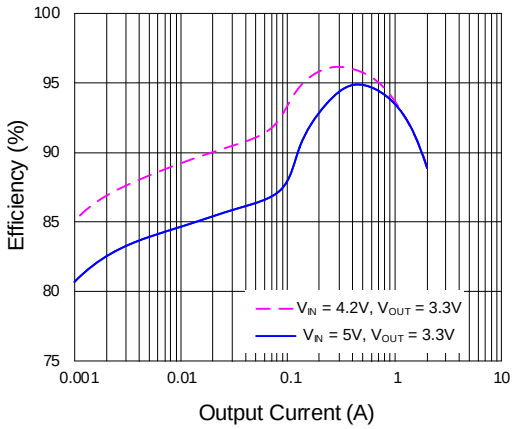

Efficiency vs. Output Current

($I_{OUT}$ = 0A ~ 2A, L = 1.0μH/0420CDMCCDS-1R0MC)



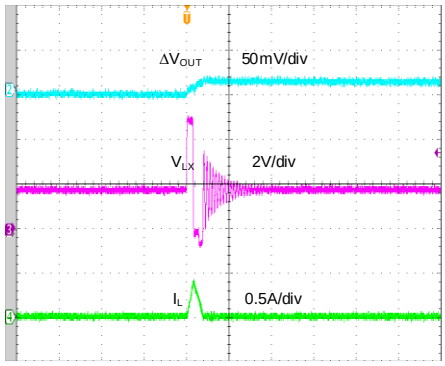

Efficiency vs. Output Current

($I_{OUT}$ = 0A ~ 2A, L = 1.0μH/0420CDMCCDS-1R0MC)



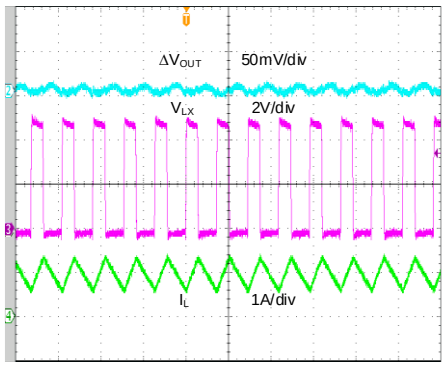

Output Ripple

($V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 2A)



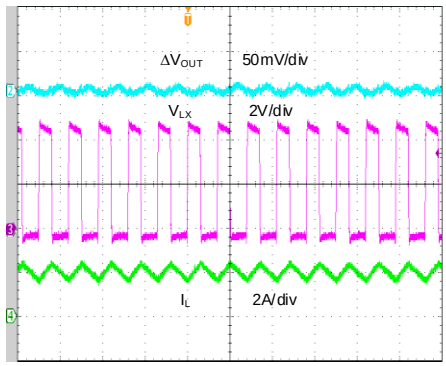

Output Ripple

($V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 1A)



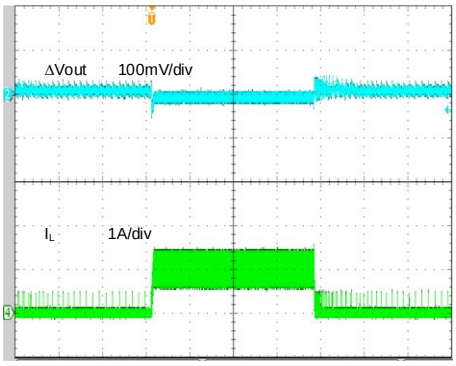

Output Ripple

($V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 2A)



Load Transient

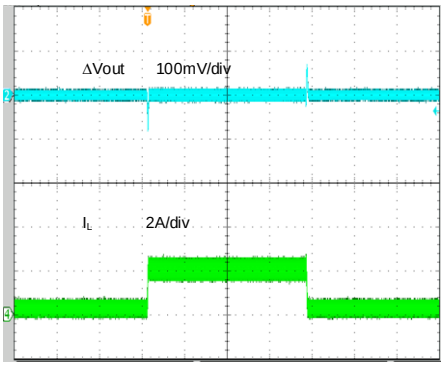
($V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 0A ~ 1A)




Time (400μs/div)

Load Transient

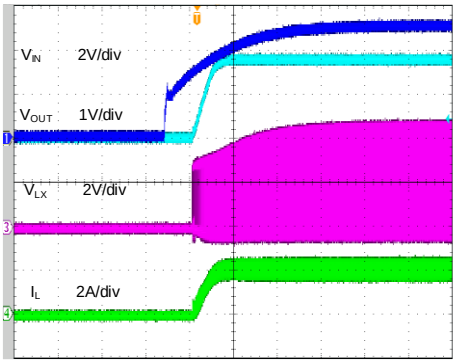
($V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 0.2A ~ 2A)




Time (400μs/div)

Startup from $V_{IN}$

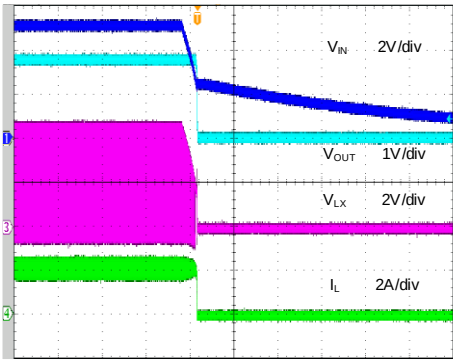
($V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 2A)




Time (2ms/div)

Shutdown from $V_{IN}$

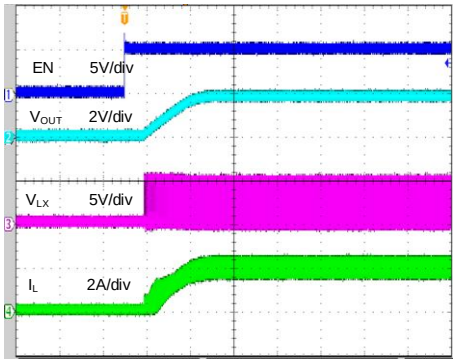
($V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 2A)




Time (2ms/div)

Startup from Enable

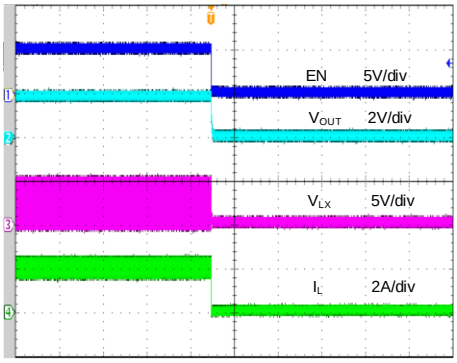
($V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 2A)




Time (800μs/div)

Shutdown from Enable

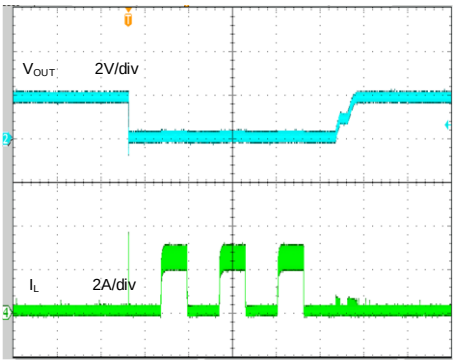
($V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 2A)




Time (800μs/div)

Short Circuit Protection

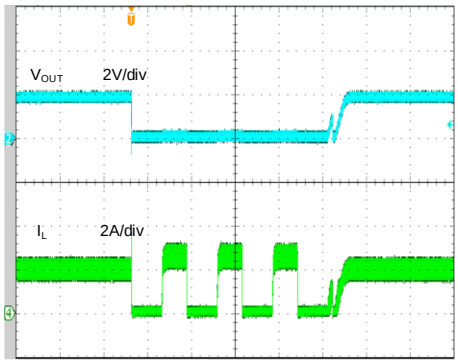
($V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 0A ~ short)




Time (4ms/div)

Short Circuit Protection

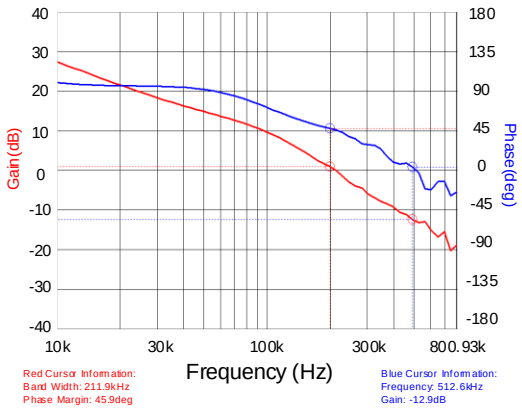
($V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 2A ~ short)




Time (4ms/div)

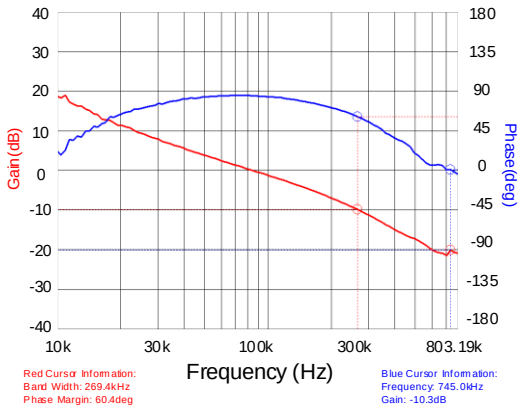
Bode Plot

($V_{IN}$ = 5V, $V_{OUT}$ = 1.2V, $I_{OUT}$ = 2A)



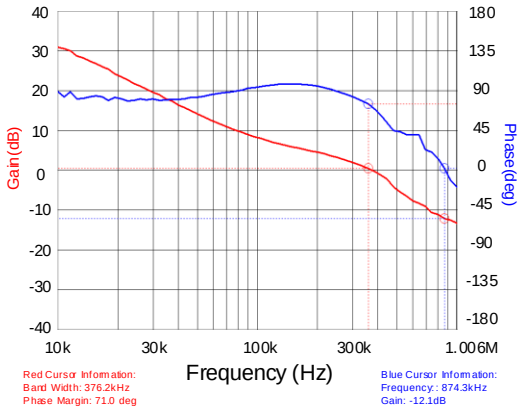

Bode Plot

($V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 2A)




Bode Plot

($V_{IN}$ = 5V, $V_{OUT}$ = 3.3V, $I_{OUT}$ = 2A)



## Detailed Description

The SY20122A1 high efficiency and low quiescent current synchronous Buck regulator operates over a wide input voltage range of 2.5V to 5.5V, and can deliver an output current up to 2A. It integrates a top FET and a bottom FET with very low $R_{DS(ON)}$ to minimize conduction loss. The 1.5MHz pseudo-constant switching frequency enables using small external inductor and capacitor values.

### Constant Off-Time and Peak Current Mode Control

The SY20122A1 adopts constant off-time and peak current mode control strategy. When the current-sense signal of the top FET reaches internal $V_{COMP}$, the top FET will turn off and the bottom FET will turn on for a fixed period of time (constant $t_{OFF}$). $t_{OFF}$ is internally calculated according to the input voltage, output voltage, and desired switching frequency ($f_{SW}$):

$$t_{OFF} = \frac{1 - V_{OUT}/V_{IN}}{f_{SW}}$$

The bottom FET will turn off then the top FET will turn on after a period of $t_{OFF}$ under continuous conduction mode (CCM) operation. Under discontinuous conduction mode (DCM) operation, the bottom FET will turn off when its current exceeds zero, the top FET will turn on once the $V_{COMP}$ quits the low clamp value.

### Input Under Voltage Lockout (UVLO)

To prevent operation before all internal circuitry is ready and to ensure that the top FET and bottom FET can be sufficiently enhanced, the SY20122A1 incorporates one input under-voltage lockout protections. The SY20122A1 remains in a low current state and all switching actions are inhibited until $V_{IN}$ exceeds its rising threshold. At that time, if EN is enabled, the device will start-up. If $V_{IN}$ falls below $V_{IN,UVLO}$ less than the input UVLO hysteresis, switching actions will again be suppressed.

### Enable Control

The EN input is a high-voltage input with logic-compatible threshold. When EN is driven above 1.2V, normal device operation is enabled. When EN is driven to less than 0.4V, the device will shut down, reducing the input current to less than 1μA.

### Output Power-Good Indicator

The power-good indicator is an open drain output controlled by a window comparator connected to the feedback signal. PG pin should be connected to $V_{IN}$ or another voltage source through a resistor (e.g., 10kΩ–100kΩ). This pin becomes low if the $V_{FB}$ < 90%$V_{REF}$ or $V_{FB}$ > 120%$V_{REF}$; this pin becomes high otherwise if the input voltage high enough.

## Fault-Protection Modes

### Output Current Limit

With load current increasing, as soon as the top FET current exceeds the top FET current limit threshold, the top FET will turn off. If the load current continues to increase, the output voltage will drop.

### Output Under Voltage Protection (UVP)

If $V_{OUT}$ is less than approximately 50% of the target output voltage for at least one UVP delay time (when the output short circuits or the load current is much higher than the maximum current capacity), the output undervoltage protection (UVP) will be triggered, and the device will enter into hiccup protection mode. The hiccup frequency is 190Hz and the hiccup duty cycle is 50%. If the output fault conditions are removed, the Buck regulator will return to normal operation in the subsequent hiccup on-time.

To avoid output overshoot, the internal soft-start circuit voltage $V_{SS}$ will be pulled low temporarily when $V_{FB}$ exceeds the UVP threshold with the output fault conditions removed during hiccup on time, and then the $V_{SS}$ will rise smoothly to ramp the output to the desired voltage during a new soft-start cycle.

### Output Overvoltage Protection (OVP)

If the output voltage rises above the feedback regulation level, the top FET will naturally remain off, and the bottom FET will remain on until the inductor current reaches zero and the switching actions are suppressed. The switching actions will be resumed once the $V_{COMP}$ quits the low clamp value.

### Over Temperature Protection (OTP)

The Buck regulator includes over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The Buck regulator will shut down when its junction temperature exceeds 160°C. Once the junction temperature cools by approximately 20°C, the Buck regulator will resume normal operation after a

complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature will not exceed the OTP threshold.

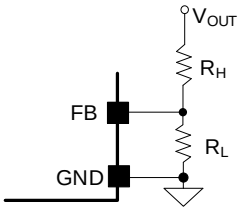
## Application Information

The following paragraphs describe the selection process for capacitor $C_{IN}$, output capacitor $C_{OUT}$, output inductor L, and feedback network components $R_H$, $R_L$ and $C_{FF}$.

**Feedback Resistor-Divider $R_H$ and $R_L$**

Choose $R_H$ and $R_L$ to program the proper output voltage. A value between 1kΩ and 1MΩ is recommended for both resistors. If $R_L$ is chosen, then $R_H$ can be calculated as follows:

$$R_L = \frac{0.6V}{V_{OUT} - 0.6V} R_H$$




**Input Capacitor $C_{IN}$**

For the best performance, select a typical X5R or better grade ceramic capacitor with a 6.3V rating, and greater than 10μF capacitance. The capacitor should be placed as close as possible to the device, while also minimizing the loop area formed by $C_{IN}$ and the IN/GND pins. When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge current capability, and high RMS current rating over a wide temperature and voltage range.

In situations where the input rail is supplied through long wires, it is recommended to add some bulk capacitance like electrolytic, tantalum or polymer type capacitors to reduce the overshoot and ringing caused by the added parasitic inductance.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1 - D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 10μF X5R capacitor is sufficient in most applications.

**Output Inductor L**

There are several considerations in choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT} / V_{IN,MAX})}{f_{sw} \times I_{OUT,MAX} \times 0.4}$$

Where $f_{SW}$ is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

2) The saturation current rating of the inductor must be greater than the peak inductor current under full-load conditions:

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is recommended to choose an inductor with DCR less than 50mΩ to achieve good overall efficiency.

**Output Capacitor $C_{OUT}$**

Select the output capacitor $C_{OUT}$ to handle the output ripple requirements. Both steady-state ripple and transient requirements must be taken into consideration when selecting the component. For the best performance, use an X5R or a better grade ceramic capacitor with a 6.3V rating, and capacitance greater than 10μF.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed:

The output voltage ripple at the switching frequency is caused by the inductor current ripple ($\Delta I_L$) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple).

When calculating total ripple, consider both.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

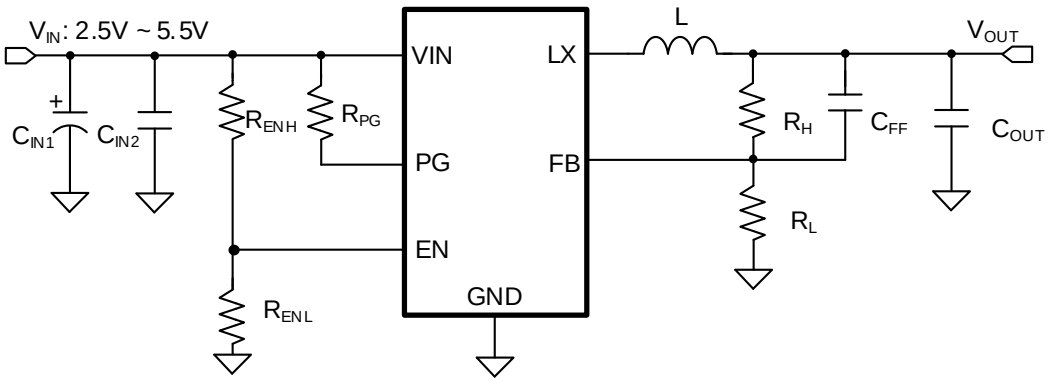
$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The capacitive ripple might be higher because the effective capacitance for ceramic capacitors decreases with the voltage across the terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

**Load Transient Considerations**

The SY20122A1 integrates compensation components to achieve good stability and fast transient responses. In some applications, adding a ceramic capacitor (feedforward capacitor $C_{FF}$) in parallel with $R_H$ can increase crossover frequency and further speed up the load transient response. The feedforward capacitor is recommended for applications with large load transient step requirements if the loop gain test is acceptable.

## Application Schematic ($V_{OUT}$ = 1.8V)




## BOM List

| Reference Designator | Description | Part Number | Manufacturer |
|---|---|---|---|
| $C_{IN1}$ | 100µF/25V(electrolytic capacitor) | | |
| $C_{IN2}$ | 10µF/6.3V, X5R, 0603 | C1608X5R0J106M | TDK |
| $C_{OUT}$ | 10µF/6.3V, X5R, 0603 | C1608X5R0J106M | TDK |
| $C_{FF}$ | 22pF/50V, C0G, 0603 | C1608C0G1H220J | TDK |
| L | 1.0µH | 0420CDMCCDS-1R0MC | Sumida |
| $R_H$ | 100kΩ, 1%, 0603 | | |
| $R_L$ | 49.9kΩ, 1%, 0603 | | |
| $R_{PG}$ | 100kΩ, 1%, 0603 | | |
| $R_{ENH}$ | 10kΩ, 1%, 0603 | | |
| $R_{ENL}$ | 1MΩ, 1%, 0603 | | |

## Recommended Component Values for Typical Applications

| $V_{OUT}$(V) | $R_H$(kΩ) | $R_L$(kΩ) | $C_{FF}$(pF) | L/Part Number | $C_{OUT}$ |
|---|---|---|---|---|---|
| 1.2 | 49.9 | 49.9 | 22 | 1.0µH/0420CDMCCDS-1R0MC | 10µF/6.3V, X5R, 0603 |
| 1.8 | 100 | 49.9 | 22 | 1.0µH/0420CDMCCDS-1R0MC | 10µF/6.3V, X5R, 0603 |
| 3.3 | 100 | 22.1 | 22 | 1.0µH/0420CDMCCDS-1R0MC | 10µF/6.3V, X5R, 0603 |

## Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

- **Input Capacitors:** Place the input capacitors as close as possible to the IN and GND pins, minimizing the loop formed by these connections. The input capacitor should be connected to the IN and GND by a wide copper plane.
- **Output Capacitors:** Connect the $C_{OUT}$ negative terminal to the GND pin using wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.
- **Feedback Network:** Place the feedback components ($R_H$, $R_L$, and $C_{FF}$) as close to the FB pin as possible. Avoid routing the feedback line near LX, or other high-frequency signals as it is noise-sensitive. Use a Kelvin connection to connect with $C_{OUT}$ rather than the inductor output terminal.
- **LX Connection:** Keep the LX area small to prevent excessive EMI, while providing a wide copper trace to minimize parasitic resistance and inductance.
- **EN Signal:** It is not recommended to connect EN signal directly to $V_{IN}$. A resistor in a range of 1kΩ to 1MΩ should be used if the lines are pulled high to $V_{IN}$.
- **GND Vias:** Place an adequate number of vias on the GND layer around the device for better thermal performance.
- **PCB Board:** To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if board space allows. Connect the ground pad to a large copper area to enhance thermal performance.

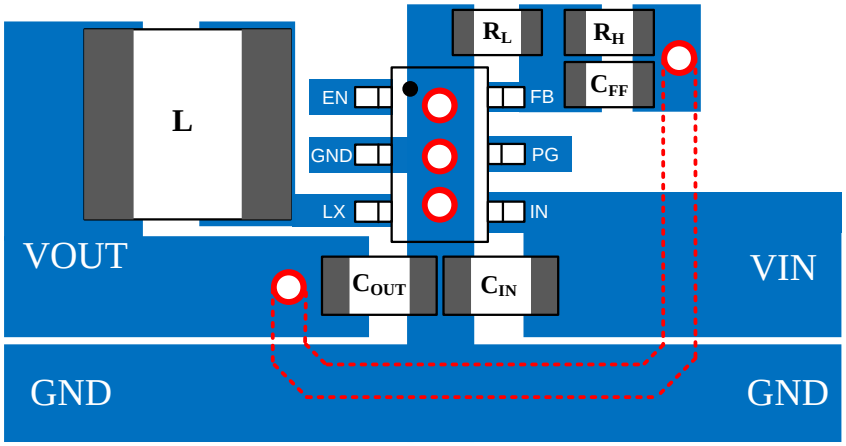
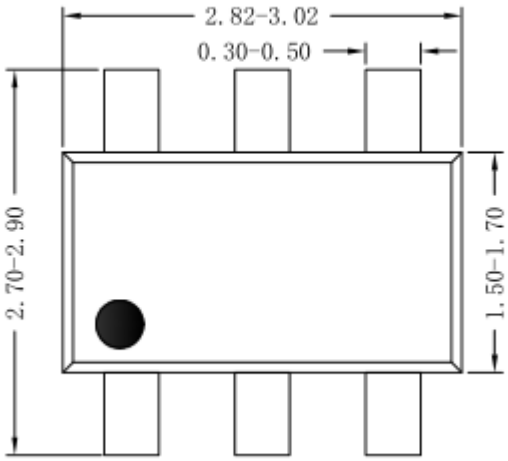
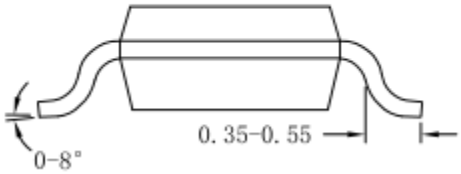



*Figure 4. Suggested PCB Layout*

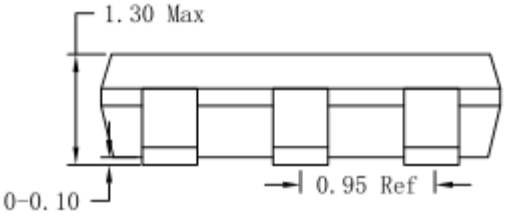
## SOT23-6 Package Outline Drawing



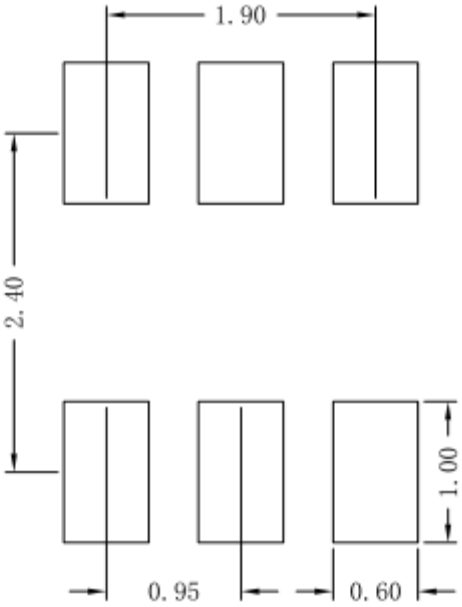

**Top View**




**Side View**




**Side View**

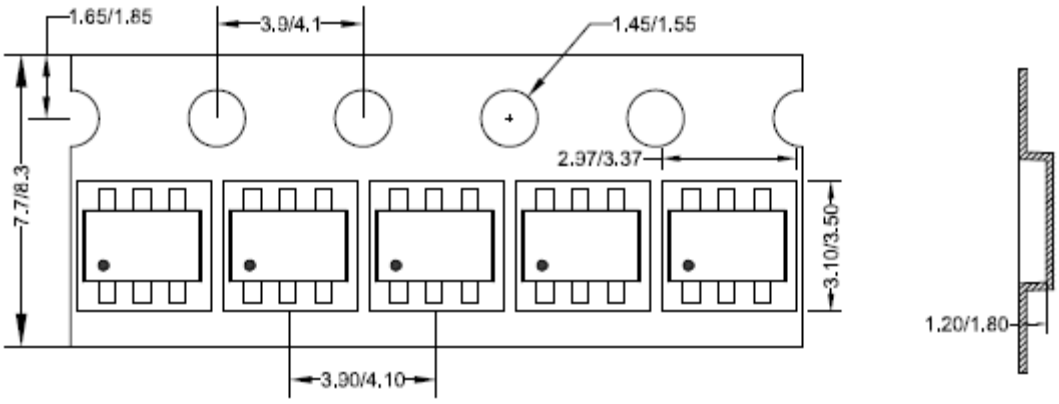



**Recommended PCB layout**
**(Reference only)**

***Note:*** *All dimensions are in millimeters and exclude mold flash and metal burr.*

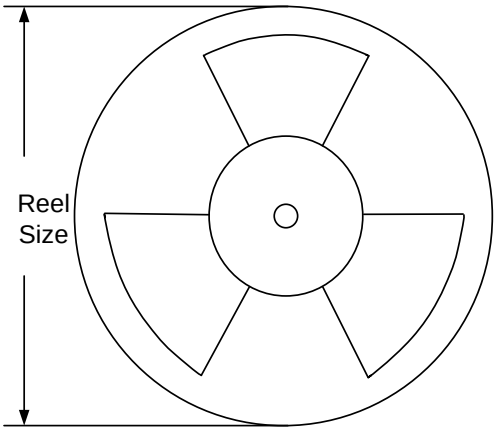
# Taping and Reel Specification

## SOT23-6 Taping Orientation




**Feeding Direction** ⟶

## Carrier Tape and Reel Specification for Packages




| Package types | Tape width (mm) | Pocket pitch(mm) | Reel size (Inch) | Trailer length(mm) | Leader length (mm) | Qty per reel (pcs) |
|---|---|---|---|---|---|---|
| SOT23-6 | 8 | 4 | 7" | 280 | 160 | 3000 |

**Others: NA**

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, it is not warrantied. Please make sure that you have the latest revision.

| Date | Revision | Change |
|---|---|---|
| Jan. 17, 2019 | Revision 0.9 | Initial Release |
| Oct. 23, 2023 | Revision 1.0 | Production Release |

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