BUJD203AX

NPN power transistor with integrated diode

9 October 2018 — Product data sheet

1. General description

High voltage, high speed, planar passivated NPN power switching transistor with integrated anti-parallel E-C diode in a SOT186A (TO220F) "full pack" plastic package.

2. Features and benefits

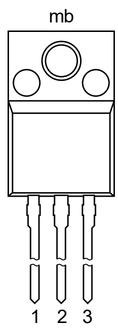
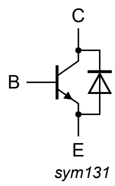
- Fast switching
- High voltage capability
- Integrated anti-parallel E-C diode
- Isolated package
- Very low switching and conduction losses

3. Applications

- DC-to-DC converters
- Electronic lighting ballasts
- Inverters
- Motor control systems

4. Pinning information

Table 1. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	B	base	 TO-220F (SOT186A)	
2	C	collector		
3	E	emitter		
mb	n.c.	mounting base; isolated		

5. Ordering information

Table 2. Ordering information

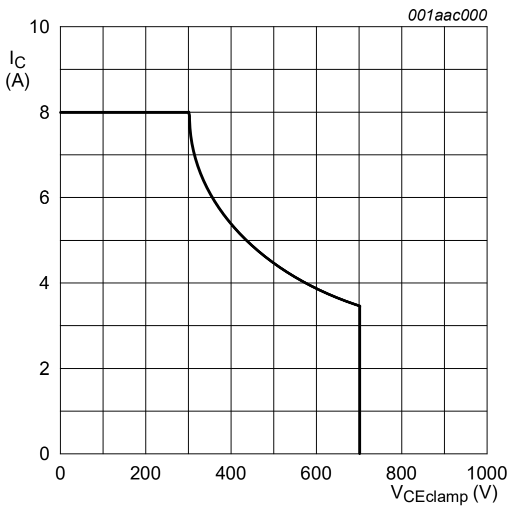
Type number	Package		
	Name	Description	Version
BUJD203AX	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

6. Limiting values

Table 3. Limiting values

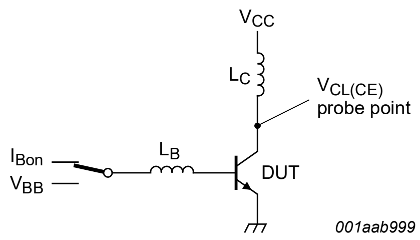
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CESM}	collector-emitter peak voltage	V_{BE} = 0 V		-	850	V
V_{CBO}	collector-base voltage	I_E = 0 A		-	850	V
V_{CEO}	collector-emitter voltage	I_B = 0 A		-	425	V
I_C	collector current	DC; Fig. 1; Fig. 2; Fig. 3		-	4	A
I_{CM}	peak collector current	Fig. 1; Fig. 2; Fig. 3		-	8	A
I_B	base current	DC		-	2	A
I_{BM}	peak base current			-	4	A
P_{tot}	total power dissipation	$T_h \leq$ 25 °C; Fig. 4		-	26	W
T_{stg}	storage temperature			-65	150	°C
T_j	junction temperature			-	150	°C



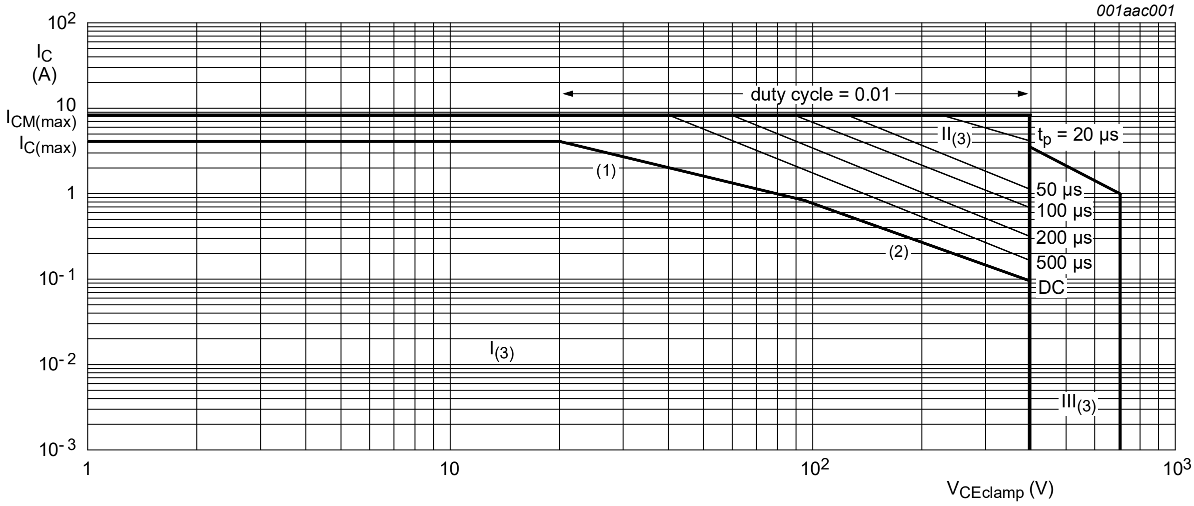
$T_j \leq T_{j(max)}$ °C

Fig. 1. Reverse bias safe operating area



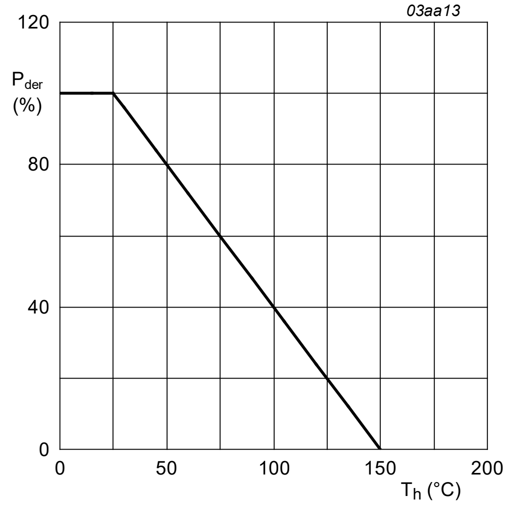
$V_{CL(CE)} \leq$ 1000 V; V_{CC} = 150 V; V_{BB} = - 5 V;
L_B = 1 μH; L_C = 200 μH

Fig. 2. Test circuit for reverse bias safe operating area



1) Ptot maximum and Ptot peak maximum lines
2) Second breakdown limits
3) I = Region of permissable DC operation
II = Extension for repetitive pulse operation
III = Extension during turn-on in single transistor converters provided that $R_{BE} \leq 100\ \Omega$ and $t_p \leq 0.6\ \mu s$

Fig. 3. Forward bias safe operating area for Tmb ≤ 25 °C



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 4. Normalized total power dissipation as a function of heatsink temperature

7. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	with heatsink compound; Fig. 5		-	-	4.8	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	in free air		-	55	-	K/W

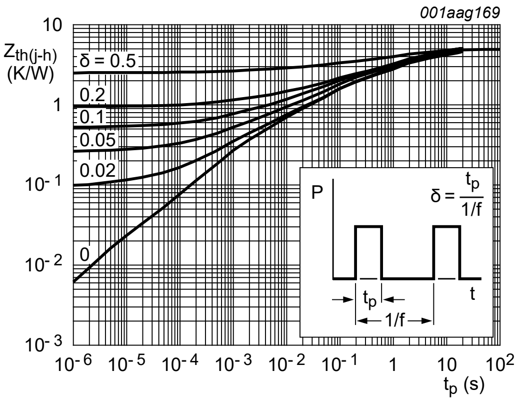


Fig. 5. Transient thermal impedance from junction to heatsink as a function of pulse duration

8. Isolation characteristics

Table 5. Isolation characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; T_h = 25 °C; from all terminals to external heatsink; clean and dust free		-	-	2500	V
C_{isol}	isolation capacitance	T_h = 25 °C; f = 1 MHz; from collector to external heatsink		-	10	-	pF

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{CES}	collector-emitter cut-off current (base shorted)	V_{BE} = 0 V; V_{CE} = 850 V; T_j = 125 °C	[1]	-	-	2	mA
		V_{BE} = 0 V; V_{CE} = 850 V; T_j = 25 °C	[1]	-	-	1	mA
I_{CBO}	collector-base cut-off current (emitter open)	V_{CB} = 850 V; I_E = 0 A	[1]	-	-	1	mA
I_{CEO}	collector-emitter cut-off current (base open)	V_{CE} = 425 V; I_B = 0 A	[1]	-	-	0.1	mA
I_{EBO}	emitter-base cut-off current (collector open)	V_{EB} = 7 V; I_C = 0 A		-	-	10	mA
V_{CEOsus}	collector-emitter sustaining voltage (base open)	I_B = 0 A; I_C = 10 mA; L_C = 25 mH; Fig. 6; Fig. 7		400	450	-	V
V_{CEsat}	collector-emitter saturation voltage	I_C = 3 A; I_B = 0.6 A; Fig. 8; Fig. 9		-	0.29	1	V
V_{BEsat}	base-emitter saturation voltage	I_C = 3 A; I_B = 0.6 A; Fig. 10		-	0.99	1.5	V
V_F	forward voltage	I_F = 2 A; T_j = 25 °C		-	1.04	1.5	V
h_{FE}	DC current gain	I_C = 1 mA; V_{CE} = 5 V; T_h = 25 °C; Fig. 11		10	15	32	
		I_C = 500 mA; V_{CE} = 5 V; T_h = 25 °C; Fig. 11		13	21	32	
		I_C = 2 A; V_{CE} = 5 V; T_h = 25 °C; Fig. 11		11	16	22	
		I_C = 3 A; V_{CE} = 5 V; T_h = 25 °C; Fig. 11		-	12.5	-	
Dynamic characteristics							
t_{on}	turn-on time	I_C = 2.5 A; I_{Bon} = 0.5 A; I_{Boff} = -0.5 A; R_L = 75 Ω; T_j = 25 °C; resistive load; Fig. 12; Fig. 13		-	0.52	0.6	µs
t_s	storage time			-	2.7	3.3	µs
		I_C = 2 A; I_{Bon} = 0.4 A; V_{BB} = -5 V; L_B = 1 µH; T_j = 25 °C; inductive load; Fig. 14; Fig. 15		-	1.2	1.4	µs
		I_C = 2 A; I_{Bon} = 0.4 A; V_{BB} = -5 V; L_B = 1 µH; T_j = 100 °C; inductive load; Fig. 14; Fig. 15		-	-	1.8	µs
t_f	fall time	I_C = 2.5 A; I_{Bon} = 0.5 A; I_{Boff} = -0.5 A; R_L = 75 Ω; resistive load; Fig. 12; Fig. 13		-	0.3	0.35	µs
		I_C = 2 A; I_{Bon} = 0.4 A; V_{BB} = -5 V; L_B = 1 µH; inductive load; Fig. 14; Fig. 15		-	-	0.12	µs
				-	0.03	0.06	µs

[1] Measured with half-sine wave voltage (curve tracer)

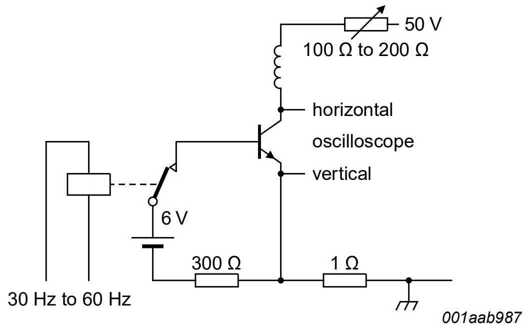


Fig. 6. Test circuit for collector-emitter sustaining voltage

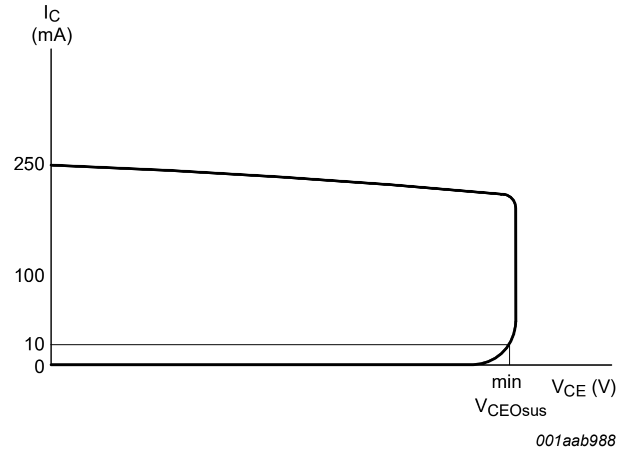


Fig. 7. Oscilloscope display for collector-emitter sustaining voltage test waveform

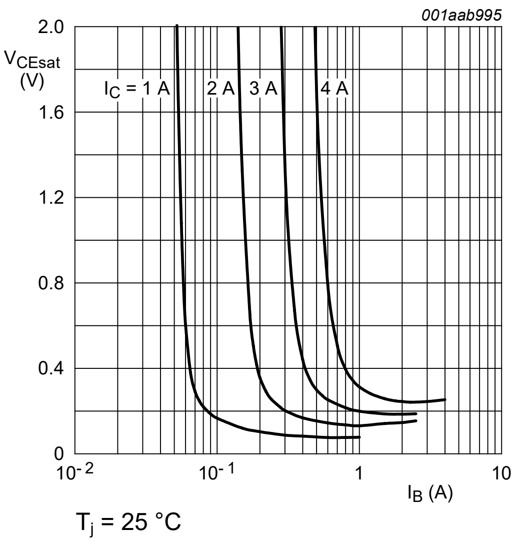


Fig. 8. Collector-emitter saturation voltage as a function of base current; typical values

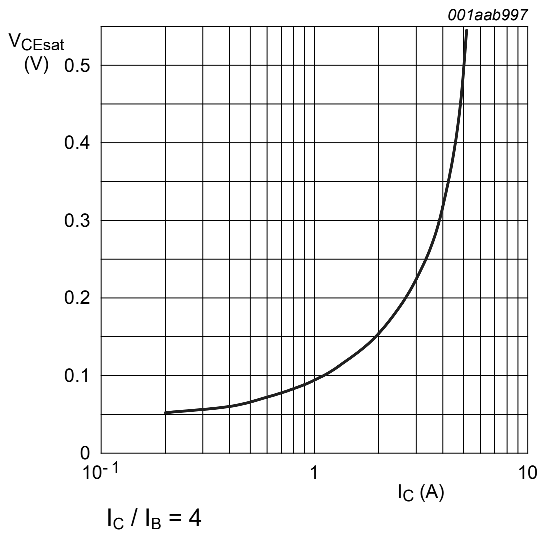


Fig. 9. Collector-emitter saturation voltage as a function of collector current; typical values

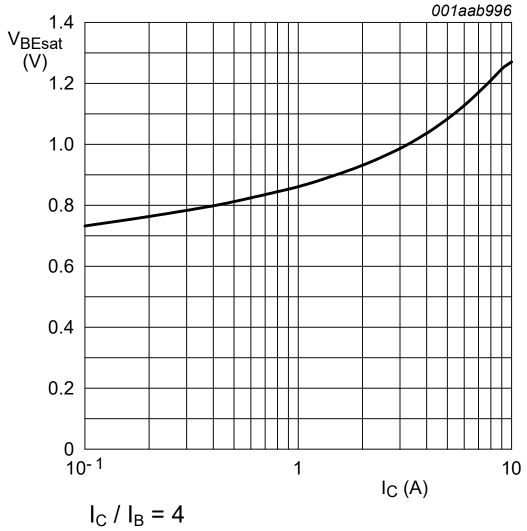


Fig. 10. Base-emitter saturation voltage as a function of collector current; typical values

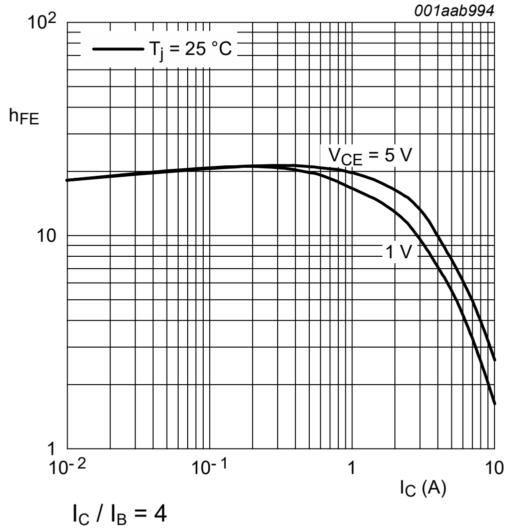
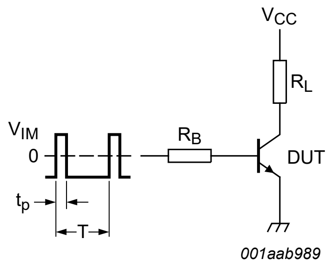


Fig. 11. DC current gain as a function of collector current; typical values



V_{IM}= - 6 to + 8 V; V_{CC} = 250 V; t_p = 20 us; $\delta = t_p/T$ = 0.01

R_B and R_L calculated from I_{Con} and I_{Bon} requirements.

Fig. 12. Test circuit for resistive load switching

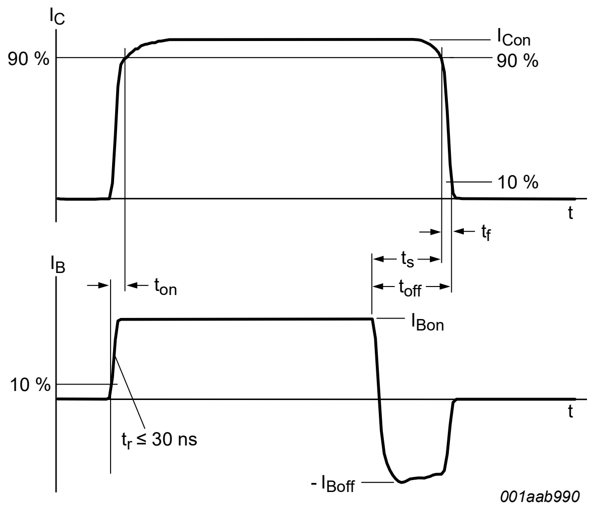
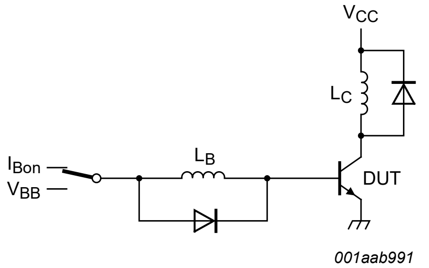


Fig. 13. Switching times waveforms for resistive load



V_{CC} = 300 V; V_{BB} = - 5 V; L_C = 200 μH; L_B = 1 μH

Fig. 14. Test circuit for inductive load switching

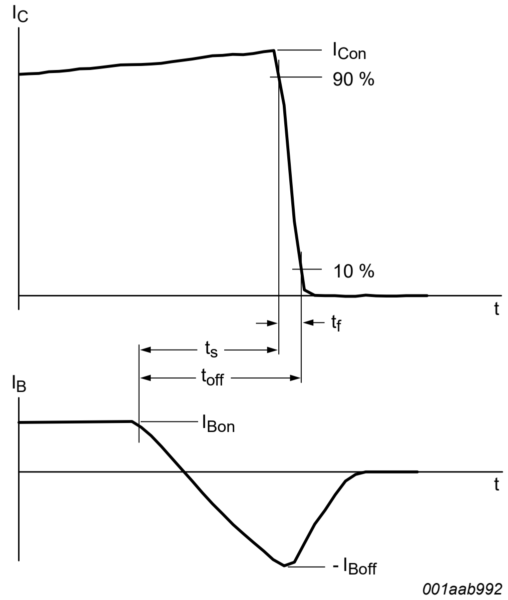
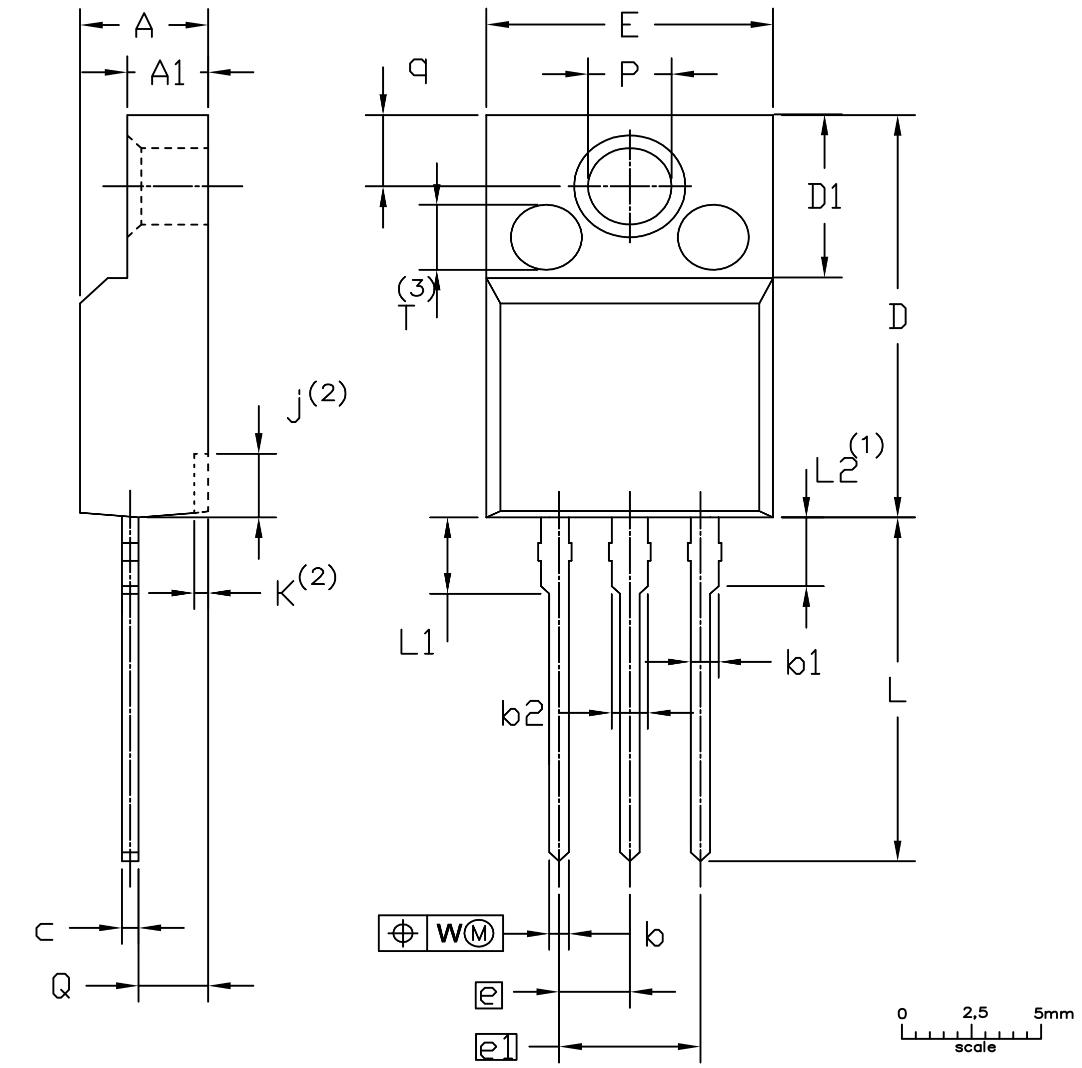


Fig. 15. Switching times waveforms for inductive load

10. Package outline

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack" SOT186A



UNIT	A	A_1	b	b_1	b_2	c	D	D_1	E	e	e_1	j(2)	k(2)	L	L_1	L_2(1) max.	P	Q	q	W	T(3)
mm	4.6 4.0	2.9 2.5	0.9 0.7	1.1 0.9	1.4 1.0	0.7 0.4	15.8 15.2	6.5 6.3	10.3 9.7	2.54	5.08	2.7 1.7	0.6 0.4	14.4 13.5	3.30 2.79	3	3.2 3.0	2.6 2.3	3.0 2.6	0.4	2.5

Notes
1. Terminal dimensions within this zone are uncotrolled
2. Dot lines area designs may vary
3. Eject pin mark is for reference only

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT186A		3 LEADS TO220F				2013-11-14

Fig. 16. Package outline TO-220F (SOT186A)

11. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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12. Contents

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