

## 1. General description

Planar passivated high commutation three quadrant triac in a SOT186A (TO-220F) "full pack" plastic package. This "series D" triac balances the requirements of commutation performance and gate sensitivity and is intended for interfacing with low power drivers and logic ICs including microcontrollers.

## 2. Features and benefits

- 3Q technology for improved noise immunity
- Direct gate triggering from low power drivers and logic ICs
- High commutation capability with maximum false trigger immunity
- High voltage capability
- Isolated mounting base package
- Planar passivated for voltage ruggedness and reliability
- Triggering in three quadrants only
- Very sensitive gate for easy logic level triggering

## 3. Applications

- AC solenoids
- General purpose motor control circuits
- Home appliances

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	-	600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 92\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	-	4	A
$I_{TSM}$	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	-	-	25	A
		full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 16.7\text{ ms}$	-	-	27	A
$T_j$	junction temperature		-	-	125	$^{\circ}\text{C}$
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_2 + G+$ ; $T_j = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 7</a>	-	-	5	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$ ; Fig. 7	-	-	5	mA
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G-; $T_j = 25\text{ }^\circ\text{C}$ ; Fig. 7	-	-	5	mA
$I_H$	holding current	$V_D = 12\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; Fig. 9	-	-	6	mA
$V_T$	on-state voltage	$I_T = 5\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; Fig. 10	-	1.4	1.7	V
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit	20	-	-	V/ $\mu\text{s}$
$dI_{com}/dt$	rate of change of commutating current	$V_D = 400\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; $I_{T(RMS)} = 4\text{ A}$ ; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$ ; (snubberless condition); gate open circuit	1.5	-	-	A/ms

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 <p>TO-220F (SOT186A)</p>	
2	T2	main terminal 2		
3	G	gate		
mb	n.c.	mounting base; isolated		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BTA204X-600D	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

7. Limiting values

Table 4. Limiting values  
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DRM</sub>	repetitive peak off-state voltage		-	600	V
I <sub>T(RMS)</sub>	RMS on-state current	full sine wave; T <sub>h</sub> ≤ 92 °C; Fig. 1; Fig. 2; Fig. 3	-	4	A
I <sub>TSM</sub>	non-repetitive peak on-state current	full sine wave; T <sub>j(init)</sub> = 25 °C; t <sub>p</sub> = 20 ms; Fig. 4; Fig. 5	-	25	A
		full sine wave; T <sub>j(init)</sub> = 25 °C; t <sub>p</sub> = 16.7 ms	-	27	A
I <sup>2</sup> t	I <sup>2</sup> t for fusing	t <sub>p</sub> = 10 ms; SIN	-	3.1	A <sup>2</sup> s
di <sub>T</sub> /dt	rate of rise of on-state current	I <sub>G</sub> = 0.2 A	-	100	A/μs
I <sub>GM</sub>	peak gate current		-	2	A
P <sub>GM</sub>	peak gate power		-	5	W
P <sub>G(AV)</sub>	average gate power	over any 20 ms period	-	0.5	W
T <sub>stg</sub>	storage temperature		-40	150	°C
T <sub>j</sub>	junction temperature		-	125	°C

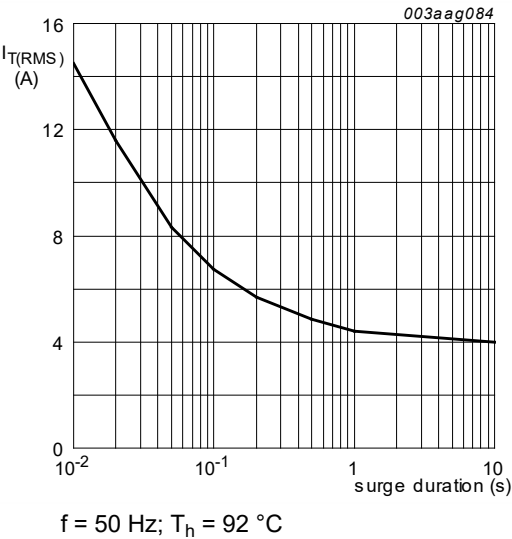


Fig. 1. RMS on-state current as a function of surge duration; maximum values

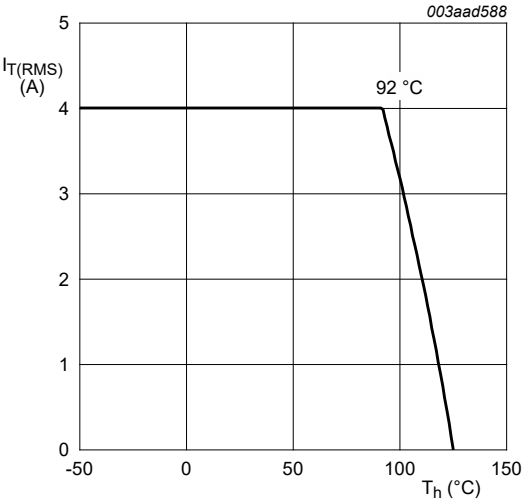


Fig. 2. RMS on-state current as a function of heatsink temperature; maximum values

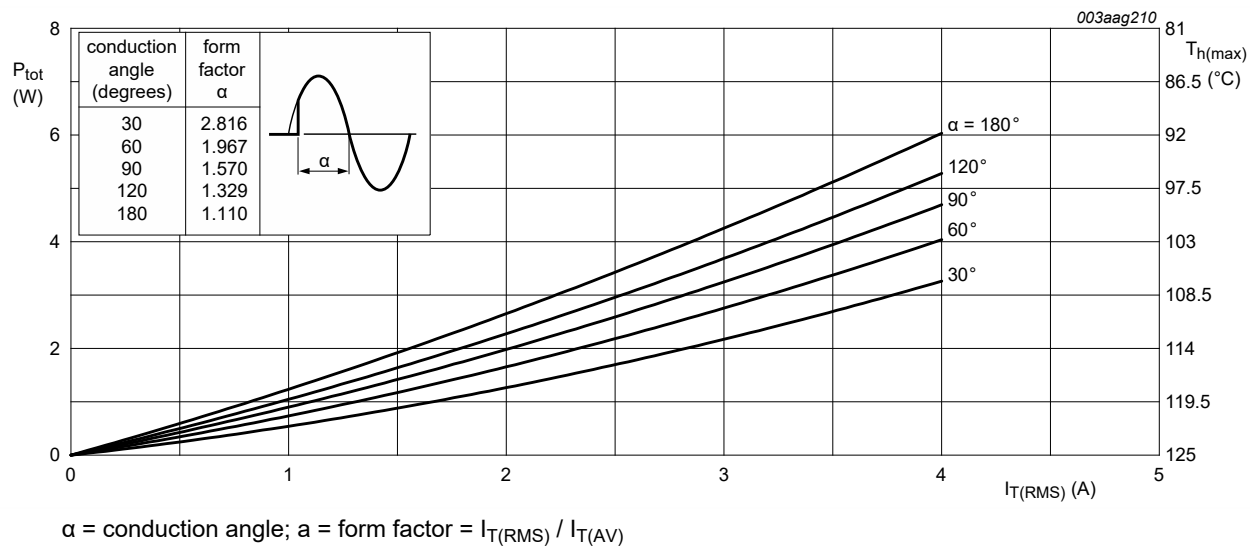


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

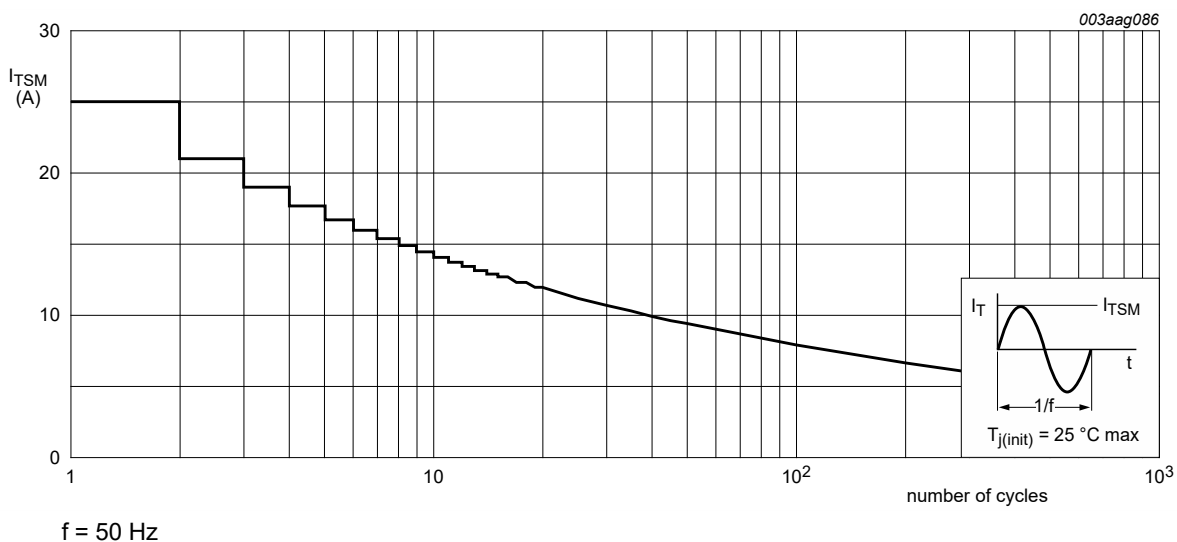
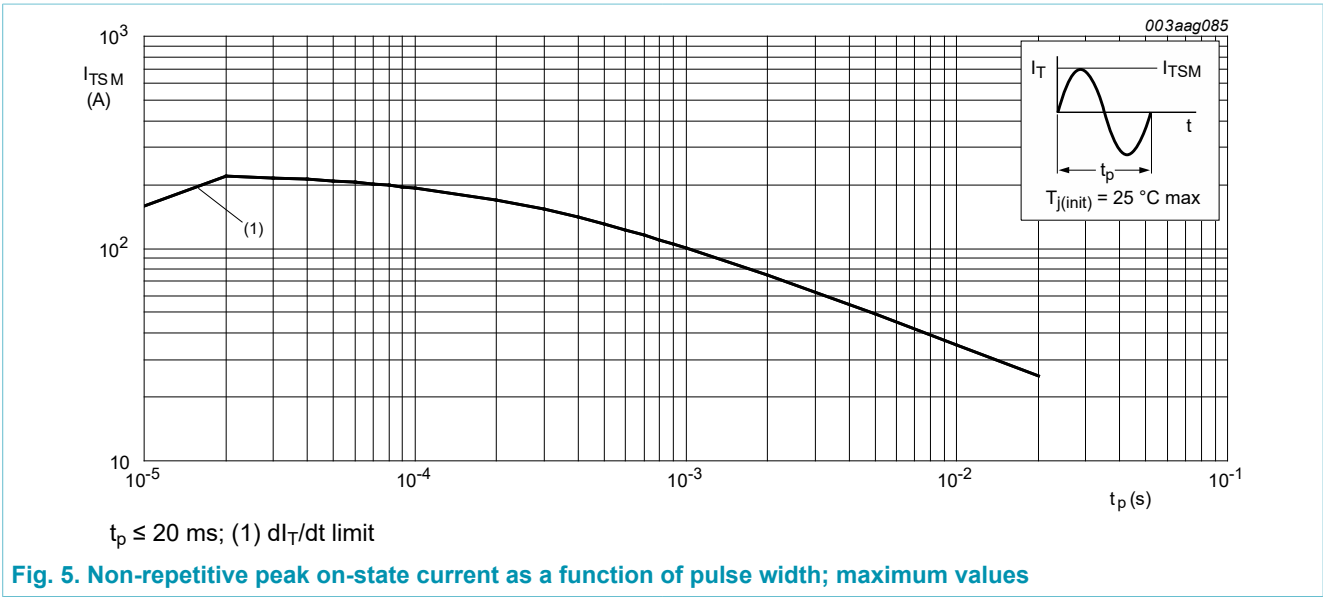


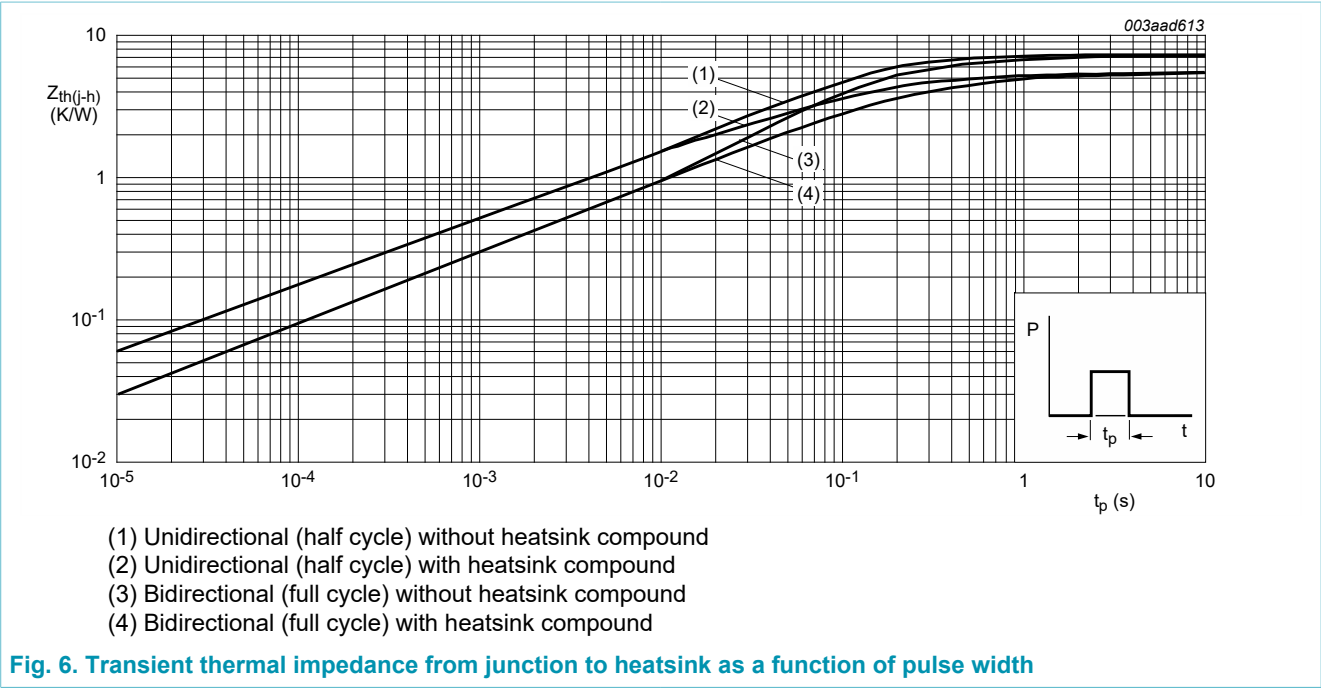
Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R <sub>th(j-h)</sub>	thermal resistance from junction to heatsink	full cycle or half cycle; with heatsink compound; Fig. 6		-	-	5.5	K/W
		full cycle or half cycle; without heatsink compound; Fig. 6		-	-	7.2	K/W
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient free air	in free air		-	55	-	K/W



9. Isolation characteristics

Table 6. Isolation characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V <sub>isol(RMS)</sub>	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; 50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; T <sub>h</sub> = 25 °C		-	-	2500	V
C <sub>isol</sub>	isolation capacitance	from main terminal 2 to external heatsink; f = 1 MHz; T <sub>h</sub> = 25 °C		-	10	-	pF

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>	-	-	5	mA
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>	-	-	5	mA
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G-; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>	-	-	5	mA
$I_L$	latching current	$V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>	-	-	6	mA
		$V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>	-	-	9	mA
		$V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2- G-; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>	-	-	6	mA
$I_H$	holding current	$V_D = 12\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 9</a>	-	-	6	mA
$V_T$	on-state voltage	$I_T = 5\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 10</a>	-	1.4	1.7	V
$V_{GT}$	gate trigger voltage	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 11</a>	-	0.7	1	V
		$V_D = 400\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; <a href="#">Fig. 11</a>	0.25	0.4	-	V
$I_D$	off-state current	$V_D = 600\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$	-	0.1	0.5	mA
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit	20	-	-	V/ $\mu\text{s}$
$dI_{com}/dt$	rate of change of commutating current	$V_D = 400\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; $I_{T(RMS)} = 4\text{ A}$ ; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$ ; (snubberless condition); gate open circuit	1.5	-	-	A/ms

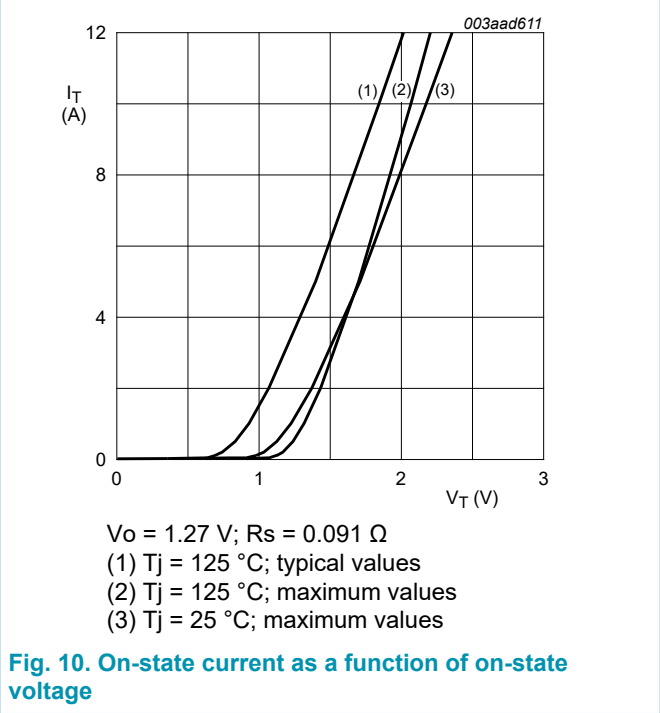
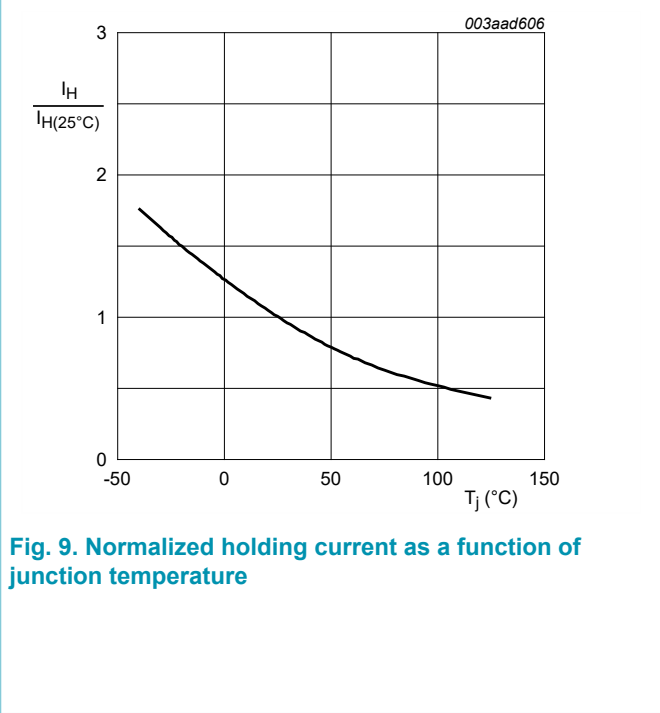
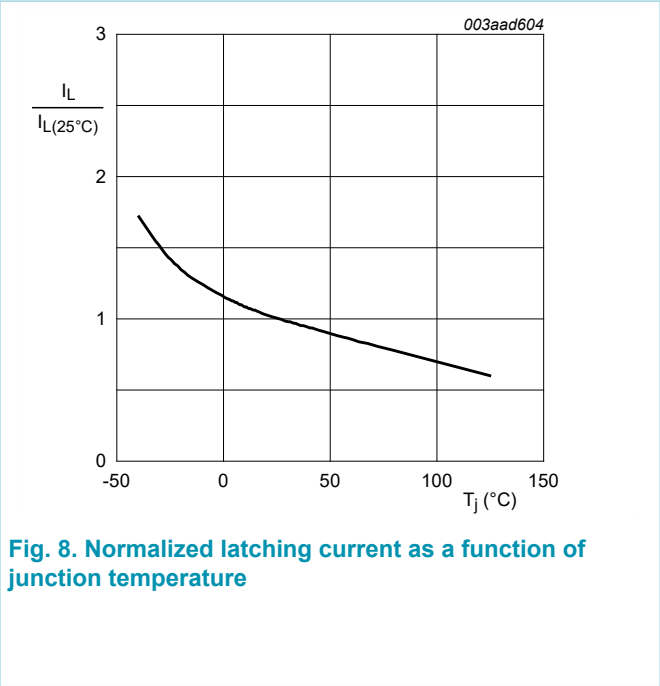
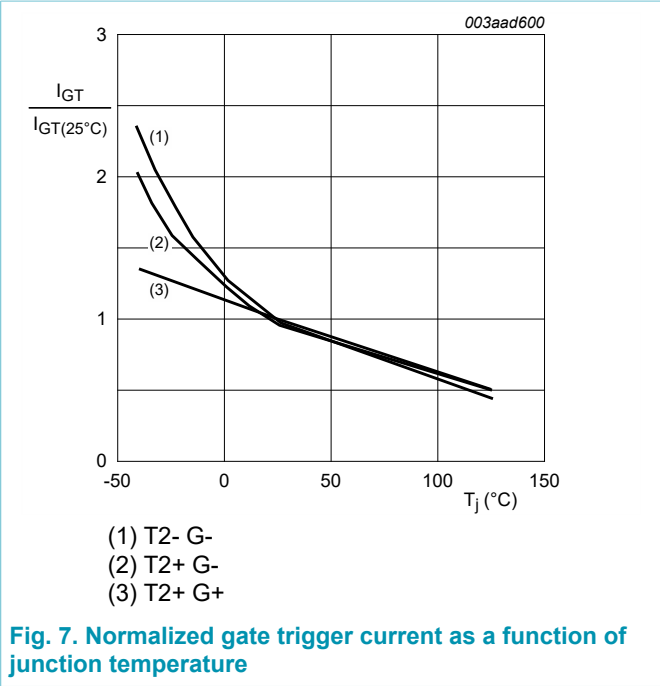






Fig. 11. Normalized gate trigger voltage as a function of junction temperature

11. Package outline



Fig. 12. Package outline TO-220F (SOT186A)

## 12. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Date of release: 19 September 2018

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