**Product data sheet** 

## 1. General description

Planar passivated high commutation three quadrant triac in a SOT186A (TO-220F) "full pack" plastic package intended for use in circuits where high static and dynamic dV/dt and high dl/dt can occur. This "series BT" triac will commutate the full RMS current at the maximum rated junction temperature ( $T_{j(max)}$  = 150 °C) without the aid of a snubber. It is used in applications where "high junction operating temperature capability" is required.

#### 2. Features and benefits

- · 3Q technology for improved noise immunity
- 2500 V RMS isolation voltage capability
- High commutation capability with maximum false trigger immunity
- High immunity to false turn-on by dV/dt
- High junction operating temperature capability
- High voltage capability
- · High current capability
- · Isolated mounting base package
- · Least sensitive gate for highest noise immunity
- · Planar passivated for voltage ruggedness and reliability
- Triggering in three quadrants only

## 3. Applications

- · Applications subject to high temperature
- Heating controls
- High power motor control
- · High power switching

### 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{DRM}$	repetitive peak off- state voltage		-	-	800	V
I <sub>T(RMS)</sub>	RMS on-state current	full sine wave; $T_h \le 44 ^{\circ}\text{C}$ ; Fig. 1; Fig. 2; Fig. 3	-	-	30	Α
I <sub>TSM</sub>	non-repetitive peak on- state current	full sine wave; $T_{j(init)} = 25 \text{ °C}$ ; $t_p = 20 \text{ ms}$ ; Fig. 4; Fig. 5	-	-	270	Α
		full sine wave; $T_{j(init)} = 25 \text{ °C}$ ; $t_p = 16.7 \text{ ms}$	-	-	297	Α
Tj	junction temperature		-	-	150	°C

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Static chara	acteristics		1				
leт	gate trigger current	V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T2+ G+; T <sub>j</sub> = 25 °C; <u>Fig. 7</u>		-	-	50	mA
		V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T2+ G-; T <sub>j</sub> = 25 °C; <u>Fig. 7</u>		-	-	50	mA
		V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T2- G-; T <sub>j</sub> = 25 °C; <u>Fig. 7</u>		-	-	50	mA
I <sub>H</sub>	holding current	V <sub>D</sub> = 12 V; T <sub>j</sub> = 25 °C; <u>Fig. 9</u>		-	-	75	mA
$V_{T}$	on-state voltage	I <sub>T</sub> = 42 A; T <sub>j</sub> = 25 °C; <u>Fig. 10</u>		-	1.2	1.55	V
Dynamic ch	naracteristics						
dV <sub>D</sub> /dt	rate of rise of off-state voltage	$V_{DM}$ = 536 V; $T_j$ = 150 °C; ( $V_{DM}$ = 67% of $V_{DRM}$ ); exponential waveform; gate open circuit		2000	-	-	V/µs
dI <sub>com</sub> /dt	rate of change of commutating current	$V_D$ = 400 V; $T_j$ = 150 °C; $I_{T(RMS)}$ = 30 A; $dV_{com}/dt$ = 20 V/ $\mu$ s; (snubberless condition); gate open circuit		15	-	-	A/ms

# 5. Pinning information

#### **Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	mb	T2
2	T2	main terminal 2		Sym051
3	G	gate		Symosi
mb	n.c.	mounting base; isolated		
			ŨŨŨ	
			1 2 3 TO-220F (SOT186A)	

# 6. Ordering information

**Table 3. Ordering information** 

Type number	Package					
	Name	Description	Version			
BTA330X-800BT	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A			

## 7. Limiting values

### **Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	800	V
I <sub>T(RMS)</sub>	RMS on-state current	full sine wave; $T_h \le 44 \text{ °C}$ ; $Fig. 1$ ; $Fig. 2$ ; $Fig. 3$	-	30	Α
I <sub>TSM</sub>	non-repetitive peak on- state current	full sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 20 ms; Fig. 4; Fig. 5	-	270	A
		full sine wave; T <sub>j(init)</sub> = 25 °C; t <sub>p</sub> = 16.7 ms	-	297	Α
l <sup>2</sup> t	I <sup>2</sup> t for fusing	t <sub>p</sub> = 10 ms; SIN	-	364.5	A²s
dl <sub>T</sub> /dt	rate of rise of on-state current	I <sub>G</sub> = 0.2 A	-	100	A/µs
I <sub>GM</sub>	peak gate current		-	2	Α
$P_{GM}$	peak gate power		-	5	W
P <sub>G(AV)</sub>	average gate power	over any 20 ms period	-	0.5	W
T <sub>stg</sub>	storage temperature		-40	150	°C
T <sub>j</sub>	junction temperature		-	150	°C

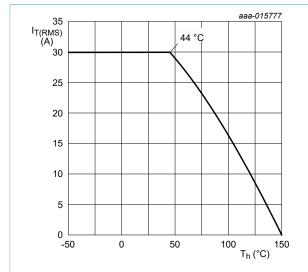


Fig. 1. RMS on-state current as a function of heatsink temperature; maximum values

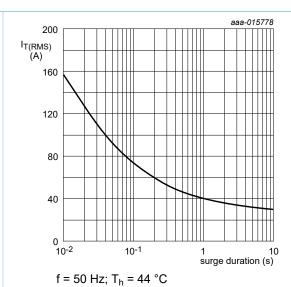


Fig. 2. RMS on-state current as a function of surge duration; maximum values

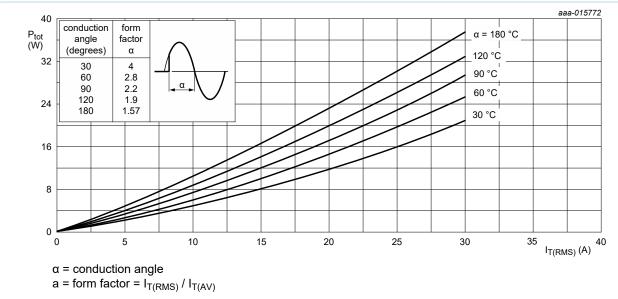


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

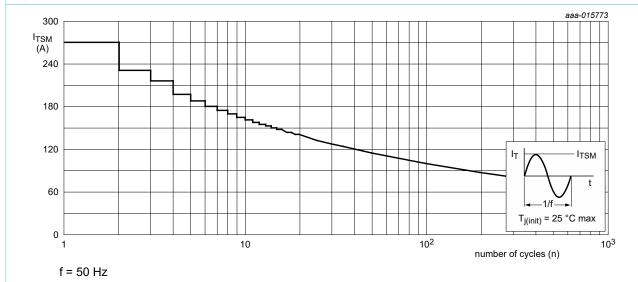
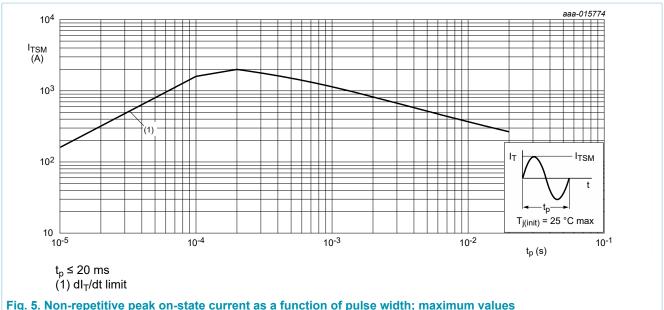


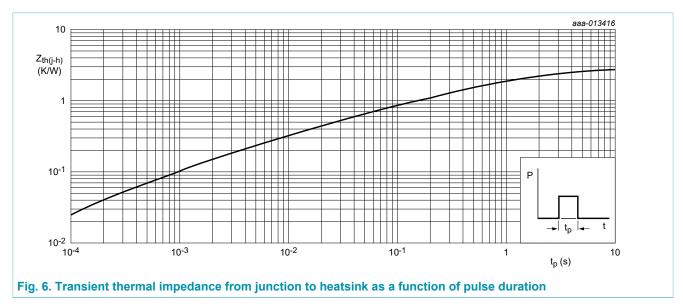
Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



### 8. Thermal characteristics

**Table 5. Thermal characteristics** 

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-h)</sub>	thermal resistance from junction to heatsink	full cycle; with heatsink compound; Fig. 6	-	-	2.8	K/W
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient free air	in free air	-	55	-	K/W



### 9. Isolation characteristics

**Table 6. Isolation characteristics** 

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>isol(RMS)</sub>	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; 50 Hz $\leq$ f $\leq$ 60 Hz; RH $\leq$ 65 %; T <sub>h</sub> = 25 °C	-	-	2500	V
C <sub>isol</sub>	isolation capacitance	from main terminal 2 to external heatsink; f = 1 MHz; T <sub>h</sub> = 25 °C	-	10	-	pF

## 10. Characteristics

#### **Table 7. Characteristics**

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics		,			,
I <sub>GT</sub>	gate trigger current	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ G+; $ $T_j = 25 \text{ °C}; Fig. 7$	-	-	50	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ \text{ G-};$ $T_j = 25 ^{\circ}\text{C}; \underline{\text{Fig. 7}}$	-	-	50	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2- \text{G-};$ $T_j = 25 \text{ °C}; \underline{\text{Fig. 7}}$	-	-	50	mA
I <sub>L</sub> latching current	latching current	$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; T2+ G+;$ $T_j = 25 \text{ °C}; Fig. 8$	-	-	80	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; T2+ G-;$ $T_j = 25 \text{ °C}; Fig. 8$	-	-	100	mA
	$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; \text{ T2- G-};$ $T_j = 25 ^{\circ}\text{C}; \text{ Fig. 8}$	-	-	80	mA	
Н	holding current	V <sub>D</sub> = 12 V; T <sub>j</sub> = 25 °C; <u>Fig. 9</u>	-	-	75	mA
V <sub>T</sub>	on-state voltage	I <sub>T</sub> = 42 A; T <sub>j</sub> = 25 °C; <u>Fig. 10</u>	-	1.2	1.55	V
V <sub>GT</sub>	gate trigger voltage	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T_j = 25 \text{ °C};$ Fig. 11	-	0.9	1.3	V
		V <sub>D</sub> = 400 V; I <sub>T</sub> = 0.1 A; T <sub>j</sub> = 150 °C; Fig. 11	0.2	0.45	-	V
D	off-state current	V <sub>D</sub> = 800 V; T <sub>j</sub> = 25 °C	-	0.4	10	μA
		V <sub>D</sub> = 800 V; T <sub>j</sub> = 150 °C	-	0.4	2	mA
Dynamic cl	naracteristics					
dV <sub>D</sub> /dt	rate of rise of off-state voltage	$V_{DM}$ = 536 V; $T_j$ = 150 °C; ( $V_{DM}$ = 67% of $V_{DRM}$ ); exponential waveform; gate open circuit	2000	-	-	V/µs
dl <sub>com</sub> /dt	rate of change of commutating current	$V_D$ = 400 V; $T_j$ = 150 °C; $I_{T(RMS)}$ = 30 A; $dV_{com}/dt$ = 20 V/µs; (snubberless condition); gate open circuit	15	-	-	A/ms

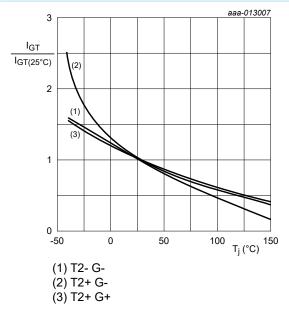


Fig. 7. Normalized gate trigger current as a function of junction temperature

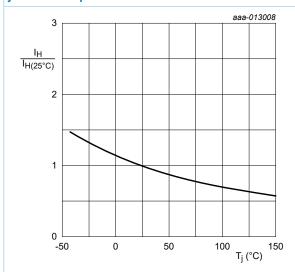


Fig. 9. Normalized holding current as a function of junction temperature

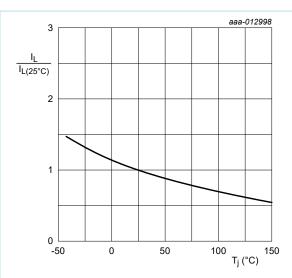
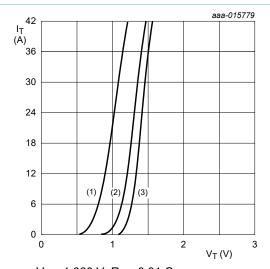
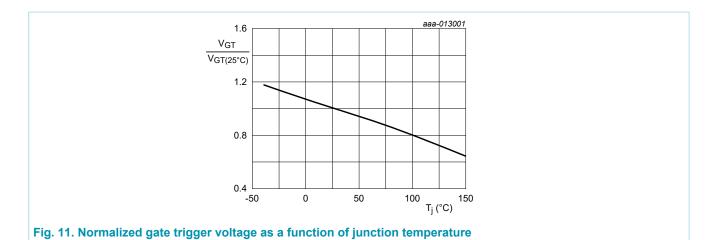


Fig. 8. Normalized latching current as a function of junction temperature



 $V_o$  = 1.060 V;  $R_s$  = 0.01 Ω (1)  $T_j$  = 150 °C; typical values (2)  $T_j$  = 150 °C; maximum values (3)  $T_j$  = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage



## 11. Package outline

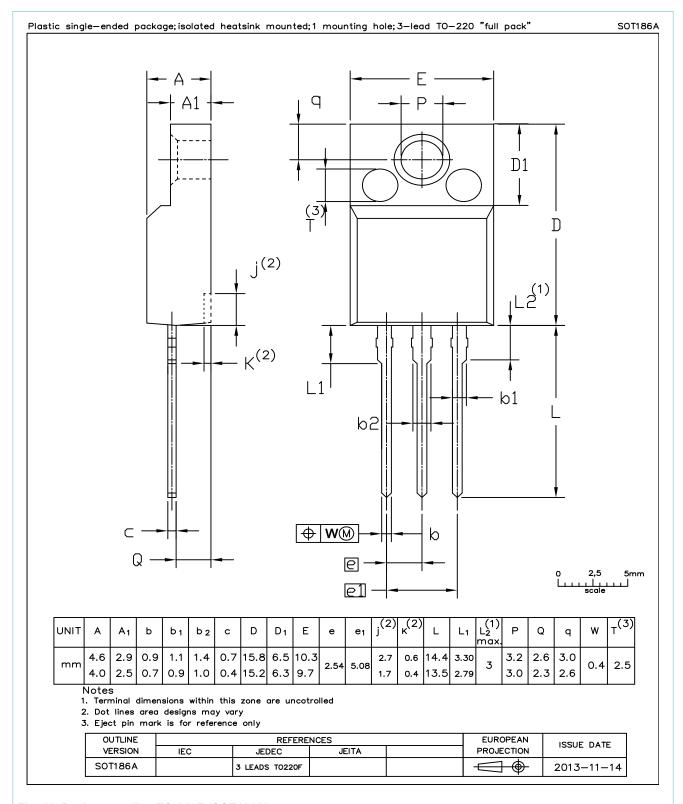


Fig. 12. Package outline TO-220F (SOT186A)

## 12. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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