DIO6912
High-Efficiency 2 A Continuous, 2.5 A Peak, 24 V Input Synchronous Step-Down Converter

Features

- Low $R_{DS(ON)}$ for internal switches (top/bottom) 130 mΩ/90 mΩ, 2.0 A DC current
- 4.5 ~ 24 V input voltage range
- High-efficiency synchronous-mode
- Internal soft start limits the inrush current
- Overcurrent protection
- Thermal shutdown
- Green package: SOT23-6 is pin compatible.

Applications

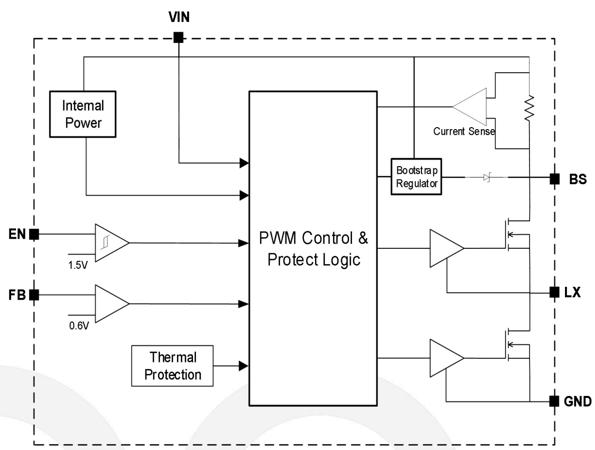
- Portable navigation device
- Set top box
- Portable TV
- LCD TV

Descriptions

The DIO6912 is high-efficiency, high frequency synchronous step-down DC-DC regulator ICs capable of delivering up to 2 A continuous output currents. The DIO6912 operates over a wide input voltage range from 4.5 V to 24 V and integrate main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The DIO6912 adopts the COT architecture to achieve fast transient responses for high step down applications and high efficiency at light loads. In addition, it operates at pseudo-constant frequency of 500 kHz under heavy load conditions to minimize the size of inductor and capacitor.

Function Block



Ordering Information

Ordering Part No.	Top Marking	MSL	RoHS	T_A	Package	
DIO6912ST6	12YW	3	Green	-40 to 85°C	SOT23-6	Tape & Reel, 3000

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Pin Assignments

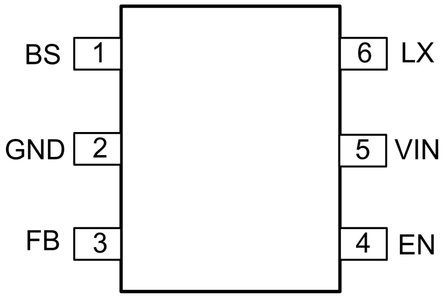

Figure 1. SOT23-6 (Top view)

Pin Definitions

Pin Name	Description
BS	Bootstrap. Connect a capacitor and a resistor between LX and BS pins to form a floating supply across the high-side switch driver. Recommend to use 0.1 μF BS capacitor.
GND	Power ground
FB	Output feedback pin. Connect this pin to the center point of the output resistor divider to program the output voltage: V_{OUT} = 0.6 × (1 + R1/R2). Add optional C2 (10 pF~47 pF) to speed up the transient response.
EN	Enable control. Pull high to turn on. Do not float.
VIN	Power input
LX	Inductor pin. Connect this pin to the switching node of inductor.

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Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maxim rating conditions for extended periods may affect device reliability.

Symbol	Parameter		Rating	Unit
V_{IN}	Supply voltage (V+ – V-)		28	V
$V_{EN, LX}$	EN, LX voltage		-0.3 to V_{IN} + 0.3	V
V_{FB}	FB voltage		-0.3 to 6	V
V_{LX}	LX pin voltage (15 ns transient)		-5 to 30	V
V_{BS}	BS Voltage		-0.3 to LX + 6	V
P_D	Power dissipation at T_A = 25°C		0.6	W
T_J	Junction temperature range		150	°C
T_L	Lead temperature		260	°C
T_{STG}	Storage temperature range		-65 to 150	°C
Θ_{JA}	Package thermal resistance		170	°C/W
Θ_{JC}			130	
HBM	JESD22-A114	VIN Pin	±1	kV
		Other Pins	±2	kV

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Rating	Unit
V_{IN}	Supply voltage	4.5 to 24	V
T_J	Junction temperature range	-40 to 125	°C
T_A	Ambient temperature range	-40 to 85	°C

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Electrical Characteristics

V_{IN} = 12 V, V_{OUT} = 1.2 V, L = 2.2 μH, C_{OUT} = 22 μF, T_A = 25°C, I_{OUT} = 1 A unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}(1)	Input voltage range		4.5		24	V
I_Q	Quiescent current	I_{OUT} = 0, V_{FB} = V_{REF} × 105%		140		μA
I_{SHDN}	Shutdown current	EN = 0		5	10	μA
V_{REF}	Feedback reference voltage		0.588	0.6	0.612	V
I_{FB}(1)	FB input current	V_{FB} = V_{IN}	-50		50	nA
$R_{DS(ON)1}$(1)	Top FET R_{ON}			130		mΩ
$R_{DS(ON)2}$(1)	Bottom FET R_{ON}			90		mΩ
I_{LIM}(1)	Bottom FET valley current limit		2.7			A
V_{ENH}	EN rising threshold	T_A = -40 to 85°C	1.5			V
V_{ENL}	EN falling threshold	T_A = -40 to 85°C			0.4	V
UVLOH	Under voltage lock out high			4.2	4.5	V
UVLOL	Under voltage lock out low			3.8	4	V
f_{SW}	Switching frequency			500		kHz
t_{ON}	ON time	V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 1 A		200		ns
	Min ON time(1)			50		ns
	Min OFF time(1)			100		ns
t_{SS}(1)	Soft start time			1		ms
T_{SD}(1)	Thermal shutdown temperature			150		°C
T_{HYS}(1)	Thermal shutdown hysteresis			15		°C

Note:

(1) Guaranteed by design.

(2) Specifications subject to change without notice.

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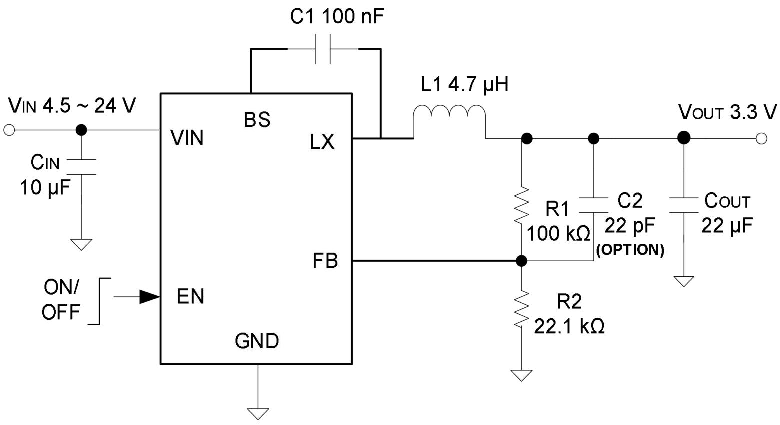
Typical Application



DIO6912 Recommended Table:

V_{OUT}(V)	R2(kΩ)	C2(pF)	L1/ Partnumber
1	150	Null	2.2μH/ SWPA4020S2R2NT (VLC60465T-2R2N)
1.2	100	Null	2.2μH/ SWPA4020S2R2NT (VLC60465T-2R2N)
1.8	49.9	Null	3.3μH/ SWPA6028S3R3NT (VLC60465T-3R3N)
2.5	31.6	Null	3.3μH/ SWPA6028S3R3NT (VLC60465T-3R3N)
3.3	22.1	22 (option)	4.7μH/ SWPA5040S4R7NT (VLC60465T-4R7M)
5	13.7	22 (option)	6.8μH/ SWPA6045S6R8MT (VLC60465T-6R8M)

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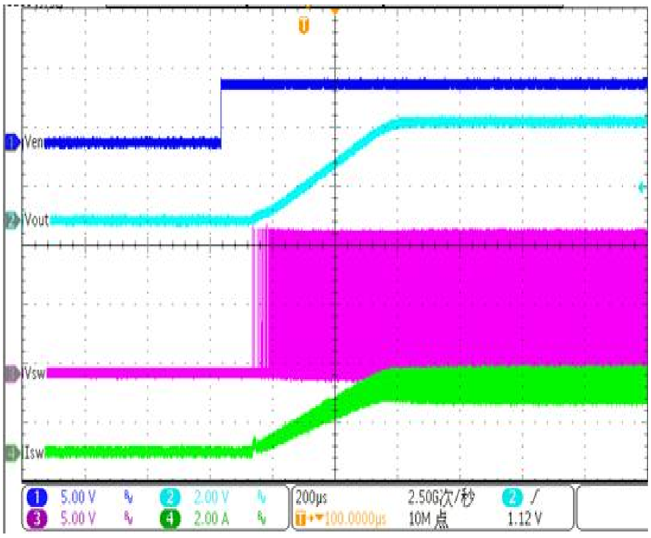
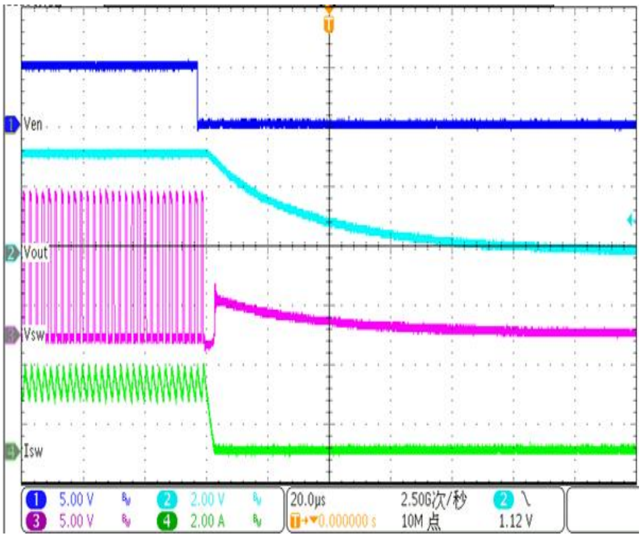
Typical Performance Characteristics



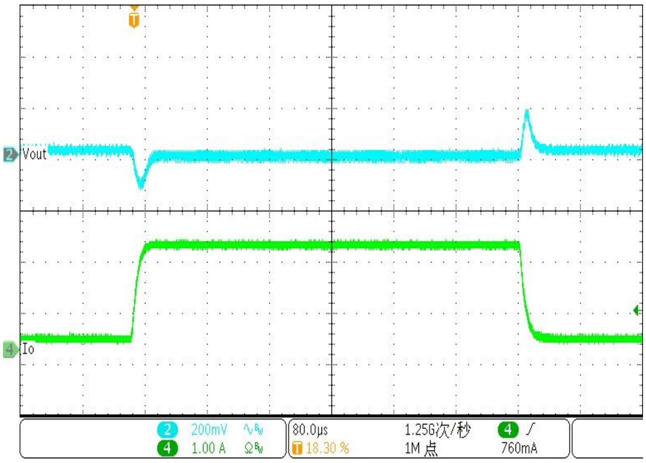
V_{IN} = 12 V, V_{OUT} = 3.3 V, Load = 1.5 Ω

Figure 2. Start up from enable



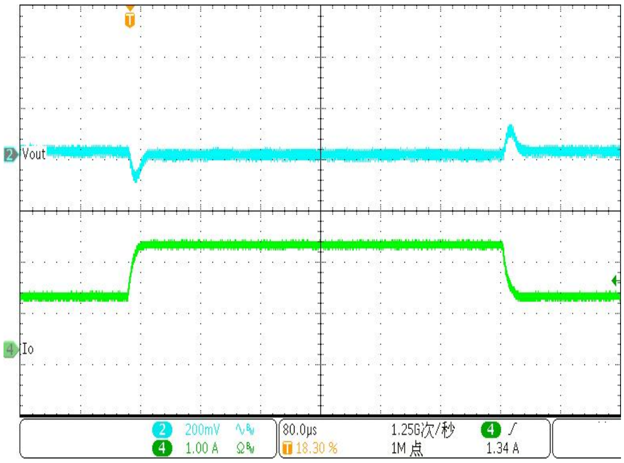
V_{IN} = 12 V, V_{OUT} = 3.3 V, Load = 1.5 Ω

Figure 3. Shut down from enable



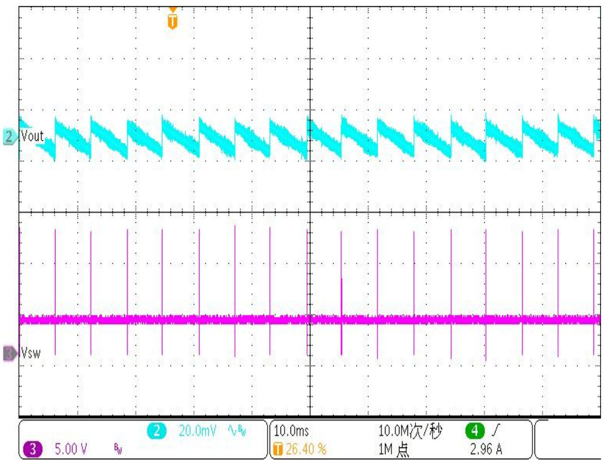
V_{IN} = 12 V, V_{OUT} = 3.3 V, Load = 0.2 ~ 2 A

Figure 4. Load transient



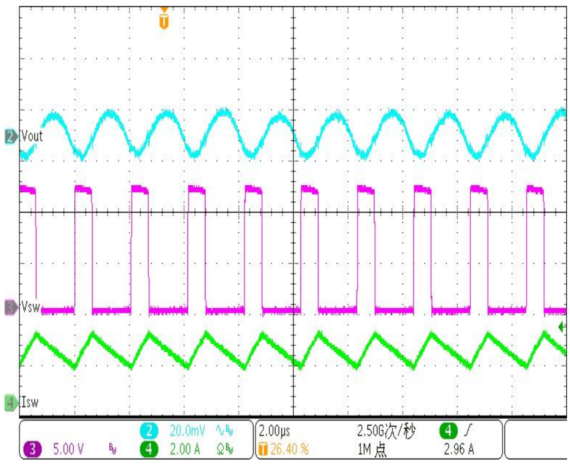
V_{IN} = 12 V, V_{OUT} = 3.3 V, Load = 1 ~ 2 A

Figure 5. Load transient



V_{IN} = 12 V, V_{OUT} = 3.3 V, Load = 0 A

Figure 6. Ripple



V_{IN} = 12 V, V_{OUT} = 3.3 V, Load = 2 A

Figure 7. Ripple

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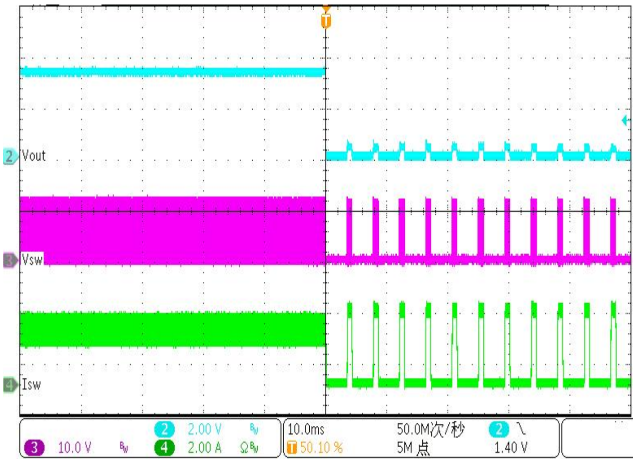
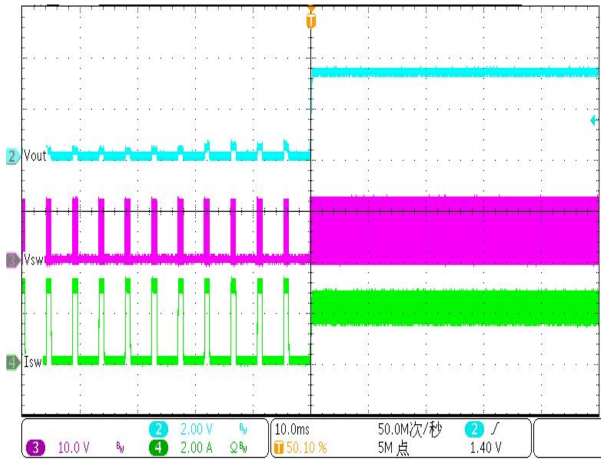


V_{IN} = 12 V, V_{OUT} = 3.3 V, Load = 2 A

Figure 8. Short circuit protection



V_{IN} = 12 V, V_{OUT} = 3.3 V, Load = 2 A

Figure 9. Short circuit recovery

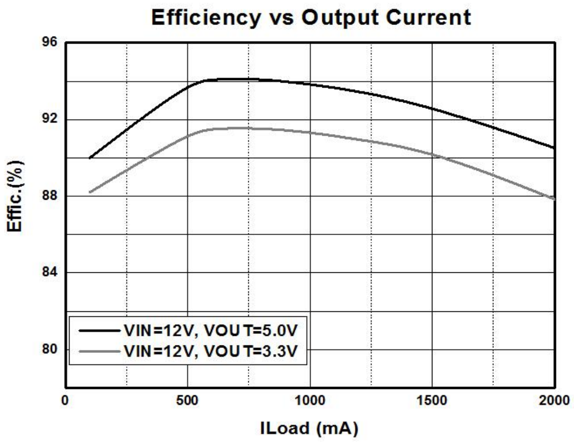


Figure 10. Efficiency vs. Output current

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Operation

The DIO6912 is a synchronous buck regulator IC that integrates the COT control, top and bottom switches on the same die to minimize the switching transition loss and conduction loss. With ultra low $R_{DS(ON)}$ power switches and proprietary COT control, this regulator IC can achieve the highest efficiency and the highest switch frequency simultaneously to minimize the external inductor and capacitor size, and thus achieving the minimum solution footprint.

The DIO6912 provides protection functions such as cycle by cycle current limiting and thermal shutdown protection. The DIO6912 will sense the output voltage conditions for the fault protection.

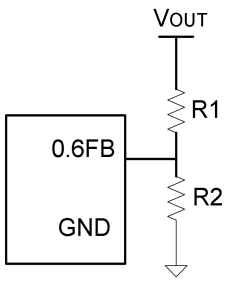
Applications Information

Because of the high integration in the DIO6912 IC, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L and feedback resistors (R1 and R2) need to be selected for the targeted applications specifications.

Feedback resistor dividers R1 and R2

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2. A value of between 10 kΩ and 1 MΩ is highly recommended for both resistors. If V_{OUT} is 3.3 V, R1 = 100 kΩ is chosen, then R2 can be calculated to be 22.1 kΩ.

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1 \quad (1)$$



Input capacitor C_{IN}

This ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D(1-D)} \quad (2)$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins. In this case, a 10 μF low ESR ceramic capacitor is recommended.

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Output capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor greater than 22 μF capacitance.

Output inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 40\%} \quad (3)$$

where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The DIO6912 regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

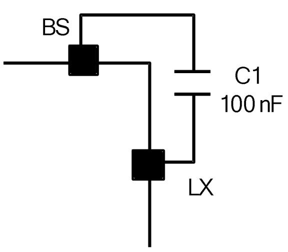
2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L} \quad (4)$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR < 50 mΩ to achieve a good overall efficiency.

External bootstrap cap

This capacitor provides the gate driver voltage for internal high side MOSFET. A 100 nF low ESR ceramic capacitor connected between BS pin and LX pin is recommended.



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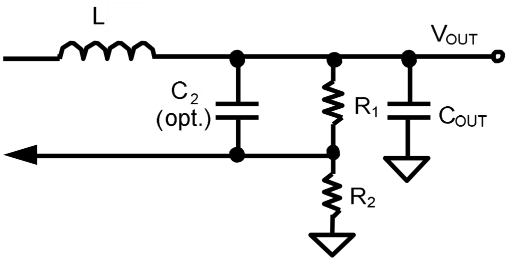
Load transient considerations

The DIO6912 regulator IC integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a 22 pF ceramic cap in parallel with R1 may further speed up the load transient responses and is thus recommended for applications with large load transient.



Layout design

The layout design of DIO6912 regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN}, L, R1 and R2.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.
2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.
3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.
4) The components R1 and R2, and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.
5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1MΩ resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

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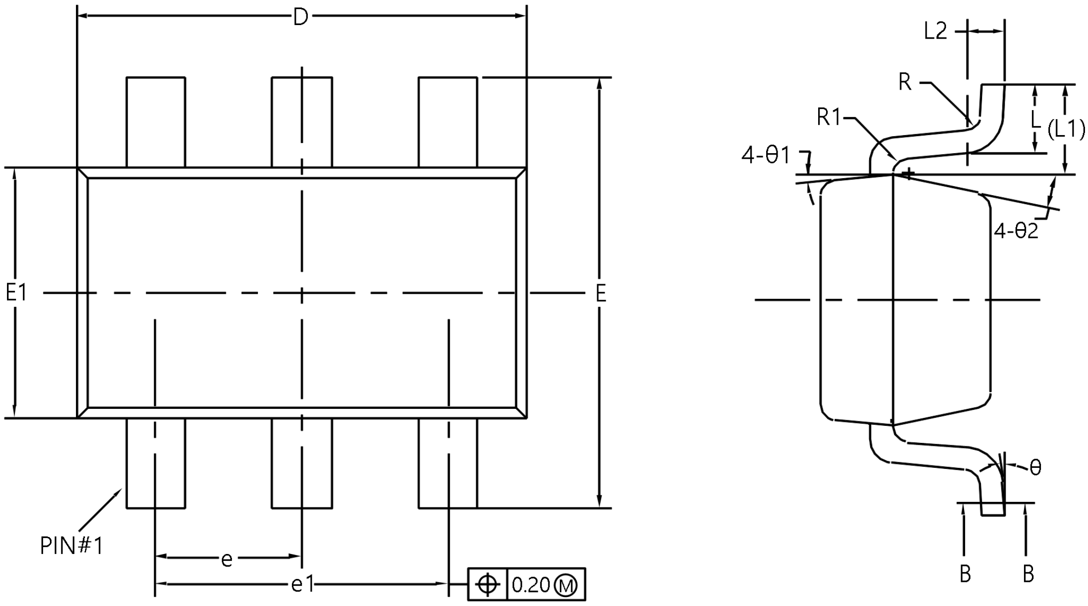
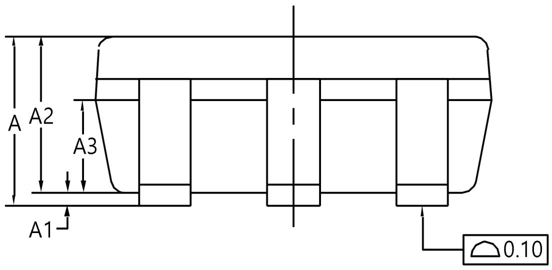
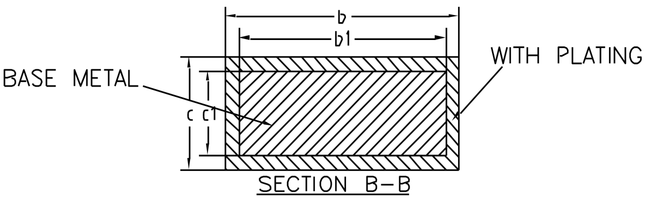
Physical Dimensions: SOT23-6







Common Dimensions (Units of measure = Millimeter)			
Symbol	Min	Nom	Max
A	-	-	1.25
A1	0	-	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.36	-	0.45
b1	0.35	0.38	0.41
c	0.14	-	0.20
c1	0.14	0.15	0.16
D	2.826	2.926	3.026
E	2.60	2.80	3.00
E1	1.526	1.626	1.726
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
L	0.30	0.40	0.60
L1	0.59 REF		
L2	0.25 BSC		
R	0.05	-	0.20
R1	0.05	-	0.20
Θ	0°	-	8°
Θ1	8°	10°	12°
Θ2	10°	12°	14°

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CONTACT US

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