DIO6182X/DIO6182XA

High-Efficiency, 2 A/3 A/4 A Output Synchronous Step-Down Converter with 1%

Features

- Low $R_{DS(ON)}$ for internal switches (25 mΩ)
- 2.5 V to 5.5 V input voltage range
- Adjustable output voltage application: 0.6 V to 5 V
- Low operating quiescent current: 10 μA
- 2 MHz typical switching frequency minimizes the external components
- Operation mode:
  - DIO6182X: Auto mode
  - DIO6182XA: Forced PWM operation
- High-efficiency for light load
- 100% duty cycle for lowest dropout
- Output discharge function
- Power good output indicator
- Protection:
  - Short circuit protection
  - Thermal shutdown protection
  - Overcurrent protection
- Package: 1.5 mm × 1.5 mm DFN-6

Applications

- IP network cameras
- Portable electronics
- Solid state drives
- Industrial PCs
- Multifunctional printers

Descriptions

The DIO6182X/DIO6182XA is a high-efficiency, high-frequency synchronous step-down DC-DC regulator IC capable of delivering up to 4 A output currents.

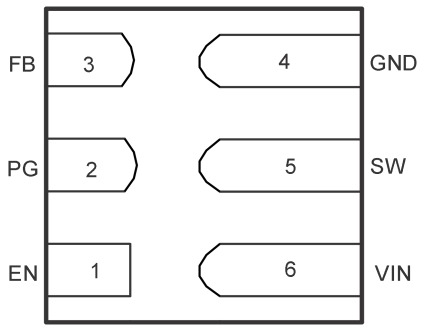
The DIO6182X operates in auto mode, which includes two modes, the PWM (Pulse Width Modulation) mode and the PSM (Power Save Mode) mode. The device operates in PWM mode for medium to heavy loads. In such conditions, the DIO6182X operates at a switching frequency of 2 MHz to minimize the size of the inductor and output capacitor. When the load current drops to light load conditions, the DIO6182X automatically enters PSM mode for high efficiency. The DIO6182XA operates in forced PWM, in which the device maintains continuous on mode operation and maintains extremely low output voltage ripple in the whole load range.

The DIO6182X/DIO6182XA has a fast transient response feature. The device operates over a wide input ranging from 2.5 V to 5.5 V with very low $R_{DS(ON)}$ to minimize the conduction loss. The DIO6182X/DIO6182XA can deliver an output down to 0.6 V with a feedback voltage of ±6 mV accuracy over -20°C to 85°C junction temperature.

Ordering Information

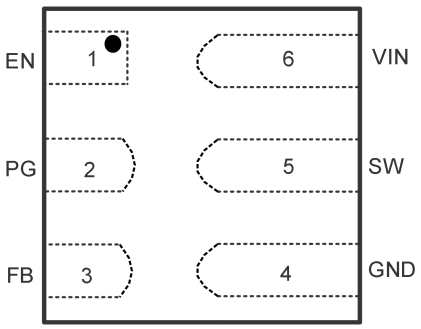
Part Number	Top Marking	MSL	Output Current	Operation Mode	RoHS	T_A	Package	
DIO61825CL6	2EYW	1	2A	Auto mode	Green	-40 to 85°C	DFN1.5*1.5-6	Tape & Reel, 3000
DIO61825CL6KS	2EYW	1	2A		Green	-40 to 85°C	DFN1.5*1.5-6	Tape & Reel, 3000
DIO61826CL6	2FYW	1	3A		Green	-40 to 85°C	DFN1.5*1.5-6	Tape & Reel, 3000
DIO61826CL6KS	2FYW	1	3A		Green	-40 to 85°C	DFN1.5*1.5-6	Tape & Reel, 3000
DIO61827CL6	2GYW	1	4A		Green	-40 to 85°C	DFN1.5*1.5-6	Tape & Reel, 3000
DIO61827CL6KS	2GYW	1	4A		Green	-40 to 85°C	DFN1.5*1.5-6	Tape & Reel, 3000
DIO61825ACL6	5AYW	1	2A	Forced PWM	Green	-40 to 85°C	DFN1.5*1.5-6	Tape & Reel, 3000
DIO61825ACL6KS	5AYW	1	2A		Green	-40 to 85°C	DFN1.5*1.5-6	Tape & Reel, 3000
DIO61826ACL6	6AYW	1	3A		Green	-40 to 85°C	DFN1.5*1.5-6	Tape & Reel, 3000
DIO61826ACL6KS	6AYW	1	3A		Green	-40 to 85°C	DFN1.5*1.5-6	Tape & Reel, 3000
DIO61827ACL6	7AYW	1	4A		Green	-40 to 85°C	DFN1.5*1.5-6	Tape & Reel, 3000
DIO61827ACL6KS	7AYW	1	4A		Green	-40 to 85°C	DFN1.5*1.5-6	Tape & Reel, 3000

Pin Assignment



DIO6182X/DIO6182XA

Figure 1. DFN 1.5*1.5-6 (Bottom view)



DIO6182X/DIO6182XA

Figure 2. DFN 1.5*1.5-6 (Top view)

Pin Descriptions

Pin No.	Pin Name	Description
1	EN	Enable control. Pull high to turn on. Do not leave it floating.
2	PG	Power-good open-drain output pin. The pull-up resistor can be connected to a voltage of up to 5.5 V. If the pin is unused, leave it floating.
3	FB	Output feedback pin. Connect this pin to the center point of the output resistor divider.
4	GND	Ground pin.
5	SW	Inductor pin. Connect this pin to the switching node of inductor.
6	VIN	Input voltage pin.

Absolute Maximum Ratings

Stresses beyond those listed under the Absolute Maximum Rating table may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Min	Max	Unit
VIN, FB, EN, PG	Input pin voltage	-0.3	6	V
SW (DC)	Output pin voltage	-0.3	VIN + 0.3	V
SW (DC, in current limit)	Output pin voltage	-1	VIN + 0.3	V
SW (AC, less than 10 ns)(2)	Output pin voltage	-2.5	10	V
T_J	Operating junction temperature	-40	150	°C
T_{STG}	Storage temperature	-65	150	°C
ESD	Human-body model (HBM)		±4000	V
	Charge-device model (CDM)		±2000	V

Note:

(1) All voltage values are with respect to the network ground terminal

(2) While switching

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. Does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Input voltage range	2.5		5.5	V
V_{OUT}	Output voltage range	0.6		5.0	V
I_{OUT}	Output current range	0		4.0	A
T_J	Operating junction temperature	-40		125	°C
$R_{\theta JA}$	Junction-to-ambient thermal resistance		107.8		°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		24.2		°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		20.5		°C/W

DC Electrical Characteristics

T_J = -40°C to 125°C, and V_{IN} = 2.5 V to 5.5 V. Typical values are at T_J = 25°C and V_{IN} = 5 V, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
I_Q	Quiescent current	EN = High, no load, device not switching		10	18	μA
		EN = High, no load, FPWM devices		10		mA
I_{SD}	Shutdown current	EN = Low, T_J = -40°C to 85°C		0.15	0.5	μA
V_{UVLO}	Undervoltage lock out threshold	V_{IN} rising	2.2	2.35	2.48	V
	Undervoltage lock out hysteresis	V_{IN} falling		150		mV
T_{JSD}	Thermal shutdown threshold	T_J rising		150		°C
	Thermal shutdown hysteresis	T_J falling		20		°C
Logic interface EN						
V_{IH}	High-level threshold voltage	V_{IN} = 2.5 V to 5.5 V	1.0			V
V_{IL}	Low-level threshold voltage	V_{IN} = 2.5 V to 5.5 V			0.4	V
Soft-start, power good						
t_{SS}	Soft-start time	Time from EN high to 95% of V_{OUT} nominal		1.8		ms
V_{PG}	Power good lower threshold	V_{PG} rising, V_{FB} referenced to V_{FB} nominal		96		%
		V_{PG} falling, V_{FB} referenced to V_{FB} nominal		92		
	Power good upper threshold	V_{PG} rising, V_{FB} referenced to V_{FB} nominal		105		
		V_{PG} falling, V_{FB} referenced to V_{FB} nominal		110		
$V_{PG,OL}$	Low-level output voltage	I_{sink} = 1 mA			0.4	V
$I_{PG,LKG}$	Input leakage current into PG pin	V_{PG} = 5.0 V		0.01		μA
$t_{PG,DLY}$	Power good deglitch delay	PG rising edge		100		μs
		PG falling edge		20		
Output						
V_{FB}(1)	Feedback regulation voltage	2.5 V ≤ V_{IN} ≤ 5.5 V, T_J = -40°C to 125°C	591	600	609	mV
		2.5 V ≤ V_{IN} ≤ 5.5 V, T_J = -20°C to 85°C	594	600	606	mV
$I_{FB,LKG}$	Feedback input leakage current for adjustable output voltage	V_{FB} = 0.6 V		0.01		μA
I_{DIS}	Output discharge current	V_{SW} = 0.4 V; EN = Low		100		mA
$Load_{REG}$	Load regulation	I_{OUT} = 0.5 A to 2 A, V_{OUT} = 1.8 V		0.1		%/A
Power switch						
$R_{DS(on)}$	High-side FET on-resistance			26		mΩ
	Low-side FET on-resistance			25		mΩ

I_{LIM}	High-side FET switch current limit, DC	I_{OUT} = 2 A	2.7	3.1		A
	High-side FET switch current limit, DC	I_{OUT} = 3 A	3.7	4.3		A
	High-side FET switch current limit, DC	I_{OUT} = 4 A	5.4	6.4		A
f_{SW}	PWM switching frequency	I_{OUT} = 1 A, V_{OUT} = 1.8 V		2		MHz

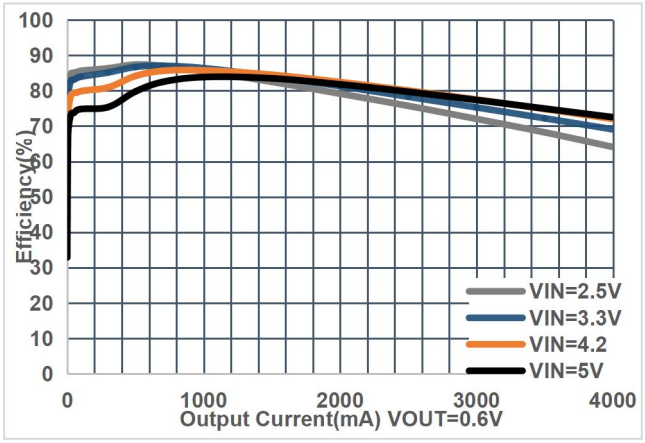
Note:

(1) Guaranteed by design.

(2) Specifications subject to change without notice.

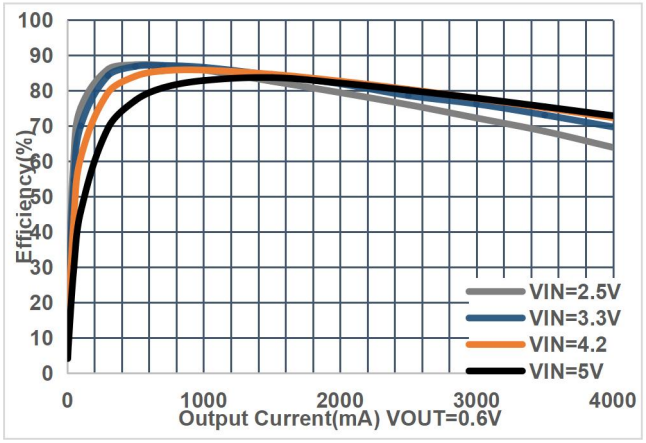
Typical Performance Characteristics

V_{IN} = 5 V, V_{OUT} = 1.8 V, C_{IN} = 10 µF, C_{OUT} = 3 × 10 µF, C_F = 120 pF, unless otherwise noted.



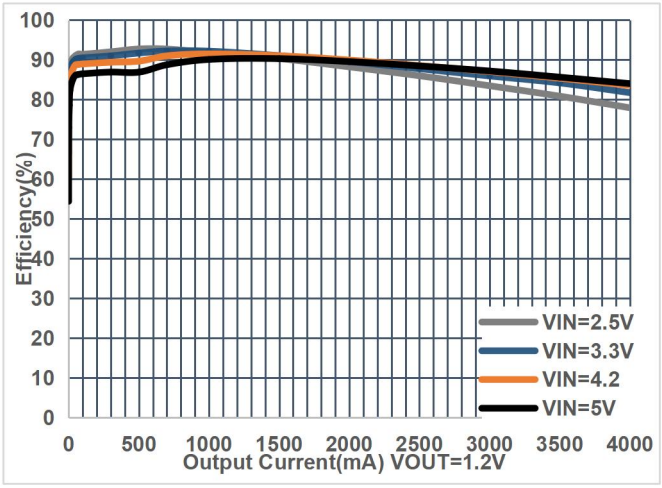
V_{OUT} = 0.6 V

Figure 3. Efficiency



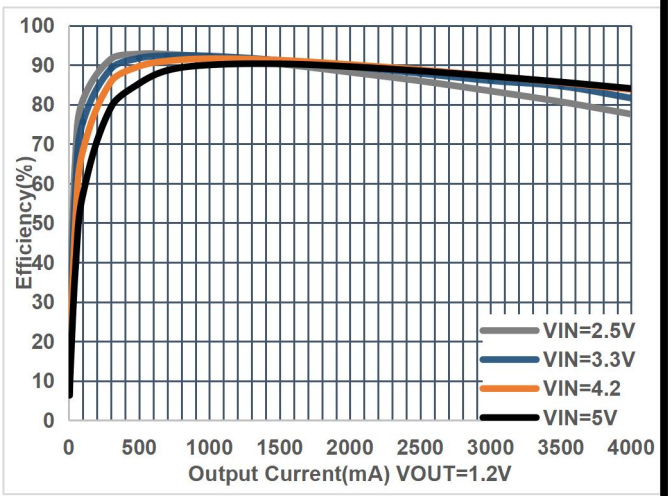
V_{OUT} = 0.6 V (FPWM devices)

Figure 4. Efficiency



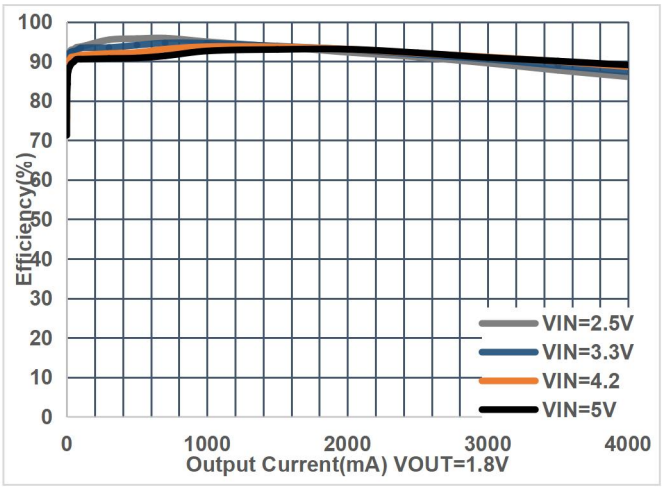
V_{OUT} = 1.2 V

Figure 5. Efficiency



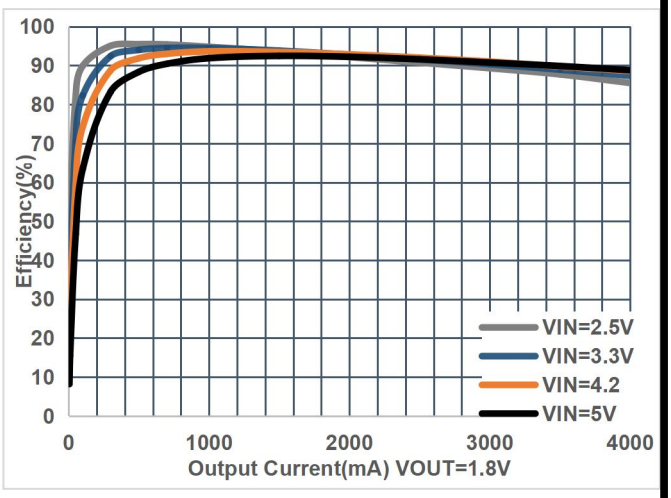
V_{OUT} = 1.2 V (FPWM devices)

Figure 6. Efficiency



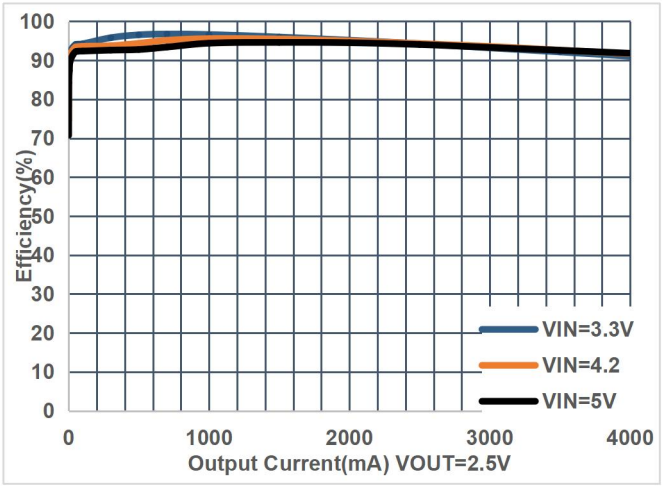
V_{OUT} = 1.8 V

Figure 7. Efficiency



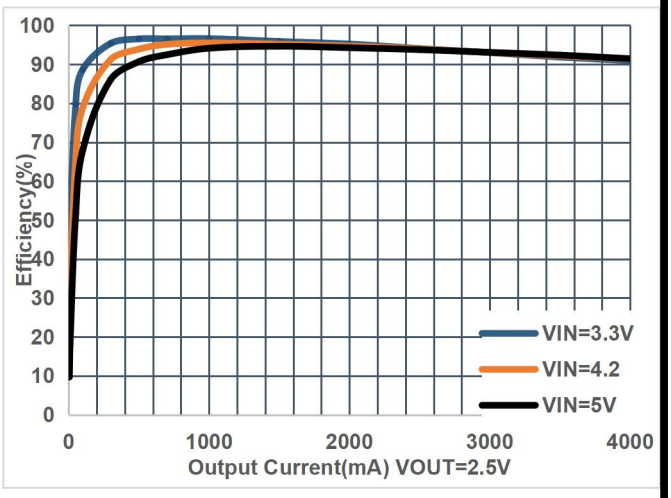
V_{OUT} = 1.8 V (FPWM devices)

Figure 8. Efficiency



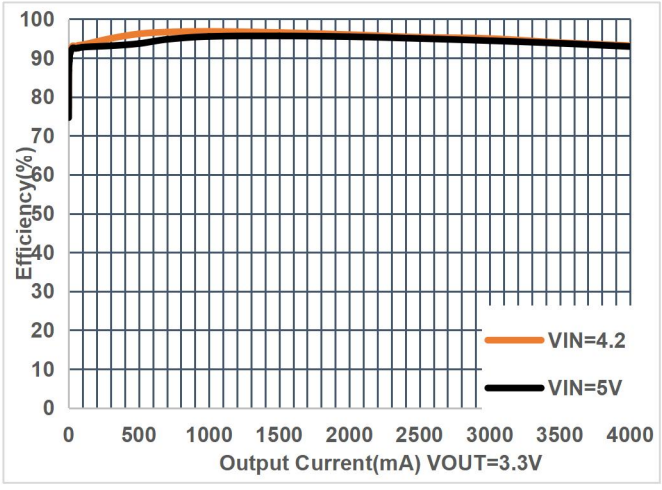
V_{OUT} = 2.5 V

Figure 9. Efficiency



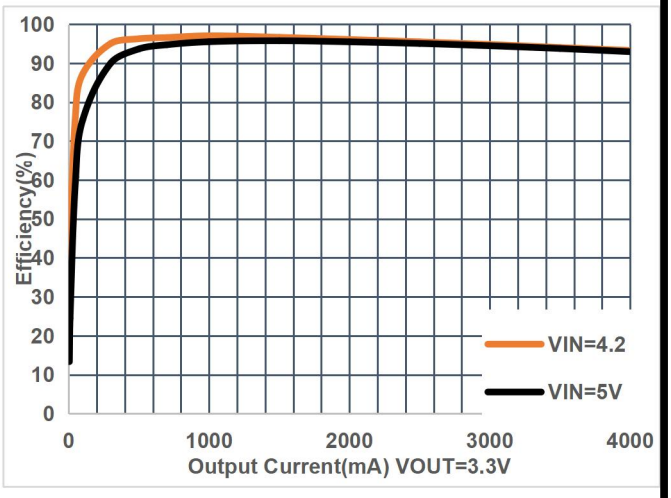
V_{OUT} = 2.5 V (FPWM devices)

Figure 10. Efficiency



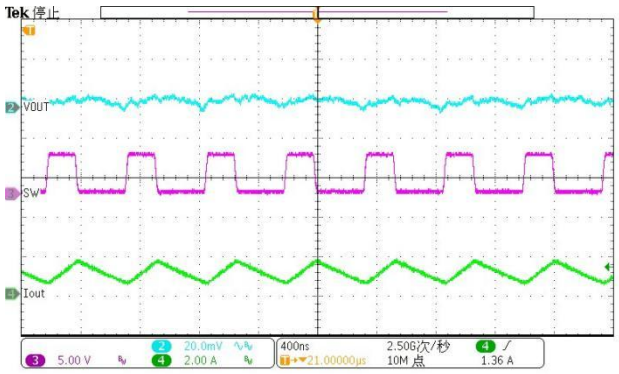
V_{OUT} = 3.3 V

Figure 11. Efficiency



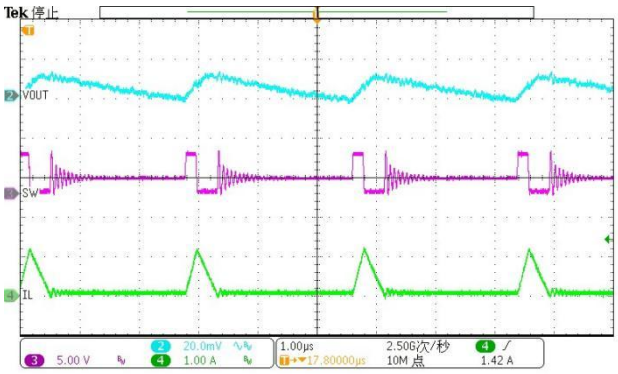
V_{OUT} = 3.3 V (FPWM devices)

Figure 12. Efficiency



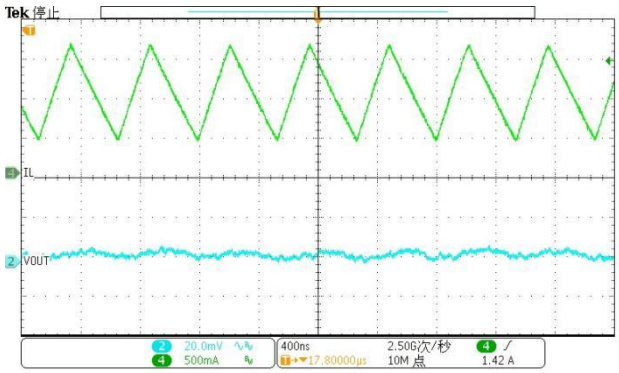
I_{OUT} = 1.0 A (DIO61825/6/7)

Figure 13. PWM operation



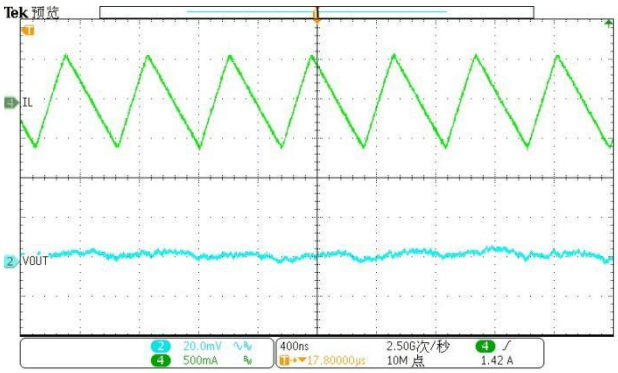
I_{OUT} = 0.1 A (DIO61825/6/7)

Figure 14. PSM operation



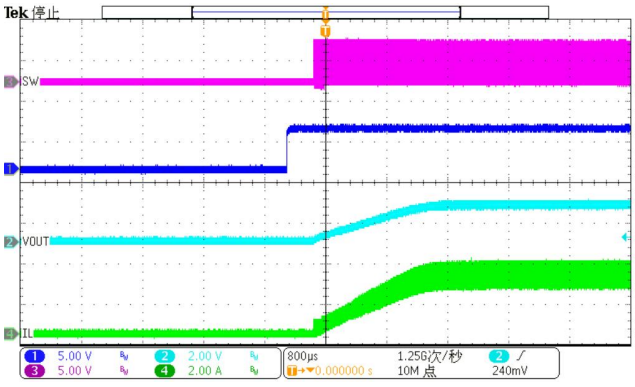
I_{OUT} = 1.0 A (DIO61825A/6A/7A)

Figure 15. PWM operation at FPWM



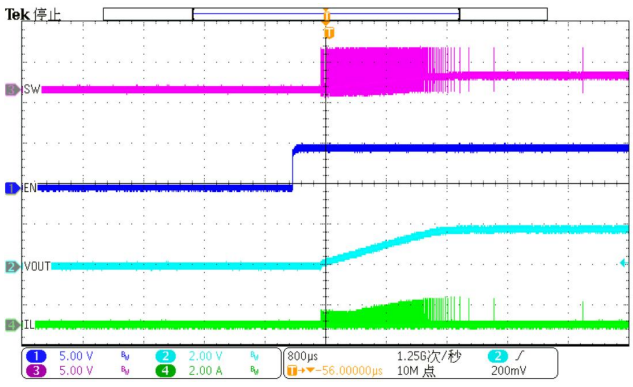
(DIO61825A/6A/7A)

Figure 16. PWM operation at FPWM without load



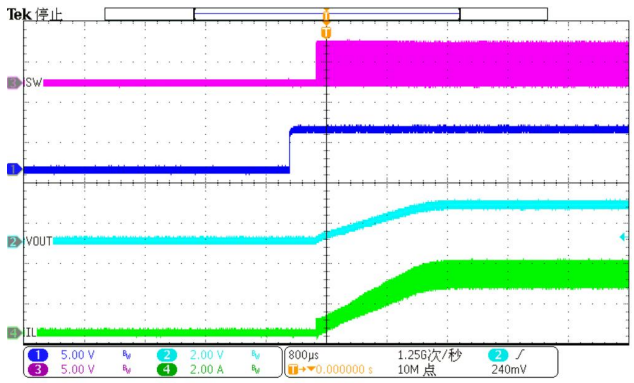
Load = 0.6 Ω (DIO61825/6/7)

Figure 17. Start-up with load



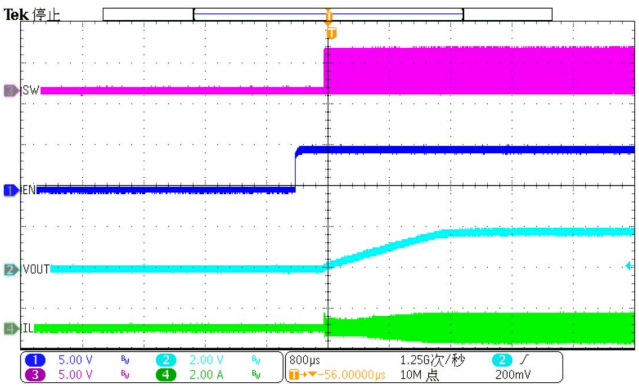
(DIO61825/6/7)

Figure 18. Start-up without load



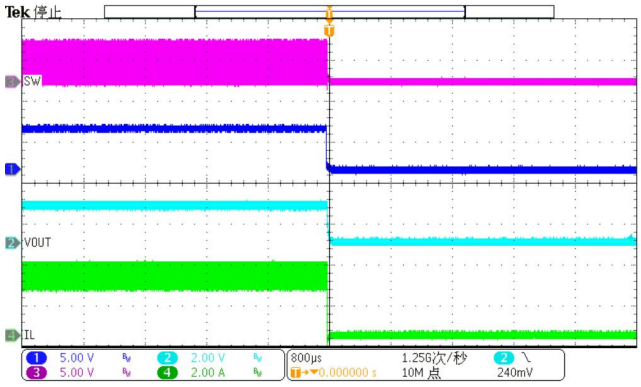
Load = 0.6 Ω (DIO61825A/6A/7A)

Figure 19. Start-up with load



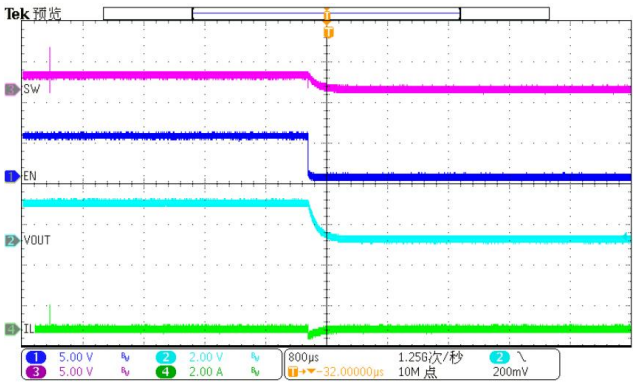
(DIO61825A/6A/7A)

Figure 20. Start-up without load



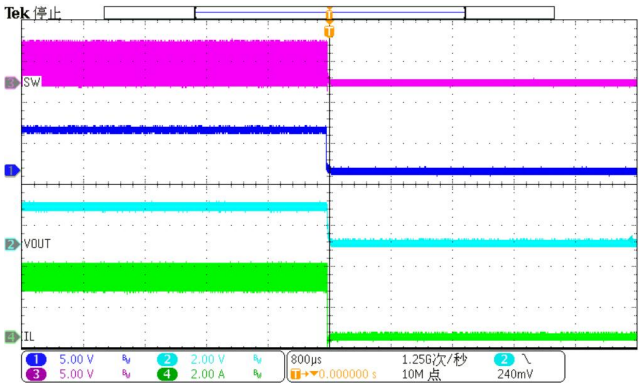
Load = 0.6 Ω (DIO61825/6/7)

Figure 21. Disable, active output discharge



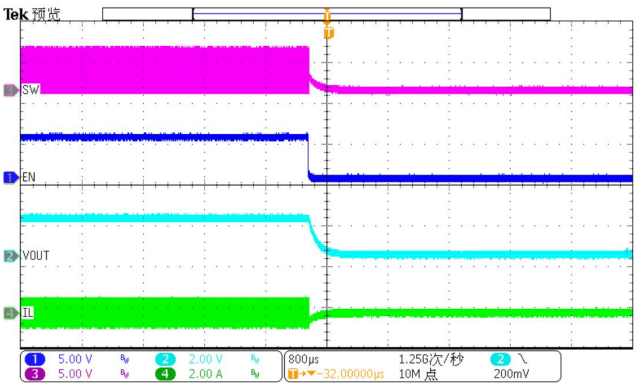
(DIO61825/6/7)

Figure 22. Disable, active output discharge without load



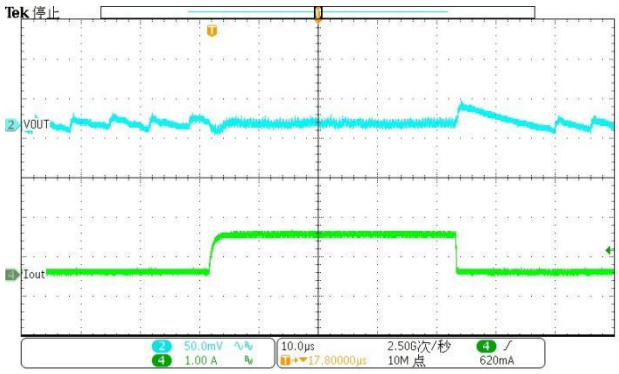
Load = 0.6 Ω (DIO61825A/6A/7A)

Figure 23. Disable, active output discharge



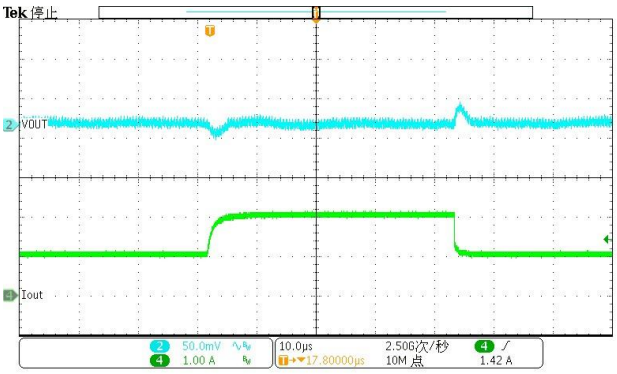
(DIO61825A/6A/7A)

Figure 24. Disable, active output discharge without load



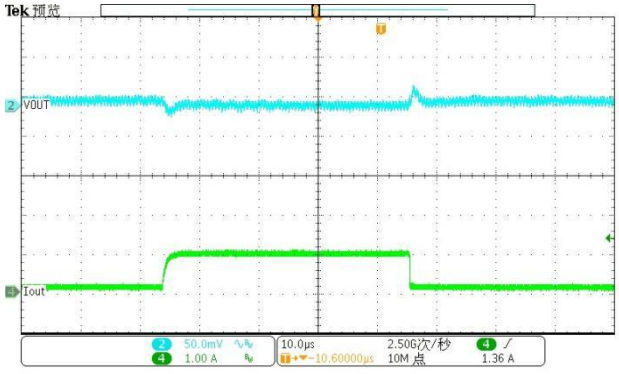
0.005 A -- 1 A (DIO61825/6/7)

Figure 25. Load transient



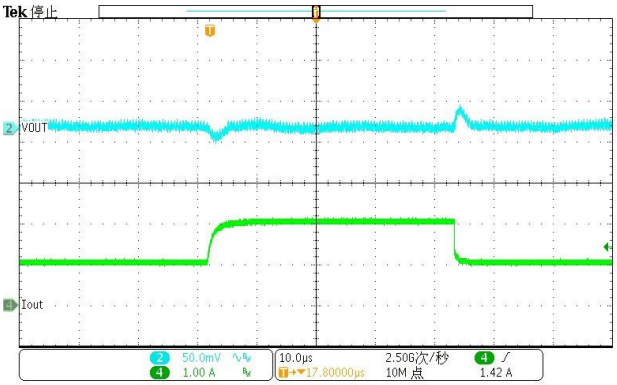
1 A -- 2 A (DIO61825/6/7)

Figure 26. Load transient



0.005 A -- 1 A (DIO61825A/6A/7A)

Figure 27. Load transient



1 A -- 2 A (DIO61825A/6A/7A)

Figure 28. Load transient

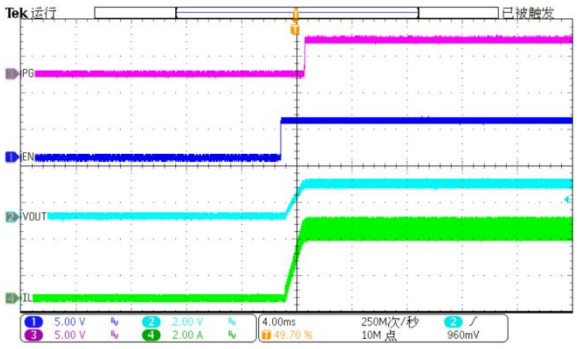


Figure 29. PG-start-up

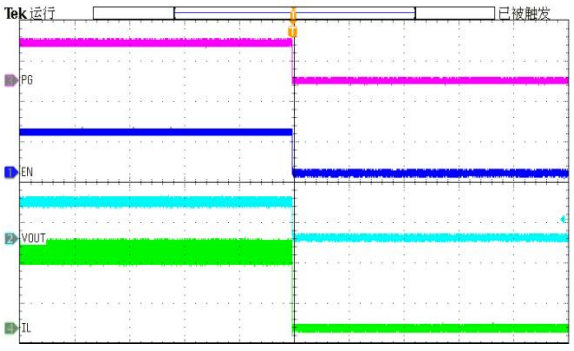


Figure 30. PG-discharge

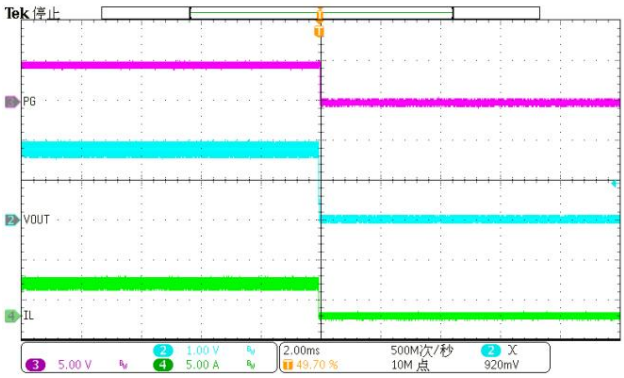


Figure 31. PG-OTP

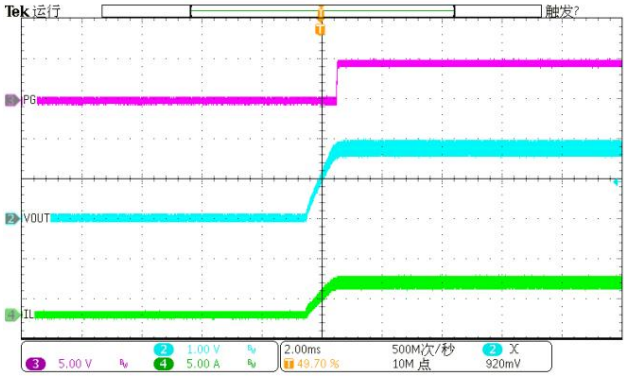


Figure 32. PG- OTP recovery

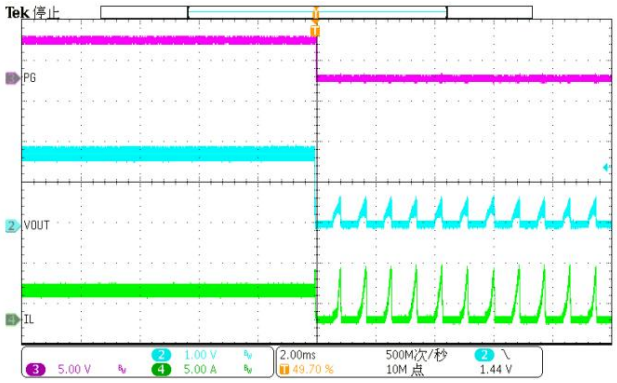


Figure 33. PG-SCP

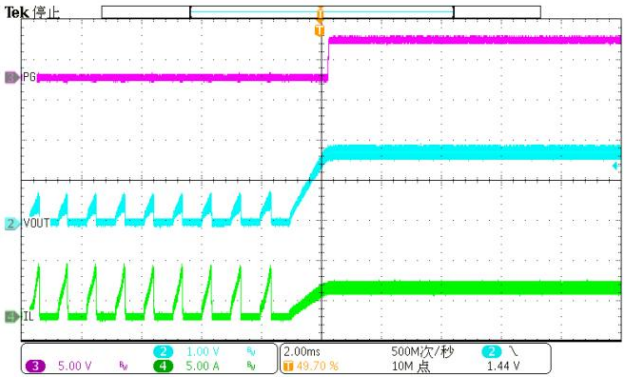


Figure 34. PG- SCP recovery

Block Diagram

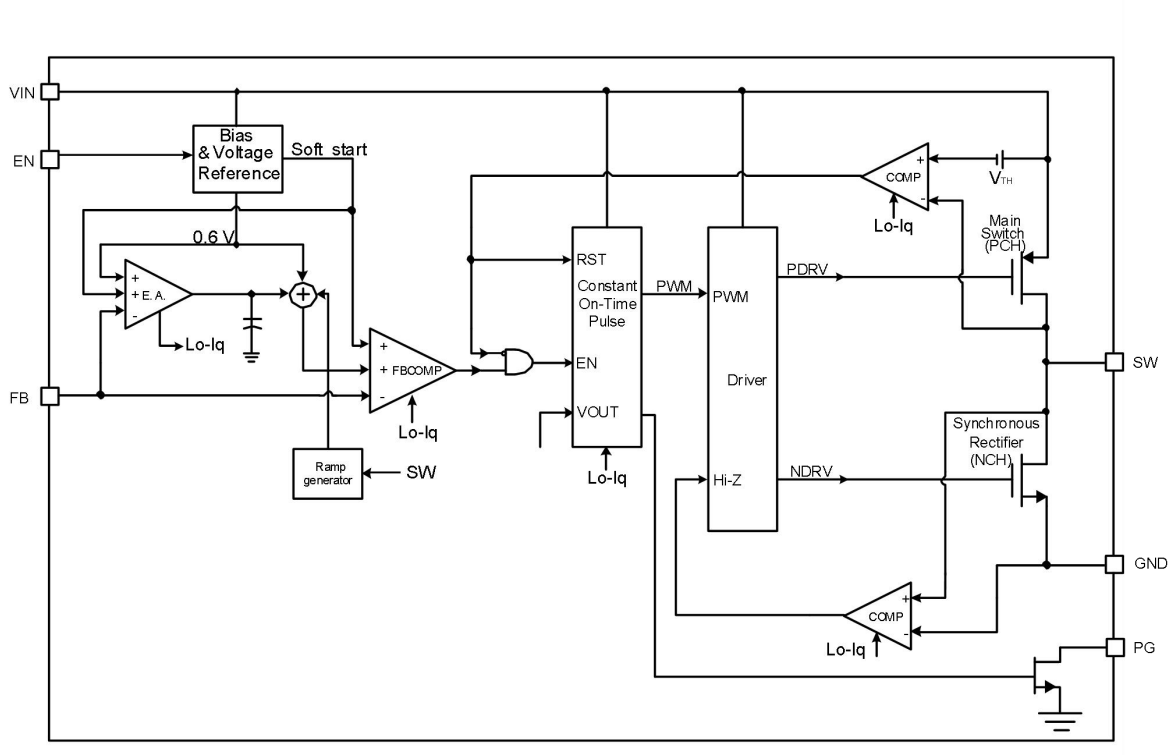


Figure 35. Block diagram

Detailed Description

Overview

The DIO6182X/DIO6182XA is a synchronous buck regulator IC with an adaptive constant on-time control and top and bottom switches on the same die to minimize the switching transition loss and conduction loss. With ultra-low $R_{DS(ON)}$ power switches and proprietary constant on-time control, this regulator IC can achieve the highest efficiency and the highest switch frequency simultaneously to minimize the external inductor and capacitor size and thus achieve the minimum solution footprint.

The DIO6182X operates in auto mode, which includes two modes, the PWM (Pulse Width Modulation) mode and the PSM (Power Save Mode) mode. The device operates in PWM mode for medium to heavy loads. In such conditions, the DIO6182X operates at a switching frequency of 2 MHz to minimize the size of the inductor and output capacitor. When the load current drops to light load conditions, the DIO6182X automatically enters PSM mode for high efficiency. The DIO6182XA operates in forced PWM, in which the device maintains continuous on mode operation and maintains extremely low output voltage ripple in the whole load range.

Pulse width modulation (PWM) operation

The device operates in continuous conduction mode (CCM) when the output current is high. The switching frequency is fairly constant in CCM operation. This is called pulse-width modulation (PWM) mode. An adaptive constant on-time (COT) control with stabilized switching frequency determines the PWM operation. In a steady state condition, the on-time is calculated as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 500ns \quad (1)$$

Power save mode (PSM) operation

Under light load conditions, the DIO6182X enters power save mode (PSM) to maintain high efficiency. Meanwhile, the device works continuously in discontinuous conduction mode (DCM). For this to occur, the output current must be less than 50% of the inductor's ripple current. The device now operates with a fixed on-time and the switching frequency further decreases proportionally to the load current. It can be calculated as:

$$f_{PSM} = \frac{2 \times I_{OUT}}{t^2_{ON} \times \frac{V_{IN}}{V_{OUT}} (\frac{V_{IN} - V_{OUT}}{L})} \quad (2)$$

The output voltage surges slightly past the nominal target in PSM, but it can be minimized by using a larger output capacitance. The device can only maintain output regulation in PWM mode and may not enter PSM when duty cycles are larger than 90%.

Soft-start

The DIO6182X/DIO6182XA employs a soft-start (SS) mechanism to ensure smooth output ramping during power-up. When EN goes high, an internal soft-start circuitry controls the output voltage during start-up. The device will initiate switching and the output voltage will smoothly ramp up to its targeted regulation voltage only after this ramp voltage is greater than the feedback voltage V_{FB}. This avoids excessive inrush current and ensures a controlled output voltage ramp.

Switch current limit and short-circuit protection

The protection function prevents the device from drawing excessive current in case of externally-caused overcurrent or short circuit conditions. If the current limit threshold is reached, the device delivers its maximum output current. If the output voltage drops below the output under-voltage protection level, the DIO6182X/DIO6182XA will stop switching to avoid excessive heat.

Undervoltage lockout

If the input voltage is larger than a typical 2.35 V while the DIO6182X/DIO6182XA is powered up, the DIO6182X/DIO6182XA will start switching. If the input voltage is lower than UVLO_falling with a 150 mV hysteresis, the DIO6182X/DIO6182XA will be shut down.

Thermal shutdown

The device goes into thermal shutdown as soon as the junction temperature exceeds a typical 150°C with a 20°C hysteresis.

Device functional modes

1. Enable, disable and output discharge

Pulling the EN pin low (< 0.4 V) will shut down the device. If the EN pin is driven high (> 1 V), the device will turn on again. Do not leave the EN pin floating. A shutdown is forced if the EN pin is pulled low with a shutdown current of a typical 150 nA. During shut down mode, the device is turned off and the output voltage is actively discharged through the SW pin by a current sink.

2. Power good

The DIO6182X/DIO6182XA has a built-in power good (PG) function. The PG pin is an open-drain output and connected to an external pull-up resistor; it is also controlled by a comparator which the feedback signal FB is fed to. If FB is above 90% of the internal reference voltage, the PG pin will be in high impedance and V_{PG} will be held high. Otherwise, including when the device is disabled in UVLO or in thermal shutdown, PG is low (see Table 2).

Table 2. PG pin logic

Device Conditions		Logic Status	
		HIGH-Z	LOW
Enable	EN = High, V_{FB} ≥ 0.576 V	√	
	EN = High, V_{FB} ≤ 0.552 V		√
	EN = High, V_{FB} ≤ 0.63 V	√	
	EN = High, V_{FB} ≥ 0.66 V		√
Shutdown	EN = Low		√
Thermal shutdown	$T_J > T_{JSD}$		√
UVLO	0.7 V < VIN < V_{UVLO}		√
Power supply removal	VIN < 0.7 V	√	

Typical Applications

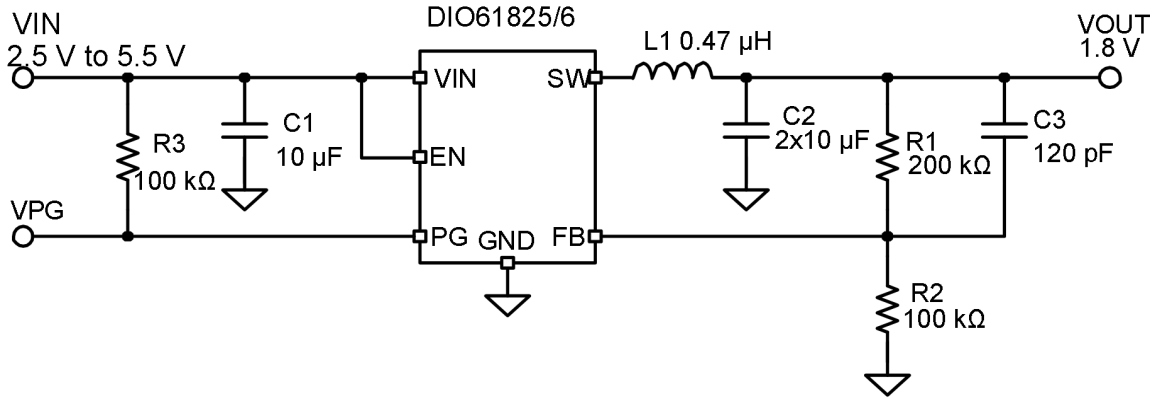


Figure 36. Typical applications

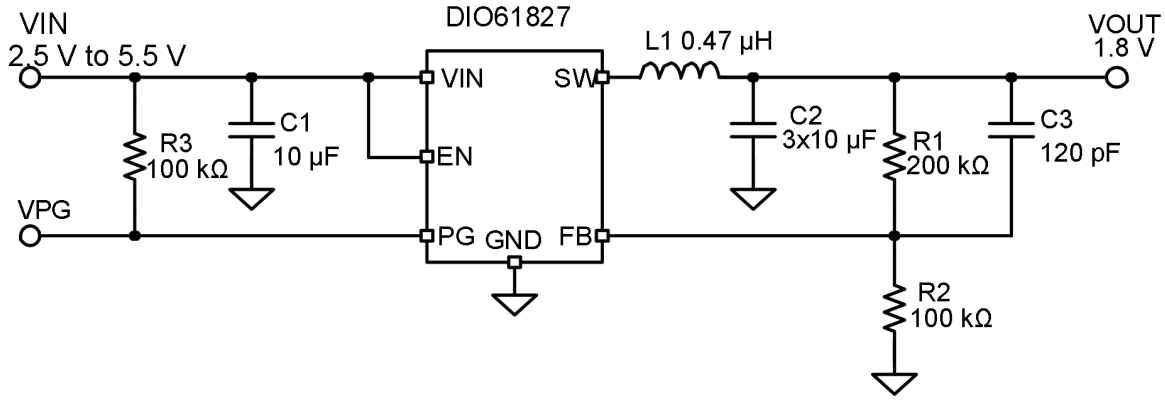


Figure 37. Typical applications

Application information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

Design requirements

For this design example, use the parameters listed in Table 3 as the input parameters.

Table 3. Design parameters

Design Parameter	Example Value
Input voltage	2.5 V to 5.5 V
Output voltage	1.8 V
Output ripple voltage	< 20 mV
Maximum output current	4 A

Table 4 lists the components used for the example.

Table 4. List of components

Reference	Description	Manufacturer
C1	10 µF, ceramic capacitor, 10 V, X7R, size 0603, GRM188Z71A106MA73D	Murata
C2	3 × 10 µF, ceramic capacitor, 10 V, X7R, size 0603, GRM188Z71A106MA73D	Murata
C3	120 pF, ceramic capacitor, 50 V, size 0402	Std
L1	0.47 µH, power inductor, XFL4015-471MEB	Coilcraft
R1	Depending on the output voltage, 1%, size 0402	Std
R2	100 kΩ, chip resistor, 1/16 W, 1%, size 0402	Std
R3	100 kΩ, chip resistor, 1/16 W, 1%, size 0402	Std

Detailed Design Procedure

Setting the output voltage

Set the desired output voltage by using a resistive divider from the output to the ground with the midpoint connected to FB. The output voltage is set by an external resistor divider according to Equation (3):

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) = R2 \times \left(\frac{V_{OUT}}{0.6V} - 1 \right) \quad (3)$$

To achieve high efficiency at light load while providing acceptable noise sensitivity, R2 cannot exceed 100 kΩ. For a given R2 value, Equation (4) demonstrates how to calculate the feedforward capacitor value. A 120 pF feedforward capacitor is used for the recommended 100 kΩ value for R2.

$$C3 = \frac{12\,\mu}{R2} \quad (4)$$

Output filter design

To provide a low-pass filter, it requires both the inductor and the output capacitor working together. To facilitate this process, Table 5 recommends the following combinations for the inductor and capacitor value. Checked cells are combinations that have proven stability through lab tests and simulations. Any other combinations should be checked for each individual application.

Table 5. Matrix of output capacitor and inductor combinations

Nominal L (µH)(2)	Nominal C_{OUT} (µF)(3)			
	10	2 × 10 or 22	47	100
0.33				
0.47	+	+ (1)	+	
1.0				

Table 6. Matrix of output capacitor and inductor combinations

Nominal L (μH)(2)	Nominal C_{OUT} (μF)(3)			
	22	3 × 10	47	100
0.33				
0.47		+ (1)	+	+
1.0				

Note：

(1) This LC combination is the standard value and recommended for most applications.

(2) Inductor tolerance and current derating are anticipated. The effective inductance can vary by 20% and -30%.

(3) Capacitance tolerance and bias voltage derating are anticipated. The effective capacitance can vary by 20% and -35%.

Inductor selection

Selecting an inductor involves specifying its inductance and also its required peak current. Lower inductor values benefit from reduced size and cost and they can improve the circuit's transient response, but they increase the inductor ripple current and output voltage ripple and reduce the efficiency due to the resulting higher peak currents. To calculate the maximum inductor current under static load conditions, Equation (5) is given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2} \quad (5)$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (6)$$

Where

- $I_{OUT,MAX}$ = Maximum output current
- ΔI_L = Inductor current ripple
- f_{SW} = Switching frequency
- L = Inductor value

It is recommended to choose a saturation current for the inductor that is approximately 20% to 30% higher than $I_{L,MAX}$. In addition, DC resistance and size should also be taken into account when selecting an appropriate inductor. Table 7 lists recommended inductors.

Table 7. List of recommended inductors

Inductance (μH)	Current Rating (A)	Dimensions (L x W x H mm)	MAX. DC Resistance (mΩ)	Manufacturer Part Number
0.47	4.8	2.0 x 1.6 x 1.0	32	HTEN20161T-R47MDR, Cyntec
	4.6	2.0 x 1.2 x 1.0	25	HTEH20121T-R47MSR, Cyntec
	4.8	2.0 x 1.6 x 1.0	32	DFE201610E - R47M, MuRata
	4.8	2.0 x 1.6 x 1.0	32	DFE201210S - R47M, MuRata
	5.1	2.0 x 1.6 x 1.0	34	TFM201610ALM-R47MTAA, TDK
	5.2	2.0 x 1.6 x 1.0	25	TFM201610ALC-R47MTAA, TDK
	6.6	4.0 x 4.0 x 1.6	8.36	XFL4015-471ME, Coilcraft
	8.0	3.5 x 3.2 x 2.0	10.85	XEL3520-471ME, Coilcraft
	6.8	4.5 x 4 x 1.8	11.2	WE-LHMI-744373240047, Würth

Capacitor selection

The IC is optimized for ceramic output capacitors and the best performance will be obtained by using them. The input capacitor is the low-impedance energy source for the converters, which help provide stable operation. A low-ESR multilayer ceramic capacitor is recommended for the best filtering and must be placed between V_{IN} and GND as close as possible to those pins.

The architecture of the device allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. DIOO recommends using X7R or X5R dielectrics.

Power supply recommendations

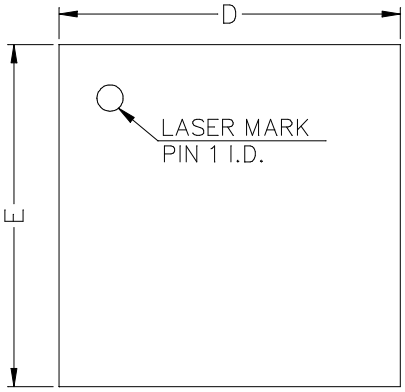
The device is designed to operate from an input voltage supply range from 2.5 V to 5.5 V. Ensure that the input power supply has a sufficient current rating for the application.

Layout Guidelines

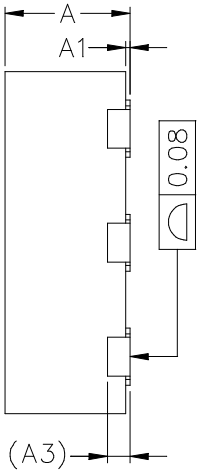
The layout design of the DIO6182X/6182XA regulator is relatively simple. For the best efficiency and minimum noise issues, we should place the following components close to the IC: C_{IN}, L, R1, and R2.

1. Maximize the PCB copper area connected to the GND pin to achieve the best thermal and noise performance. If the board space allows, a ground plane is highly desirable.
2. C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.
3. The PCB copper area associated with the SW pin must be minimized to avoid the potential noise issue.
4. The components R1 and R2, and the trace connected to the FB pin must NOT be adjacent to the SW net on the PCB layout to avoid the noise issue.

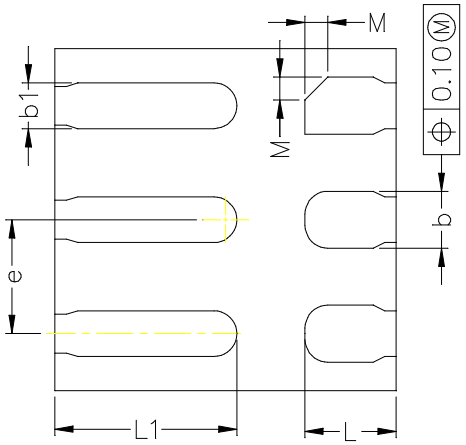
Physical Dimensions: DFN1.5*1.5-6



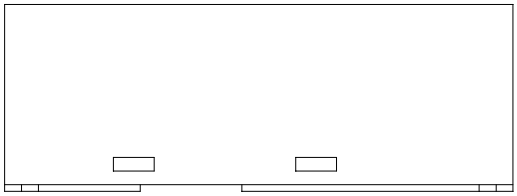
TOP VIEW



SIDE VIEW

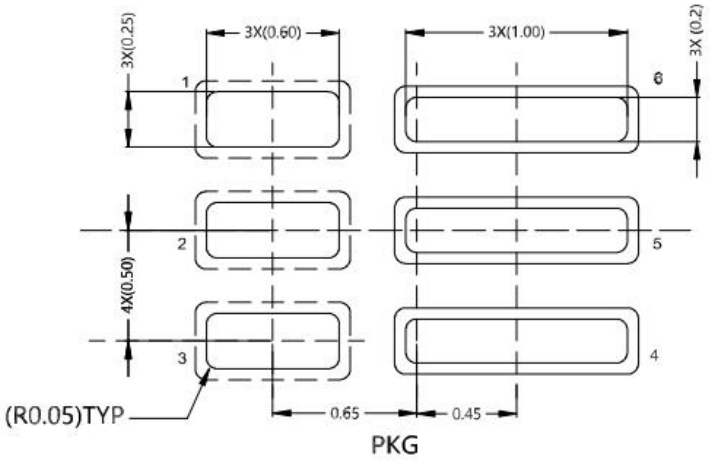


BOTTOM VIEW

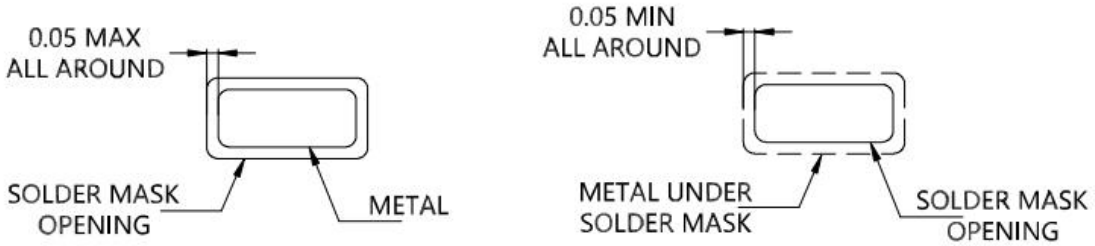


SIDE VIEW

Common Dimensions (Units of measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3		0.10 REF	
b	0.20	0.25	0.30
b1	0.15	0.20	0.25
D	1.40	1.50	1.60
E	1.40	1.50	1.60
e	0.40	0.50	0.60
L	0.30	0.40	0.50
L1	0.70	0.80	0.90
M		0.10 REF	



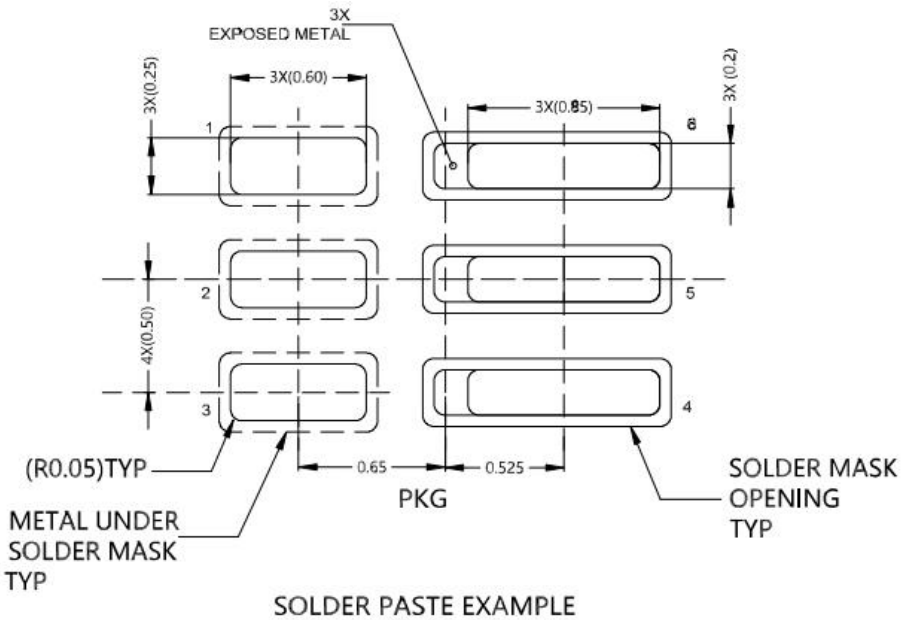
LAND PATTERN EXAMPLE



PADS 4-6
NON SOLDER MASK
DEFINED

PADS 1-3
SOLDER MASK
DEFINED

SOLDER MASK DETAILS



SOLDER PASTE EXAMPLE

Revision History

- Revision 0.1 initial preliminary datasheet
- Revision 0.2 change the Adjustable output voltage application from “0.6 V to 4 V”to “0.6 V to 5 V”
- Revision 0.3 change the DC Electrical Characteristics-I_Q(EN = High, no load, FPWM devices, TYP) from “9 mA” to “10 mA”,delete the I_Q(MAX).
- Revision 1.0 change Human-body model (HBM) from “±3000” to “±4000”；add Charge device model (CMD) (±2000)；delete Ψ_{JT} and Ψ_{JB}；change the $R_{\theta JA}$ from “129.5” to “107.8”,change the $R_{\theta JC(top)}$ from “103.9” to “24.2”,change the $R_{\theta JA}$ from “33.1” to “20.5”； Added the Typical Performance Characteristic.
- Revision 1.1 remove "DIO61824CL6/DIO61824ACL6" from part number; Update the Typical Performance Characteristics
- Revision 1.2 added the pin assignment (top view).
- Revision 1.3 added the Ordering Information of DIO6182XCL6KS/DIO6182XACL6KS

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