# DIO54302
# High-Efficiency 3 A, 28 V Input Synchronous Step-Down Converter

## Features

- Low $R_{DS(ON)}$ for internal switches (top/bottom) 80 mΩ/40 mΩ, 3.0 A
- 4.5 ~ 28 V input voltage range
- High-efficiency synchronous mode
- Internal soft-start limits the inrush current
- Over-current protection
- Output short circuit protection with hiccup
- Thermal shutdown
- Available in the TSOT23-6 package

## Applications

- Portable navigation devices
- Set-top boxes
- Portable TVs
- LCD TVs

## Descriptions

The DIO54302 is a high-efficiency, high-frequency synchronous step-down DC-DC regulator IC capable of delivering up to 3 A output currents. The DIO54302 operates over a wide input voltage range from 4.5 V to 28 V and integrates the main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The COT architecture with pseudo-fixed switching frequency operation provides a fast transient response and eases loop stabilization. The DIO54302 operates in pulse skip mode where the device maintains a high efficiency during light load operation.

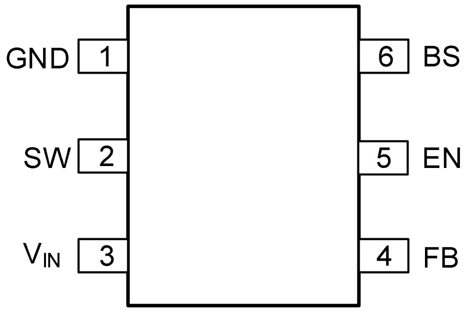
Protection features include over-current protection and thermal shutdown.

The DIO54302 requires a minimal number of readily-available, standard, external components and is available in a space-saving TSOT23-6 package.

## Ordering Information

| Order Part Number | Top Marking | MSL | RoHS | $T_A$ | Package | |
|---|---|---|---|---|---|---|
| DIO54302TST6 | W402 | 3 | Green | -40 to 105°C | TSOT23-6 | Tape & Reel, 3000 |

## Pin Assignments




**TSOT23-6**

**Figure 1. Pin Assignment (Top View)**

## Pin Definitions

| Pin Name | Description |
|---|---|
| GND | Power ground |
| SW | Inductor pin. Connect this pin to the switching node of inductor. |
| $V_{IN}$ | Power input |
| FB | Output feedback pin. Connect this pin to the center point of the output resistor divider to program the output voltage: $V_{OUT}$ = 0.6 × (1 + R1/R2).<br>Add optional C2 (10 pF ~ 47 pF) to speed up the transient response. |
| EN | Enable pin. Float the EN pin to enable. |
| BS | Bootstrap. Connect a capacitor and a resistor between SW and BS pins to form a floating supply across the high-side switch driver. Recommend to use 0.1 µF BS capacitor. |

## Absolute Maximum Ratings

Stresses beyond those listed under the Absolute Maximum Rating table may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{IN}$ | Supply voltage (V+ – V-) | -0.3 to 32 | V |
| | EN, SW voltage | -0.3 to $V_{IN}$ + 0.3 | V |
| $V_{FB}$ | FB voltage | -0.3 to 6 | V |
| $V_{BS}$ | BS voltage | -0.3 to $V_{SW}$ + 6 | V |
| $V_{SW}$ | SW (15 ns transient) voltage | -5 to 32 | V |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 87.9 | °C/W |
| $\theta_{JC}$ | Junction-to-case thermal resistance | 42.2 | |
| $T_{STG}$ | Storage temperature range | -65 to 150 | °C |
| $T_J$ | Junction temperature range | 150 | °C |
| $T_L$ | Lead temperature range | 260 | °C |
| ESD | Human body model (HBM) | ±2500 | V |
| | Charged device model (CDM) | ±2000 | V |

## Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{IN}$ | Supply voltage | 4.5 to 28 | V |
| $T_J$ | Junction temperature range | -40 to 125 | °C |
| $T_A$ | Ambient temperature range | -40 to 105 | °C |

## Electrical Characteristics

$V_{IN}$ = 12 V, $V_{OUT}$ = 1.2 V, L = 2.2 μH, $C_{OUT}$ = 47 μF, $T_A$ = 25°C, $I_{OUT}$ = 1 A, unless otherwise specified.

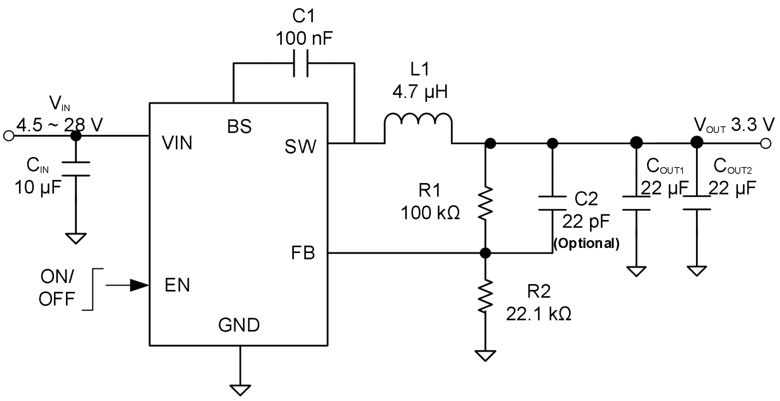
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Supply voltage | | 4.5 | | 28 | V |
| $I_Q$ | Quiescent current | $I_{OUT}$ = 0, $V_{FB}$ = $V_{REF}$ × 105% | | 140 | | μA |
| $I_{SHDN}$ | Shutdown current | EN = 0 | | 5 | 15 | μA |
| $V_{REF}$ | Feedback reference voltage | | 0.588 | 0.6 | 0.612 | V |
| $I_{FB}$(2) | FB input current | $V_{FB}$ = 3.3 V | -50 | | 50 | nA |
| $R_{DS(ON)}$(2) | Top FET $R_{ON}$ | | | 80 | | mΩ |
| $R_{DS(ON)}$(2) | Bottom FET $R_{ON}$ | | | 40 | | mΩ |
| $I_{LIM}$(2) | Low side power FET current limit | | 3.0 | 4.0 | | A |
| $V_{ENH}$ | EN rising threshold | | | 1.21 | 1.28 | V |
| $V_{ENL}$ | EN falling threshold | | 1.1 | 1.19 | | V |
| $I_{ENP}$ | EN integrated pull-up current | | 1 | 3 | 5 | μA |
| $V_{UVLO}$ | $V_{IN}$ under-voltage unlock threshold, rising | | | | 4.45 | V |
| $f_{SW}$ | Switching frequency | | | 500 | | kHz |
| | Min ON time(2) | | | 40 | | ns |
| | Min OFF time(2) | | | 180 | | ns |
| $t_{SS}$(2) | Soft-start time | | | 1 | | ms |
| $T_{SD}$(2) | Thermal shutdown temperature | | | 150 | | °C |
| $T_{HYS}$(2) | Thermal shutdown hysteresis | | | 20 | | °C |

**Note:**

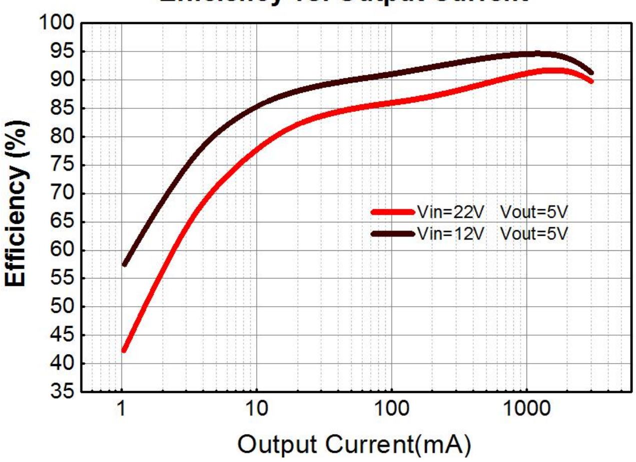
(1) Specifications subject to change without notice.

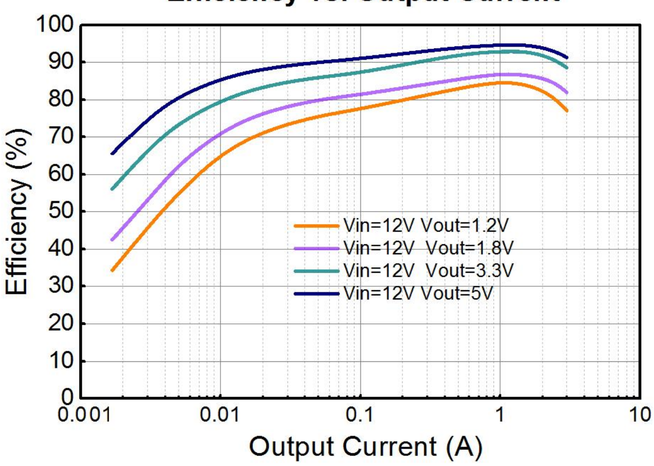
(2) Guaranteed by design.

## Typical Application



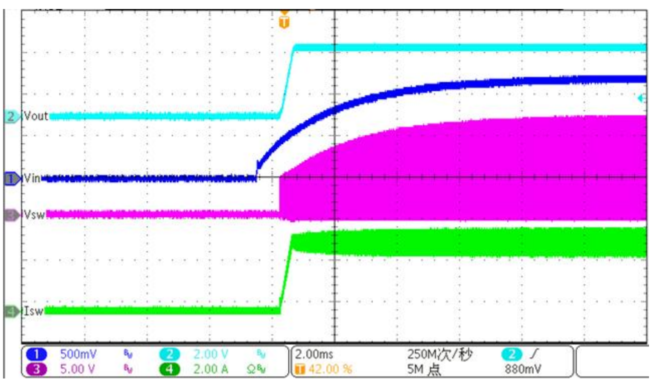

## Typical Performance Characteristics



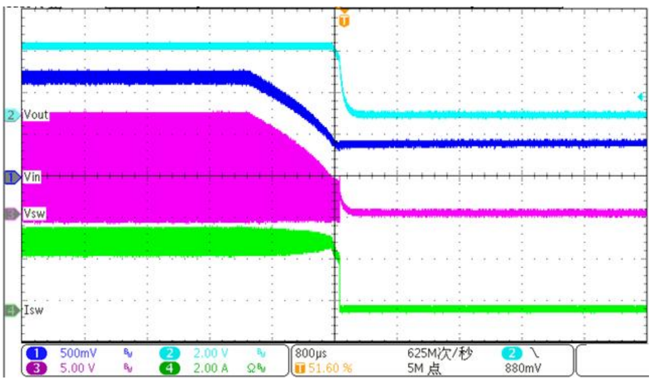

**Start up from $V_{IN}$**

($V_{IN}$ = 12 V, $V_{OUT}$ = 3.3 V, Load = 1 Ω)



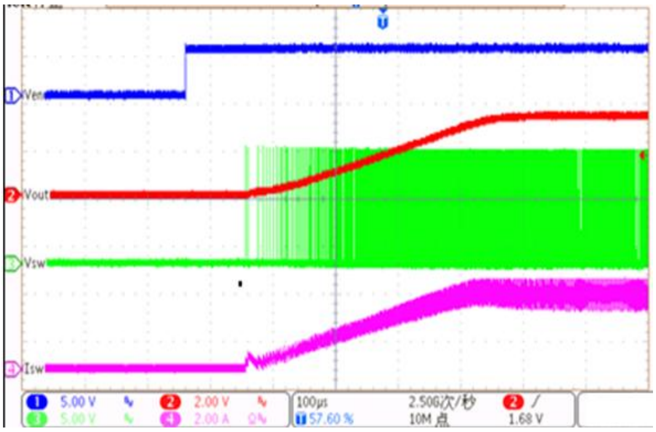

**Shut down from $V_{IN}$**

($V_{IN}$ = 12 V, $V_{OUT}$ = 3.3 V, Load = 1 Ω)



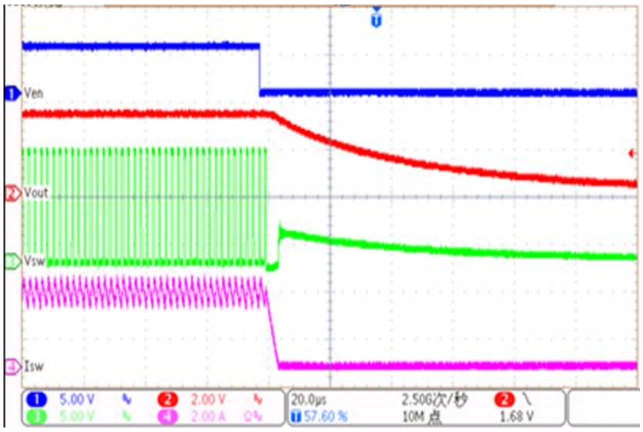
**Start up from Enable**

($V_{IN}$ = 12 V, $V_{OUT}$ = 3.3 V, Load = 1 Ω)



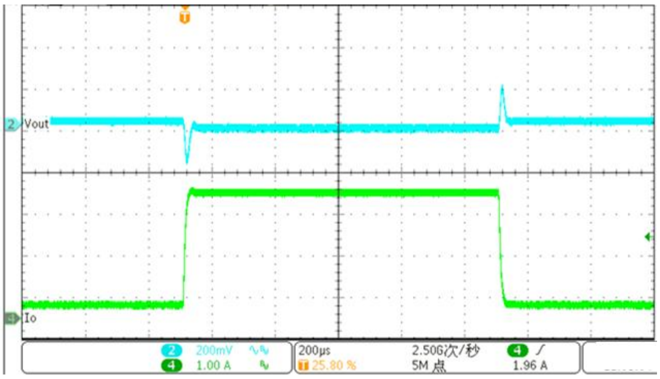

**Shut down from Enable**

($V_{IN}$ = 12 V, $V_{OUT}$ = 3.3 V, Load = 1 Ω)



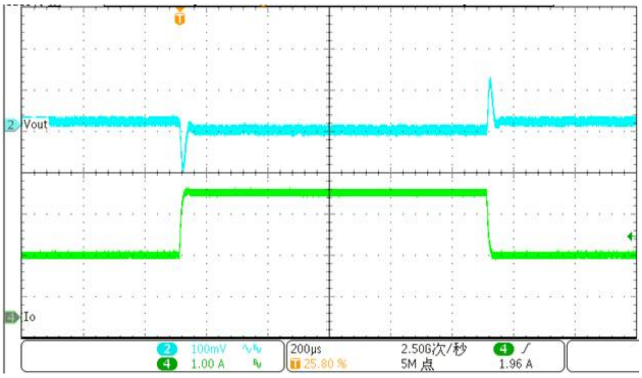

**Load transient**

($V_{IN}$ = 12 V, $V_{OUT}$ = 3.3 V, Load = 0.3 ~ 3 A)



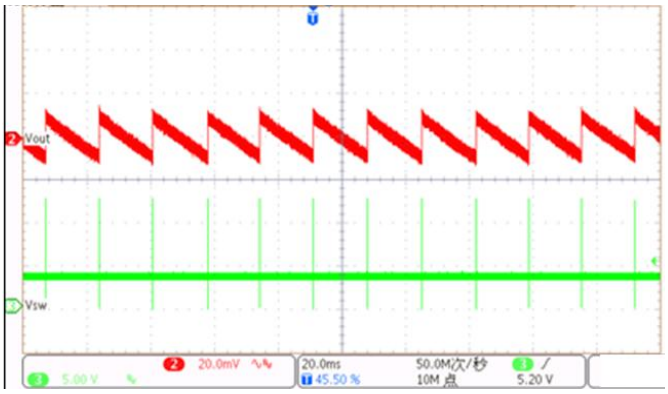

**Load transient**

($V_{IN}$ = 12 V, $V_{OUT}$ = 3.3 V, Load = 1.5 ~ 3 A)



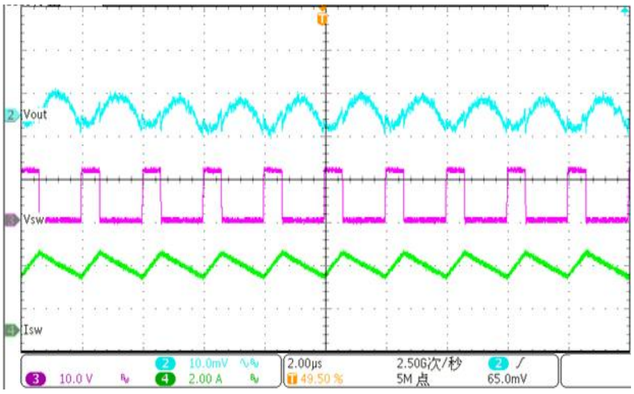

**Ripple**

($V_{IN}$ = 12 V, $V_{OUT}$ = 3.3 V, Load = 0 A)



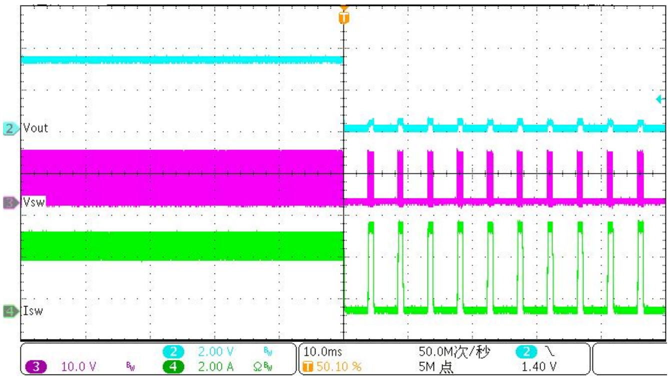

**Ripple**

($V_{IN}$ = 12 V, $V_{OUT}$ = 3.3 V, Load = 3 A)



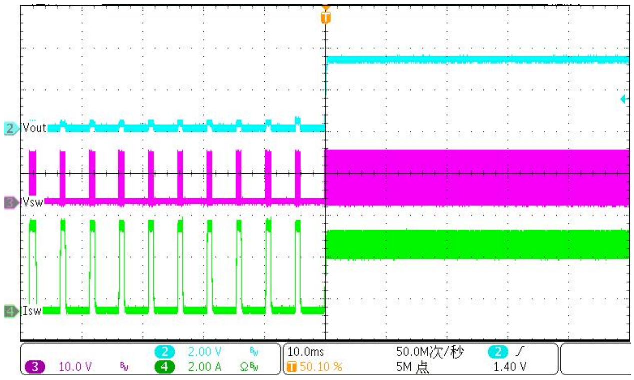
**Short circuit protection**

($V_{IN}$ = 12 V, $V_{OUT}$ = 3.3 V, Load = 3 A)

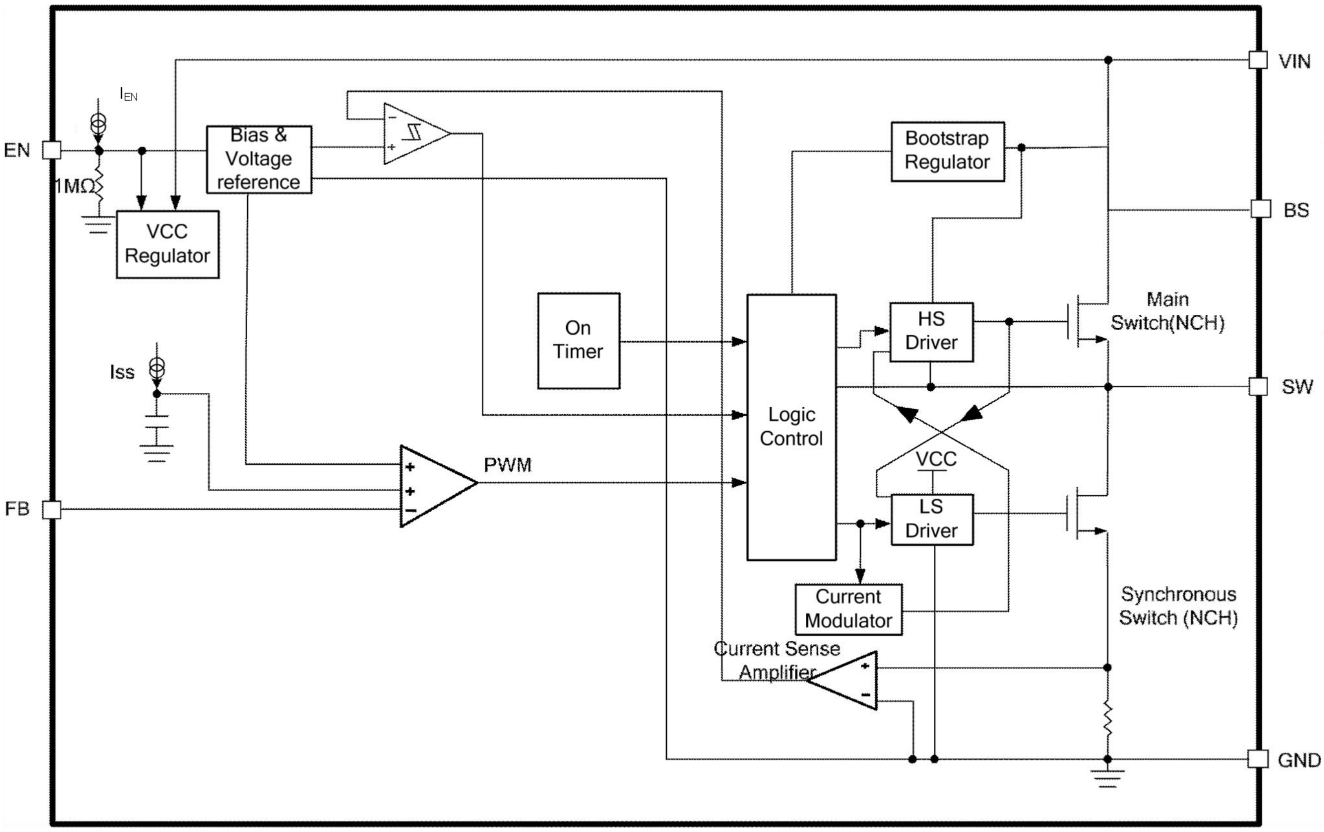



**Short circuit recovery**

($V_{IN}$ = 12 V, $V_{OUT}$ = 3.3 V, Load = 3 A)




## Functional Block Diagram



# Function Description

### Enable and Adjusting Undervoltage Lockout

The EN pin electrically controls the device. The device begins the operation when the EN pin voltage exceeds the threshold voltage. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters the low-quiescent ($I_Q$) state.

With the internal pull-up current source in the EN pin, users can float the EN pin to enable the device. Users can interface with the EN pin by using open-drain or open-collector output logic.

The device implements internal undervoltage-lockout (UVLO) circuitry on the VIN pin. In case of a VIN pin voltage below the internal UVLO threshold, the device is disabled. The internal VIN UVLO threshold has a hysteresis of 300 mV.

If an application requires a higher UVLO threshold on the VIN pin, then the EN pin can be configured as shown in Figure 2. A hysteresis higher than 400 mV is recommended for the external UVLO function.

The EN pin has a small pull-up current, $I_{ENP}$, which sets the default state of the pin to enable when no external components are connected. Use Equation (1) and Equation (2) to calculate the values of R4 and R5 for a specified UVLO threshold.

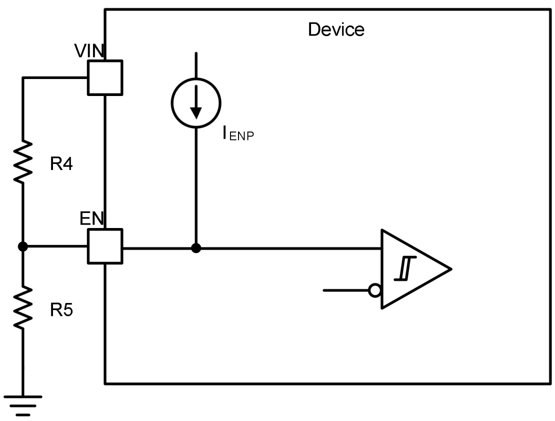



**Figure 2. Adjustable $V_{IN}$ Undervoltage Lockout**

$$R4 = \frac{V_{START} \times \left(\frac{V_{ENfalling}}{V_{ENrising}}\right) - V_{STOP}}{I_{ENP} \times \left(1 - \frac{V_{ENfalling}}{V_{ENrising}}\right)} \quad (1)$$

Where

$I_{ENP}$ = 3 μA

$V_{ENfalling}$ = 1.19 V

$V_{ENrising}$ = 1.21 V

$$R5 = \frac{R4 \times V_{ENfalling}}{V_{STOP} - V_{ENfalling} + R4 \times I_{ENP}} \quad (2)$$

**Over-current protection (OCP) and short circuit protection (SCP)**

The DIO54302 has a valley current limit control. During LS-FET ON state, the inductor current is monitored. When the sensed inductor current hits the valley current limit, the LS limit comparator (shown in functional block diagram) turns over, the device enters over-current protection mode, and HS-FET will wait until the valley current limit disappears to turn on again. Meanwhile, the output voltage drops until $V_{FB}$ is below the under-voltage (UV) threshold—typically 55% below the reference. As soon as UV is triggered, the DIO54302 enters hiccup mode and periodically restart the part. During over-current protection, the device tries to recover from over-current fault with hiccup mode, which means the chip will disable output power stage, discharge soft-start and then automatically try to operate the soft-start again. If the over-current condition still holds after the soft-start ends, the device repeats this operation cycle until over-current conditions disappear and then output rises back to regulation level. So the OCP is non-latch protection.

**Thermal shutdown**

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, it shuts down the whole chip. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

# Application Information

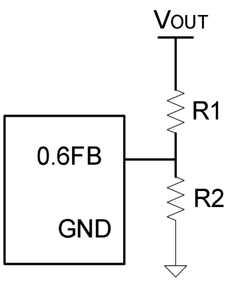
The DIO54302 is a synchronous buck regulator IC that integrates the COT control, top and bottom switches on the same die to minimize the switching transition loss and conduction loss. With ultra-low $R_{DS(ON)}$ power switches and proprietary COT control, this regulator IC can achieve the highest efficiency and the highest switch frequency simultaneously to minimize the external inductor and capacitor size, thus achieving the minimum solution footprint.

Because of the high integration in the DIO54302 IC, the application circuit based on this regulator IC is rather simple. Only input capacitor $C_{IN}$, output capacitor $C_{OUT}$, output inductor L and feedback resistors (R1 and R2) need to be selected for the targeted applications specifications.

**Feedback resistor dividers R1 and R2**

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2. A value of between 10 k and 1 M is highly recommended for both resistors. If $V_{OUT}$ is 3.3 V, R1 = 100 kΩ is chosen, then R2 is 22.1 kΩ.

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1 \tag{3}$$




**Input capacitor $C_{IN}$**

This ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D(1-D)} \tag{4}$$

This formula has a maximum at $V_{IN} = 2\ V_{OUT}$ condition, where $I_{CIN\_RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for the DC/DC design.

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by $C_{IN}$, and IN/GND pins. In this case, a 10 μF low ESR ceramic capacitor is recommended.

**Output capacitor $C_{OUT}$**

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor greater than 22 μF capacitance.

**Output inductor L:**

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 40\%} \quad (5)$$

where $f_{sw}$ is the switching frequency and $I_{OUT,MAX}$ is the maximum load current. The DIO54302 regulator IC is quite tolerant of different ripple current amplitudes. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L} \quad (6)$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR < 50 mΩ to achieve a good overall efficiency.

**Layout Design:**

The layout design of the DIO54302 regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: $C_{IN}$, L, R1, and R2.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allows, a ground plane is highly desirable.

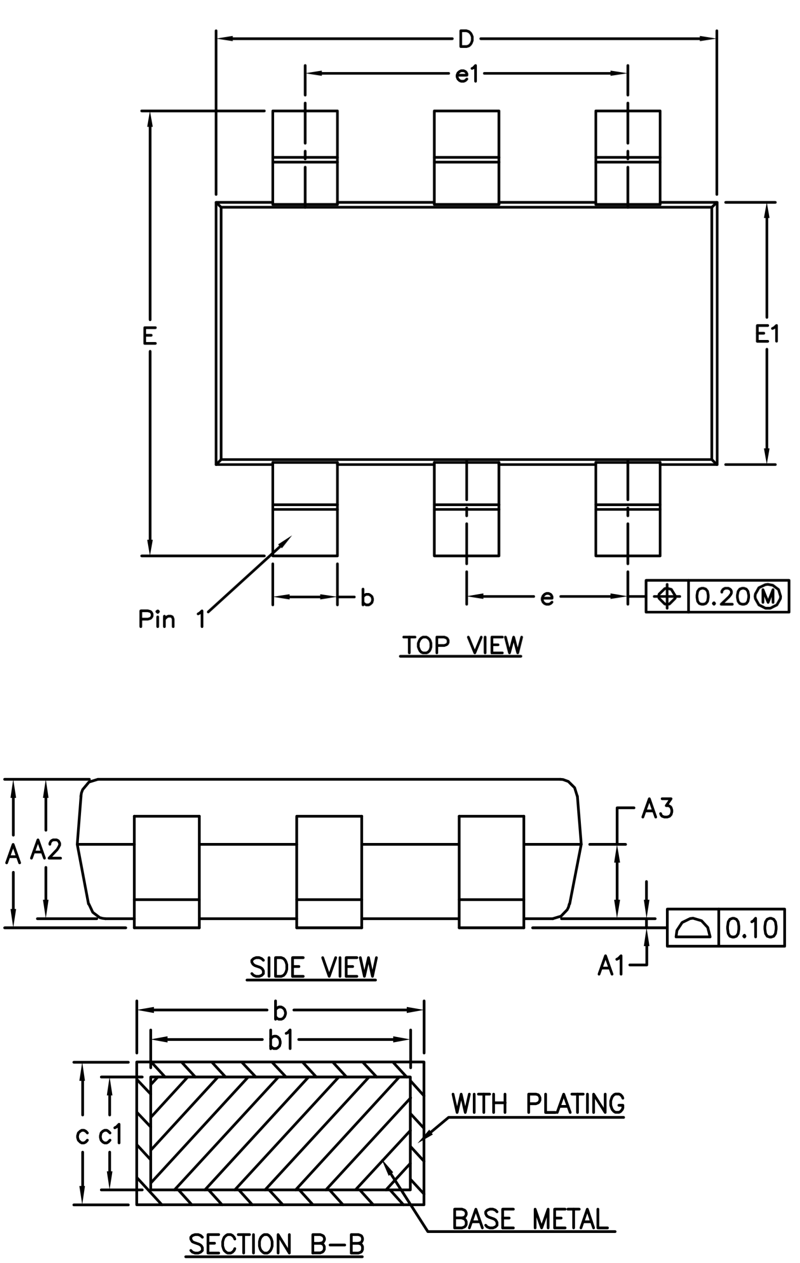
2) $C_{IN}$ must be close to pins IN and GND. The loop area formed by $C_{IN}$ and GND must be minimized.

3) The PCB copper area associated with the SW pin must be minimized to avoid the potential noise problem.

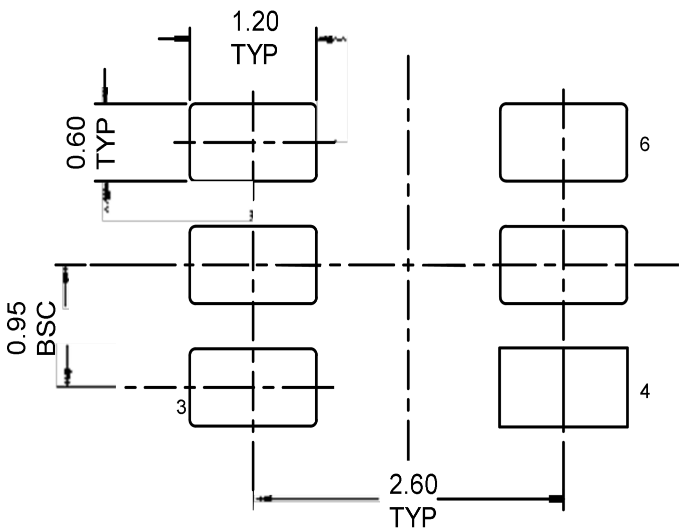
4) The components R1 and R2, and the trace connecting to the FB pin must NOT be adjacent to the SW net on the PCB layout to avoid the noise problem.

5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-ion battery, it is desirable to add a pull-down 1 MΩ resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

## Physical Dimensions: TSOT23-6




| Common Dimensions (Units of measure = Millimeter) | | | |
|---|---|---|---|
| Symbol | Min | Nom | Max |
| A | - | - | 0.90 |
| A1 | 0 | - | 0.15 |
| A2 | 0.65 | 0.75 | 0.85 |
| A3 | 0.35 | 0.40 | 0.45 |
| b | 0.36 | - | 0.50 |
| b1 | 0.36 | 0.38 | 0.45 |
| c | 0.14 | - | 0.20 |
| c1 | 0.14 | 0.15 | 0.16 |
| D | 2.85 | 2.95 | 3.05 |
| E | 2.60 | 2.80 | 3.00 |
| E1 | 1.60 | 1.65 | 1.70 |
| e | 0.90 | 0.95 | 1.00 |
| e1 | 1.80 | 1.90 | 2.00 |
| L | 0.30 | 0.45 | 0.60 |
| L1 | 0.575 REF | | |
| L2 | 0.25 BSC | | |
| R | - | - | 0.25 |
| R1 | - | - | 0.25 |
| Θ | 0° | - | 8° |
| Θ1 | 3° | 5° | 7° |
| Θ2 | 10° | 12° | 14° |




RECOMMENDED LAND PATTERN

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For additional product information or full datasheet, please contact our sales department or representatives.