DIO6145P

5.5 V, 6 A, 1.2 MHz, High-Efficiency Synchronous Step-Down Converter

Features

- Operating input range: 2.8 V to 5.5 V
- Quiescent current: 40 μA
- Up to 6 A output current
- Fixed switching frequency: 1.2 MHz
- Adjustable output from 0.6 V
- 700 μs internal SS time with pre-bias startup
- 20 mΩ and 12 mΩ internal power MOSFETs
- Output discharge resistance: 600 Ω
- 100% duty cycle in dropout
- 1% feedback accuracy
- External mode control
- External VCON control
- Cycle-by-cycle overcurrent protection
- Short-circuit protection with hiccup mode
- Stable with low-ESR output ceramic capacitors
- Thermal shutdown
- Package: QFN2*3-12, QFN2*1.5-12

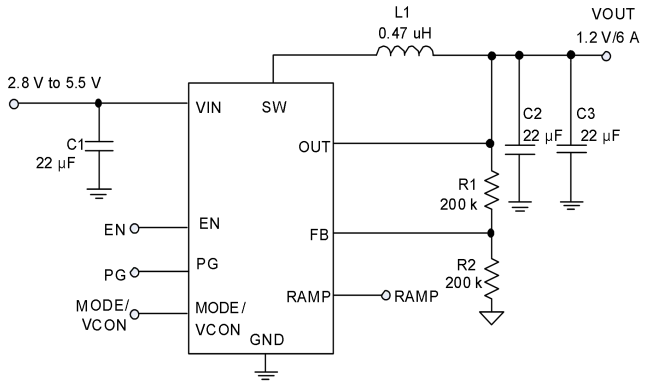
Descriptions

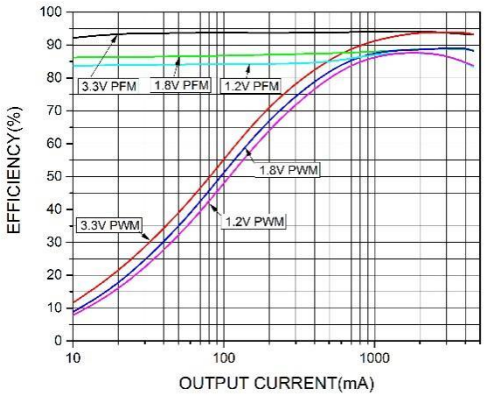
The DIO6145P is a step-down DC/DC converter with power MOSFETs integrated. It is able to provide a continuous output current of up to 6 A. The output voltage can be regulated as low as 0.6 V. It also offers various protection schemes such as current-limit and thermal shutdown. Optimized COT architecture (Constant on Time) allows both fast transient response and loop stability. Housed in a small flip-chip based QFN2*3-12 and QFN2*1.5-12 package, the DIO6145P requires minimal external components to implement 6 A output capability with superior thermal performance.

Applications

- Mobile or battery-powered devices
- Storage (SSD, HDD)

Typical Application



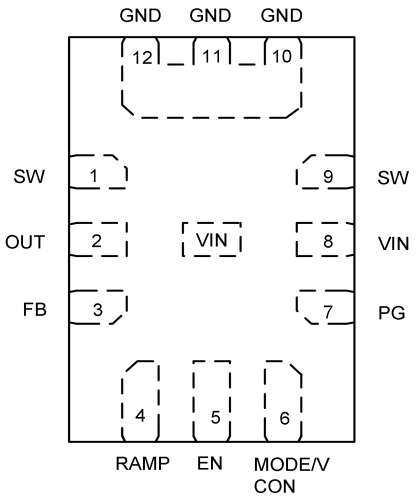


Efficiency (V_{IN} = 5 V)

Ordering Information

Ordering Part No.	Top Marking	MSL	RoHS	T_A	Package	
DIO6145PQN12	DFAD5	3	Green	-40 to 85°C	QFN2*3-12	Tape & Reel, 3000
DIO6145PFT12	45YW	1	Green	-40 to 85°C	QFN2*1.5-12	Tape & Reel, 3000

Pin Assignments



QFN2*3-12 / QFN2*1.5-12

Figure 1. Pin assignment (Top view)

Pin Definitions

Pin Name	Description
SW	Inductor pin. This pin is connected to the internal high-side and low-side power MOSFET.
OUT	Output voltage pin.
FB	Output feedback pin. Connect this pin to the center point of the output resistor,divider to program the output voltage; V_{OUT} = 0.6 (1 + R1/R2).
RAMP	External ramp pin. Sets the ramp to optimize the transient performance.
EN	Enable pin. Active high. The EN pull-down resistance is 1 MΩ.
MODE /VCON	Multi-functional pin. 1. PWM and PFM selection pin. When MODE pin is higher than 1.2 V, the DIO6145P enters PWM mode. The DIO6145P enters into PFM mode while MODE is lower than 0.4 V or floating. 2. Analog voltage dynamic regulation function pin. Analog voltage input pin which controls output voltage by PWM mode.
PG	Power good. The open-drain output with internal pull-up resistor. PG is pulled up to VIN when the FB voltage is within 10% of the regulation level, otherwise it is low. From the instant when V_{FB} crosses PG threshold to the state when the PG pin goes high, the delay is about 120 μs.
VIN	Power input supply.
GND	Power ground.

Absolute Maximum Ratings

Stresses beyond those listed under the Absolute Maximum Rating table may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter		Rating	Unit
V_{IN}	Supply voltage		6.0	V
V_{SW}	SW voltage		-0.3 (-3 V for <10 ns) to 6.0 (8 V for <10 ns)	V
V_{EN}	Enable voltage		-0.3 to V_{IN} + 0.3	V
	All other pins		-0.3 to 6.0	V
T_J	Junction temperature range		150	°C
T_L	Lead temperature range		260	°C
P_D	Continuous power dissipation (T_A = 25°C)		1.78	W
$R_{\theta JA}$	Package thermal resistance	QFN2*3-12	70	°C/W
		QFN2*1.5-12	80	
$R_{\theta JC}$	Package thermal resistance	QFN2*3-12	15	
		QFN2*1.5-12	25	
ESD	HBM		±4000	V

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating	Unit
V_{IN}	Supply voltage	2.8 to 5.5	V
V_{OUT}	Output voltage	0.6 to 5.5	V
T_J	Operating junction temperature range	-40 to 125	°C

Electrical Characteristics

V_{IN} = 3.6 V, T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{FB}	Regulated FB voltage	2.8 V < V_{IN} < 5.5 V	0.594	0.600	0.606	V
V_{UVLO}	IN under-voltage lockout threshold		2.4	2.55	2.7	V
	IN under-voltage lockout hysteresis			300		mV
V_{IH}	EN high threshold		1.6			V
V_{IL}	EN low threshold				0.4	V
I_Q	Supply current (quiescent)	V_{IN} = 3.6 V, V_{EN} = 2 V, V_{FB} = 0.65 V		40	60	μA
I_{SD}	Shutdown current	V_{EN} = 0 V		0.1	1	μA
	FB input current	V_{FB} = 0.65 V		50		nA
I_{LKG_EN}	EN input current	V_{EN} = 2 V		2		μA
		V_{EN} = 0 V		0		
R_{DSON_P}	High-side switch on-resistance			20		mΩ
R_{DSON_N}	Low-side switch on-resistance			12		mΩ
I_{LKG_P}	SW leakage current			0	1	μA
	High-side switch current limit	sourcing	7.3	8.2		A
	Low-side switch current limit (2)	sinking, PWM mode		6		A
		sinking, PFM mode		0		
	Oscillator frequency		0.96	1.2	1.8	MHz
t_{SS}	Internal soft-start time (1)			700		μs
t_{ON_MIN}	Minimum on time			50		ns
t_{OFF_MIN}	Minimum off time			60		ns
PGUV_Hi	PG UV threshold rising			0.9		V_{FB}
PGUV_Lo	PG UV threshold falling			0.85		V_{FB}
PGOV_Hi	PG OV threshold rising			1.15		V_{FB}
PGOV_Lo	PG OV threshold falling			1.1		V_{FB}
PG_{TD}	PG delay			120		μs
	PG sink current capability	sink 1 mA			0.4	V
	PG internal pull-up resistor			500		kΩ
	Thermal shutdown threshold (2)			150		°C
	Thermal shutdown hysteresis (2)			20		°C
	MODE forced PWM threshold	V_{IN} = 3.6 V, V_{EN} = 2 V	1.2			V
	MODE PFM threshold	V_{IN} = 3.6 V, V_{EN} = 2 V			0.4	V

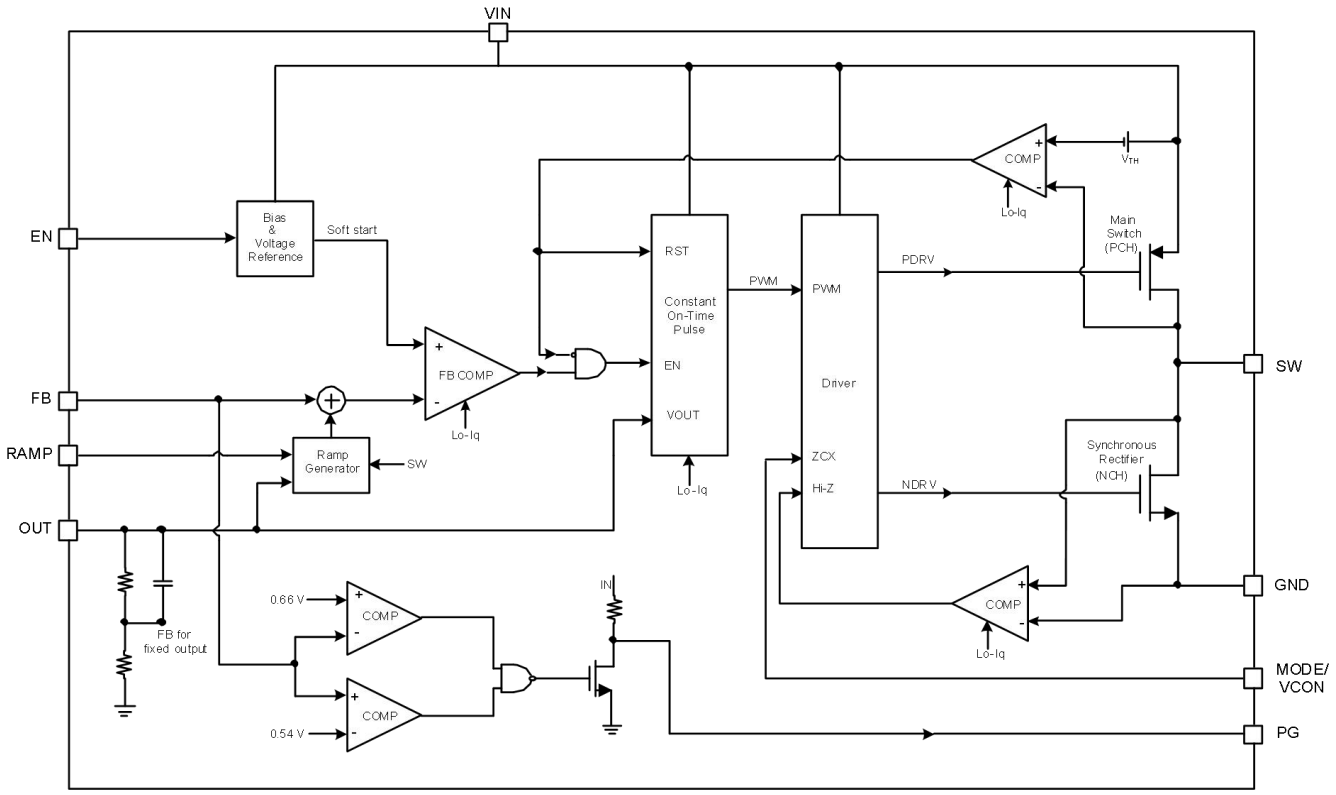
Note:

(1) Guaranteed by characterization.

(2) Guaranteed by design.

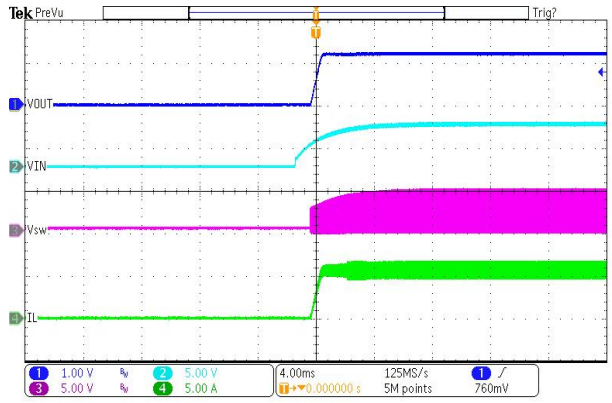
(3) Specifications subject to change without notice.

Block Diagram



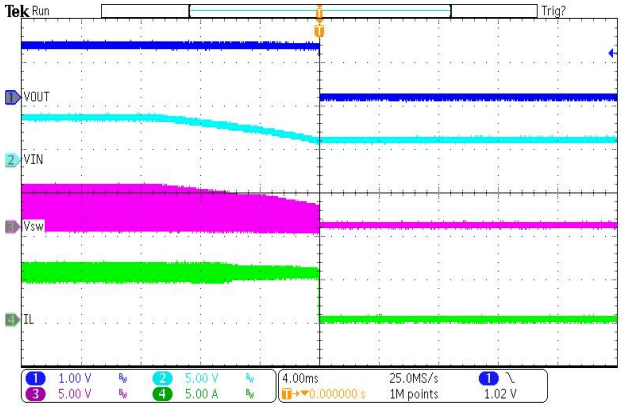
Typical Performance Characteristic

V_{IN} = 5 V, V_{OUT} = 1.2 V, L = 0.47 μH, C_{OUT} = 22 μF × 2, T_A = 25℃, unless otherwise specified.



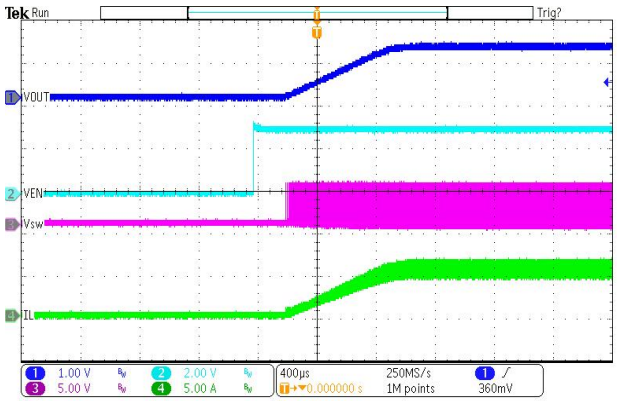
V_{IN} = 5 V, V_{OUT} = 1.2 V, I_{OUT} = 6 A

Figure 2. Power on



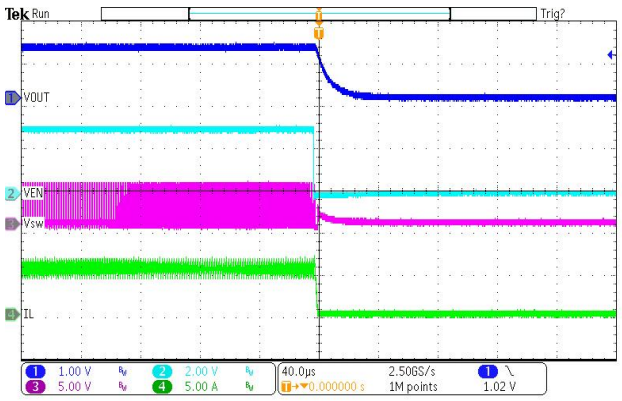
V_{IN} = 5 V, V_{OUT} = 1.2 V, I_{OUT} = 6 A

Figure 3. Power off



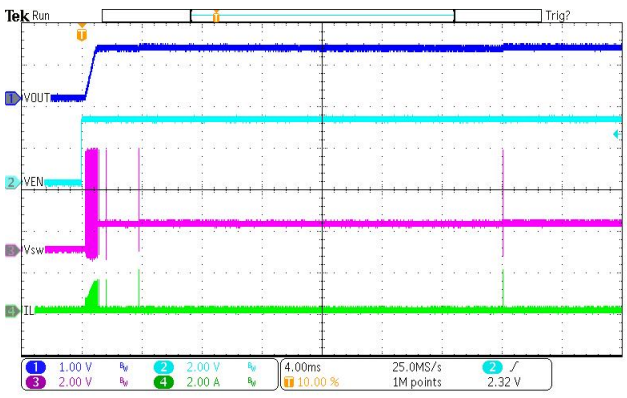
V_{IN} = 5 V, V_{OUT} = 1.2 V, I_{OUT} = 6 A

Figure 4. Enable on



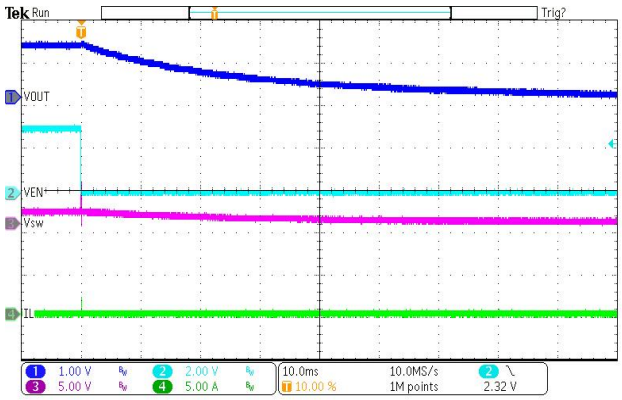
V_{IN} = 5 V, V_{OUT} = 1.2 V, I_{OUT} = 6 A

Figure 5. Enable off



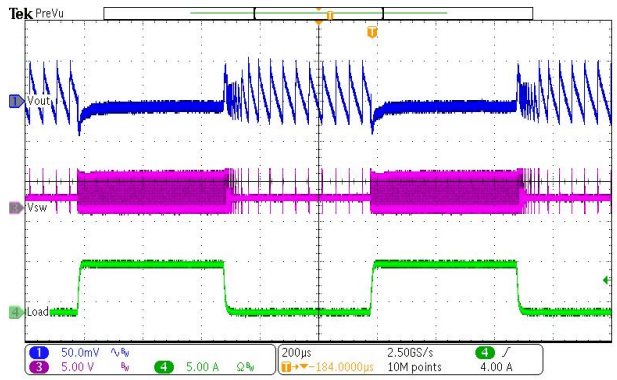
V_{IN} = 5 V, V_{OUT} = 1.2 V, I_{OUT} = 0 A, PFM

Figure 6. Enable on



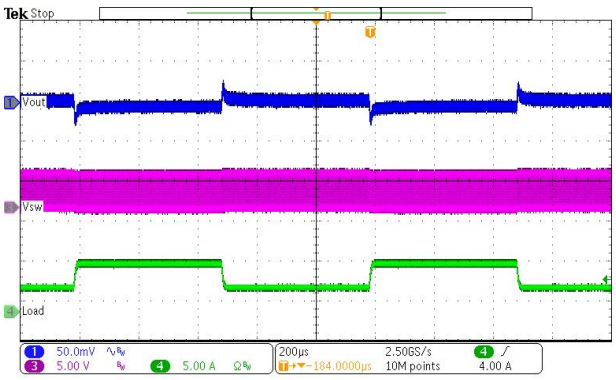
V_{IN} = 5 V, V_{OUT} = 1.2 V, I_{OUT} = 0 A, PFM

Figure 7. Enable off



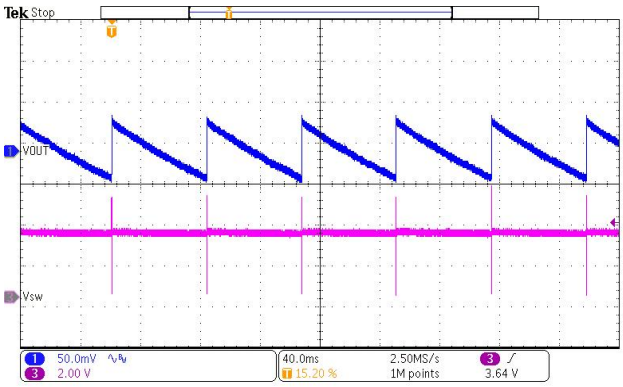
V_{IN} = 5 V, V_{OUT} = 1.2 V, I_{OUT} = 0 A ~ 6 A, PFM

Figure 8. Load transient



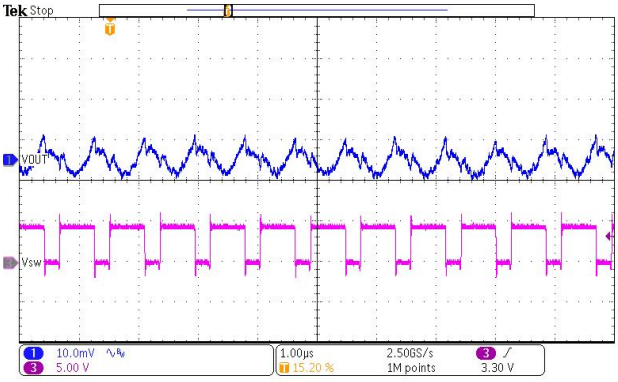
V_{IN} = 5 V, V_{OUT} = 1.2 V, I_{OUT} = 3 A~ 6 A, PFM

Figure 9. Load transient



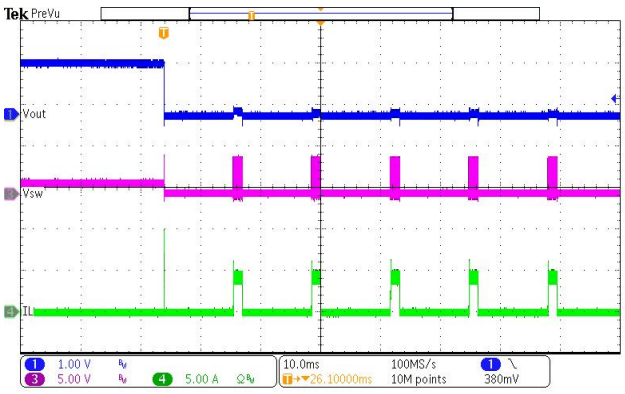
V_{IN} = 5 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A, PFM

Figure 10. Ripple



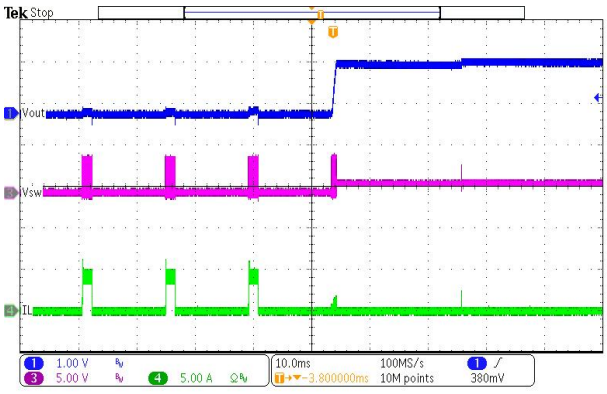
V_{IN} = 5 V, V_{OUT} = 3.3 V, I_{OUT} = 6 A, PWM

Figure 11. Ripple



V_{IN} = 5 V, V_{OUT} = 1.2 V, No Load -> short

Figure 12. Short-circuit protection



V_{IN} = 5 V, V_{OUT} = 1.2 V, short -> No load

Figure 13. Short-circuit recovery

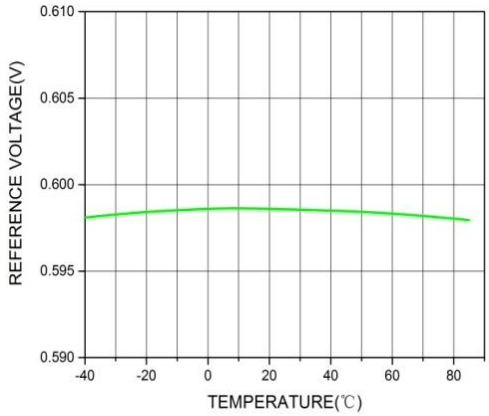


Figure 14. Reference voltage vs. Temperature

Detailed Description

The DIO6145P is a step-down DC/DC converter with power MOSFETs integrated. It is able to provide a continuous output current of up to 6 A. The output voltage can be regulated as low as 0.6 V. It uses COT architecture with input voltage feed-forward to stabilize the switching frequency over its full input voltage range. During light loads, the DIO6145P employs a proprietary control over the low-side MOSFET (LS-FET) and inductor current to improve efficiency.

COT architecture

When compared to fixed-frequency PWM control, COT control offers a simpler control loop and faster transient response. By using input voltage feed-forward, the DIO6145P maintains a nearly constant switching frequency across the input and output voltage ranges. The switching pulse on time can be estimated with Equation:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 0.83\ \mu s \quad (1)$$

To prevent inductor current runaway during the load transient, the DIO6145P has a fixed minimum off time of 60 ns. However, this minimum off-time limit does not impact the operation of the DIO6145P in steady-state.

Sleep mode operation

The DIO6145P adopts sleep-mode to achieve high efficiency under extremely light load condition. In such sleep-mode, most of the circuitry is turned off, except the EA (error amplifier) and the PWM comparator, which results in minimum operation current as shown in Figure 15.

When the loading gets lighter, the ripple of the output voltage is bigger and therefore the DIO6145P enters sleep mode. Under the sleep-mode situation, the valley of the FB pin voltage is regulated to the internal reference voltage. Thus, the average output voltage is slightly higher than the output voltage in DCM or CCM mode. The on-time pulse in sleep mode is about 40% larger than that under DCM or CCM mode. Figure 16 shows the average FB pin voltage relationship with the internal reference in sleep mode.

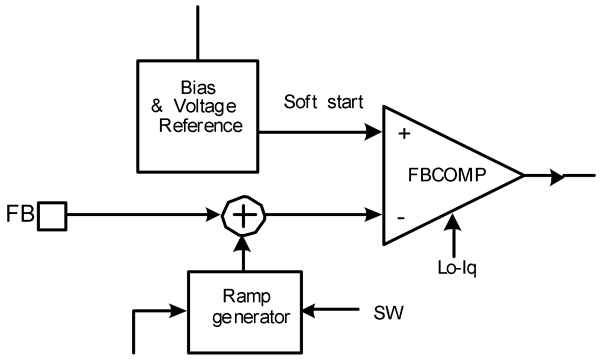


Figure 15. Operation blocks at sleep mode

Figure 16. FB average voltage at sleep mode

Light-load mode

During light loads, the DIO6145P uses a proprietary control scheme to save power and improve efficiency: there is a zero current cross circuit to detect if the inductor current starts to reverse. LS-FET turns off immediately when the inductor current starts to reverse and trigger the ZCD in discontinuous conduction mode (DCM) operation.

Considering the internal circuit propagation time, the typical delay is 50 ns. It means the inductor current still falls after the ZCD is triggered in this delay. If the inductor current falling slew rate is fast (V_{OUT} voltage is high or close to V_{IN}), the low side MOSFET is turned off and the inductor current may be negative. This phenomenon will cause the DIO6145P not to enter DCM operation. If the DCM mode is required, the off time of low-side MOSFET in CCM should be longer than 100 ns. For example, if V_{IN} is 3.6 V and V_O is 3.3 V, the off time in CCM is 70 ns. It is difficult to enter DCM at a light load. And using a smaller inductor can improve it and make it enter DCM easily.

Enabled situation

When the input voltage exceeds the undervoltage lockout (UVLO) threshold(typically 2.55 V), the DIO6145P can be enabled by pulling the EN pin above 1.6 V. Leaving the EN pin floating or grounded will disable the DIO6145P. There is an internal 1 MΩ resistor from the EN pin to ground.

Mode selection and analog voltage dynamic regulation

The DIO6145P offers programmable PWM and PFM work modes. When MODE/VCON pin is more than 1.2 V, the DIO6145P enters PWM mode. When MODE/VCON pin is lower than 0.4 V or floating, the DIO6145P enters PFM mode. PFM mode can achieve high efficiency by the light-load operation described above. PWM mode can keep a constant switch frequency and smaller V_O ripple, but it has lower efficiency at light load.

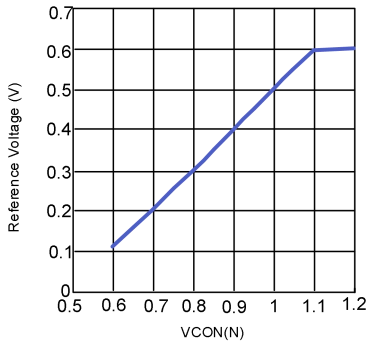


Figure 17. Reference voltage change with VCON

The DIO6145P can dynamically regulate output voltage by MODE/VCON pin to meet some situation need and change output voltage directly. When MODE/VCON pin get an appropriate voltage value (from 0.6 V to 1.1 V), the DIO6145P will work with PWM mode and the internal reference voltage changes smoothly to achieve a new output voltage without changing the external resistor divider as Figure 17 shows. When VCON function is enabled and set the reference voltage from 0.35 V to 0.6 V, the accuracy is 3% typically. When set the reference voltage from 0.1 V to 0.35 V, the accuracy is 10% typically. Detail reference voltage calculation formula such as the following Equation:

$$Ref(V) = 0.985 \times V_{CON(V)} - 0.486 \quad (2)$$

Soft-start details

The DIO6145P has a built-in soft-start that ramps up the output voltage at a constant slew rate that avoids

overshooting at startup. The soft-start time is typically about 700 µs.

Pre-bias startup

The DIO6145P supports start-up with a pre-bias output voltage. If the internal SS voltage is lower than the FB voltage, the HS-FET and LS-FET remain off until the SS voltage crosses the FB voltage.

Power-good indicator

The DIO6145P has an open drain with a 500 kΩ pull-up resistor as a power-good (PG) indication. When the FB voltage is within 10% of the regulation level, the power-good pin is pulled up to VIN. Otherwise, the power-good pin is pulled to ground by an internal MOSFET. The MOSFET has a maximum R_{DSON} of less than 100 Ω.

Current limit

The DIO6145P provides HS-FET current limiting. When the current through the HS-FET arrives at 8.2 A, the DIO6145P enters hiccup mode until the current drops to prevent the inductor current from rising and possibly damaging the components.

Short-circuit protection and recovery

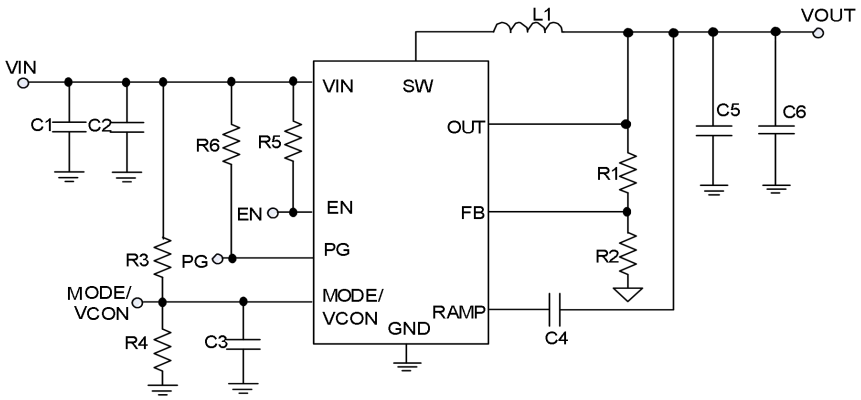
The DIO6145P enters short-circuit protection (SCP) mode when it hits the current limit, and tries to recover from the short-circuit by entering hiccup mode. In SCP, the DIO6145P disables the output power stage, discharges a soft-start capacitor, and then enacts a soft-start procedure. If the short-circuit condition still holds after the soft-start ends, the DIO6145P repeats this operation until the short-circuit ceases and output rises back to the regulation level.

100% duty cycle mode

When the input voltage reduces and is lower than the regulation output voltage, the output voltage drops and the on-time increases. Further reducing the input voltage drives the DIO6145P into 100% duty cycle mode. The high-side switch is always on, and the output voltage is determined by the loading current times the R_{DSON} composed of the high-side switch and inductor.

Application Information

Typical application circuit



Note: V_{IN} < 3.6 V may need more input capacitor.

Figure 18. Typical application circuit for V_{IN} = 5 V, I_{OUT} = 6 A

Component selection

Setting the output voltage

The external resistor divider sets the output voltage (see the typical application schematic). The feedback resistor R1 is typically between 40 kΩ to 200 kΩ, which can reduce the V_{OUT} leakage current. There is no strict requirement for a feedback resistor. R1 > 10 kΩ is reasoned for some applications. R2 can be calculated with Equation:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6} - 1} \quad (3)$$

The feedback circuit is shown in Figure 19:

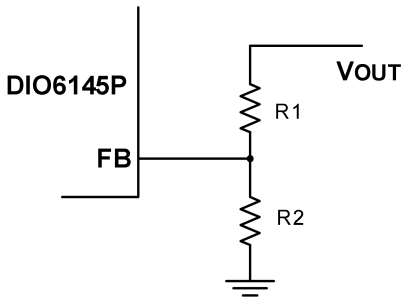


Figure 19. Feedback network

Table 1 lists the recommended resistors values for common output voltages:

Table 1. Resistor values for common output voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	200 (1%)	300 (1%)
1.2	200 (1%)	200 (1%)
1.8	200 (1%)	100 (1%)
2.5	200 (1%)	63.2 (1%)
3.3	200 (1%)	44.2 (1%)

Selecting the inductor

Most applications are recommended to use low value inductors, such as 0.47 μH, in order to achieve high efficiency under light load. For highest efficiency, chose an inductor with a DC resistance less than 30 mΩ. For most designs, the inductance value can be derived from the following equation.

$$L_1 = \frac{V_{OUT} \times (1 - \frac{V_{OUT}}{V_{IN}})}{\triangle I_L \times f_{OSC}} \quad (4)$$

Where ΔI_L is the inductor ripple current.

Choose an inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\triangle I_L}{2} \quad (5)$$

Selecting the input capacitor

The input current to the step-down converter is discontinuous and requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR values and a small 22 μF capacitor is sufficient for a higher output system stability.

Because the input capacitor absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (6)$$

The worst case condition occurs at V_{IN} = 2 V_{OUT}, where:

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (7)$$

For simplification, choose an input capacitor whose RMS current rating is greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, use a small high-quality ceramic capacitor (0.1 μF) placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\triangle V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

Selecting the output capacitor

The output capacitor stabilizes the DC output voltage. Ceramic capacitors are recommended. Low ESR capacitors are preferred to limit the output voltage ripple. Estimate the output voltage ripple as:

$$\triangle V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_S \times C2}) \quad (9)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, the output voltage ripple can be estimated as:

$$\triangle V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated as:

$$\triangle V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

The characteristics of the output capacitor also affect the stability of the regulation system. For the DIO6145P, 2pcs 22 μF C_O can satisfy most applications. Add C_O can reduce DCM and CCM output ripple effectively. However, a very large C_O may cause light group pulse in sleep mode.

Load transient optimization

The DIO6145P can add a capacitor (Cc) between the ramp pin and the output sense pin to improve load transient. The larger Cc value is, the faster load transient respond speed is. A typical Cc 22 pF trades off load transient and loop stability, maximum Cc is less than 200 pF in case of SW instability issue. Further, the DIO6145P internally has optimized compensation block to cover most application. The Ramp pin can be floated in normal application.

PCB layout recommendation

Proper layout of the switching power supplies is very important and sometimes critical to make it work properly. Especially, for the high switching converter, if the layout is not carefully done, the regulator could show poor line or load regulation stability issues.

For the DIO6145P, the high speed step-down regulator, the input capacitor should be placed as close as possible to the IC pins. As shown in Figure 20, the 0805 size ceramic capacitor is used. Please make sure the two ends of the ceramic capacitor be directly connected to pin 8 (the power input pin) and pin 10/11/12 (the power GND pins).

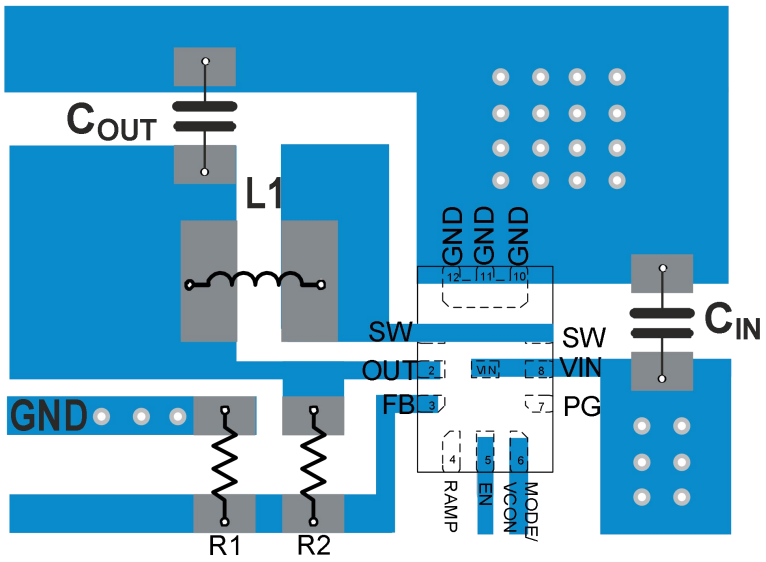
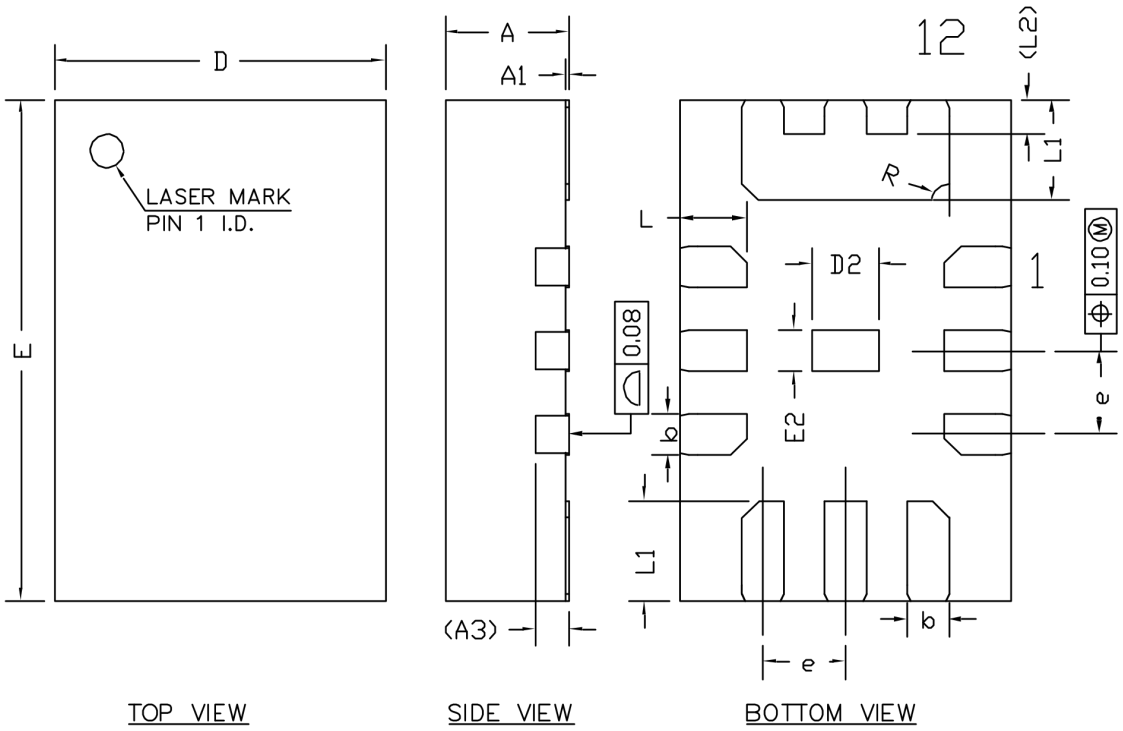


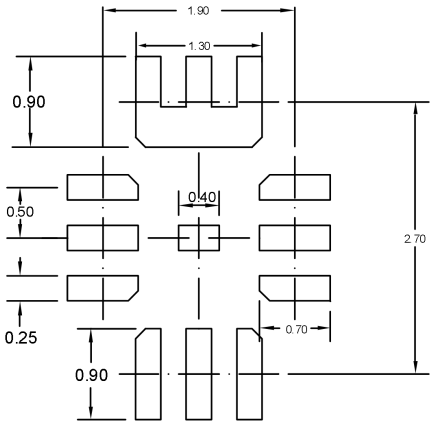
Figure 20. Two ends of Input decoupling capacitor close to pin 8 and pin 10/11/12

Physical Dimensions: QFN2*3-12



TOP VIEW SIDE VIEW BOTTOM VIEW

SIDE VIEW

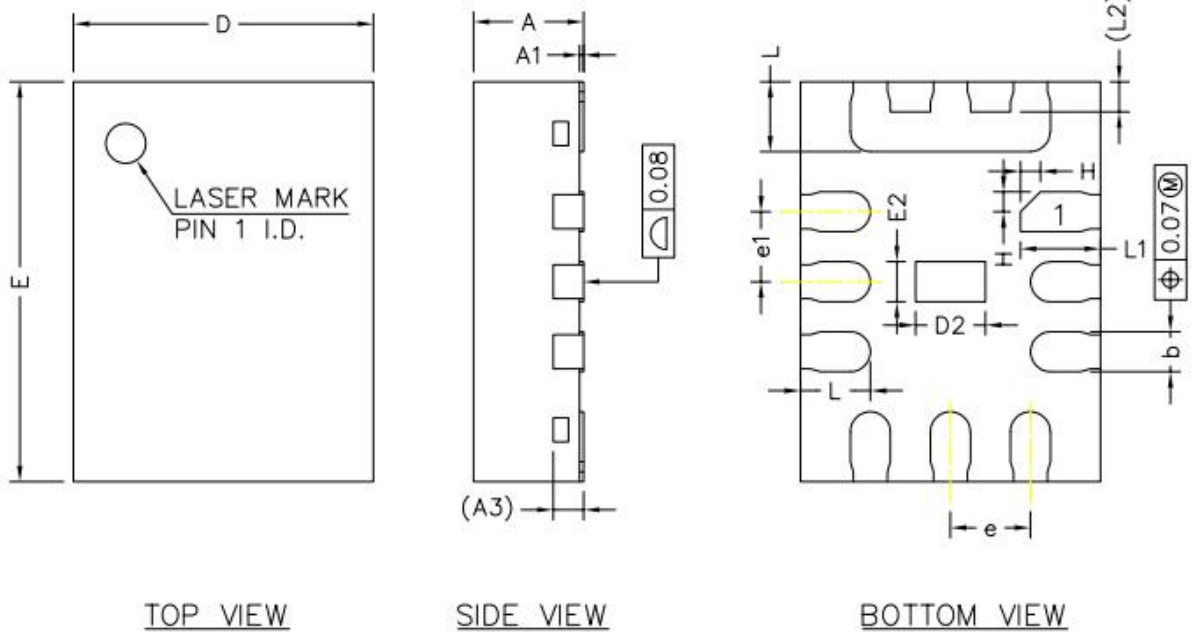


Recommended Land Pattern

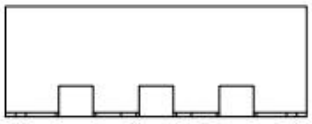
Common Dimensions (Units of measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.20	0.25	0.30
D	1.90	2.00	2.10
E	2.90	3.00	3.10
D2	0.35	0.40	0.45
E2	0.20	0.25	0.30
e	0.40	0.50	0.60
L	0.35	0.40	0.45
L1	0.55	0.60	0.65
L2		0.200 REF	
R		0.100 REF	

Note：10 μm thickness PI layer added.

Physical Dimensions: QFN2*1.5-12



TOP VIEW SIDE VIEW BOTTOM VIEW



SIDE VIEW

Common Dimensions (Units of measure = Millimeter)			
Symbol	Min	Nom	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D	1.40	1.50	1.60
E	1.90	2.00	2.10
D2	0.30	0.35	0.40
E2	0.15	0.20	0.25
e	0.35	0.40	0.45
e1	0.30	0.35	0.40
H		0.10 REF	
L	0.30	0.35	0.40
L1	0.35	0.40	0.45
L2		0.15 REF	

Note：10 μm thickness PI layer added.

CONTACT US

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