DIO5613
Triple-Output AMOLED Display Power Supply

Features

- Input Voltage Range: 2.9V~4.5V
- Synchronous Boost Converter (AVDD)
  - 5.8V to 7.9V Output Voltage (programmable)
  - 6.1V Default Output Voltage
  - 1% Accuracy
  - 160mA Output Current Protection (±20%)
  - V_I to V_O and V_O to V_I Isolation
- Synchronous Boost Converter (ELVDD)
  - 4.6V to 5V Output Voltage (programmable)
  - 4.6V Default Output Voltage
  - 0.5% Accuracy
  - 700mA Output Current Capability
  - External Output Voltage Sensing Pin for Load Drop Compensation
  - V_I to V_O and V_O to V_I Isolation
- Synchronous Inverting Buck-Boost Converter (ELVSS)
  - –5.4V to –1.4V Output Voltage (programmable)
  - –2.5V Default Output Voltage
  - 1% Accuracy at –2.5V (±30mV)
  - 700mA Output Current Capability
  - V_I to V_O and V_O to V_I Isolation
- Single-Wire Digital Interface for Programming
- VELVSS Start-up Delay: 40ms
- Short Circuit and OLP Detect time: 4ms
- Thermal Shutdown
- Available in TQFN3*3-16 Package

Descriptions

The DIO5613 is designed to drive AMOLED displays (Active Matrix Organic Light Emitting Diode) requiring $V_{(AVDD)}$, $V_{(ELVDD)}$ and $V_{(ELVSS)}$. The device integrates a boost converter for $V_{(ELVDD)}$, an inverting buck-boost converter for $V_{(ELVSS)}$ and a boost converter for $V_{(AVDD)}$, which are suitable for battery operated products. The digital interface control pin (CTRL) allows programming $V_{(AVDD)}$, $V_{(ELVDD)}$ and $V_{(ELVSS)}$ in digital steps. The DIO5613 uses a novel technology enabling excellent line and load regulation.

Applications

- Smartphones
- Small Size Tablets
- Active Matrix OLED Displays ≤ 8

Ordering Information

Order Part Number	Top Marking		T_A	Package	
DIO5613CL16	DEF3	Green	-40 to 85°C	TQFN3*3-16	Tape & Reel, 5000

Pin Assignment

TQFN3*3-16

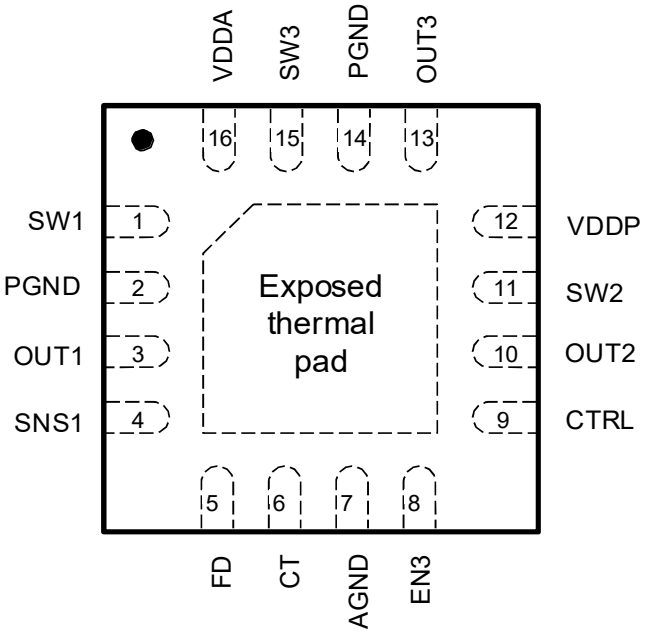


Figure 1. Top View

Pin Descriptions

Name	Description
SW1	Switch pin of the ELVDD boost converter.
PGND	Power ground of the ELVDD boost converter.
OUT1	Output of the ELVDD boost converter.
SNS1	ELVDD sense input.
FD	Active discharge enable / disable during shut-down.
CT	Control of the ELVSS transition time.
AGND	Analog ground.
EN3	Enable AVDD boost converter.
CTRL	Enable ELVDD boost converter and delayed ELVSS inverting buck-boost converter. Digital programming.
OUT2	Output of the ELVSS inverting buck-boost converter.
SW2	Switch pin of the ELVSS inverting buck-boost converter.
VDDP	Supply for ELVSS inverting buck-boost converter.
OUT3	Output of the AVDD boost converter.
PGND	Power ground of the AVDD boost converter.
SW3	Switch pin of the AVDD boost converter.
VDDA	Supply for the internal analog circuits.
Exposed thermal pad	Connect this pad to AGND and PGND.

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter		Rating	Unit
Voltage	VDDP, VDDA, EN3, CTRL, CT, FD, SW1, OUT1, SNS1	-0.3 to 6	V
	SW3, OUT3	-0.3 to 10	V
	OUT2	-6.5 to 0.3	V
	SW2	-6.5 to 5.5	V
Operating Junction temperature		-40 to 150	°C
Storage temperature range, T_{stg}		-65 to 150	°C
Junction-to-ambient thermal resistance, $R_{\theta JA}$		42.9	°C/W
ESD	HBM	±2000	V

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	MIN	NOM	MAX	Unit
V_I	Supply input voltage range	2.9	3.7	4.5	V
T_J	Operating Junction temperature	-40		125	°C
ELVDD BOOST Converter (OUT1)					
V_O	ELVDD boost converter output voltage range	4.6	4.6	5	V
L	Inductance	-30%	4.7	30%	μH
C_I	Input capacitance placed at the inductor	2.5	5		μF
C_O	Output capacitance placed at OUT1 pin	10	20	44	μF
ELVSS Inverting BUCK-BOOST Converter (OUT2)					
V_O	ELVSS inverting buck-boost output voltage range	-5.4	-2.5	-1.4	V
L	Inductance	-30%	4.7	30%	μH
$C_{(VDDP)}$	Input capacitance placed at VDDP pin	2.5	5		μF
C_O	Output capacitance placed at OUT2 pin	20	30	66	μF
$C_{(CT)}$	CT-pin capacitance			300	nF
AVDD BOOST Converter (OUT3)					
V_O	AVDD boost converter output voltage range	5.8	6.1	7.9	V
L	Inductance	-30%	10	30%	μH
C_I	Input capacitance placed at the inductor	2.5	5		μF
C_O	Output capacitance placed at OUT3 pin	2.5	5	24	μF

Electrical Characteristics

V_I = 3.7V, CTRL = V_I, EN3 = V_I, $V_{(ELVDD)}$ = 4.6V, $V_{(ELVSS)}$ = –2.5V, $V_{(AVDD)}$ = 6.1V, T_J = –40°C to 85°C, typical values are at T_J = 25°C (unless otherwise noted).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply and Thermal Protection						
V_I	Operating Input Voltage		2.9	3.7	4.5	V
	Shutdown current into V_I	$V_{(CTRL)}$=$V_{(EN3)}$=GND, $V_{(FD)}$=3.7V or GND		0.1		μA
V_{IT-}	Under-voltage lockout threshold (VDDA)	V_I falling	2.2	2.3	2.4	V
V_{IT+}		V_I rising	2.35	2.45	2.55	V
	Thermal shutdown temperature	Junction temperature rising		135		°C
	Thermal shutdown hysteresis	Junction temperature falling		10		°C
Logic Signals (EN3, CTRL, FD)						
V_{IH}	High-level input voltage (EN3, CTRL, FD)	V_I = 2.9V to 4.5V	1.2			V
V_{IL}	Low-level input voltage (EN3, CTRL, FD)	V_I = 2.9V to 4.5V			0.4	V
	Pull-down resistance (EN3, CTRL)		250	500	900	kΩ
ELVDD BOOST Converter (OUT1)						
V_O	Output voltage (OUT1)		4.6	4.6	5	V
	Output voltage accuracy (OUT1)	T_J = 25°C, no load	-0.5%		0.5%	
		–40°C ≤ T_J ≤ 85°C, no load	-0.8%		0.8%	
$r_{DS(on)}$	MOSFET on-state resistance (Q1)	I_{DS} = 100mA		125		mΩ
$r_{DS(on)}$	MOSFET on-state resistance (Q2)	I_{DS} = 100mA		155		mΩ
	Current limit (Q1)	Inductor valley current		2		A
	Short-circuit threshold in operation (SNS1)	Percentage of nominal V_O	85%	90%	95%	
	Voltage-sensing threshold (OUT1)	$V_{(OUT1)}$ – $V_{(SNS1)}$ increasing	200	300	450	mV
	Voltage-sensing threshold (SNS1)	$V_{(OUT1)}$ – $V_{(SNS1)}$ decreasing	100	200	350	mV
	Off current (combined) (OUT1, SNS1)	$V_{(FD)}$ = $V_{(CTRL)}$) = GND		0.8	5	μA
$R_{(SNS1)}$	Pull-down resistance (SNS1)			4		MΩ
	Discharge resistance (OUT1)	$V_{(CTRL)}$ =GND, I_O = 1mA	15	30	55	Ω
	Line regulation	I_O = 100mA, V_I = 2.9V to 4.5V		0.01		%/V
	Load regulation	1mA ≤ I_O ≤ 800mA		0.1		%/A

Specifications subject to change without notice.

Electrical Characteristics (continued)

V_I = 3.7V, CTRL = V_I, EN3 = V_I, $V_{(ELVDD)}$ = 4.6V, $V_{(ELVSS)}$ = –2.5V, $V_{(AVDD)}$ = 6.1V, T_J = –40°C to 85°C, typical values are at T_J = 25°C (unless otherwise noted).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
ELVSS Inverting BUCK-BOOST Converter (OUT2)						
V_O	Output voltage (OUT2)		-1.4	-2.5	-5.4	V
	Output voltage accuracy (OUT2)	T_J = 25°C, no load	-30		30	mV
		–40°C ≤ T_J ≤ 85°C, no load	-50		50	mV
$r_{DS(on)}$	MOSFET on-state resistance (Q3)	I_{DS} = 100mA		110		mΩ
$r_{DS(on)}$	MOSFET on-state resistance (Q4)	I_{DS} = 100mA		100		mΩ
	Current limit (Q3)	Inductor peak current		3.2		A
	Off current (OUT2)	$V_{(FD)}$ = $V_{(CTRL)}$ = GND		0.01	5	μA
	Discharge comparator threshold (OUT2)		-950	-700	-400	mV
	Discharge resistance (OUT2)	$V_{(CTRL)}$ =GND, I_O = 1mA	130	150	175	Ω
$R_{(CT)}$	Output resistance (CT)		150	325	500	kΩ
	Input threshold voltage (CT)	$V_{(CT)}$ rising	10	50	200	mV
	Line regulation	I_O = 100mA, V_I = 2.9V to 4.5V		0.02		%/V
	Load regulation	1mA ≤ I_O ≤ 800mA		-0. 5		%/A
AVDD BOOST Converter (OUT3)						
V_O	Output voltage (OUT3)		5.8	6.1	7.9	V
	Output voltage accuracy (OUT3)	–40°C ≤ T_J ≤ 85°C, no load	-1%		1%	
$r_{DS(on)}$	MOSFET on-state resistance (Q5)	I_{DS} = 100mA		500		mΩ
$r_{DS(on)}$	MOSFET on-state resistance (Q6)	I_{DS} = 100mA		1200		mΩ
	Current limit (Q5)	Inductor peak current		0.4		A
	Overload current threshold (OUT3)			160		mA
	Short-circuit threshold voltage (OUT3)	Percentage of nominal V_O	85	90	95	%
	Off current (OUT3)	$V_{(FD)}$ = $V_{(EN3)}$ = GND		1.5	5	μA
	Discharge resistance (OUT3)	$V_{(EN3)}$ = GND, I_O = 1mA	15	30	55	Ω
	Line regulation	I_O = 30mA, V_I = 2.9V to 4.5V		0.02		%/V
	Load regulation	1mA ≤ I_O ≤ 80mA		-0.4		%/A

Timing Requirements

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
CTRL Interface						
t_w	High-level pulse duration (CTRL)		2	10	25	μs
	Low-level pulse duration (CTRL)		2	10	25	μs
$t_{d(reset)}$	Reset time to ensure proper logic reset			50		μs

Switching Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
CTRL Interface						
$t_{d(on)}$	Turn-on delay time			300	400	us
$t_{d(off)}$	Turn-off delay time		30		80	us
$t_{d(store)}$	Data storage / accept time period		30		80	us
Protection and Discharge						
$t_{d(short)}$	Short-circuit detection delay during start up (OUT1)		32	40	48	ms
	Short-circuit detection delay during operation (OUT1)		3.2	4	4.8	ms
	Short-circuit detection delay during start up (OUT2)		32	40	48	ms
	Short-circuit detection delay during operation (OUT2)		3.2	4	4.8	ms
	Short-circuit detection delay during operation (OUT3)		3.2	4	4.8	ms
$t_{d(overload)}$	Overload detection delay (OUT3)		3.2	4	4.8	ms
$t_{d(discharge)}$	Discharge time after CTRL goes high (OUT2)		32	40	48	ms
Switching Frequency						
	AVDD boost converter switching frequency	I_O = 30mA	1.3	1.6	1.75	MHz
	ELVDD boost converter switching frequency	I_O = 30mA	1.3	1.6	1.75	MHz
	ELVSS inverting buck-boost converter switching frequency	I_O = 100mA		1.6		MHz
ELVSS BUCK-BOOST Converter Transition Time Control (CT)						
	Transition time programmed to 'fast'	V_O = –2.5V to –3V		5		µs
	Transition time programmed to 12ms			12		ms

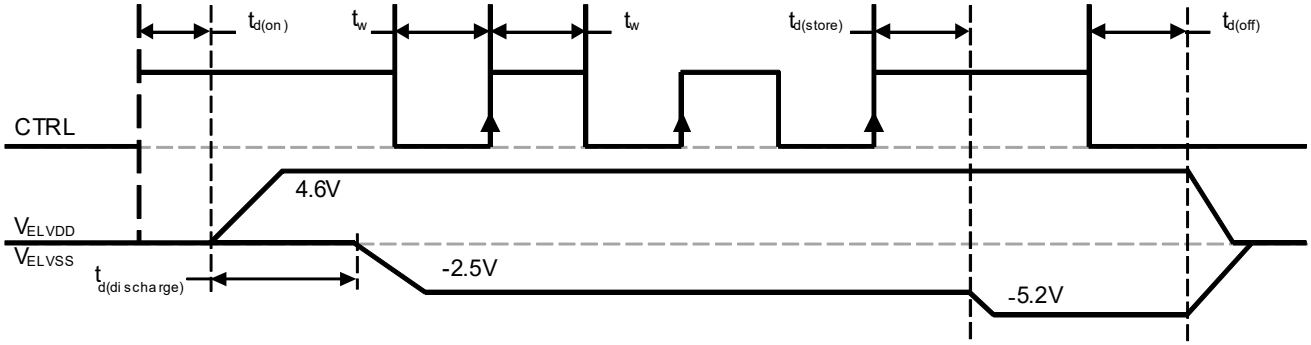
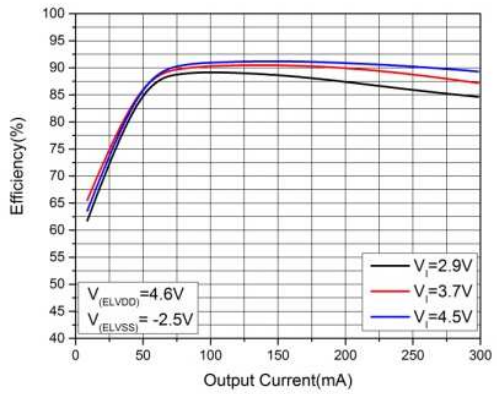


Figure 2. Timing Diagram

Typical Performance Characteristic

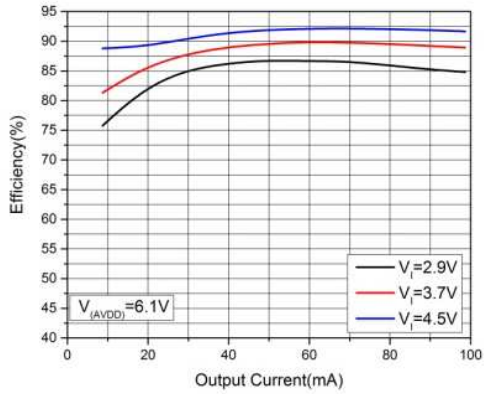
Typically at T_J = 25°C (unless otherwise noted).



$V_{(ELVDD)}$=4.6V $V_{(ELVSS)}$=-2.5V V_I=2.9V, 3.7V, 4.5V

EN3=GND CTRL=V_I

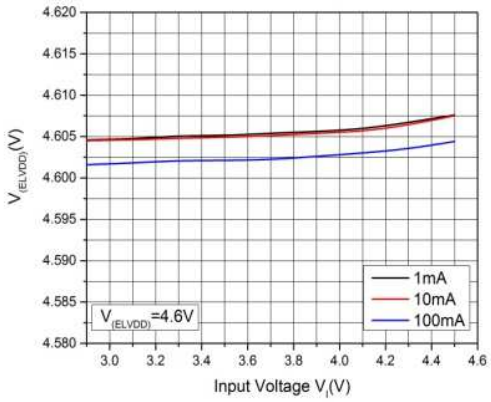
Figure 3. $V_{(ELVDD)}$ and $V_{(ELVSS)}$ Combined Efficiency



$V_{(AVDD)}$=6.1V V_I=2.9V, 3.7V, 4.5V

EN3= V_I CTRL= GND

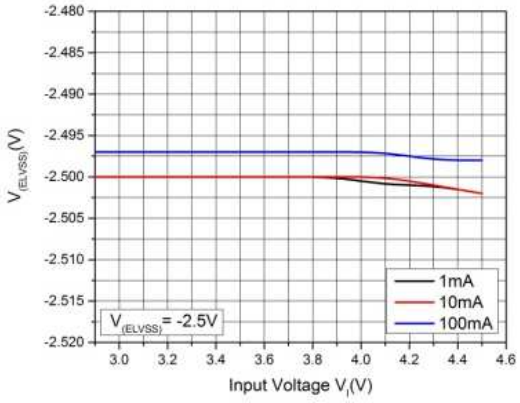
Figure 4. $V_{(AVDD)}$ Efficiency



$V_{(ELVDD)}$=4.6V V_I=2.9V to 4.5V

EN3=GND CTRL=V_I

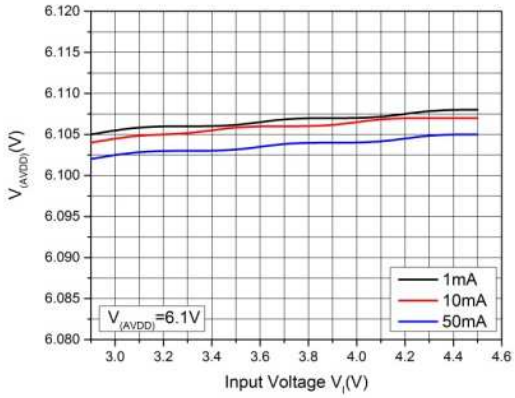
Figure 5. $V_{(ELVDD)}$ Line Regulation



$V_{(ELVSS)}$=-2.5V V_I=2.9V to 4.5V

EN3=GND CTRL=V_I

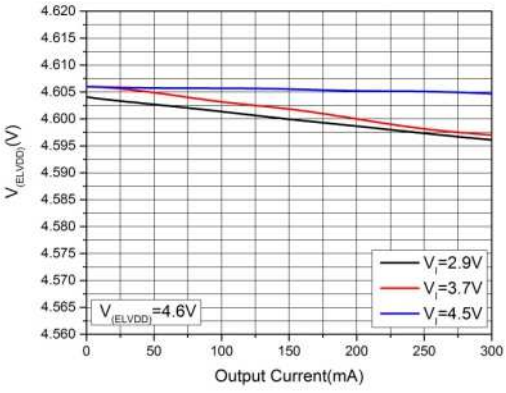
Figure 6. $V_{(ELVSS)}$ Line Regulation



$V_{(AVDD)}$=6.1V V_I=2.9V to 4.5V

EN3= V_I CTRL= GND

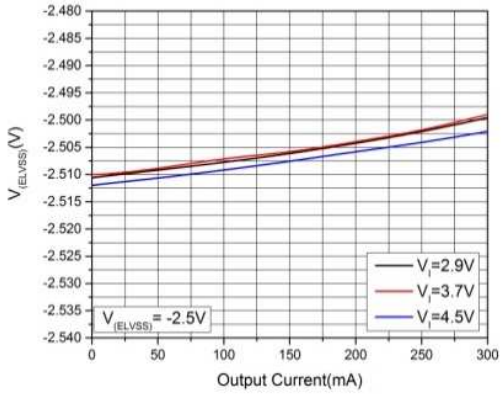
Figure 7. $V_{(AVDD)}$ Line Regulation



$V_{(ELVDD)}$=4.6V V_I=2.9V, 3.7V, 4.5V

EN3 = GND CTRL= V_I

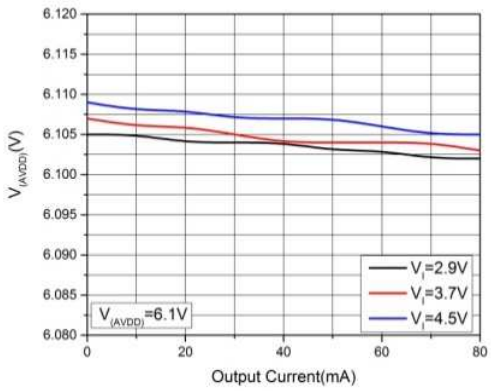
Figure 8. $V_{(ELVDD)}$ Load Regulation



$V_{(ELVSS)}$=-2.5V V_I=2.9V, 3.7V, 4.5V

EN3 = GND CTRL= V_I

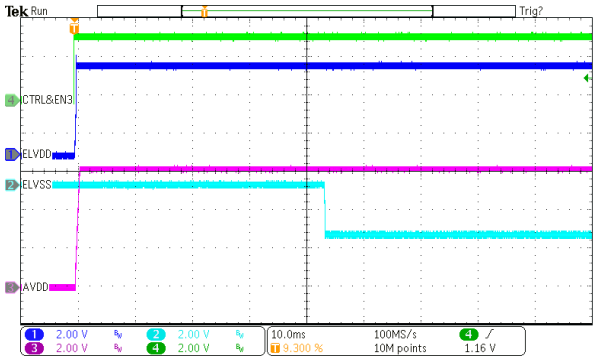
Figure 9. $V_{(ELVSS)}$ Load Regulation



$V_{(AVDD\ )}$=6.1V V_I=2.9V, 3.7V, 4.5V

EN3= V_I CTRL= GND

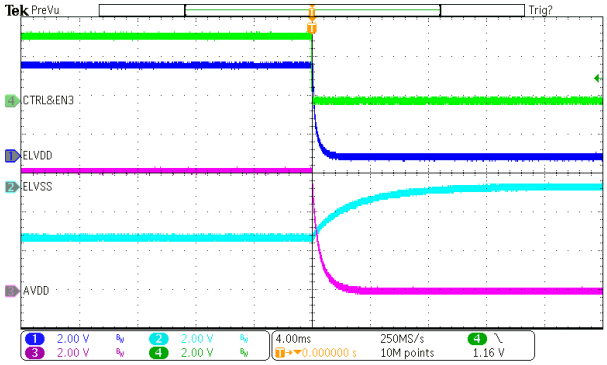
Figure 10. V(AVDD) Load Regulation



EN3= CTRL=3.3V FD=V_I=3.7V

$V_{(ELVDD)}$= 4.6V $V_{(ELVSS)}$= -2.5V $V_{AVDD)}$=6.1V

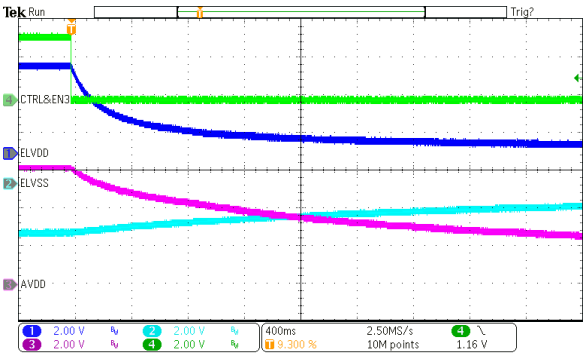
Figure 11. Start up Sequence



EN3= CTRL=3.3V FD=V_I=3.7V

$V_{(ELVDD)}$= 4.6V $V_{(ELVSS)}$= -2.5V $V_{AVDD)}$=6.1V

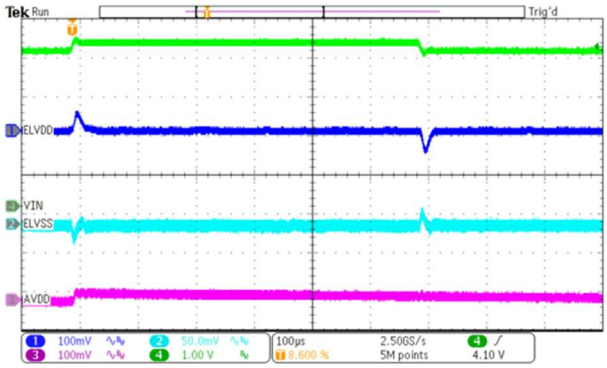
Figure 12. Shutdown Sequence Discharge=ON



EN3= CTRL=3.3V FD=GND V_I=3.7V

$V_{(ELVDD)}$= 4.6V $V_{(ELVSS)}$= -2.5V $V_{AVDD)}$=6.1V

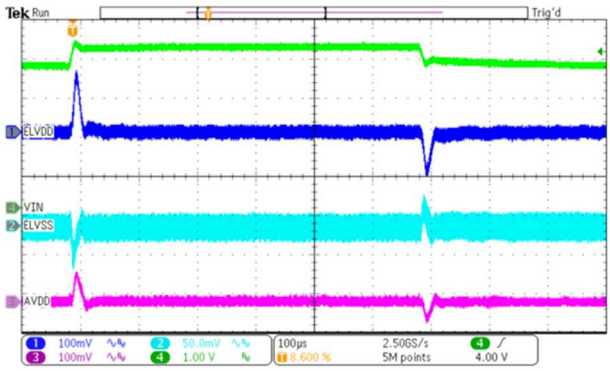
Figure 13. Shutdown Sequence Discharge=OFF



EN3= CTRL=FD= V_I V_I=3.7V to 4.2V

$I_{(ELVDD)}$= 0mA $I_{(ELVSS)}$= 0mA $I_{(AVDD)}$=0mA

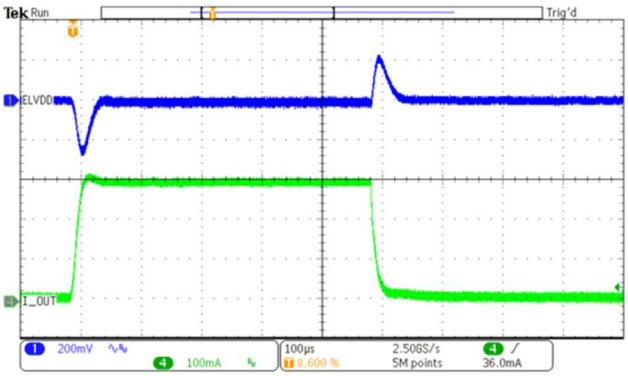
Figure 14. Line transient no load



EN3= CTRL=FD= V_I V_I=3.7V to 4.2V

$I_{(ELVDD)}$= 300mA $I_{(ELVSS)}$= 300mA $I_{(AVDD)}$=55mA

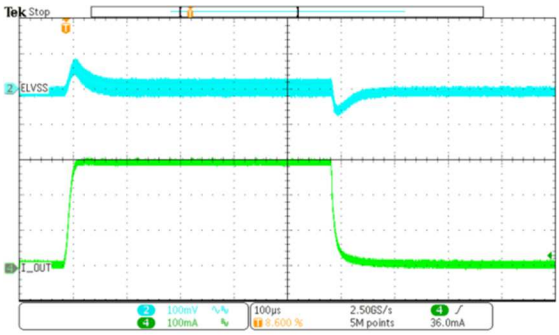
Figure 15. Line transient maximum load



EN3= CTRL=FD=V_I=3.7V

$I_{(ELVDD)}$= 10mA to 300mA $I_{(ELVSS)}$= 0mA $I_{(AVDD)}$=0mA

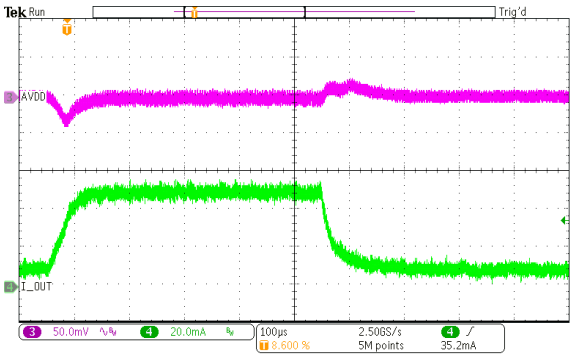
Figure 16. ELVDD Load transient



EN3= CTRL=FD=V_I=3.7V

$I_{(ELVDD)}$=0mA $I_{(ELVSS)}$= 10mA to 300mA $I_{(AVDD)}$=0mA

Figure 17. ELVSS Load transient



EN3= CTRL=FD=V_I=3.7V

$I_{(ELVDD)}$=0mA $I_{(ELVSS)}$=0mA $I_{(AVDD)}$=10mA to 50mA

Figure 18. AVDD Load transient

Detailed Description

Overview

The DIO5613 consists of two boost converters and an inverting buck-boost converter. $V_{(ELVDD)}$ is programmable in the range of 4.6V to 5V (default = 4.6V), $V_{(ELVSS)}$ is programmable in the range of –1.4V to –5.4V (default = –2.5V) and $V_{(AVDD)}$ is programmable between 5.8V and 7.9V (default = 6.1V). The transition time when $V_{(ELVSS)}$ is programmed to a different voltage is adjustable by the CT-pin capacitor or by digital programming.

Functional Block Diagram

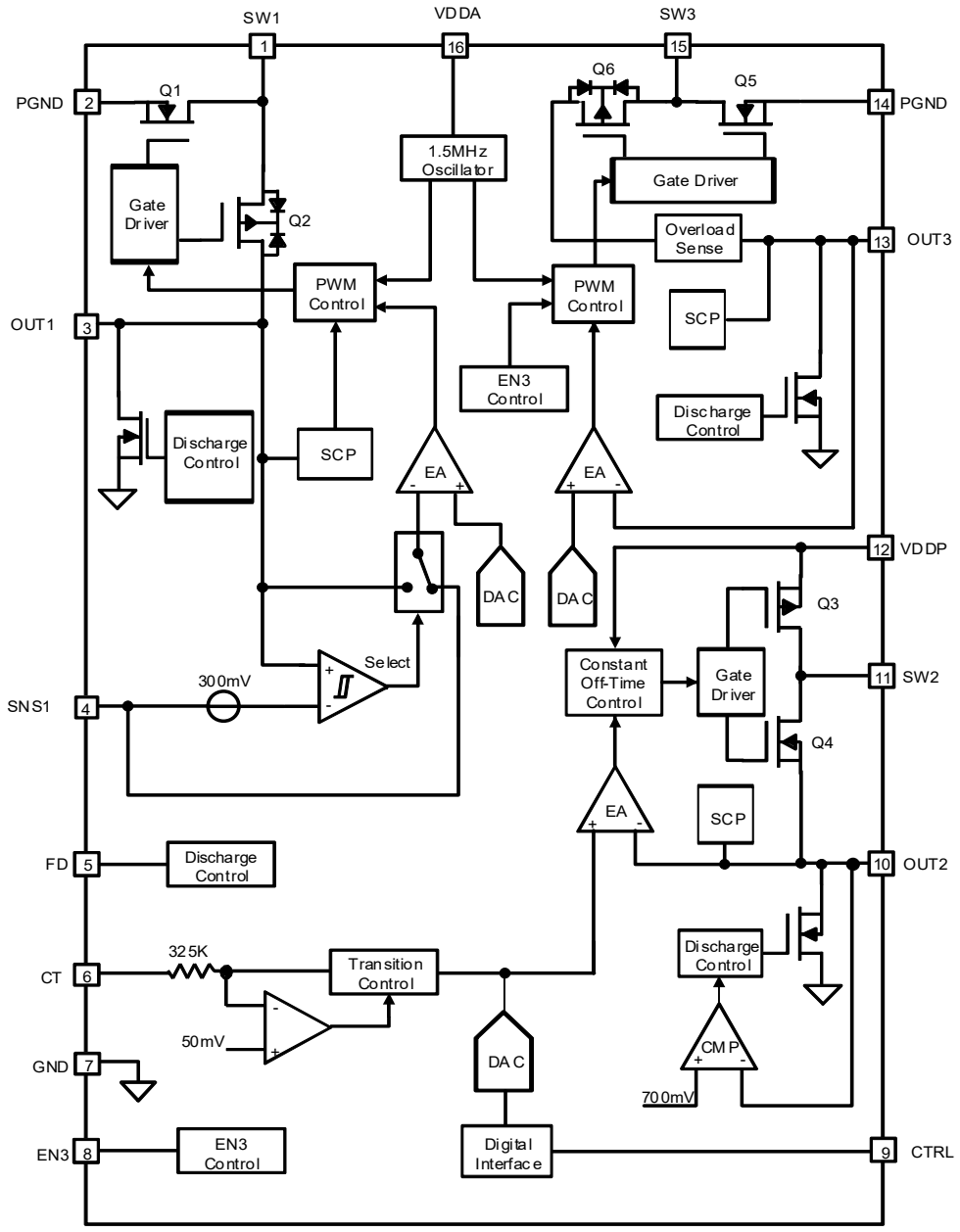


Figure 19. Function Block Diagram

Functional Description

Undervoltage Lockout

The device has a build in undervoltage lockout function that disables the device when the input supply voltage is too low for normal operation.

Thermal Shutdown

A thermal shutdown is implemented to prevent damage because of excessive heat and power dissipation. Once a temperature of typically 135°C is exceeded the device shuts down (the programming is not lost). When the temperature decreases to typ 130°C the device automatically restarts performing the start-up sequencing with the same voltages and programming as programmed before the thermal shutdown.

ELVDD Boost Converter (OUT1)

The ELVDD boost converter uses a fixed-frequency valley-current-mode topology. The output voltage $V_{(ELVDD)}$ is adjustable between 4.6V and 5V with a default voltage of 4.6V (see Table 1). In shutdown its output is fully isolated (input to output and output to input).

For the highest output voltage accuracy, connect the output sense pin (SNS1) directly to the positive pin of the output capacitor. If not used, the SNS1 pin can be left floating or connected to ground, then the output voltage is sensed at the OUT1 pin.

ELVSS Inverting Buck-Boost Converter (OUT2)

The ELVSS inverting buck-boost converter uses a constant-off-time peak-current-mode topology. The output voltage $V_{(ELVSS)}$ is adjustable between –5.4V and –1.4V with a default voltage of –2.5V (see Table 1). In shutdown its output is fully isolated (input to output and output to input).

AVDD Boost Converter (OUT3)

The AVDD boost converter uses a fixed-frequency peak-current-mode topology. The output voltage $V_{(AVDD)}$ is adjustable between 5.8V and 7.9V with a default voltage of 6.1V (see Table 1). In shutdown its output is fully isolated (input to output and output to input).

Start-up Sequence, Soft-Start and Shut-down

The device has an implemented soft-start which limits the inrush current. When V_I is applied, the Output Discharge is undefined until the rising edge of CTRL sets the Output Discharge to follow the FD-pin setting. When the converters are disabled all outputs are discharged if FD = high or high impedance if FD = low. If only the AVDD converter is disabled (EN3 = low, CTRL = high) a forward biased diode charges the AVDD output to V_I until CTRL = low, then the AVDD output is disconnected from V_I. The typical start-up sequence is shown in Figure 20.

- Pulling EN3 high starts the AVDD boost converter. $V_{(AVDD)}$ follows a linear 1.5ms long voltage ramp until it reaches its default value of 6.1V, the switch current is limited to typ. 0.4A.
- Pulling CTRL high starts the ELVDD boost converter. $V_{(ELVDD)}$ starts with a reduced switch current limit of 0.1A until it reaches its default voltage of 4.6V then the full current limit is released.
- 40ms after CTRL is pulled high the ELVSS inverting buck-boost converter starts. $V_{(ELVSS)}$ starts with a reduced switch current limit of 0.4A until it reaches its default voltage of –2.5V, then the full current limit is released.

All converters can start into an existing output voltage without generating a voltage drop at the output. When $V_{(ELVSS)}$ is < –0.7V during startup, the 40ms long discharge at $V_{(ELVSS)}$ is disabled to avoid a voltage drop.

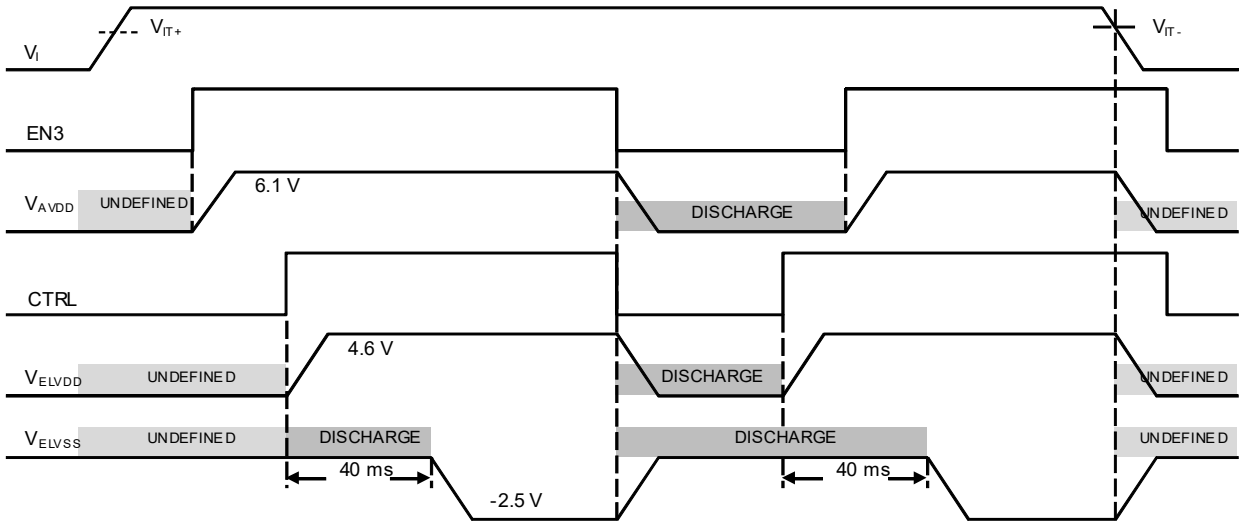


Figure 20. Start-up Sequencing Active Discharge Enabled

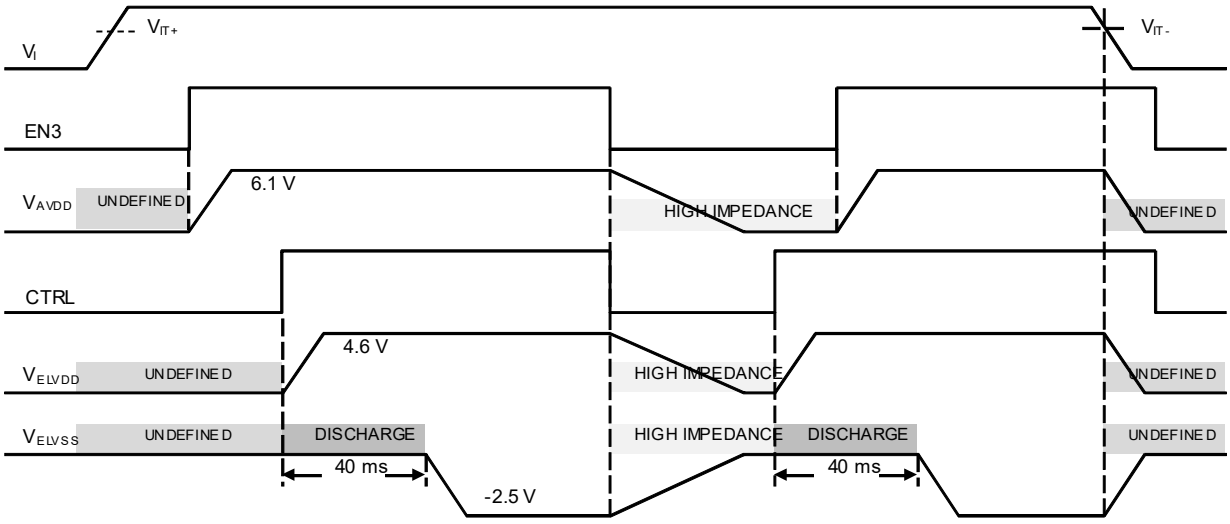


Figure 21. Start-up Sequencing Active Discharge Disabled

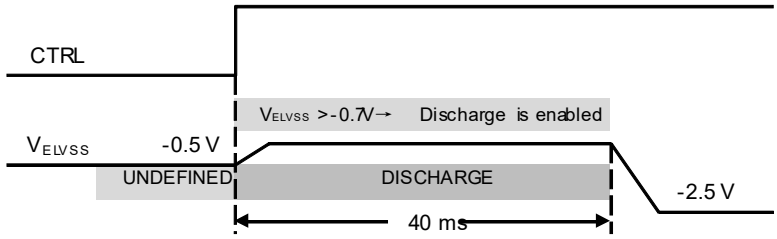


Figure 22. $V_{(ELVSS)}$ > -0.7V→Discharge is enabled

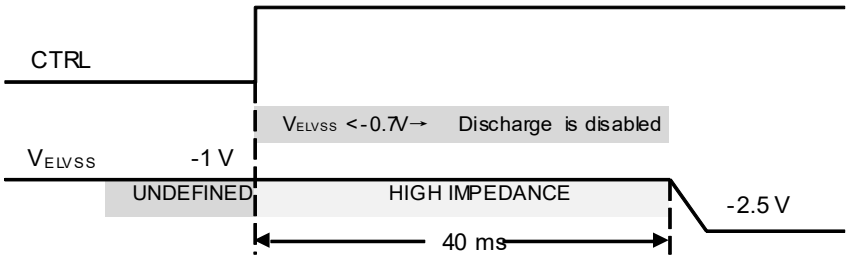


Figure 23. $V_{(ELVSS)}$ < -0.7V→Discharge is disabled

$V_{(ELVSS)}$ Transition Time Control (CT Pin)

The transition time is the time required to move $V_{(ELVSS)}$ from the actual voltage level to the new programmed voltage level. The transition time can be controlled by an external capacitor connected to the CT pin or by digital programming. The digital programming, 52 or 53 CTRL pulses, overwrites the CT pin setting until the function is reset. For the first $V_{(ELVSS)}$ voltage level change the transition time is as fast as possible, for all following $V_{(ELVSS)}$ changes the transition time is controlled by the capacitor connected to the CT pin or the programmed setting. The typical 50mV CT pin comparator detects when the CT pin is connected to GND or floating, then the fastest possible transition time is used. When a capacitor is connected the R-C time constant T sets the transition time. The output voltage is almost settled after 3T, which means 95% of the target voltage is reached.

$$T = \text{Internal CT resistance x external capacitor} = R_{(CT)} \times C_{(CT)} = 32k\Omega \times 100nF = 32.5ms \quad (1)$$

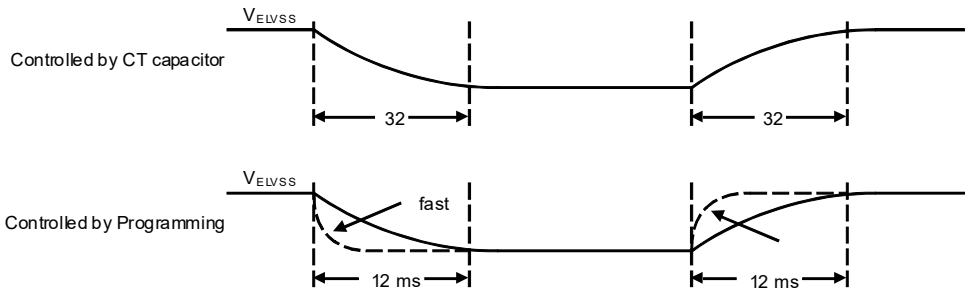


Figure 24. $V_{(ELVSS)}$ Transition Time Control

Digital Interface (CTRL Pin)

The digital interface allows programming of the positive output voltages $V_{(AVDD)}$, $V_{(ELVDD)}$ and the negative output voltage $V_{(ELVSS)}$ in discrete steps. By default the $V_{(ELVSS)}$ transition time and the Output Discharge during shutdown are controlled by the CT and FD pin, the setting can be overwritten by programming. If programming is not required the CTRL pin can also be used as a standard enable pin. Once the device is enabled the device starts with its default values (grey marked values in Table 1). The interface counts the rising edges applied to the CTRL pin and sets the new values as shown in Table 1. The settings are stored in a volatile memory, the reset behavior is described in the Device Reset section.

Table 1. Programming Table

Rising Edges	$V_{(ELVSS)}$	Rising Edges	$V_{(ELVSS)}$	Rising Edges	$V_{(AVDD)}$	Rising Edges	Outputs Discharge	Rising Edges	$V_{(ELVSS)}$ transition time	Rising Edges	$V_{(ELVDD)}$
0 / no pulse	–2.5 V	21	–3.4 V	0 / no pulse	6.1 V	0 / no pulse	controlled by FD pin	0 / no pulse	controlled by CT pin	0 / no pulse	4.6 V
1	–5.4 V	22	–3.3 V	42	7.9 V	50	ON	52	fast	54	4.7 V
2	–5.3 V	23	–3.2 V	43	7.6 V	51	OFF	53	12 ms	55	4.8 V
3	–5.2 V	24	–3.1 V	44	7.3 V					56	4.9 V
4	–5.1 V	25	–3.0 V	45	7.0 V					57	5.0 V
5	–5.0 V	26	–2.9 V	46	6.7 V						
6	–4.9 V	27	–2.8 V	47	6.4 V						
7	–4.8 V	28	–2.7 V	48	6.1 V						
8	–4.7 V	29	–2.6 V	49	5.8 V						
9	–4.6 V	30	–2.5 V								
10	–4.5 V	31	–2.4 V								
11	–4.4 V	32	–2.3 V								
12	–4.3 V	33	–2.2 V								
13	–4.2 V	34	–2.1 V								
14	–4.1 V	35	–2.0 V								
15	–4.0 V	36	–1.9 V								
16	–3.9 V	37	–1.8 V								
17	–3.8 V	38	–1.7 V								
18	–3.7 V	39	–1.6 V								
19	–3.6 V	40	–1.5 V								
20	–3.5 V	41	–1.4 V								

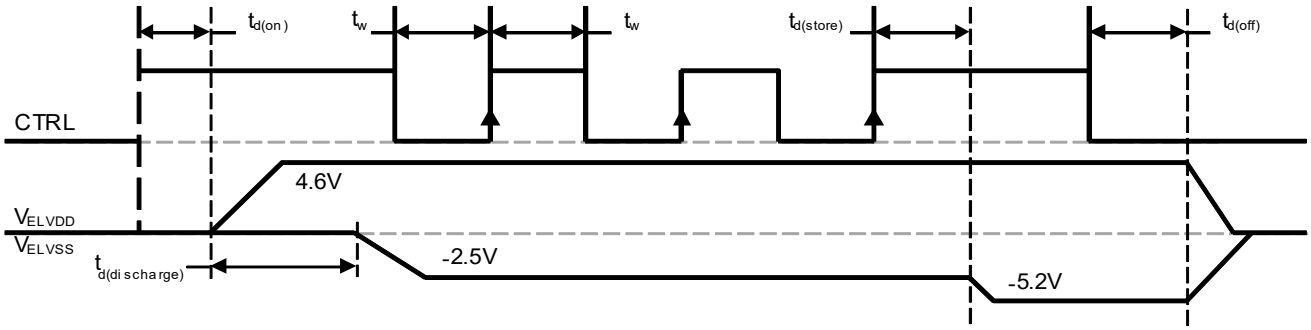


Figure 25. Timing Diagram

Short Circuit and Overload Protection

The device is protected against short of $V_{(AVDD)}$, $V_{(ELVDD)}$ and $V_{(ELVSS)}$ to ground. $V_{(ELVDD)}$ and $V_{(ELVSS)}$ are also protected when they are shorted together. In addition to the switch current limit, which also limits the output current, $V_{(AVDD)}$ has a more accurate typ. 160mA output current protection. A short at any converter and the $V_{(AVDD)}$ overload protection shuts down the whole device, the shut-down state is latched, input and outputs are fully disconnected. To reset the whole device VI has to cycle below Undervoltage Lockout or EN3 and CTRL have to be low at the same time for minimum $t_{d(reset)}$. The device detects a short or an overload when one of the below conditions is fulfilled:

- $V_{(ELVDD)}$ is not in regulation 40ms after $V_{(ELVDD)}$ is enabled (CTRL = HIGH) → shut-down all
- $V_{(ELVSS)}$ is not in regulation 40ms after $V_{(ELVSS)}$ is enabled (80ms after CTRL = HIGH) → shut-down all
- $V_{(AVDD)}$ falls below 90% of its programmed voltage longer than 4ms → shut-down all
- $V_{(ELVDD)}$ falls below 90% of its programmed voltage longer than 4ms → shut-down all
- $V_{(ELVSS)}$ rises above 500mV of its programmed voltage longer than 4ms → shut-down all
- $V_{(AVDD)}$ output current is > 160mA longer than 4ms → shut-down all

Enable/Disable Active Discharge During Shutdown

The Active Discharge during shutdown can be enabled and disabled by the FD pin or by programming. The programming overwrites the FD pin setting until the function is reset.

- FD pin connected to GND or 51 CTRL pulses

  → Active discharge is disabled and all outputs are high impedance.

- FD pin connected to HIGH (VIH > 1.2V) or 50 CTRL pulses

  → Active discharge is enabled and all outputs are discharged.

Device Reset

- A power cycle resets all settings to default values as well as the short-circuit and overload protection.
- Enabling the $V_{(ELVDD)}$ converter (first rising edge of CTRL) resets the Output Discharge

  → Output Discharge is controlled by FD pin.

- When CTRL is low for $t_{d(reset)}$ then $V_{(ELVDD)}$, $V_{(ELVSS)}$ and $V_{(ELVSS)}$ transition time are reset to default values

  → 4.6V, –2.5V, $V_{(ELVSS)}$ transition time is controlled by CT pin.

- EN3 and CTRL are low at the same time for td(reset)

  → $V_{(AVDD)}$ is reset to its default value of 6.1V, short-circuit and overload protection is reset.

Device Functional Modes

Operation with V_I < 2.9V

The recommended minimum input supply voltage for full performance is 2.9V. The device continues to operate with input supply voltages below 2.9V, however, full performance is not ensured. The device does not operate with input supply voltages below the Undervoltage Lockout threshold.

Operation with V_I > 4.4 V (Diode Mode for $V_{(ELVDD)}$)

For V_I >4.4V and $V_{(ELVDD)}$=4.6V the ELVDD boost converter cannot support the duty cycle anymore. It enables its build in Diode-Mode which enables the converter to regulate the output voltage even when the input supply very close or higher than the output. When operating in Diode-Mode the converter's rectifier switch stops switching and regulates the output voltage. The efficiency during Diode-Mode operation is reduced. At low output current (< 2mA), the converter automatically transitions from pulse-width modulation to pulse-skip mode. This ensures that $V_{(ELVDD)}$ stays in regulation, but increases the output voltage ripple.

Application Information

Figure 26 shows a typical application circuit suitable for supplying AMOLED displays in smartphone applications. The circuit is designed to operate from a single-cell Li-Ion battery and generates positive output voltages $V_{(AVDD)}$ of 6.1V and $V_{(ELVDD)}$ of 4.6V as well as a negative output voltage $V_{(ELVSS)}$ of –2.5V. ELVDD and ELVSS are capable of supplying up to 700mA of output current.

Typical Application

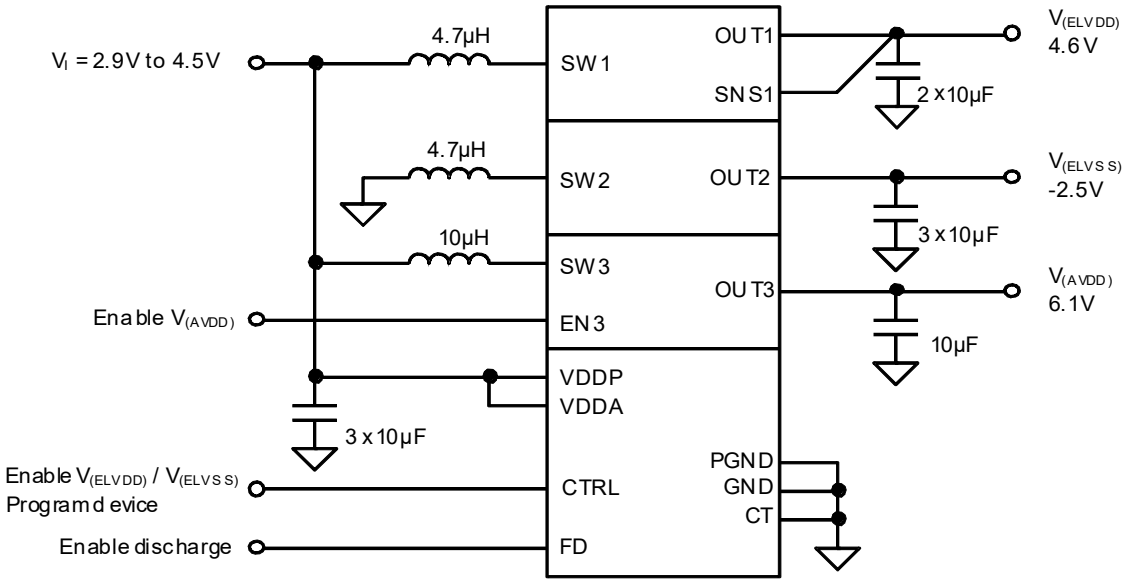


Figure 26. Typical Application Schematic

Design Requirements

For this design example, use the following input parameters in Table 2.

Table 2. Design Parameters

Design Parameter	Example Value
Input voltage	2.9V to 4.5V
Output	$V_{(AVDD)}$ = 6.1V, $V_{(ELVDD)}$ = 4.6V, $V_{(ELVSS)}$ = –2.5V
Switching	ELVDD, ELVSS and AVDD = 1.6MHz

Detailed Design Procedure

In order to maximize performance, the device has been optimized for use with a relatively narrow range of component values. The $V_{(AVDD)}$ boost converter typically requires a 10μH inductor, $V_{(ELVDD)}$ and $V_{(ELVSS)}$ require a 4.7μH inductor. Ceramic capacitors are usually used for input and output capacitors. It is recommended to use the suggested values in all applications. Customers using other values are strongly recommended to characterize circuit performance on a case-by-case basis.

ELVDD Boost Converter (OUT1)

Inductor Selection

The main parameter for the inductor selection is the inductor saturation current, which must be higher than the peak switch current. Inductors with lower saturation current than the minimum switch current limit can be used when the maximum output current is not required, however a minimum saturation current of 0.5A is required to ensure proper startup. The minimum required saturation current is calculated by the peak inductor current formula.

The inductors DC resistance as well as its core losses affect the efficiency. Lower DC resistance results in higher high load efficiency. The core losses are especially important for light load efficiency. The core material as well as the inductors physical size has an influence on the core losses. The higher the quality factor Q of the inductor at the switching frequency (1.6MHz) the lower the core losses. Table 3 shows examples of suitable inductors, equivalent parts can be used.

- Minimum 3.3μH, maximum 6.1μH inductance.
- Minimum 0.5A saturation current, for full output current capability 2A.
- Minimum V_I and maximum I_O must be taken to calculate the required saturation current.
- Duty Cycle: $$D = \frac{V_O - V_I \times \eta}{V_O}$$

  Where
  - V_I is the boost converter input supply voltage.
  - V_O is the boost converter output voltage.
  - η is the boost converter efficiency.
- Peak Inductor Current: $$I_{(SW)M} = \frac{I_O}{1-D} + \frac{V_I \times D}{2 \times f \times L}$$

  Where
  - I_O is the boost converter output current.

- f=1.6MHz (the boost converter switching frequency).
- L is the boost converter inductance (4.7μH).

Table 3. Design Parameters

Inductance	I_{SAT}	DCR	Manufacturer	Part Number	Dimensions
4.7μH	5.7A	53mΩ	TOKO	FDV0620-4R7M	7.4mm × 6.7mm × 2mm
	5.0A	75mΩ	Cyntec	CMLE061E-4R7MS	7.4mm × 6.7mm × 1.5mm
	4.1A	58mΩ	Cyntec	HBLE061E-4R7MS	6.4mm × 6.4mm × 1.5mm

Capacitor Selection

The main parameter for the capacitor selection is the capacitance at the operating voltage. The more voltage is applied at the capacitor the lower is its resulting capacitance (DC-bias effect), also temperature and AC-Voltage changes the capacitance, however the DC-bias effect is dominant. For best voltage filtering (lowest voltage ripple), low ESR capacitors are recommended. Ceramic capacitors have a low ESR value, but also other types can be used. Table 4 and Table 5 show examples of suitable capacitors, equivalent parts can be used.

Input Capacitor:

- Minimum 2.5μF resulting capacitance.
- Minimum 6.3V voltage rating.

Output Capacitor:

- Minimum 2.5μF, maximum 24μF resulting capacitance.
- Minimum 6.3V voltage rating.

Table 4. Input Capacitor Selection ELVDD Boost Converter (OUT1)

Capacitance	Voltage Rating	Manufacturer	Part Number	Size
10μF	6.3V	muRata	GRM188R60J106ME84	0603
10μF	10V	muRata	GRM219R61A106ME47	0805
22μF	10V	Semco	CL21A226MPCLRNC	0805

Table 5. Output Capacitor Selection ELVDD Boost Converter (OUT1)

Capacitance	Voltage Rating	Manufacturer	Part Number	Size
10μF	10V	muRata	GRM219R61A106ME47	0805
22μF	10V	Semco	CL21A226MPCLRNC	0805

Inductor Selection

The main parameter for the inductor selection is the inductor saturation current, which must be higher than the peak switch current. Inductors with lower saturation current than the minimum switch current limit can be used when the maximum output current is not required, however a minimum saturation current of 0.5A is required to ensure proper startup. The minimum required saturation current is calculated by the peak inductor current formula.

The inductors DC resistance as well as its core losses affect the efficiency. Lower DC resistance results in

higher high load efficiency. The core losses are especially important for light load efficiency. The core material as well as the inductors physical size has an influence on the core losses. The higher the quality factor Q of the inductor at the switching frequency (1.6MHz) the lower the core losses. Table 6 shows examples of suitable inductors, equivalent parts can be used.

- Minimum 3.3μH, maximum 6.1μH inductance.
- Minimum 0.5A saturation current, for full output current capability 3.2A.
- Minimum V_I and maximum I_O must be taken to calculate the required saturation current.
- Duty Cycle: $$D = \frac{V_O}{V_O - V_I \times \eta}$$

  Where
  - V_I is the inverting buck-boost converter input supply voltage.
  - V_O is the inverting buck-boost converter output voltage.
  - η is the inverting buck-boost converter efficiency.
- Peak Inductor Current: $$I_{(SW)M} = \frac{I_O}{1-D} + \frac{V_I \times D}{2 \times f \times L}$$

  Where
  - I_O is the inverting buck-boost converter output current.
  - f=1.6MHz (the inverting buck-boost converter switching frequency).
  - L is the inverting buck-boost converter inductance (4.7μH).

Table 6. ELVSS Inverting Buck-Boost Converter (OUT2) Inductor Selection

Inductance	I_{SAT}	DCR	Manufacturer	Part Number	Dimensions
4.7μH	5.7A	53mΩ	TOKO	FDV0620-4R7M	7.4mm × 6.7mm × 2mm
	5.0A	75mΩ	Cyntec	CMLE061E-4R7MS	7.4mm × 6.7mm × 1.5mm
	4.1A	58mΩ	Cyntec	HBLE061E-4R7MS	6.4mm × 6.4mm × 1.5mm

Capacitor Selection

The main parameter for the capacitor selection is the capacitance at the operating voltage. The more voltage is applied at the capacitor the lower is its resulting capacitance (DC-bias effect), also temperature and AC-Voltage changes the capacitance, however the DC-bias effect is dominant. For best voltage filtering (lowest voltage ripple), low ESR capacitors are recommended. Ceramic capacitors have a low ESR value, but also other types can be used. Table 7 and Table 8 show examples of suitable capacitors, equivalent parts can be used.

Input Capacitor:

- Minimum 2.5μF resulting capacitance.
- Minimum 6.3V voltage rating.

Output Capacitor:

- Minimum 2.5μF, maximum 24μF resulting capacitance.
- Minimum 10V voltage rating, when maximum –6V are used also 6.3V rated capacitors can be used.

Table 7. Input Capacitor Selection ELVSS Inverting Buck- Boost Converter (OUT2)

Capacitance	Voltage Rating	Manufacturer	Part Number	Size
10μF	6.3V	muRata	GRM188R60J106ME84	0603
10μF	10V	muRata	GRM219R61A106ME47	0805
22μF	10V	Semco	CL21A226MPCLRNC	0805

Table 8. Output Capacitor Selection ELVSS Inverting Buck- Boost Converter (OUT2)

Capacitance	Voltage Rating	Manufacturer	Part Number	Size
10μF	10V	muRata	GRM219R61A106ME47	0805
22μF	10V	Semco	CL21A226MPCLRNC	0805

Inductor Selection

The main parameter for the inductor selection is the inductor saturation current, which must be higher than the peak switch current. Inductors with lower saturation current than the minimum switch current limit can be used when the maximum output current is not required, however a minimum saturation current of 0.5A is required to ensure proper startup. The minimum required saturation current is calculated by the peak inductor current formula.

The inductors DC resistance as well as its core losses affect the efficiency. Lower DC resistance results in higher high load efficiency. The core losses are especially important for light load efficiency. The core material as well as the inductors physical size has an influence on the core losses. The higher the quality factor Q of the inductor at the switching frequency (1.6MHz) the lower the core losses. Table 9 shows examples of suitable inductors, equivalent parts can be used.

- Minimum 3.3μH, maximum 6.1μH inductance.
- Minimum 0.2A saturation current, for full output current capability 0.25A.
- Minimum V_I and maximum I_O must be taken to calculate the required saturation current.
- Duty Cycle: $$D = \frac{V_O - V_I \times \eta}{V_O}$$

  Where
  - V_I is the boost converter input supply voltage.
  - V_O is the boost converter output voltage.
  - η is the boost converter efficiency.
- Peak Inductor Current: $$I_{(SW)M} = \frac{I_O}{1-D} + \frac{V_I \times D}{2 \times f \times L}$$

  Where
  - I_O is the boost converter output current.
  - f=1.6MHz (the boost converter switching frequency).
  - L is the boost converter inductance (10μH).

Table 9. AVDD Boost Converter (OUT3) Inductor Selection

Inductance	I_{SAT}	DCR	Manufacturer	Part Number	Dimensions
10μH	1.3A	400mΩ	TOKO	DFE252012C-100M	2.5mm x 2mm x 1.2mm
	1.2A	530mΩ	TOKO	DFE252010C-100M	2.5mm x 2mm x 1mm
	0.75A	600mΩ	Taiyo Yuden	MDKK2020T-100MM	2mm x 2mm x 1mm
	0.8A	359mΩ	CYNTEC	SDET25201B-100MS	2.5mm x 2mm x 1.2mm
	0.48A	817mΩ	CYNTEC		2mm x 1.2mm x 1mm

Capacitor Selection

The main parameter for the capacitor selection is the capacitance at the operating voltage. The more voltage is applied at the capacitor the lower is its resulting capacitance (DC-bias effect), also temperature and AC-Voltage changes the capacitance, however the DC-bias effect is dominant. For best voltage filtering (lowest voltage ripple), low ESR capacitors are recommended. Ceramic capacitors have a low ESR value, but also other types can be used. Table 10 and Table 11 show examples of suitable capacitors, equivalent parts can be used.

Input Capacitor:

- Minimum 2.5μF resulting capacitance.
- Minimum 6.3V voltage rating.

Output Capacitor:

- Minimum 2.5μF, maximum 24μF resulting capacitance.
- Minimum 10V voltage rating.

Table 10. Input Capacitor Selection AVDD Boost Converter (OUT3)

Capacitance	Voltage Rating	Manufacturer	Part Number	Size
10μF	6.3V	muRata	GRM188R60J106ME84	0603
10μF	10V	muRata	GRM219R61A106ME47	0805
22μF	10V	Semco	CL21A226MPCLRNC	0805

Table 11. Output Capacitor Selection AVDD Boost Converter (OUT3)

Capacitance	Voltage Rating	Manufacturer	Part Number	Size
10μF	10V	muRata	GRM219R61A106ME47	0805
22μF	10V	Semco	CL21A226MPCLRNC	0805

Typical Application

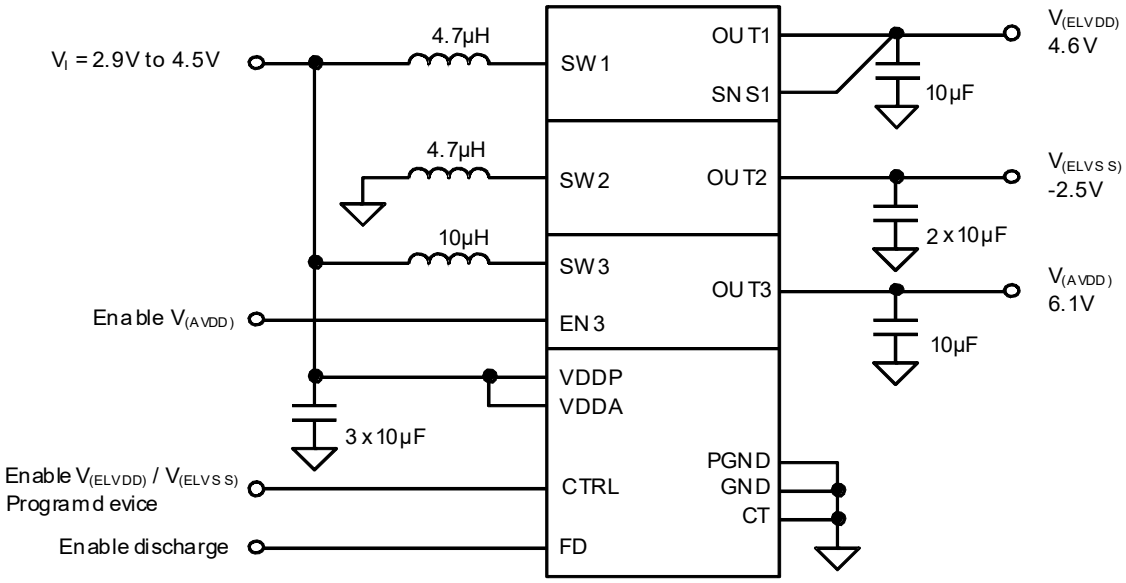


Figure 27. Typical Application Circuit for Load Current Lower than 500mA

Power Supply Recommendations

The DIO5613 device is designed to operate with input supplies from 2.9V to 4.5V. The input supply should be stable and free of noise if the device's full performance is to be achieved. If the input supply is located more than a few centimeters away from the device, additional bulk capacitance may be required. The input capacitance shown in the application schematics is sufficient for typical applications.

Layout

Layout Guideline

The PCB layout is an important step in the power supply design. An incorrect layout could cause converter instability, load regulation problems, noise, and EMI issues. Especially with a switching DC-DC converter at high load currents, too thin PCB traces can cause significant voltage spikes. Good grounding becomes important as well. If possible a common ground plane to minimize ground shifts between analog ground (GND) and power ground (PGND) is recommended.

- Place the input capacitor on VDDP and the output capacitor on OUT2 as close as possible to the device. Use short and wide traces to connect the input capacitor on VDDP and the output capacitor on OUT2.
- Place the output capacitor on OUT1 and OUT3 as close as possible to the device. Use short and wide traces to connect the output capacitor on OUT1 and OUT3.
- Connect the ground of the CT capacitor with AGND (pin 7) directly.
- Connect input ground and output ground on the same board layer, not through via hole.
- Connect AGND and PGND with the exposed thermal pad.

Layout Example

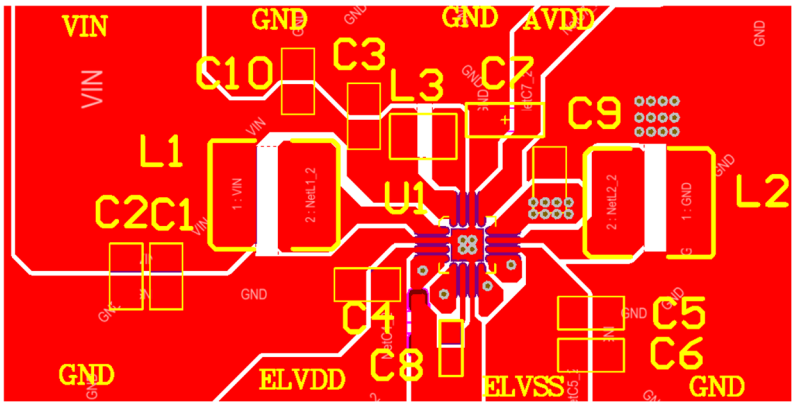
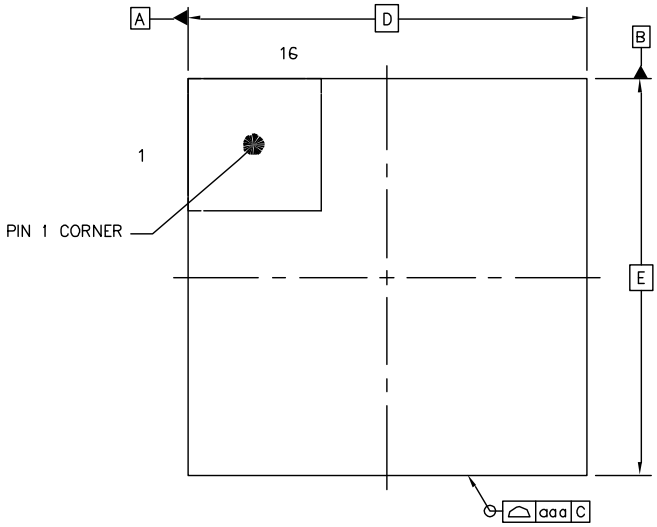
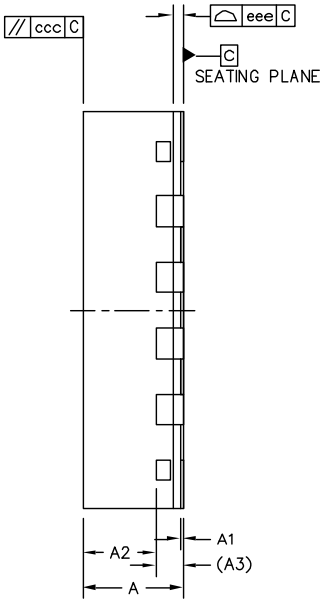


Figure 28. PCB Layout Example

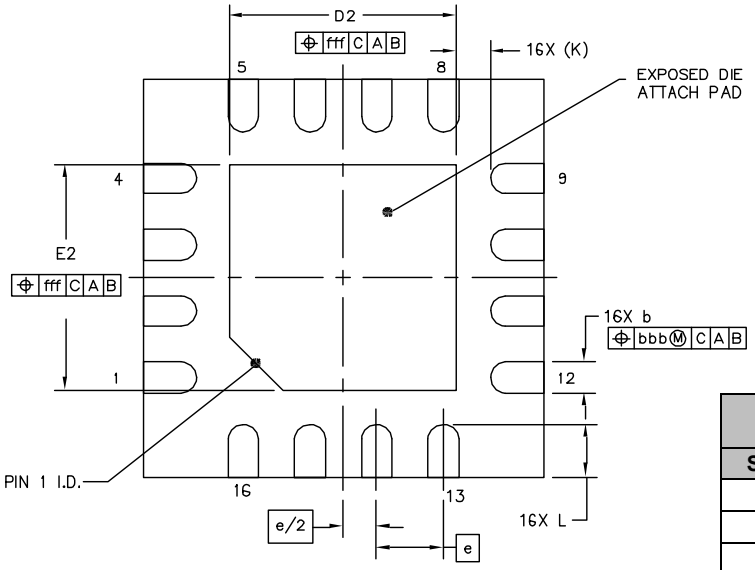
Physical Dimensions: TQFN3*3-16



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS (UNITS OF MEASURE=MILLIMETER)			
SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	-	0.55	-
A3		0.203REF	
b	0.18	0.23	0.28
D		3 BSC	
E		3 BSC	
e		0.5 BSC	
D2	1.60	1.70	1.80
E2	1.60	1.70	1.80
L	0.3	0.4	0.5
K		0.25 REF	
aaa		0.1	
ccc		0.1	
eee		0.08	
bbb		0.1	
fff		0.1	

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