

2 to 4 Serial Cell Li-ion Battery Protection IC for Secondary Protection

NO.EA-426-181212

OVERVIEW

The R5641L is an overcharge protection IC for 2- to 4-series cell Li-ion / Li-polymer rechargeable battery pack, with built-in high-accuracy voltage detection circuits and delay circuits. Controlling the supply voltage to the CTLC pin can control the COUT pin output. The shutdown detection can reduce the supply current to the minimum.

KEY BENEFITS

- Reducing the supply current to 0.2 μ A or less after shutdown detection can achieve the longer battery life.
- Temperature protection enabled with an external PTC thermistor.
- Be adaptable to 30 V input voltage by using high-voltage process.

KEY SPECIFICATIONS

- Overcharge Detection Voltage ($V_{DET1n}^{(1)}$): 4.10 V to 4.60 V (5 mV step)
- Overcharge Detection Voltage Accuracy: ± 0.016 V ($T_a = 25^\circ\text{C}$)
 ± 0.025 V ($0^\circ\text{C} < T_a < 60^\circ\text{C}$)
- Overcharge Release Voltage($V_{REL1n}^{(1)}$): $V_{DET1n} - 0\text{V}$ to $V_{DET1n} - 0.4\text{V}^{(2)}$ (50mV step)
- Overcharge Detection Delay Time: 2- / 4- / 6-sec
- Release Condition: Voltage Release Type
- Low Supply Current: Typ. 2.8 μ A
- Shutdown Current: Max. 0.2 μ A
- Shutdown Detection Voltage: Typ. 2.5 V $\pm$ 0.3 V / 3.7 V $\pm$ 0.3 V
- 2 to 4 Cells Selectable Battery Protection by External Wirings
- Selectable Timer Reset Delay Function
- Temperature Protection with External PTC Thermistor
- CTLC Pin Detection Delay Time: 2 msec
- Output Type: CMOS Output

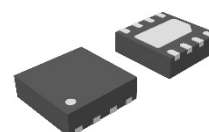
OPTIONAL FUNCTIONS

User-selectable Delay Time and Function:

Code (\$)	Overcharge Detection Delay Time
A	2 sec
B	4 sec
C	6 sec

Code (*)	CTLC at Shutdown	Timer Reset Delay
C	Disable	Disable
D	Enable	Disable
E	Disable	Enable
F	Enable	Enable

PACKAGE



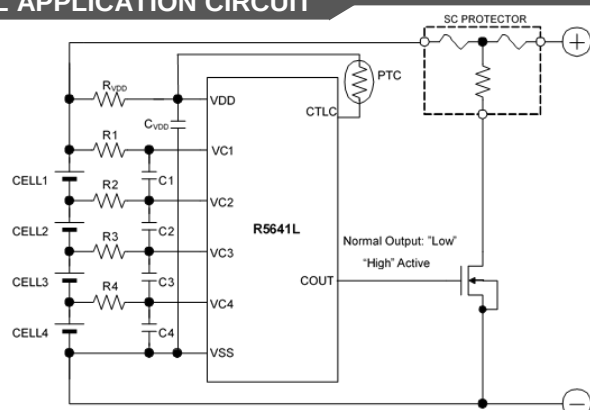
DFN2020-8C

2.0 mm x 2.0 mm x 0.6 mm

APPLICATIONS

- Li-Ion or Li-Polymer Battery Protection

TYPICAL APPLICATION CIRCUIT



4-cell Protection Circuit with PTC Thermistor

⁽¹⁾ V_{DET1n} , V_{REL1n} : $n = 1, 2, 3, 4$

⁽²⁾ Min. 4.05 V when shutdown detection voltage (V_{SHTh}) is 3.7 V.

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SELECTION GUIDE

Overcharge detection / release voltages and delay time are user-selectable options.

Selection Guide

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R5641Lxxx\$*-TR	DFN2020-8C	3,000 pcs	Yes	Yes

xxx: Specify the combination of the overcharge detection voltage (V_{DET1n}), the overcharge release voltage (V_{REL1n}), and the shutdown detection voltage (V_{SHTn})⁽¹⁾.

V_{DET1n} ⁽²⁾: 4.1 V to 4.6 V in 5 mV step

V_{REL1n} ⁽¹⁾: $V_{DET1n} - 0V$ to $V_{DET1n} - 0.4V$ in 50 mV step⁽³⁾

V_{SHTn} ⁽¹⁾: 2.5V / 3.7 V

\$: Specify the delay time code defined a combination of the overcharge detection delay time (t_{VDET1}), the overcharge release delay time (t_{VREL1}), and the CTLC detection delay time (t_{CDET}).

Code \$	t_{VDET1} (s)	t_{VREL1} (ms)	t_{CDET} (ms)
A	2	16.5	2
B	4	16.5	2
C	6	16.5	2

*: Specify the CTLC function and the timer reset delay function.

Code *	CTLC Function at Shutdown	Timer Reset Delay Function
C	Disable	Disable
D	Enable	Disable
E	Disable	Enable
F	Enable	Enable

⁽¹⁾ Refer to *Product Code Table* for details.

⁽²⁾ V_{DET1n} , V_{REL1n} , V_{SHTn} : n =1, 2, 3, 4

⁽³⁾ Min. 4.05 V when shutdown detection voltage (V_{SHTn}) is 3.7 V.

Product Code List

The product code is determined by the combination of the set output voltage (overcharge detector threshold: V_{DET1n} , overcharge release voltage: V_{REL1n} , shutdown detector threshold: V_{SHTn}), the delay time (overcharge detection delay time: t_{VDET1} , overcharge release delay time: t_{VREL1} , CTLC detection delay time: t_{CDET}), the CTLC function and the timer reset delay time (t_{VTR}) option.

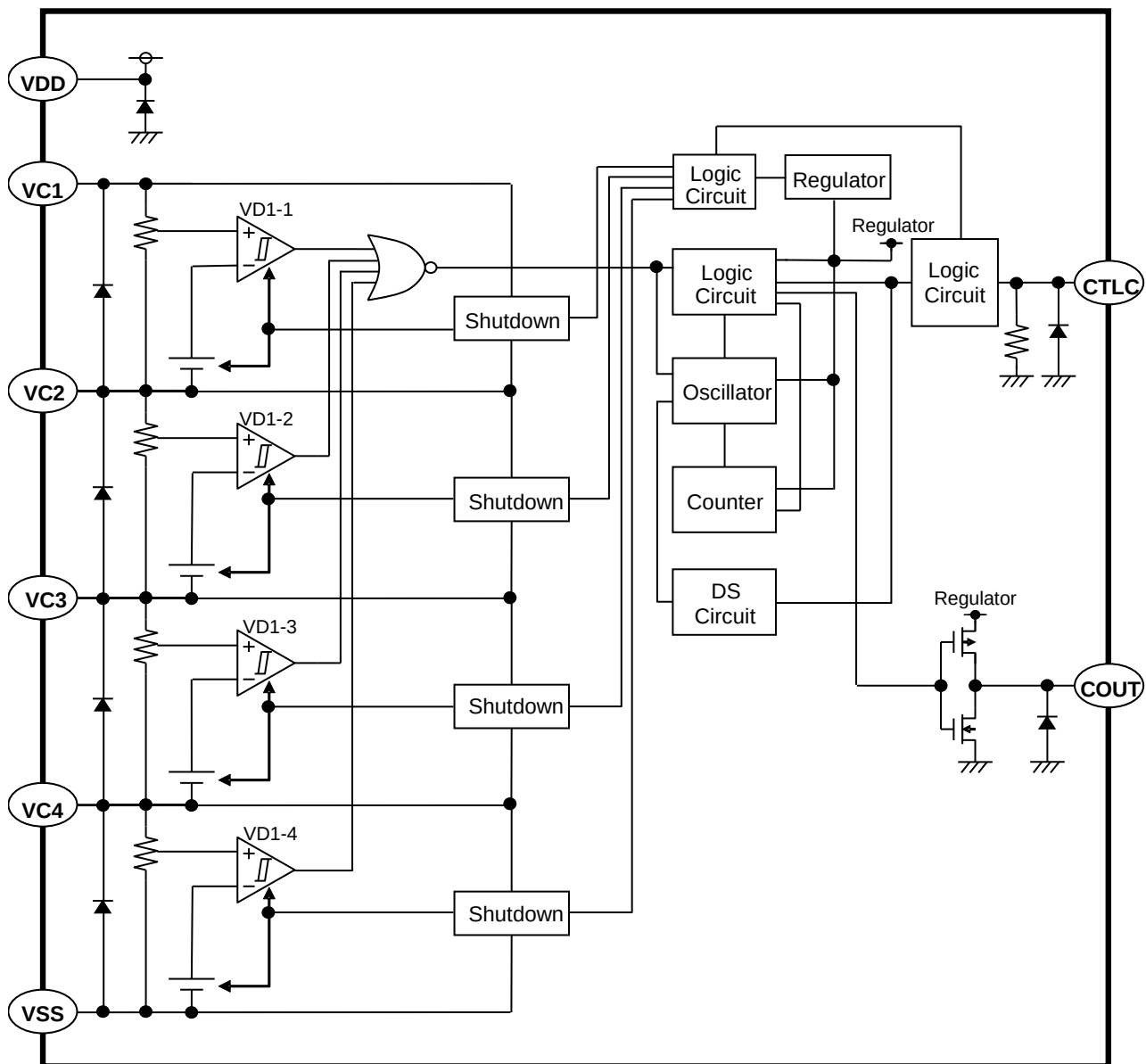
Product Code Table

Product Name	Set Output Voltage (V)			Delay Time			CTLC Function (at Shutdown)	Timer Reset Delay Time (Yes/No ⁽¹⁾)
	V_{DET1n}	V_{REL1n}	V_{SHTn}	$t_{VDET1}(s)$	$t_{VREL1}(ms)$	$t_{CDET}(ms)$		
R5641L252AF	4.220	4.120	3.700	2	16.5	2	Enable	Yes
R5641L255AF	4.250	4.150	3.700	2	16.5	2	Enable	Yes
R5641L301CC	4.300	4.000	2.500	6	16.5	2	Disable	No
R5641L302BD	4.350	4.050	2.500	4	16.5	2	Enable	No
R5641L303BD	4.500	4.100	2.500	4	16.5	2	Enable	No
R5641L304BD	4.450	4.050	2.500	4	16.5	2	Enable	No
R5641L306BC	4.550	4.150	2.500	4	16.5	2	Disable	No
R5641L307BC	4.600	4.200	2.500	4	16.5	2	Disable	No
R5641L303BC	4.500	4.100	2.500	4	16.5	2	Disable	No
R5641L352CC	4.350	4.050	3.700	6	16.5	2	Disable	No

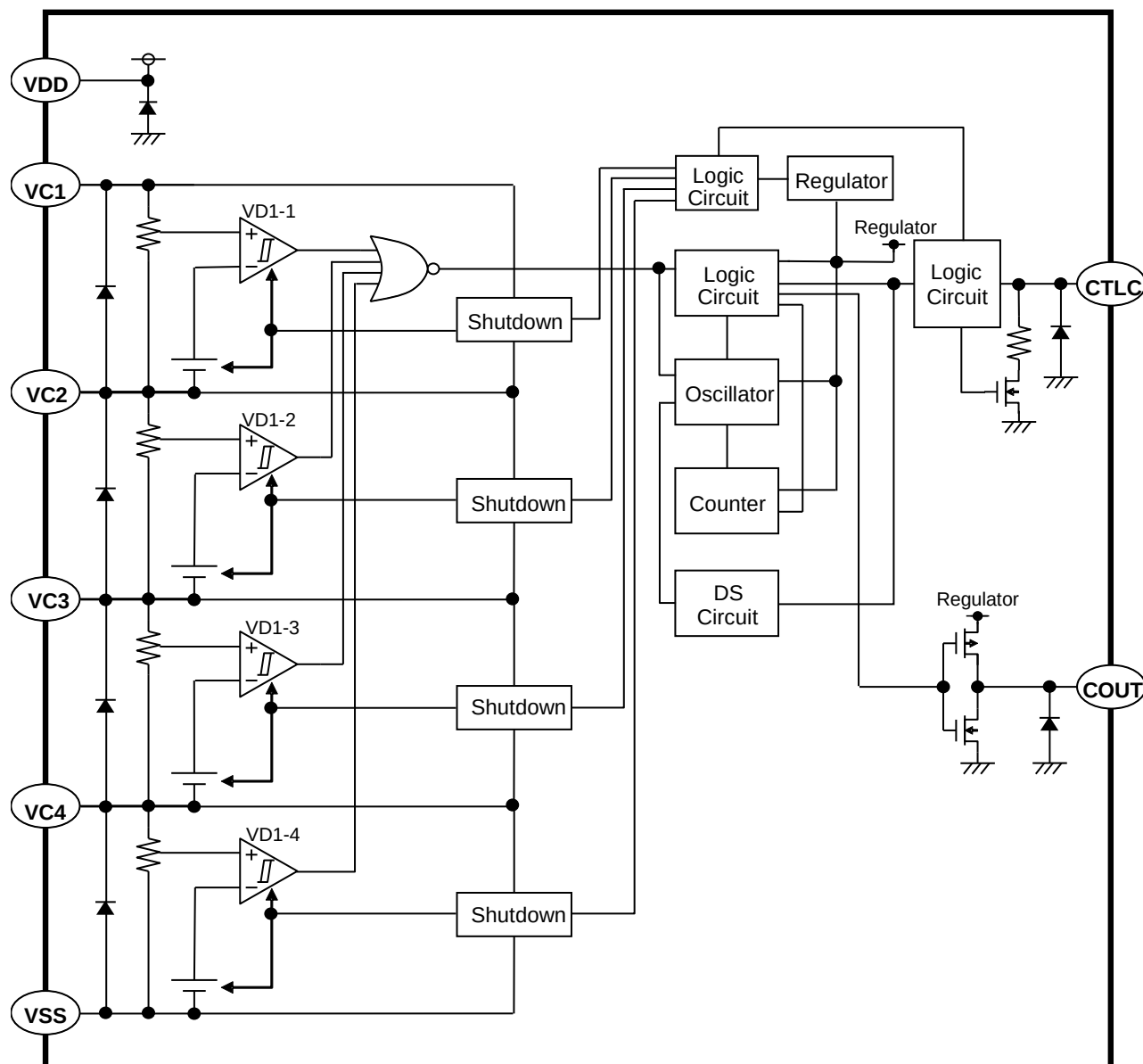
⁽¹⁾ "No" means the timer reset delay time option is absence.

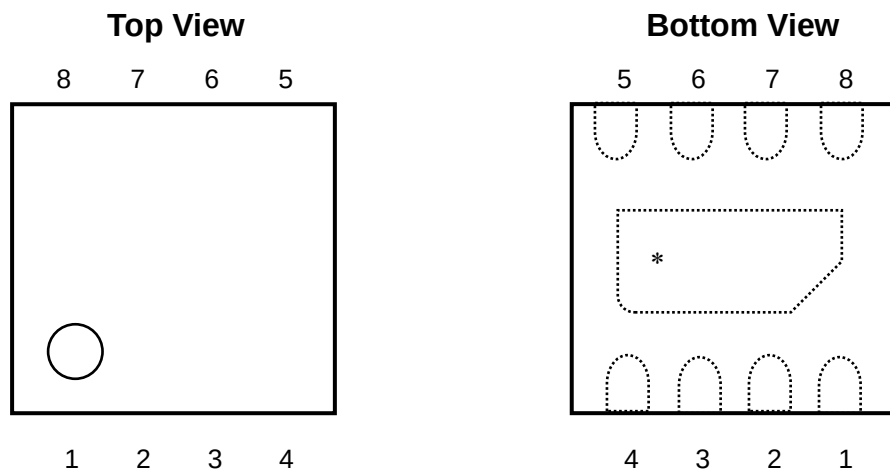
BLOCK DIAGRAM

R5641Lxxx\$D/\$F Block Diagram (Enabled CTLC Function at Shutdown)



R5641Lxxx\$C/\$E Block Diagram (Disabled CTLC Function at Shutdown)



PIN DESCRIPTION**DFN2020-8C Pin Configuration**

Pin No.	Symbol	Description
1	VDD	Power Supply Pin,
2	VC1	Positive Terminal for CELL1
3	VC2	Positive Terminal for CELL2
4	VC3	Positive Terminal for CELL3
5	VC4	Positive Terminal for CELL4
6	VSS	Ground Pin
7	CTLC	COUT Control Pin / Output Delay Time Shortening Pin
8	COUT	Overcharge Detection Output Pin, CMOS Output

*The tab on the bottom of the package is not connected with the IC chip, so the tab should be left open.

ABSOLUTE MAXIMUM RATINGS(Ta = 25°C, V_{SS} = 0V)

Symbol	Item	Rating	Unit
V _{DD}	Supply Voltage	-0.3 to 30	V
V _{C1}	Positive Terminal Voltage for CELL1	V _{C2} -0.3 to V _{C2} +6.5	V
V _{C2}	Positive Terminal Voltage for CELL2	V _{C3} -0.3 to V _{C3} +6.5	V
V _{C3}	Positive Terminal Voltage for CELL3	V _{C4} -0.3 to V _{C4} +6.5	V
V _{C4}	Positive Terminal Voltage for CELL4	-0.3 to 6.5	V
V _{CTL}	CTL Pin Voltage	-0.3 to 30	V
V _{COU}	COU Pin Output Voltage	-0.3 to V _{OH1} +0.3	V
P _D	Power Dissipation ⁽¹⁾ (DFN2020-8C, JEDEC STD.51-7)	1400	mW
T _j	Junction Temperature Range	-40 to 125	°C
T _{stg}	Storage Temperature Range	-55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITION

Symbol	Item	Rating	Unit
V _{DD}	Operating Input Voltage	4.0 to 20	V
T _a	Operating Temperature Range	-40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

⁽¹⁾ Refer to *POWER DISSIPATION* in *SUPPLEMENTARY ITEMS* for detail information.

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ELECTRICAL CHARACTERISTICS

$V_{CELLn} = CELLn$ (Ex. V_{CELL1} is a voltage difference between VC1 and VC2), $n = 1, 2, 3, 4$, unless otherwise noted. The specifications surrounded by are guaranteed by Design Engineering at $0^{\circ}\text{C} \leq T_a \leq 60^{\circ}\text{C}$.

R5641L Electrical Characteristics

(Ta = 25°C)

Symbol	Parameter	Conditions	Ratings			Unit	Circuit (1)
			Min.	Typ.	Max.		
V_{DET1n}	CELLn overcharge detection voltage	at rising edge of voltage	V_{DET1n} -0.016V -0.025V	V_{DET1n}	V_{DET1n} +0.016V +0.025V	V	A
V_{REL1n}	CELLn overcharge release voltage	at falling edge of voltage	V_{REL1n} -0.050V	V_{REL1n}	V_{REL1n} +0.050V	V	A
t_{VDET1}	Overcharge detection delay time	$V_{CELLn} = V_{DET1n} - 0.1\text{V}$ (n=2,3,4) $V_{CELL1} = V_{DET1n} - 0.1\text{V} \rightarrow 4.7\text{V}$	t_{VDET1} x 0.8	t_{VDET1}	t_{VDET1} x 1.2	s	B
t_{VD1DS}	Overcharge detection delay time at delay shortening mode	$V_{CELLn} = V_{DET1n} - 0.1\text{V}$ (n=2,3,4) $V_{CELL1} = V_{DET1n} - 0.1\text{V} \rightarrow 4.7\text{V}$ $V_{CTLC} = V_{DD} + 1.5\text{V}$	0.5	4	8	ms	B
t_{VREL1}	Overcharge release delay time	$V_{CELLn} = V_{REL1n} - 0.1\text{V}$ (n=2,3,4) $V_{CELL1} = 4.7\text{V} \rightarrow V_{REL1n} - 0.1\text{V}$	t_{VREL1} x 0.8	t_{VREL1}	t_{VREL1} x 1.2	ms	B
t_{VTR}	Overcharge detection timer reset delay time (2)	$V_{CELLn} = V_{DET1n} + 0.05\text{V} \rightarrow V_{REL1n} - 0.10\text{V}$ $\rightarrow V_{DET1n} + 0.05\text{V} \rightarrow V_{REL1n} - 0.10\text{V}$	2	6	10	ms	B
V_{SHTn}	Shutdown detection voltage	at falling edge of voltage	V_{SHTn} -0.3V	V_{SHTn}	V_{SHTn} +0.3V	V	C
V_{IH}	CTLC pin input voltage, high		V_{DD} +1.0V			V	D
V_{IL}	CTLC pin input voltage, low	$V_{DD} = 4\text{V}$ or more			V_{DD} -2.0V	V	D
t_{CDET}	CTLC pin detection delay time	$V_{CELLn} = 4.0\text{V}$ $V_{CTLC} = 16.0\text{V} \rightarrow 13.0\text{V}$	t_{CDET} x 0.8	t_{CDET}	t_{CDET} x 1.2	ms	D
		For CTLC enabled product (3) $V_{CELLn} = V_{SHTn} - 0.4\text{V}$ $V_{CTLC} = V_{DD} + 0\text{V} \rightarrow V_{DD} - 3\text{V}$		$t_{CDET} + 1$			
I_{CTLC}	CTLC pin current	$V_{CELLn} = 4.0\text{V}$ $V_{CTLC} = 16.0\text{V}$	1.2	1.6	2.4	μA	D
		For CTLC enabled product (3) $V_{CELLn} = 2.0\text{V}$, $V_{CTLC} = 8.0\text{V}$	0.6	0.8	1.2		
		For CTLC disabled product (3) $V_{CELLn} = 2.0\text{V}$, $V_{CTLC} = 8.0\text{V}$	-0.2		0.2		
V_{OL}	COUT pin Nch. ON voltage1	$I_{OL} = 50\mu\text{A}$, $V_{CELLn} = V_{DET1n} - 0.1\text{V}$		0.08	0.5	V	E
V_{OH1}	COUT pin Pch. ON voltage1	$I_{OH} = -1\mu\text{A}$, $V_{CELLn} = 4.7\text{V}$	4.0	4.7	5.4	V	F
V_{OH2}	COUT pin Pch. ON voltage2	$I_{OH} = -50\mu\text{A}$, $V_{CELLn} = 4.7\text{V}$	V_{OH1} -0.5V	V_{OH1} -0.14V		V	G

(1) Refer to *TEST CIRCUITS* for detail information.

(2) For the timer reset delay function enabled product only

(3) At shutdown

$V_{CELLn} = CELLn$ (Ex. V_{CELL1} is a voltage difference between VC1 and VC2), $n = 1, 2, 3, 4$, unless otherwise noted. The specifications surrounded by are guaranteed by Design Engineering at $0^{\circ}\text{C} \leq T_a \leq 60^{\circ}\text{C}$.

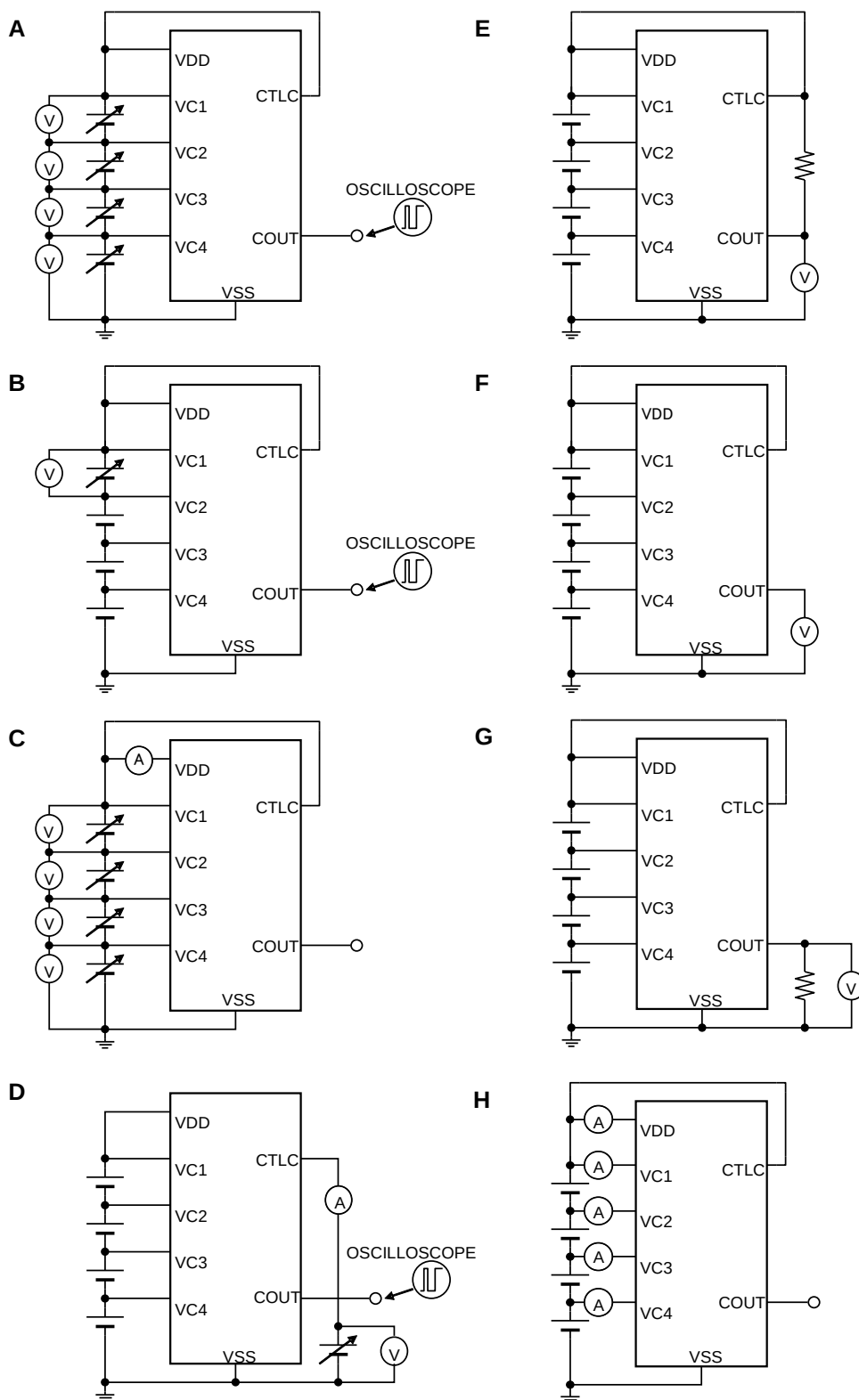
R5641L Electrical Characteristics (Continued)

(Ta = 25°C)

Symbol	Parameter	Conditions	Ratings			Unit	Circuit (1)
			Min.	Typ.	Max.		
I _{SHT}	Shutdown current	$V_{CELLn} = V_{SHTn} - 0.4\text{V}$			0.2	μA	H
I _{SS}	Supply current	$V_{CELLn} = 4.0\text{V}$ (the total current value of I _{VDD} and I _{VC1})		2.8	5.0	μA	H
I _{VC1}	VC1 pin current	$V_{CELLn} = V_{DET1n} - 0.1\text{V}$		1.0	2.0	μA	H
I _{VC2}	VC2 pin current	$V_{CELLn} = V_{DET1n} - 0.1\text{V}$	-0.3		0.3	μA	H
I _{VC3}	VC3 pin current	$V_{CELLn} = V_{DET1n} - 0.1\text{V}$	-0.3		0.3	μA	H
I _{VC4}	VC4 pin current	$V_{CELLn} = V_{DET1n} - 0.1\text{V}$	-0.3		0.3	μA	H

(1) Refer to *TEST CIRCUITS* for detail information.

Test Circuits



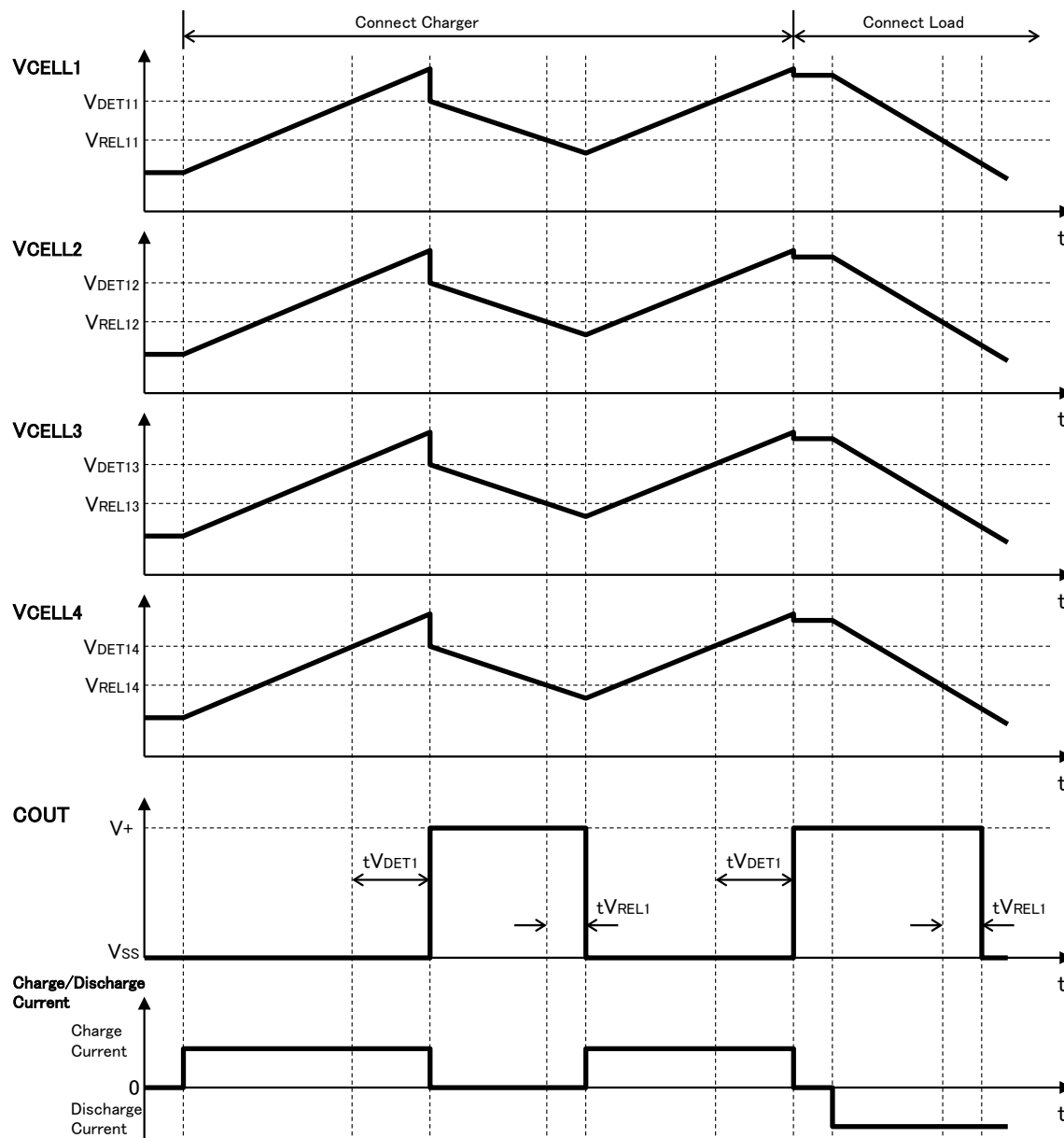
THEORY OF OPERATION

Overcharge Detector, V_{DET1n} ($n = 1, 2, 3, 4$)

During charging, the device supervises the voltage between VC1 pin and VC2 pin (V_{CELL1}), the voltage between VC2 pin and VC3 pin (V_{CELL2}), the voltage between VC3 pin and VC4 pin (V_{CELL3}), and the voltage between VC4 pin and VSS pin (V_{CELL4}). If at least one of the cell voltages exceeds more than the overcharge detection voltage (V_{DET1n}), the overcharge is detected, and an external charge control Nch. MOSFET turns on with COUT pin being at "High" level and by cutting a fuse on the charger path, and charge stops. If all the cell voltages become lower than the overcharge release voltage (V_{REL1n}), the overcharge is released and COUT pin outputs "Low".

The device has internal fixed output delay times for overcharge detection, overcharge detection timer reset, and overcharge release. If the output delay time passes on when any one of cell voltages is more than V_{DET1n} , the overcharge is detected. In the case of Timer Reset Delay available version, if all the cell voltages become lower than V_{DET1n} within the overcharge detection delay time by noise or other reasons, the time period is less than overcharge detection timer reset delay time, the overcharge delay time is accumulated and maintained, and the accumulated delay time reaches the overcharge detection delay time, the overcharge is detected. After detecting overcharge, even if all the cell voltages reduce less than the release voltage, if at least one of the cells voltage exceeds more than the release voltage within the overcharge release delay time, then overcharge is not released.

The output type of the COUT pin is CMOS output between VSS and the built-in regulator, and "High" level of COUT pin is the output voltage of the built-in regulator.



Overcharge Operation Timing Chart

Shutdown Function

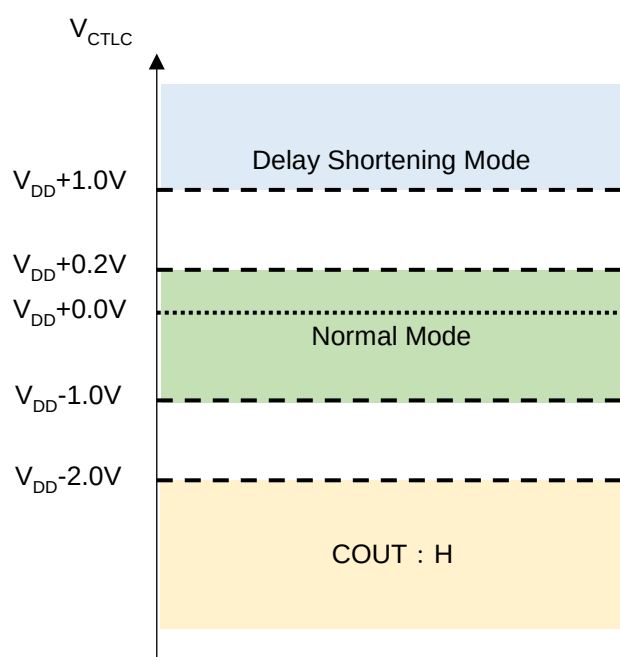
The voltage between VC1 pin and VC2 pin (V_{CELL1}), the voltage between VC2 pin and VC3 pin (V_{CELL2}), the voltage between VC3 pin and VC4 pin (V_{CELL3}), and the voltage between VC4 pin and VSS pin (V_{CELL4}) are supervised. If all of V_{CELLn} ($n=1$ to 4) become less than the shutdown detection voltage, the device halts the operation, and the supply current (shutdown current) of the device can be reduced to the minimum. If one of V_{CELLn} ($n=1$ to 4) becomes more than the shutdown detection voltage, the device will release from the shutdown state.

CTLC Function

When expiring the CTLC detection delay time or more after applying the voltage of $V_{DD}-2.0V$ or less to CTLC pin, the COUT pin outputs “High” level. Enabling/ disabling of this function in the shutdown state is user-selectable.

Delay Shortening (DS)

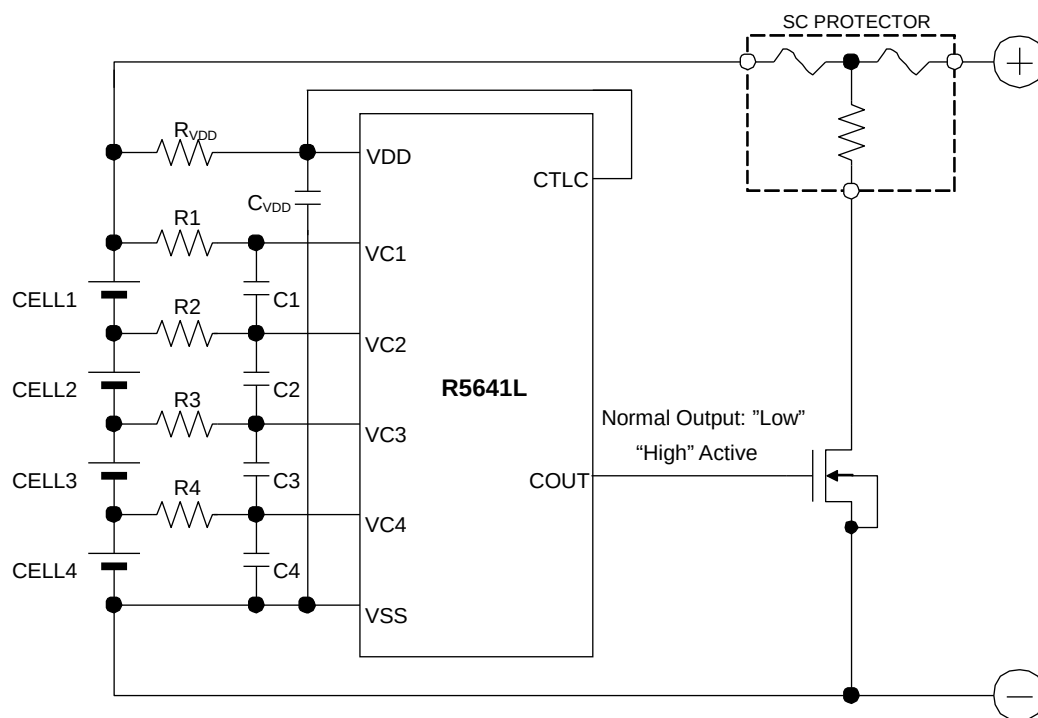
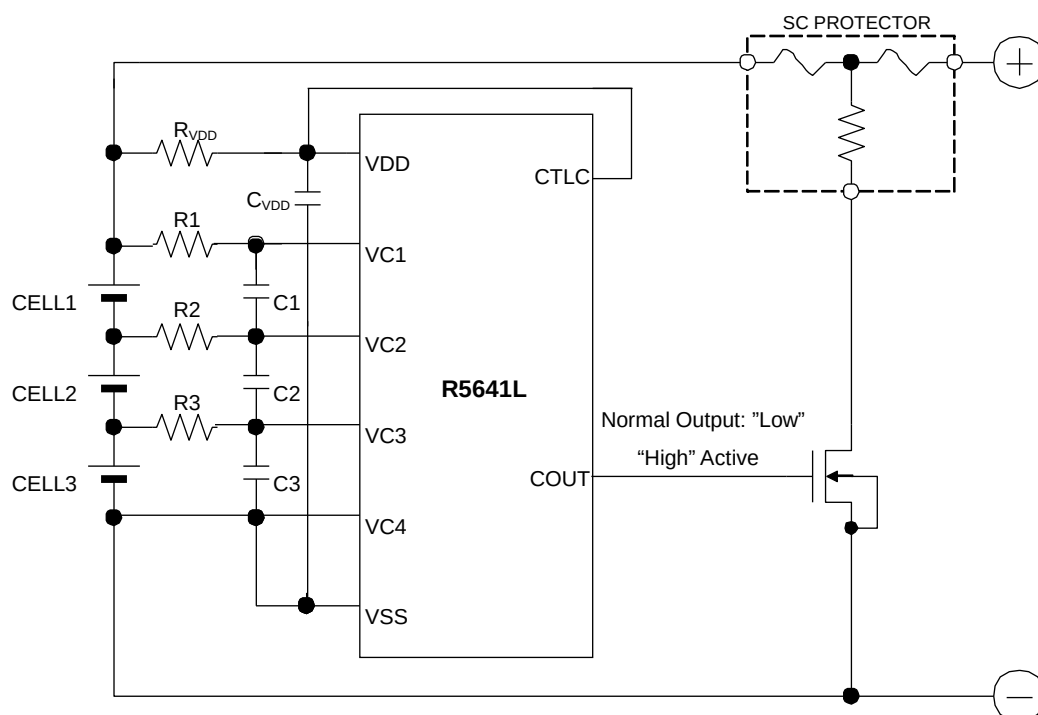
Applying the voltage of $V_{DD}+1.0V$ or more to the CTLC pin can shorten the overcharge detection delay time to a few millisecond (ms).

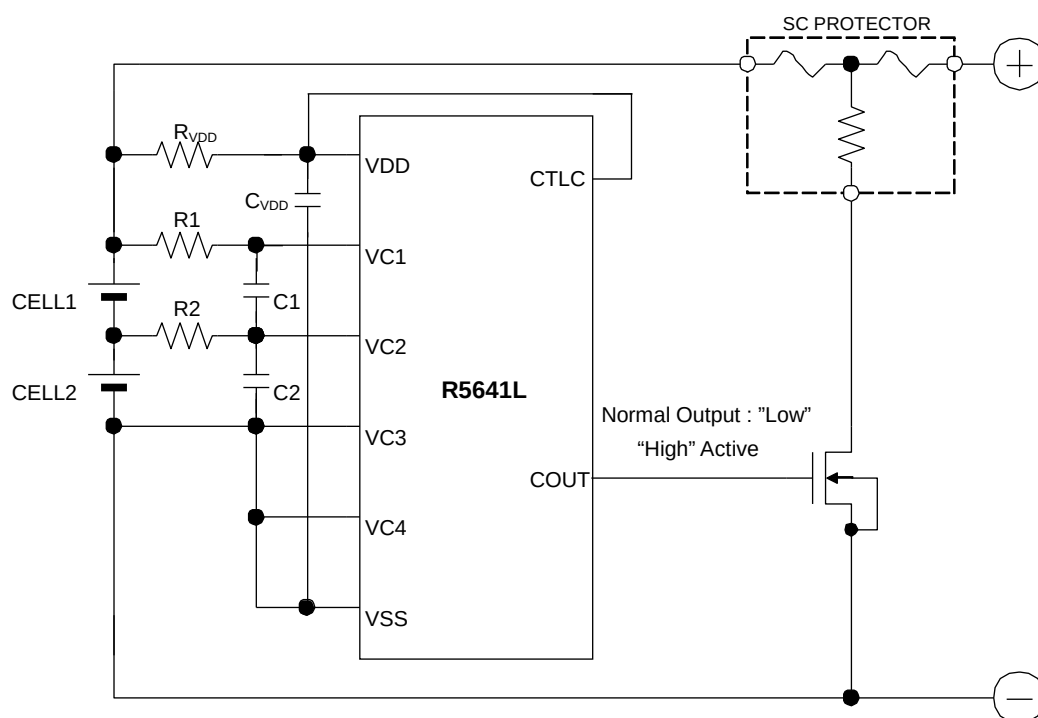


Setting for 2- to 4-Cell Protection

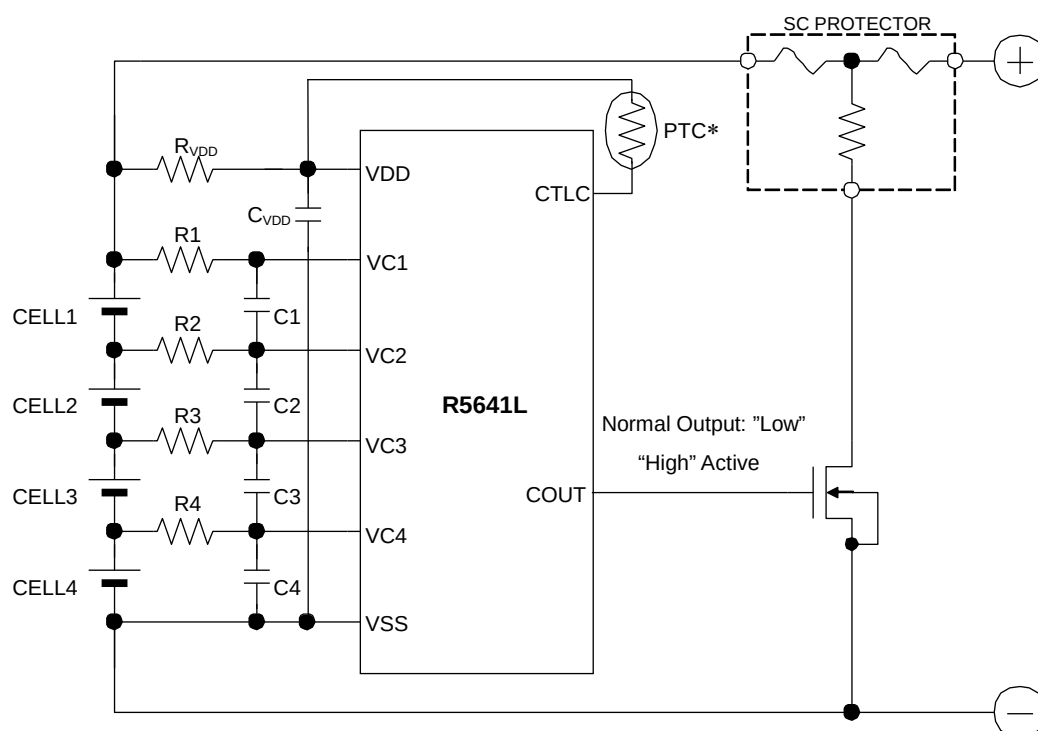
By short-circuiting between cells, the device can meet as a protection IC for 2- / 3- / 4-cell placed in series. The following table indicates pins to short-circuit to VSS depending on cells protected.

Protected Cells	Short-circuited Pins to VSS
2-cell Protection	VC3 and VC4 pins
3-cell Protection	VC4 pin
4-cell Protection	None (No short circuit)

APPLICATION INFORMATION**Typical Application Circuits****4-cell Protection Circuit****3-cell Protection Circuit**



2-cell Protection Circuit



* If using a PTC, connect the battery directly behind the PTC.

Temperature Protection Circuit

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External Components

Symbol	Typ.	Permissible Range	Unit
R_{VDD}	100	100 to 1000	Ω
R1 / R2 / R3 / R4	330	330 to 1000	Ω
C_{VDD}	0.1	0.1 to 1.0	μF
C1 / C2 / C3 / C4	0.1	0.01 to 1	μF

Technical Notes on Component Selection

- R_{VDD} and C_{VDD} stabilize the voltage fluctuation. The IC might occur a malfunction by a current flowed depending on the battery voltage fluctuation when R_{VDD} is small, and it might occur an unexpected malfunction by a current flowed depending on the supply power voltage fluctuation when R_{VDD} is big. To make the IC stable, please connect a resistor and a capacitor within the permissible range to each of R_{VDD} and C_{VDD} .
- R1 to R4 resistors and C1 to C4 capacitors stabilize the voltage fluctuation. Since increasing their resistors make the detection voltage be higher by the conduction current at detection, the appropriate value of R1 to R4 must be less than 1k Ω . And, the appropriate value of C1 to C4 must be 0.01 μF or more in order to make a stable operation of the IC.
- The typical application circuits are just examples and do not guarantee the operation. Conduct the sufficient evaluation in the actual application circuit in order to select external components.
- The protection IC and external components must not be applied overvoltage and overcurrent beyond the absolute maximum ratings. Especially, after detecting overcharge, a large heater current might flow through the MOSFET during the fuse blowout time. To prevent the MOSFET from being burnt, select a MOSFET with considering a current capacity of it.
- To connect the SC protector, connect the SC protector to the cell must be the last.

Contact Information for Inquiries regarding SC PROTECTOR

Dexerials Corporation (Sony Chemical & Information Device Company Ltd.)
Gate-city Osaki East Tower 8F, 1-11-2 Osaki, Shinagawa, Tokyo, 141-0032
TEL: 03-5435-3946
URL: <http://www.dexerials.jp>

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

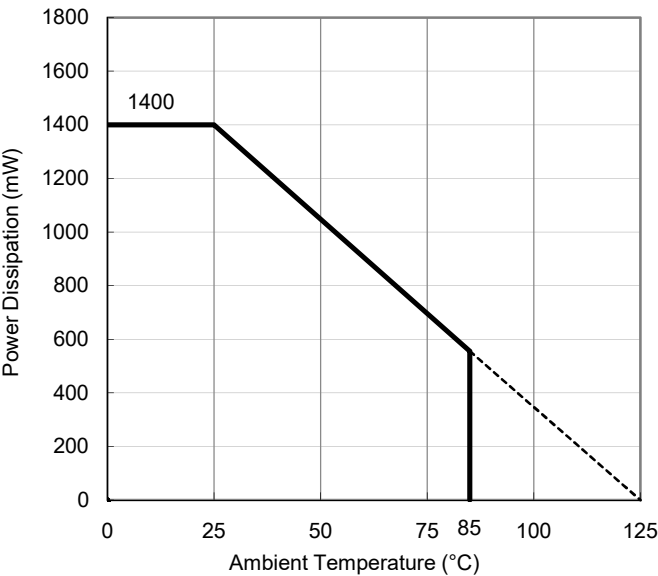
Measurement Conditions

Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	φ 0.3 mm × 23 pcs

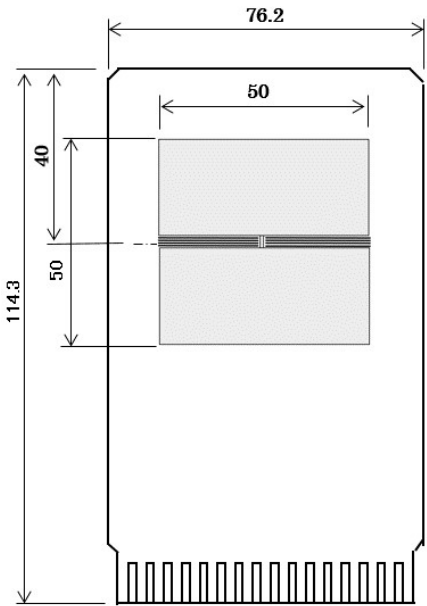
Measurement Result (Ta = 25°C, Tjmax = 125°C)

Item	Measurement Result
Power Dissipation	1400 mW
Thermal Resistance (θja)	θja = 71°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 34°C/W

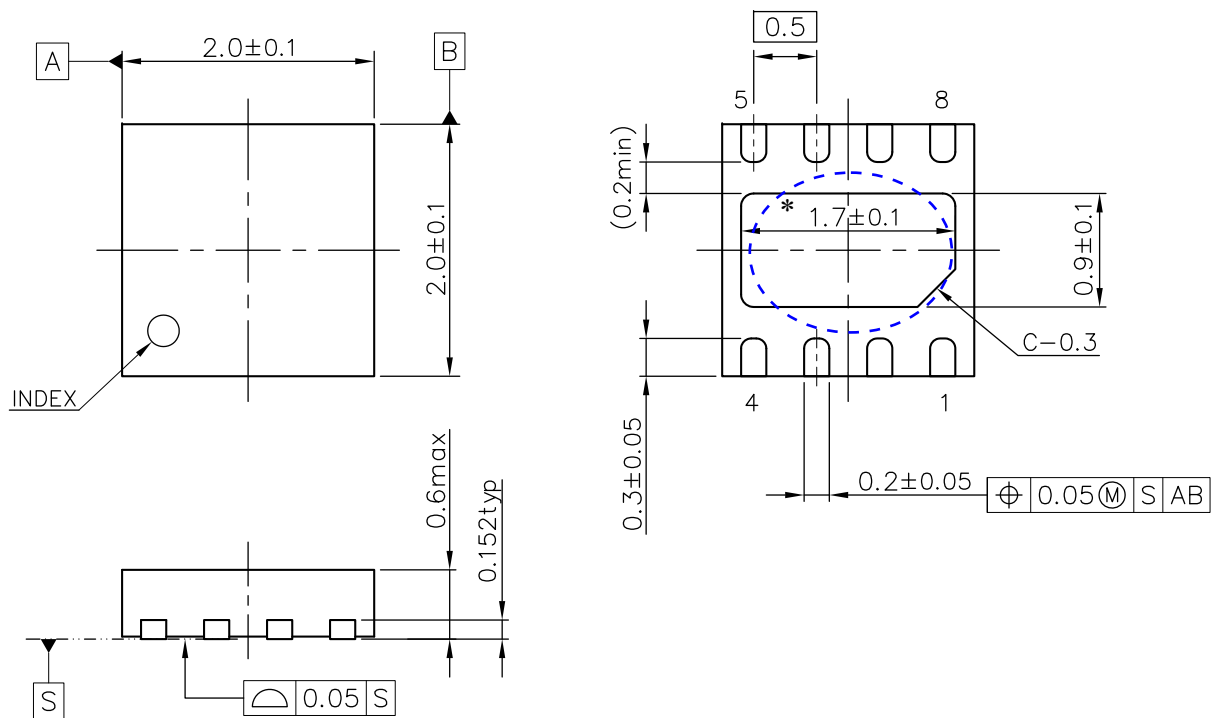
θja: Junction-to-Ambient Thermal Resistance
ψjt: Junction-to-Top Thermal Characterization Parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern



DFN2020-8C Package Dimensions (Unit: mm)

* The tab on the bottom of the package shown by blue circle is a substrate potential (GND). It is recommended that this tab be connected to the ground plane on the board but it is possible to leave the tab floating.



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