RICOH R5601T Series

Lithium-Ion/ Lithium Polymer Battery Management Analog Front-End

NO.EA-356-190910

OVERVIEW

The R5601T is a battery management IC designed for use with a microcontroller and features and analog front-end with overcurrent protection for multi-cell Li-ion/ Li-polymer battery packs. The R5601T supports battery packs consisting of up to 5 cells in series. The R5601T provides a cell selection switch, a decoder that selects the cell to be monitored based on input signals from external devices, an amplifier that outputs the monitored battery voltage, an additional amplifier that monitors charge and discharge currents based on the voltage at both ends of external resistors and then converts the current values to voltage and outputs the voltage values, a low-current voltage regulator that provides voltage to the MCU, a thermal shutdown circuit, an alert output pin that notifies external devices of any errors, and various logic circuits. The R5601T is offered in a 16-pin TSSOP-16 package.

FEATURES

- High-voltage Process ····· Absolute Maximum Rating: 32 V
- Low Current Consumption ····· Normal Mode: Typ. 36 µA
  Low Consumption Mode: Typ. 6.5 µA
  (Only VR and wakeup function operating)
  Standby Mode: Max. 2.0 µA
- High-accuracy Voltage Monitor ····· Gain: 0.6 Input-referred Voltage Error: ±9 mV
  Output-referred Voltage Error: ±5.4 mV
- High-accuracy Current Monitor ····· R5601TxxxAA Gain: 10 ±1.0%, 40 ±2.0%
  R5601TxxxAC Gain: 5 ±0.8%, 10 ±1.0%
- Short-circuit Current Detection ····· The detector threshold/ time are settable using I^2C interface.
  Detector Threshold: 0.10, 0.15, 0.20, 0.40 V
  Delay Time: 50, 100, 200, 400, 800 µs
- External Reference Voltage Output ····· 3.0000 V ±3.5 mV
  Temp. Characteristics: ±30 ppm/°C (0 ≤ Ta ≤ 50°C, Ta ≈ Tj)
- Voltage Regulator Output Voltage ····· 3.3 V, Output Voltage Accuracy: 1.5% (−20°C to 60°C)
  Output Current Limit: Min. 30 mA
- Thermal Shutdown ····· can be enabled or disabled by using I^2C interface
- Built-in FET Switch ····· FET Switch can be set with MCU using I^2C interface
- Alert Output ····· provides a notification to MCU when detecting an event
- Low-Power Mode ····· disables some of the internal function by the MCU control
- Standby Mode ····· sets the IC to standby mode by inputting an external signal to reduce the consumption current.
- Wake-up Function ····· sets the IC to normal mode when detecting a discharging current to reduce the consumption current.
- I^2C Interface ····· using an I^2C allows to control the IC with MCU
- Package ····· TSSOP-16 (0.65 mm pitch)

APPLICATIONS

- Power Tools
- Power Storages
- Cordless Vacuum Cleaners/ Robot Vacuum Cleaners

SELECTION GUIDE

The I²C slave address and the IC functions are user-selectable options with the R5601T.

Selection Guide

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R5601TxxxYY-E2-FE	TSSOP-16	2,500 pcs	Yes	Yes

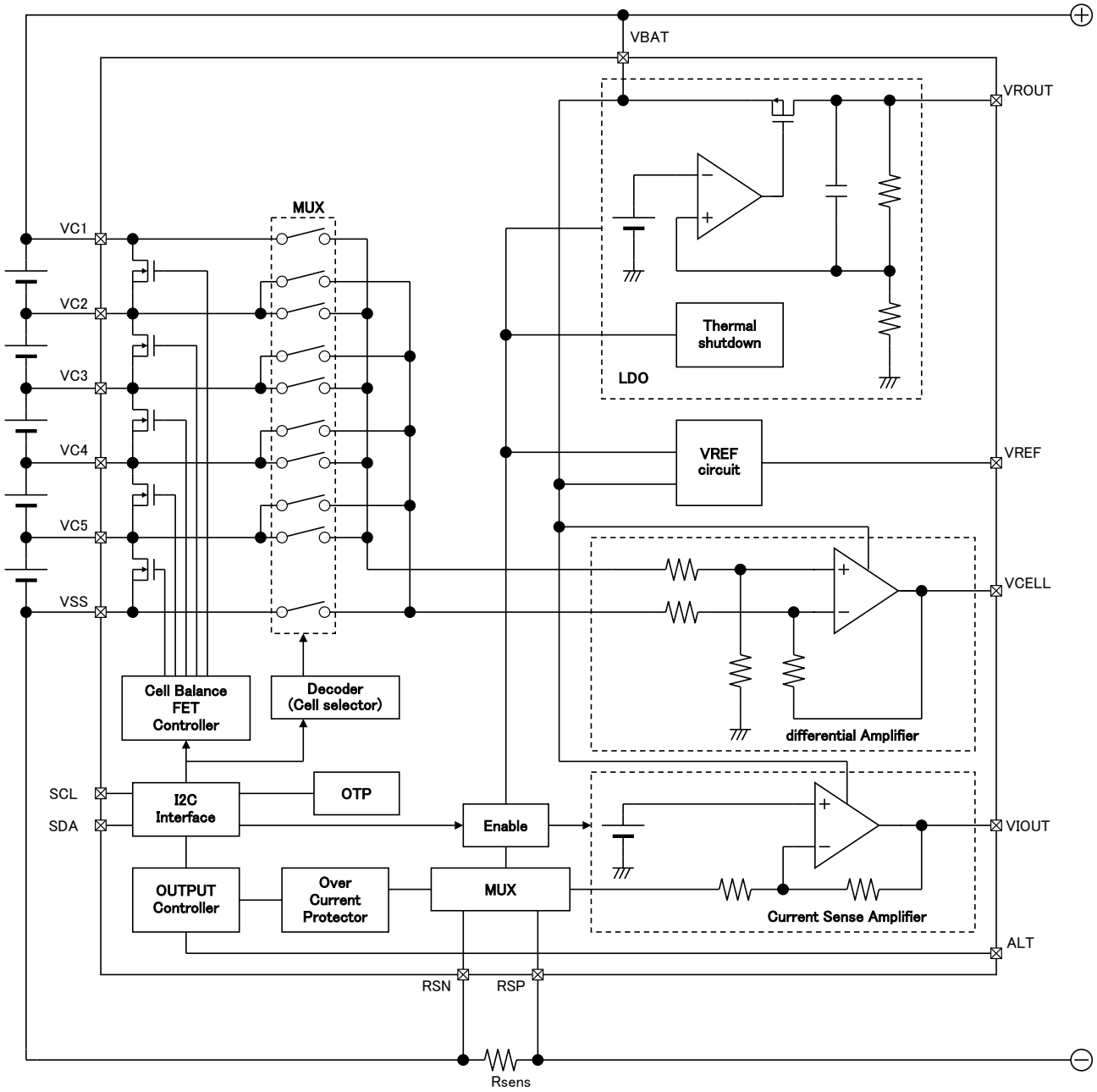
xxx: Specify the I²C slave address from below.

xxx	I²C Slave Address
047	2Fh
063	3Fh

YY: Specify the IC functions from below.

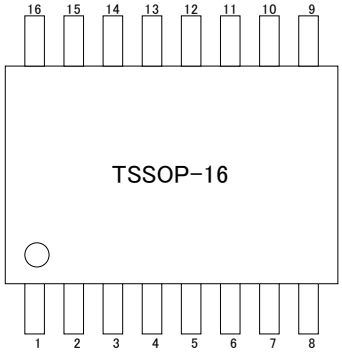
YY	VROUT Output Voltage	Voltage Monitoring Gain	Current Monitoring Gain	External Output Reference Voltage
AA	3.3 V	0.6	10/40	3.000 V
AC	3.3 V	0.6	5/10	3.000 V

BLOCK DIAGRAM



R5601T Block Diagram

PIN DESCRIPTIONS



R5601T (TSSOP-16) Pin Configuration

R5601T Pin Descriptions

Pin No.	Pin Name	Description
1	VROUT	Voltage Regulator Output Pin
2	VCELL	Cell Voltage Monitoring Output Pin
3	VREF	External Reference Voltage Output Pin
4	VIOUT	Current Monitoring Output Pin
5	ALT	Alert I/O Pin
6	SDA	Serial Data I/O Pin
7	SCL	Serial Clock Input Pin
8	RSP	R_{SENS} Positive Input Pin
9	RSN	R_{SENS} Negative Input Pin
10	VSS	IC Ground Pin
11	VC5	Positive Terminal of Cell 5
12	VC4	Positive Terminal of Cell 4
13	VC3	Positive Terminal of Cell 3
14	VC2	Positive Terminal of Cell 2
15	VC1	Positive Terminal of Cell 1
16	VBAT	Power Supply Pin

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings (Ta = 25°C, V_{SS} = 0 V)

Symbol	Description	Rating	Unit
V_{BAT}	Power Supply Voltage	−0.3 to 32	V
	[Input Voltage]		
V_{C1}	Positive Terminal Pin Voltage of CELL1	V_{C2} −0.3 to V_{C2} +9.0, V_{C2} −0.3 to V_{SS} +32	V
V_{C2}	Positive Terminal Pin Voltage of CELL2	V_{C3} −0.3 to V_{C3} +9.0	V
V_{C3}	Positive Terminal Pin Voltage of CELL3	V_{C4} −0.3 to V_{C4} +9.0, V_{C4} −0.3 to V_{SS} + 24	V
V_{C4}	Positive Terminal Pin Voltage of CELL4	V_{C5} −0.3 to V_{C5} +9.0	V
V_{C5}	Positive Terminal Pin Voltage of CELL5	V_{SS} −0.3 to V_{SS} +9.0	V
V_{SDA}	SDA Input Voltage	V_{SS} −0.3 to V_{ROUT} +0.3	V
V_{SCL}	SCL Input Voltage	V_{SS} −0.3 to V_{ROUT} +0.3	V
V_{RSN}	RSN Pin Input Voltage	V_{ROUT} −6.0 to V_{ROUT} +0.3	V
V_{RSP}	RSP Pin Input Voltage	V_{ROUT} −6.0 to V_{ROUT} +0.3	V
V_{ALT}	ALT Pin Input Voltage	−0.3 to 32	V
	[Output Voltage]		
V_{CELL}	Cell Voltage Monitoring Output Voltage	V_{SS} −0.3 to 6.5	V
V_{IOUT}	Current Monitoring Output Voltage	V_{SS} −0.3 to 6.5	V
V_{REF}	External Reference Voltage Output Voltage	V_{SS} −0.3 to 6.5	V
V_{ROUT}	VR Output Voltage	V_{SS} −0.3 to 6.5	V
	[Output Current]		
I_{CELL}	Cell Voltage Monitoring Output Current	1.0	mA
I_{IOUT}	Current Monitoring Output Current	1.0	mA
I_{REF}	External Reference Voltage Output Current	1.0	mA
I_{OUT}	VR Output Current	80	mA
P_D	Power Dissipation	Refer to Appendix “Power Dissipation”.	
Tj	Junction Temperature Range	−40 to 125	°C
Tstg	Storage Temperature Range	−55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITIONS

Recommended Operating Conditions

Symbol	Item	Rating	Unit
V_{BAT}	Input Voltage	4.0 to 22.5	V
Ta	Operating Temperature Range	−40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics (Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input Section						
$R_{CB}n$	Built-in FET ON Resistance	V_{CN} = 4.0 V		10		Ω
$I_{LVC}n$	Cell Voltage Input Leakage	V_{CN} = 4.5 V, Built-in FET: OFF Cell Voltage Monitoring: OFF			0.3	µA
Voltage Regulator						
V_{ROUT}	Output Voltage	I_{OUT} = 1 mA, V_{BAT} = 4.0 to 22.5 V	3.27	3.30	3.33	V
ΔV_{ROUT}	Output Voltage Temperature Characteristics	−20°C ≤ Ta ≤ 60°C, I_{OUT} = 1 mA(1)	−1.5		1.5	%
I_{LIM}	Output Current Limit		30			mA
I_{SC}	Short Current Limit	V_{ROUT} = 0 V		20		mA
V_{DIF}	I/O Voltage Difference	I_{OUT} = 30 mA, V_{ROUT} = 3.3 V R_{BAT} = 10 Ω			0.7	V
T_{SDD}	Thermal Shutdown Temperature	(2)		150		°C
T_{SDR}	Thermal Shutdown Released Temperature	(2)		125		°C
Cell Voltage Monitoring / External Reference Voltage						
V_{VCIN}	Cell Voltage Input Range		1.5		4.5	V
V_{VCA}	Cell Voltage Monitoring Accuracy(3) (Output- Referred Voltage Error)	I_{VC} = 1 µA	−5.4		5.4	mV
		−20°C ≤ Ta ≤ 60°C, I_{VC} = 1 µA(1)	−7.8		7.8	mV
G_{VC}	Cell Voltage Monitoring Gain	I_{VC} = 1 µA		0.6		
I_{VC}	Cell Voltage Monitoring Pin Output Current	V_{BAT} = 18 V			10	µA
tvcset	Cell Voltage Monitoring Output Delay Time	C_{CEL} = 0.1 µF(2)			200	µs
V_{REF}	External Reference Voltage(4)	I_{REF} = 1 µA	2.9965	3.000	3.0035	V
ΔV_{REF} / ΔTa	External Reference Voltage Temperature Characteristics	0°C ≤ Ta ≤ 50°C, I_{REF} = 1 µA(1)		±30		ppm /°C
		−20°C ≤ Ta ≤ 60°C, I_{REF} = 1 µA(1)		±60		
I_{REF}	External Reference Voltage Output Current				10	µA

(1) Measurements are performed in an environment in which Tj is nearly equal to Ta. High and low temperature tests are not executed at the mass production line, therefore, this specification in the specified temperature range is guaranteed by design.
(2) guaranteed by design
(3) The Input-referred voltage error can be calculated as V_{VCA} / G_{VC}. This is the after correction value.
(4) This is the after correction value.

Electrical Characteristics (Continued) (Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Current Monitor /Short-Circuit Protection							
V_{CUIN10}	Voltage Input Range (Gain 10)			−25		225	mV
V_{CUIN40}	Voltage Input Range (Gain 40)			−6.25		56.25	mV
V_{CUIN5}	Voltage Input Range (Gain 5)			−50		450	mV
G_{CU10}	Current Monitoring Gain 10	(1) (2)			10		
G_{CU40}	Current Monitoring Gain 40	(1) (2)			40		
G_{CU5}	Current Monitoring Gain 5	(1) (2)			5		
G_{CUA10}	Current Monitoring Gain Accuracy 10	When G_{CU10} is selected(1)		−1.0		1.0	%
G_{CUA40}	Current Monitoring Gain Accuracy 40	When G_{CU40} is selected(1)		−2.0		2.0	%
G_{CUA5}	Current Monitoring Gain Accuracy 5	When G_{CU5} is selected(1)		−0.8		0.8	%
V_{CU0}	Zero-Current Output	V_{RSP} = 0 V			2.5		V
I_{CU}	Current Monitoring Output Current					10	uA
V_{SHORT}	Short-Circuit Detector Threshold Setting Range	four-steps variable settings via I^2C: 0.10 V, 0.15 V, 0.20 V, 0.40 V		0.1		0.4	V
V_{STACC}	Short-Circuit Detector Threshold Accuracy			−10		10	%
t_{SHORT}	Short-Circuit Detect Output Delay Time Setting Range	five-steps variable settings via I^2C: 50, 100, 200, 400, 800 µs		50		800	µs
t_{STACC}	Short-Circuit Detect Output Delay Time Accuracy	V_{RSP}: 0V -> 1 V, V_{SHORT} = 0.4 V	T_{SHORT} = 50 µs			100	µs
			T_{SHORT} ≥ 100 µs	−50		50	%

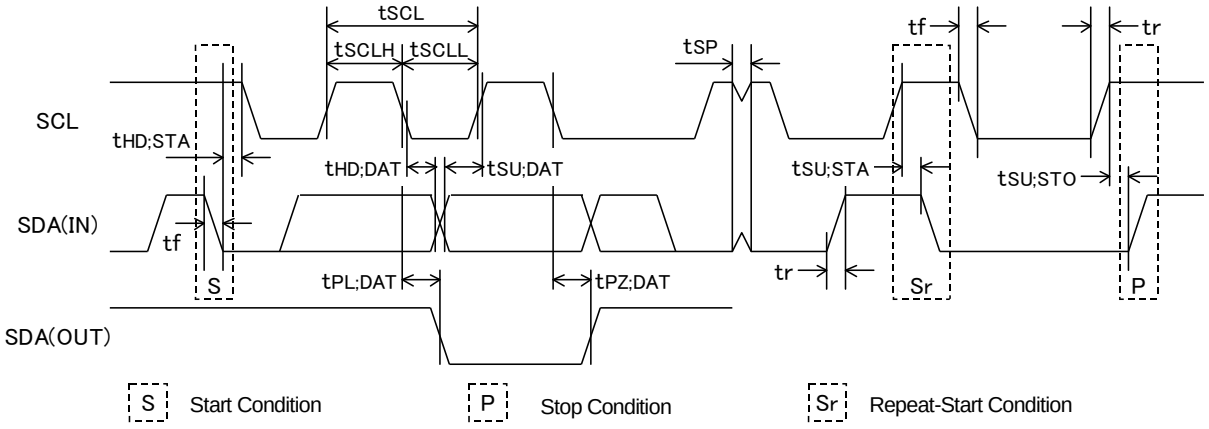
(1) Settings depending on the preset product code.
(2) Calculated from the minimum and maximum input voltage range at each gain.

Electrical Characteristics (Continued) (Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input Function						
V_{IHDA}	SDA "High" Input Voltage	V_{ROUT} = 3.3 V	V_{ROUT} x 0.8			V
V_{ILDA}	SDA "Low" Input Voltage	V_{ROUT} = 3.3 V			V_{ROUT} x 0.2	V
V_{IHCL}	SCL "High" Input Voltage	V_{ROUT} = 3.3 V	V_{ROUT} x 0.8			V
V_{ILCL}	SCL "Low" Input Voltage	V_{ROUT} = 3.3 V			V_{ROUT} x 0.2	V
V_{IHAL}	ALT "High" Input Voltage	In standby mode	2.0			V
V_{ILAL}	ALT "Low" Input Voltage	In standby mode			0.3	V
I_{IHDA}	SDA "High" Input Current	V_{ROUT} = 3.3 V	−1		1	µA
I_{IHCL}	SCL "High" Input Current	V_{ROUT} = 3.3 V	−1		1	µA
I_{IHAL}	ATL "High" Input Current	V_{BAT} = 22.5 V	−1		1	µA
Output Function						
V_{OLDA}	SDA "Low" Output Voltage	I_{OL} = 3 mA, V_{ROUT} = 3.3 V			0.4	V
V_{OLAL}	ALT "Low" Output Voltage	I_{OL} = 50 µA, V_{ROUT} = 3.3 V			0.4	V
Wakeup /Standby Function						
V_{POR}	Power ON Reset Voltage			2.0	2.5	V
V_{WUP}	Wakeup Voltage Setting Range	variable settings via I^2C: 10 mV, 20 mV, 40 mV, or 80 mV.	10		80	mV
V_{WUPAC}	Wakeup Voltage Accuracy	V_{WUP} = 10 mV 20 mV ≤ V_{WUP}	−3 −25		3 25	mV %
twupdl	Wakeup Delay Time Setting Range	variable settings via I^2C: 2 ms, 4 ms, 8 ms, 16 ms, 32 ms, 64 ms	2		64	ms
twupac	Wakeup Delay Time Accuracy	T_{WUP} ≤ 4 ms, 4 ms < T_{WUP}	−50 −30		50 30	%
I_{SS1}	VBAT Supply Current 1	Normal mode, V_{CX} = 3.7 V		36	48	µA
I_{VCEL}	Cell Voltage Monitoring Operating Current	V_{CX} = 3.7 V		10		µA
I_{VIO}	Current Monitoring Operating Current	V_{CX} = 3.7 V		10		µA
I_{VREF}	External Reference Voltage Operating Current	V_{CX} = 3.7 V		10		µA
I_{SS2}	VBAT Supply Current 2	Low Power Mode (Only VR and wakeup function operating), V_{CX} = 3.7 V		6.5	9.0	µA
I_{STB}	Standby Current	V_{CX} = 3.7 V		1.5	2.0	µA

Electrical Characteristics (Continued) (Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Serial Interface AC Characteristics						
fclk	SCL Clock Frequency				400	kHz
tclk	SCL Clock Cycle		2.5			µs
tscll	SCL Clock "Low" Time		1.3			µs
tsclh	SCL Clock "High" Time		0.6			µs
tsu:sta	Start Condition Setup Time		0.6			µs
tsu:dat	Data Setup Time		200			ns
tsu:sto	Stop Condition Setup Time		0.6			µs
thd:sta	Start Condition Hold Time		0.6			µs
thd:dat	Data Hold Time		0			ns
tr	SDA and SCL Rise Time(1)				300	ns
tf	SDA and SCL Fall Time(1)				300	ns
tpl:dat	SDA "Low" Determination Time after the Falling of SCL				0.9	µs
tpz:dat	SDA "High" Determination Time after the Falling of SCL				0.9	µs
tsp	Removal Spike Width by Input Filters				50	ns
C_B	Capacitive Load for SDA and SCL Bus Lines				50	pF



AC Specifications for the I²C Bus (Data Transfer Method)

(1) The relationship between the I²C bus capacity (C_B) and the pull-up resistance values (R_P: 3.3 kΩ is recommended).

THEORY OF OPERATION

Cell Voltage Monitoring

The R5601T is an IC that monitors the voltage of each cell of lithium-ion and lithium polymer secondary batteries of up to five cells. If a cell whose voltage is to be monitored is selected by controlling the IC from the MCU via the I²C interface, the voltage of that cell will be multiplied by the gain and then output from the VCELL pin. Accordingly, the following equation can be obtained by calculating the battery voltage from the output voltage:

$$VC_x - VC_{x+1} = \frac{Vvc}{Gvc}$$

Herein, the offset and the gain error are included in the output voltage, therefore values for adjustment are stored in the registers of each IC. Adjustment can be done by the next formula.

Correction value for voltage monitoring offset: $CVOS$
Correction value for voltage monitoring gain: $CGVC$

$$VC_x - VC_{x+1} = \frac{Vvc \times (1 + 10^{-4} \times CVOS + 10^{-6} \times CGVC \times VC_{x+1})}{Gvc}$$

Note: When you monitor the voltage between VC_5 and VSS, 0V should be input VC_{x+1}.

If there is no cell voltage output instruction from the external MCU, or if a cell voltage monitoring amplifier stop instruction has been issued, or if the R5601T is in standby mode, the output will be pulled down to the VSS by an internal resistor.
To ensure accurate monitoring of the cell voltage, make measurements with the built-in FET switch turned off. If you do not do so, the input resistance and current will cause the voltage to drop when a current flows through the built-in FET switch, thereby preventing the expected level of voltage from being output from the VCELL pin.

Internal FET Control

By controlling the internal FET by the external MCU via the I²C Interface, the R5601T can flow the discharge current into the IC from each cell. The discharge current can be set by external resistor. When select external resistor, pay attention to the power dissipation of the external resistor and the input current tolerance of the IC. The internal FET must be controlled so that the adjacent internal FET is not also turned on at the same time. When selecting a cell for voltage monitoring during the internal FET's on, the internal FET capability is limited

Current Monitoring

The R5601T outputs a current that flows through the RSENS resistor located between the RSN and RSP pins after conversion to a voltage. The R5601T always outputs a positive voltage, but outputs V_{CU0} at zero current. Because the voltage of the RSP pin is inversely amplified by the G_{CU} gain, the output will be smaller than V_{CU0} when a discharge current flows, and will be larger than V_{CU0} when a charging current flows. Moreover, the built-in multiplexer enables switching between RSP input and RSN input, in which case the following equation can be used by the host to adjust the current value to the more accurate I_{SENS} value:

$$I_{SENS} = \frac{V_{CU}(RSP) - V_{CU}(RSN)}{G_{CU} \times R_{SENS}}$$

G_{CU} can be switched via I^2C communication. The following table shows the amplifier input and output ranges. The I_{SENS} range in the table shows discharge current as positive values and charging current as negative values.

When R_{SENS} is 1 mΩ and a 10-bit ADC is used

G_{CU}	V_{CU0} [V]	RSP Input Voltage Range [mV]		V_{IOUT} Output Voltage Range [V]		I_{SENS} Range [A] (R_{SENS} = 1 mΩ)		I_{SENS} Resolution [mA] (When 10-bit ADC used)
		Min.	Max.	Min.	Max.	Min.	Max.	
5	2.5	−50	450	0.25	2.75	−50	450	586
10	2.5	−25	225	0.25	2.75	−25	225	293
40	2.5	−6.25	56.25	0.25	2.75	−6.25	56.25	73

When R_{SENS} is 0.5 mΩ and a 10-bit ADC is used

G_{CU}	V_{CU0} [V]	RSP Input Voltage Range [mV]		V_{IOUT} Output Voltage Range [V]		I_{SENS} Range [A] (R_{SENS} = 0.5 mΩ)		I_{SENS} Resolution [mA] (When 10-bit ADC used)
		Min.	Max.	Min.	Max.	Min.	Max.	
5	2.5	−50	450	0.25	2.75	−100	900	1172
10	2.5	−25	225	0.25	2.75	−50	450	586
40	2.5	−6.25	56.25	0.25	2.75	−12.5	112.5	146

When R_{SENS} is 0.5 mΩ and a 12-bit ADC is used

G_{CU}	V_{CU0} [V]	RSP Input Voltage Range [mV]		V_{IOUT} Output Voltage Range [V]		I_{SENS} Range [A] (R_{SENS} = 0.5 mΩ)		I_{SENS} Resolution [mA] (When 12-bit ADC used)
		Min.	Max.	Min.	Max.	Min.	Max.	
5	2.5	−50	450	0.25	2.75	−100	900	293
10	2.5	−25	225	0.25	2.75	−50	450	146
40	2.5	−6.25	56.25	0.25	2.75	−12.5	112.5	37

If the stop command is set for the external voltage reference output or the current monitoring amplifier by the MCU, or if the R5601T is in standby mode, the output will be pulled down to the V_{SS} by an internal resistor.

External Reference Voltage Output

The R5601T outputs the reference voltage that is used by the external A/D converters and for current monitoring. If an external reference voltage output stop instruction is received from the external MCU or if the R5601T is in standby mode, the output will be pulled down to the VSS by the internal resistor. The externally output reference voltage has an offset against the preset value. This offset value is stored in the register.

Short-circuit Current Detection

The R5601T contains a function that detects a short-circuit current through the discharge path and makes the output of the ALT pin to "Low" by monitoring the RSP pin voltage as both ends of the resistor located on the discharge path. If the load is removed and identified opening the load, the output of the ALT pin can be changed into "Hi-Z" by a reset command from the external MCU. Not only the short detector threshold and delay time can be changed, but also the short-circuit detection function can be invalid by the external MCU command.

Voltage Regulator

The R5601T contains a 30-mA voltage regulator for operation of the external MCU. The voltage regulator operates when the voltage of the VBAT pin is between 4.0 and 22.5 V. When the R5601T is in standby mode, the output will be pulled down to the VSS by the internal resistor. The R5601T also contains a thermal shutdown function to protect itself from overheating. If the heat generated by the voltage regulator causes the junction temperature (Tj) to exceed 150°C (Typ.), the output driver will turn off to protect the IC, thereby causing the output of the voltage regulator to turn off. If the junction temperature (Tj) drops below 125°C (Typ.), the output driver will turn on and the output of the voltage regulator will turn on. Operation of the thermal shutdown function can be stopped from the external MCU.

ALT pin Output Function

The R5601T can drive the output of the ALT (normally Hi-Z) low to prevent the reporting of an event that the R5601T itself has detected to external devices. The output format of the ALT pin is N-channel Open Drain.

Because information on an event that has been detected is stored in an internal register, the MCU can identify the event by reading the event information in the register via the I^2C interface. To return the ALT pin's output from "Low" to "Hi-Z", write "0" to all EVT registers while R5601T is not detecting an event.

Wakeup Function

The R5601T has a wakeup function. When detected the increase of the voltage of the RSP pin by the action of the discharge current and the sense resistance (R_{SENS}), the R5601T's action varies with modes. In the case of the standby mode, the R5601T is restored after a preprogrammed delay time.

Also, in the case of the other modes except the standby mode, after the delay time, the R5601T sets the ALT pin to "Low" and provides notification of this event to the MCU.

The RSP pin voltage and delay time for this event and the enabled / disabled of the wakeup circuit can be set by the MCU via the I^2C interface.

Standby Function

The R5601T has a standby function. The MCU provides an instruction to switch to standby mode to the R5601T via the I²C interface. The R5601T can restore from the standby mode by the wakeup function, or else by the ALT pin's pulled-up.

I²C SERIAL COMMUNICATIONS

Overview: The I²C interface for the R5601T chip is used in slave mode.

I²C Interface Pins

Signal Name	I/O	Polarity	Description	Remarks
SDA	I/O	-	Serial Data Input/ Output	Open Drain
SCL	I	-	Serial Clock Input	CMOS Input

[Slave Address]

The slave address consists of seven bits and is fixed as "xxxxxxx : yyh".

(For details about the settings of the slave address, see the Selection Guide.)

[Read / Write Processing]

The following are the specifications of the read/write processing as viewed from the MCU:

0: Write processing (Inputs the data transferred from the MCU at the rising edge of SCL)

1: Read processing (Outputs data at the falling edge of SCL)

Data Transfer Method

(1) Start and stop conditions

Basically, the I²C bus must remain in a constant state while the SCL signal level is high during data transfers, as shown in Figure A.

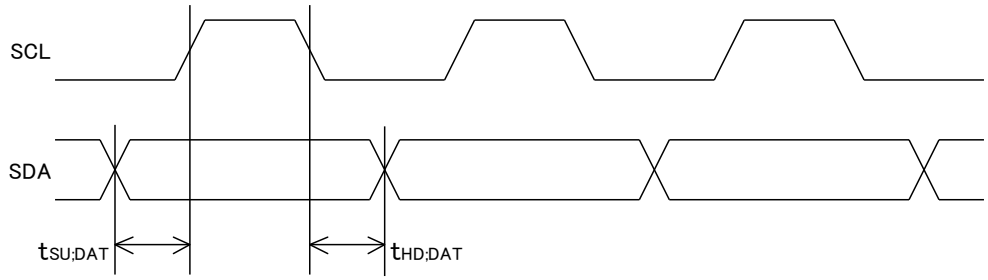


Figure A. SCL and SDA Signals

Both the SCL and SDA signals are high when no data is being transferred. If the SDA signal changes from high to low while both the SCL and SDA signals are high, a start condition is generated and access processing starts. However, if the SDA signal changes from low to high while the SCL signal is high, a stop condition is generated and access processing ends. (See Figure B.) Start and stop conditions are always generated by the master.

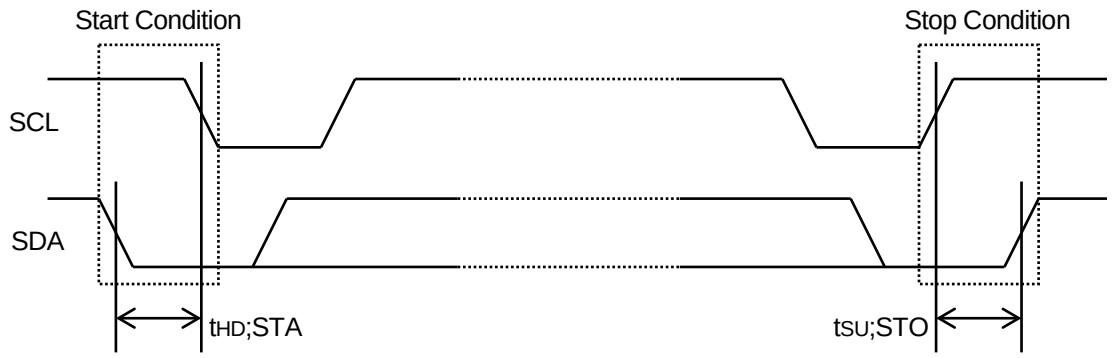


Figure B. Start and Stop Conditions

(2) Data transfer and acknowledgment (ACK)

After a start condition is generated, data is transferred one byte (eight bits) at a time. Any number of bytes of data can be transferred in succession. An ACK signal is sent from the receiver to the sender to acknowledge that eight bits of data has been received.

As soon as the clock pulse of the eighth bit of the SCL signal in the transfer data goes low, an ACK signal is generated that causes the sender that has been asserting the bus up to that point to release the SDA pin and the receiver to drive the SDA signal low. If there is another byte of transfer data to be received after the receiver has sent an ACK signal, the sender will transfer the data. If the master is the receiver, the master will not generate an ACK signal after the last byte of data has been sent from the slave in order to notify the sender device that the data transfer is complete. In this case, the slave, which is the sender, will leave the SDA pin in the released state so that the master can generate a stop condition.

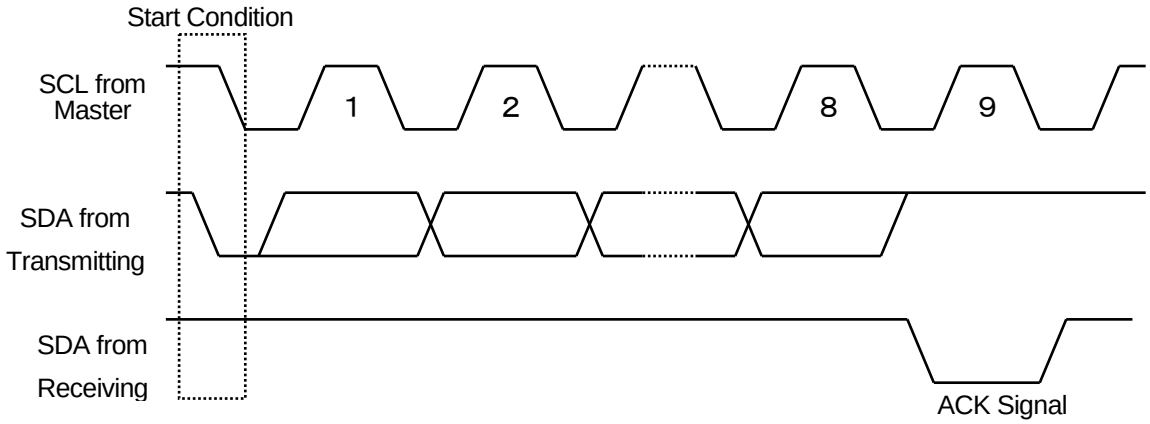


Figure C. Data Transfer and ACK Signal

Basically, the I^2C bus must remain in a constant state while the SCL signal is high during data transfers, as shown in Figure A.

Data Write Method

Figure D shows the data write format.

1st byte: Slave address + Write instruction.
2nd byte: Address of the internal register to which the data is to be written.
3rd byte: Data to be written to the address specified in the second byte.
4th and subsequent bytes: Data to be written to the automatically incremented address.

The master issues a start condition, and the slave receives the first byte of data that follows the start condition and returns an ACK signal to the master.
If the slave address that the slave receives matches its own address, the slave receives the second and subsequent bytes of data in order and returns an ACK signal to the master each time a byte is received.
After all necessary data has been written, the master will issue a stop condition to end the write operation.
If, however, the slave address that the slave receives does not match its own address, the slave will not return an ACK signal to the master.

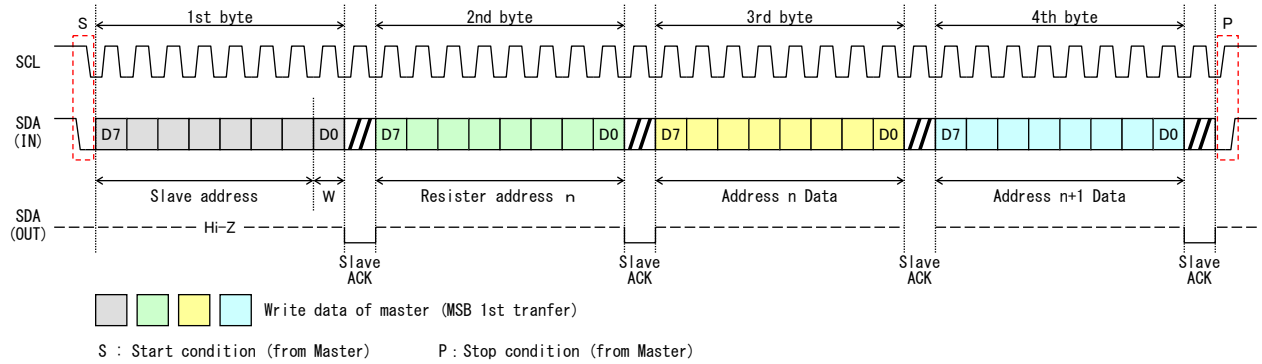


Figure D. Data Write Method

Data Read Method

Figure E shows the data read format.

1st byte: Slave address + Write instruction.
2nd byte: Address of the internal register from which the data is to be read.
3rd byte: Slave address + Read instruction.
4th byte: Data to be read from the address specified in the second byte.
5th and subsequent bytes: Data to be read from the automatically incremented address.

The master issues a start condition, and the slave receives the first byte of data that follows the start condition and returns an ACK signal to the master. If the slave address that the slave receives matches its own address, the slave receives the second byte of data and returns an ACK signal to the master. Next, the master issues a repeated start condition, sends the slave address and a read instruction with the third byte of data, and then switches the serial access direction.
The data with the address specified as the second byte of data is read as the fourth byte of data, and the master issues an ACK signal.
The fifth and subsequent bytes of data are read sequentially by automatically incrementing the address. When all necessary data has been read, the master does not return an ACK signal to notify the slave that the read processing has completed. Instead, the master issues a stop condition to end the read operation.

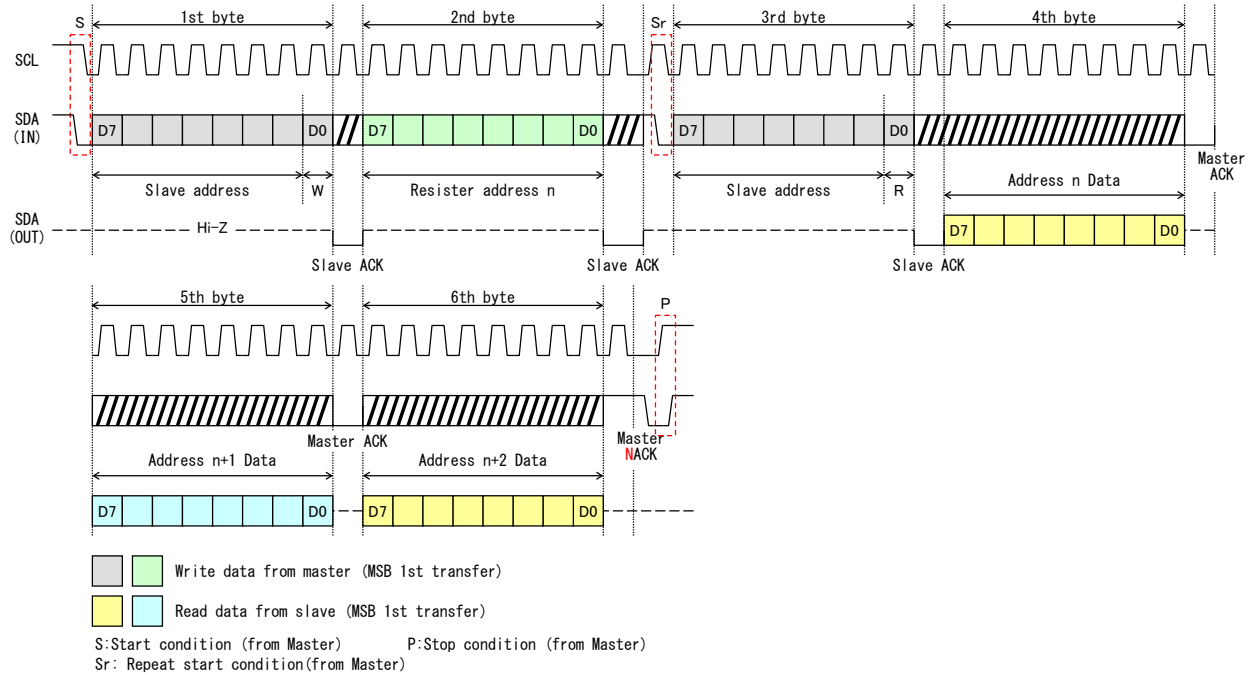


Figure E. Data Read Method

Repeated Start Condition

Figure F shows the format of a repeated start condition. The master issues a repeated start condition, and the slave receives the first byte of data that follows the repeated start condition and returns an ACK signal to the master. After a repeated start condition is issued, the write instruction writes data by using the same procedure that is used for a normal start condition. This is shown in the seventh to the tenth bytes of data in Figure F. After a repeated start condition is issued, the read instruction starts to read from the addresses specified as the second and eighth bytes of data in Figure F. Each time an ACK signal is returned from the master, the address is automatically incremented and the data at that address is read.

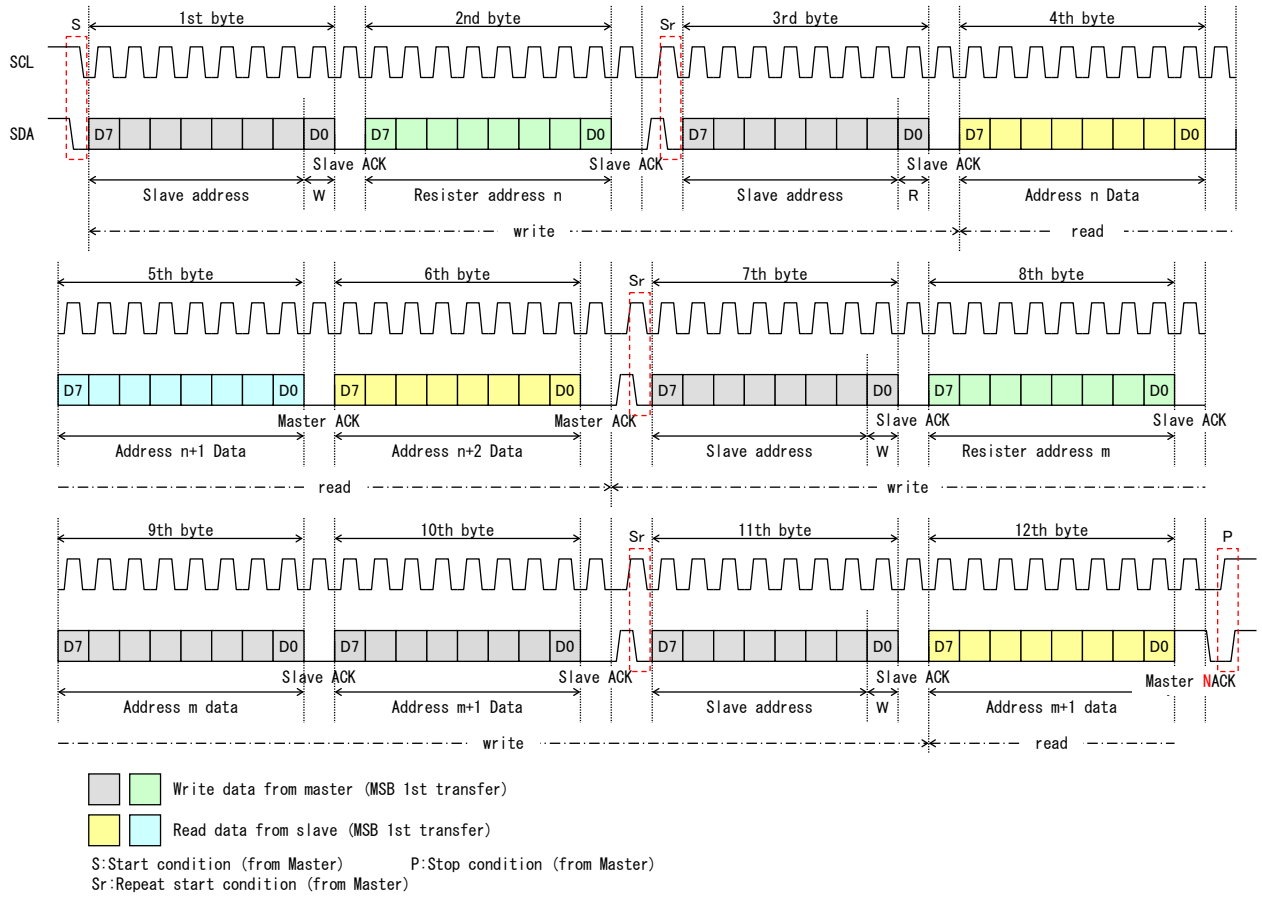


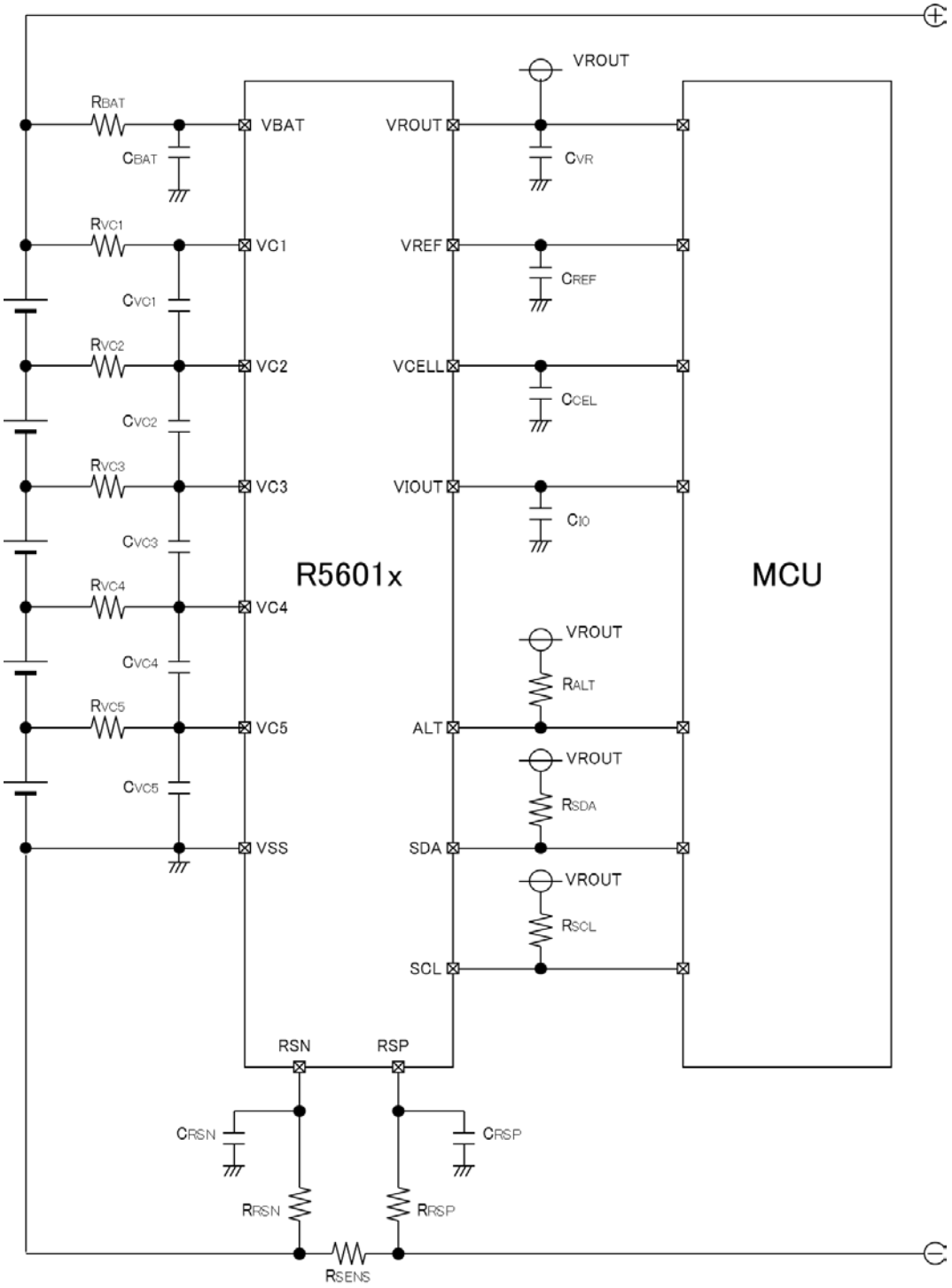
Figure F. Repeated Start Condition

Error Processing

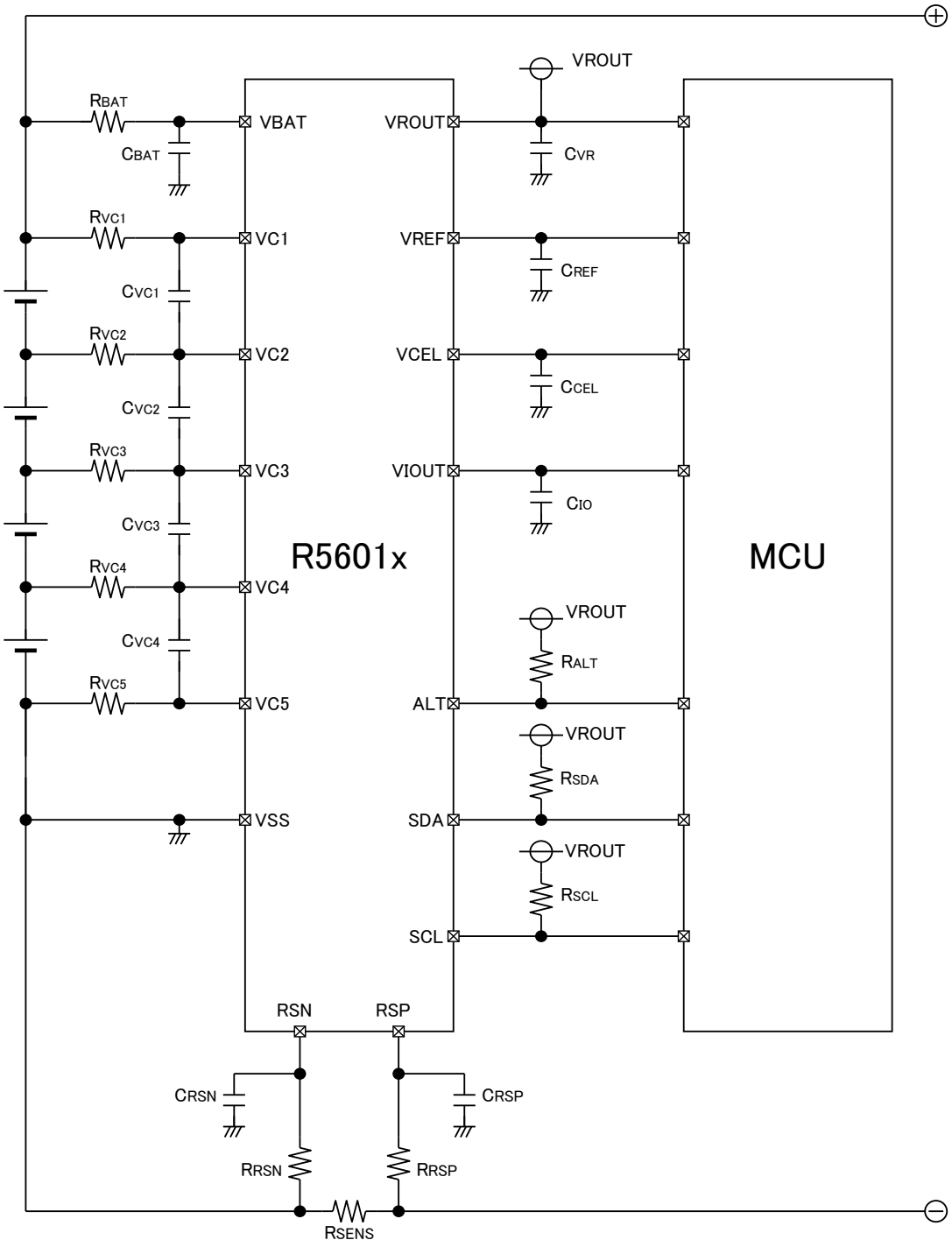
- If an ACK signal is not returned from the slave during data write processing, temporarily terminate the write processing, issue a stop condition or repeated start condition, and the restart the write processing.
- If, for some reason, a data transfer either has been stopped or has stopped during communication, issue another start condition and then restart the data transfer from scratch according to the specified procedure.
- If the master issues a condition instruction while the slave has control of the bus, the slave will not accept the instruction. Accordingly, avoid this kind of usage.
- If the master device is turned off and then on again when the slave is active, communication might not be possible, depending on the slave status when the maser device is turned off (for example, when the slave is in read mode).
- In such cases, continue to send clock signals from the master, and either issue a condition when the slave receives an ACK signal from the master, or reset the R5601T as described later.
- If the action just described does not resolve the problem, reset the R5601T by turning the power off and then on again.

APPLICATION INFORMATION

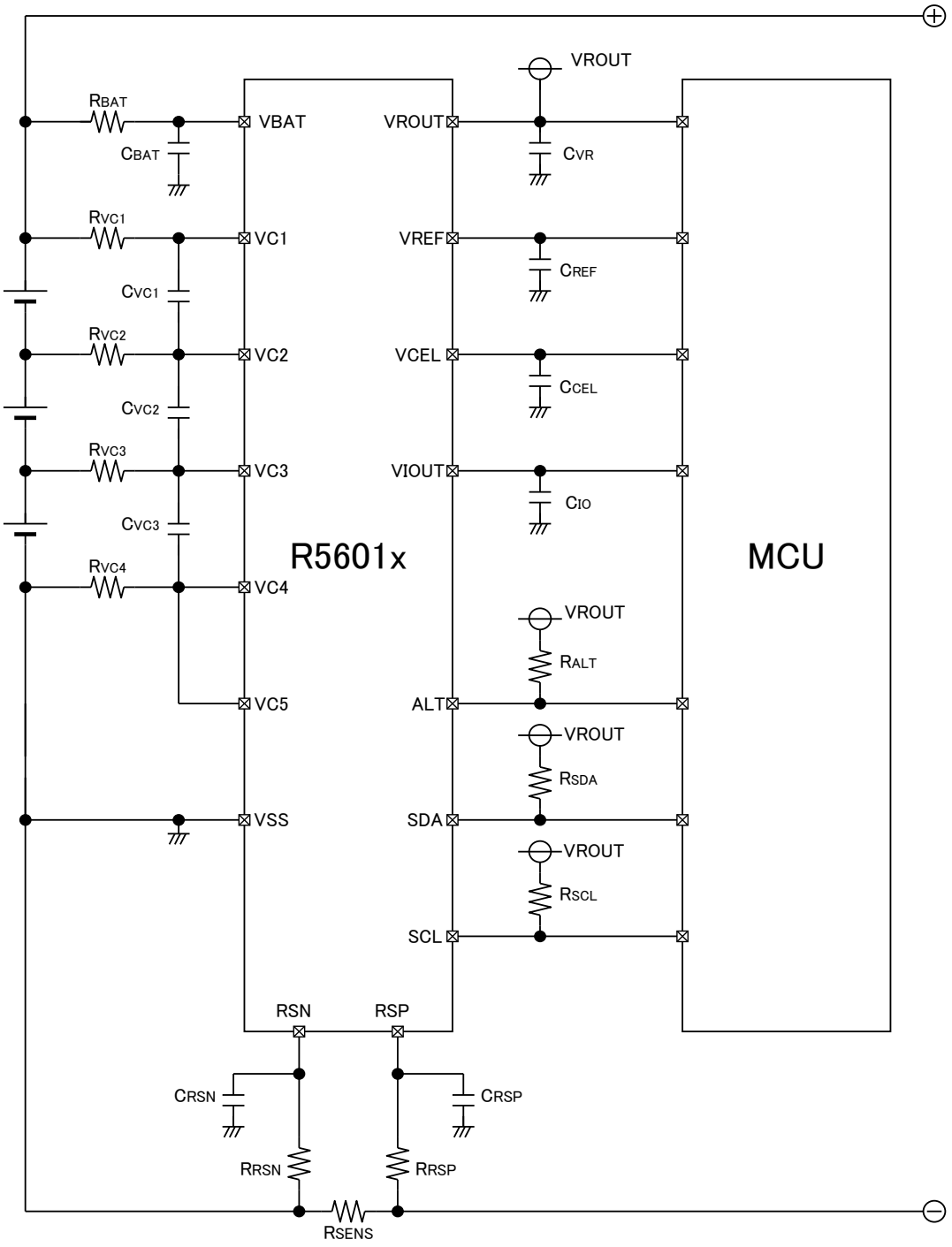
- **TYPICAL APPLICATIONS（ 5 Cells /4 Cells / 3 Cells）**



R5601T Typical Application for 5 Cells



R5601T Typical Application for 4 Cells



R5601T Typical Application for 3 Cells

External Components List

Symbol	Typ.	Unit	Setting Range	Remarks
R_{BAT}	10	Ω	10 or more	Pay careful attention to the power dissipation for R_{BAT}.
R_{VC1}	100	Ω	100 to 1000	(1)
R_{VC2}	100	Ω	100 to 1000	(1)
R_{VC3}	100	Ω	100 to 1000	(1)
R_{VC4}	100	Ω	100 to 1000	(1)
R_{VC5}	100	Ω	100 to 1000	(1)
R_{SDA}	3.3	kΩ	3.3 or more	
R_{SCL}	3.3	kΩ	3.3 or more	
R_{ALT}	1	MΩ	1 or more	
R_{SENS}	1	mΩ	0.5 or more	(2)
R_{RSN}	1	kΩ	0.1 to 10	
R_{RSP}	1	kΩ	0.1 to 10	(3)
C_{BAT}	4.7	µF	1.0 or more	
C_{VC1}	0.47	µF	0.1 or more	
C_{VC2}	0.47	µF	0.1 or more	
C_{VC3}	0.47	µF	0.1 or more	
C_{VC4}	0.47	µF	0.1 or more	
C_{VC5}	0.47	µF	0.1 or more	
C_{VR}	1	µF	1.0 to 4.7	
C_{REF}	0.1	µF	0.1 to 1	
C_{CEL}	0.1	µF	0.1 to 1	
C_{IO}	0.1	µF	0.1 to 1	
C_{RSN}	0.1	µF		
C_{RSP}	0.1	µF		(3)

(1) This value affects internal FET current

(2) R_{SENS} affects the range and resolution of current monitoring. For detailed information, see tables in Current Monitoring section of *THEORY OF OPERATION* chapter.

(3) This value affects short detector delay time and wake-up detector delay time.

REGISTER DESCRIPTION

Address Map

The table below shows the register address map. The data width of each internal register is eight bits, and data is accessed one byte at a time.

Address Map of Internal Registers

Address (hex)	Settings	R/W	Remarks
00	Operation Mode Selection	R/W	
01	Cell Selection	R/W	
02	Built-in FET Control	R/W	
03	Current Monitoring, Short-Circuit Operation Settings	R/W	
04	Event Storage Register	R/W	
05	Wakeup Settings	R/W	
06	Short-Circuit Detection Settings	R/W	
07	External Output VREF Offset Correction Value	R	
08	Voltage Monitoring Offset Correction Value	R	
09	Voltage Monitoring Gain Correction Value	R	

Details of Register Map

Note: A hyphen (-) indicates an unused bit. It is not possible to write to register bits that are not used. Reading these register bits results in a “0” value.

Operation Mode Selection Register (Read/Write)

This register is used to set the operation mode.

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
00	STB	-	STB [6:0]						
Initial Value		0	0	0	0	0	0	0	0

1. STB [6:0]

Setting a bit to “1” stops the corresponding internal circuit.

The correspondence between each bit and its internal circuit is as follows:

STB [0] (= D0) ····· Stops the cell voltage monitoring amplifier.

STB [1] (= D1) ····· Stops the current monitoring amplifier.

STB [2] (= D2) ····· Stops the external reference voltage output.(1)

STB [3] (= D3) ····· Stops the thermal shutdown function.

STB [4] (= D4) ····· Stops the short-circuit detection circuit.

STB [5] (= D5) ····· Stops the wakeup function.

STB [6] (= D6) ····· Moves to the standby mode.

(1) Stopping the external reference voltage output automatically stops the current monitoring amplifier.

Cell Selection Register (Read/Write)

This register selects a monitoring cell.

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
01	SEL	-	-	-	-	-	SEL [2:0]		
Initial Value		0	0	0	0	0	0	0	0

SEL [2:0]

Entering the values shown in the table below in the register decodes the values internally and multiplies each cell voltage by the gain before output from the VCELL pin. If the voltage monitoring amplifier has been stopped by setting the operation mode, no cell voltage will be output even though values have been entered in register SEL [x].

Combination of Cell Selection and SEL Register Input

D2	D1	D0	VCELL
0	0	0	Pull-Down
0	0	1	Cell 1 Voltage Monitoring
0	1	0	Cell 2 Voltage Monitoring
0	1	1	Cell 3 Voltage Monitoring
1	0	0	Cell 4 Voltage Monitoring
1	0	1	Cell 5 Voltage Monitoring
1	1	0	Pull-Down
1	1	1	Pull-Down

Built-in FET Switch Control Register (Read/Write)

This register selects the cell whose built-in FET is to be turned on.

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
02	CB	-	-	-	CB [4:0]				
Initial Value		0	0	0	0	0	0	0	0

The built-in FET is turned on by writing a “1” to the bit corresponding to the cell whose built-in FET is to be turned on. The correspondence of bit and cell is as follows:

CB [0] (= D0): Turns on the built-in FET switch for the first cell.

CB [1] (= D1): Turns on the built-in FET switch for the second cell.

CB [2] (= D2): Turns on the built-in FET switch for the third cell.

CB [3] (= D3): Turns on the built-in FET switch for the fourth cell.

CB [4] (= D4): Turns on the built-in FET switch for the fifth cell.

Built-in FETs must be controlled so that two adjacent FETs do not turn on simultaneously. When two adjacent FETs turn on, the status before writing is maintained.

Current Monitoring Settings Register (Read/Write)

This register sets up current monitoring.

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
03	RS	-	-	-	-	-	-	RS [1:0]	
Initial Value		0	0	0	0	0	0	0	0

RS [0] (= D0): Conversion from a VSS-RSP voltage when this bit is “0”.
Conversion from a VSS-RSN voltage when this bit is “1”.
RS [1] (= D1): Output gain is Low(1) when this bit is “0”.
Output gain is High(1) when this bit is “1”.

Event Storage Register (Read/Write)

This register stores events detected by the R5601T.

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
04	EVT	-	-	-	-	EV [3:0]			
Initial Value		0	0	0	0	0	0	0	0

The correspondence of bit and event is as follows:
EVT [0] (= D0): Detected a short-circuit.
EVT [1] (= D1): Detected a momentary voltage drop.
EVT [2] (= D2): Detected a wakeup.
EVT [3] (= D3): Detected an error in the IC.

When at least one of the above-mentioned registers becomes “1”, the output of ALT pin becomes "Low".
To return the ALT pin’s output from "Low" to "Hi-Z", write “0” to all EVT registers while R5601T is not detecting an event.

(1) The value is different by the product code option.

Wakeup Settings Register (Read/Write)

This register sets the voltage and the delay time of RSP that detects wakeup.

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
05	WU	-	WUD [4:0]					WUV [1:0]	
Initial Value		0	0	0	0	0	0	0	0

Entering the values shown in the following table in the register decodes the values internally and sets the corresponding detection thresholds.

Setting	WUV [1] D1	WUV [2] D0	Detector Threshold (mV)
1	**0**	**0**	10
2	**0**	**1**	20
3	**1**	**0**	40
4	**1**	**1**	80

Entering the values shown in the following table in the register decodes the values internally and sets the corresponding delay times at wakeup detection.

Setting	WUD [4] D6	WUD [3] D5	WUD [2] D4	WUD [1] D3	WUD [0] D2	Delay Time (ms)
1	0	0	0	0	0	2
2	0	0	0	0	**1**	4
3	0	0	0	**1**	0	8
4	0	0	**1**	0	0	16
5	0	**1**	0	0	0	32
6	**1**	0	0	0	0	64

Any operations are not guaranteed other than the settings shown in the table above.

Short-circuit Detection Settings Register (Read/Write)

The short-circuit detection voltage and the delay time are set to this register.

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
06	SC	SCD [3:0]				SCV [3:0]			
Initial Value		0	0	0	0	0	0	0	0

The short-circuit detector threshold is set as shown in the next table according to the registers SCV [3:0]. Any operations are not guaranteed other than the settings showing in the next table.

Setting	SCV [3] D3	SCV [2] D2	SCV [1] D1	SCV [0] D0	Short-Circuit Detector Threshold (V)
1	0	0	0	0	0.400
2	0	0	0	**1**	0.200
3	0	**1**	0	**1**	0.150
4	0	0	**1**	**1**	0.100

The short-circuit detector output delay time is set as shown in the next table according to the registers SCD [3:0]. If "1" is set to two or more registers, the shorter delay time is set.

Setting	SCD [3] D7	SCD [2] D6	SCD [1] D5	SCD [0] D4	Short-Circuit Detect Output Delay Time (µs)
1	0	0	0	0	50
2	0	0	0	**1**	100
3	0	0	**1**	0	200
4	0	**1**	0	0	400
5	**1**	0	0	0	800

Offset Correction Value for External Output VREF Register (Read)

This register stores the offset correction value for the R5601T external output VREF.

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
07	RF	RF [7]	RF [6:0]						
Initial Value		Correction Value of Individual IC							

RF [0 to 6] (= D0 to D6): Expresses the absolute value of a VREF offset as 0 to 12.7 mV in 0.1 mV increments.
RF [7] (= D7): Expresses the sign of a VREF offset. “0” indicates plus, and “1” indicates minus.
For example, in our test environment, if the output is 2.9980 V when the external output VREF is set to 3.0000 V, −2.0 mV is stored in this register.

Correction Value for Cell Voltage Monitoring Offset Register (Read)

This register stores the offset correction value of the Cell voltage monitoring.

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
08	VOS	VOS [7]	VOS [6:0]						
Initial Value		Correction Value of Individual IC							

VOS [0 to 6] (= D0 to 6): Reflects the absolute value of the correction value for cell voltage monitoring offset as 0 to 127.
VOS [7] (= D7): Reflects the plus or minus sign of the cell voltage monitoring offset. ”0”: plus, “1”: minus.

Correction Value for Cell Voltage Monitoring Gain Register (Read)

This register stores the gain correction value of the Cell voltage monitoring.

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
09	VCG	VCG [7]	VCG [6:0]						
Initial Value		Correction Value of Individual IC							

VCG [0 to 6] (= D0 to 6): Reflects the absolute value of the correction value for cell voltage monitoring gain as 0 to 127.
VCG [7] (= D7): Reflects the plus or minus sign of the gain correction value for cell voltage monitoring. “0”: plus, “1”: minus.

Ver. B

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

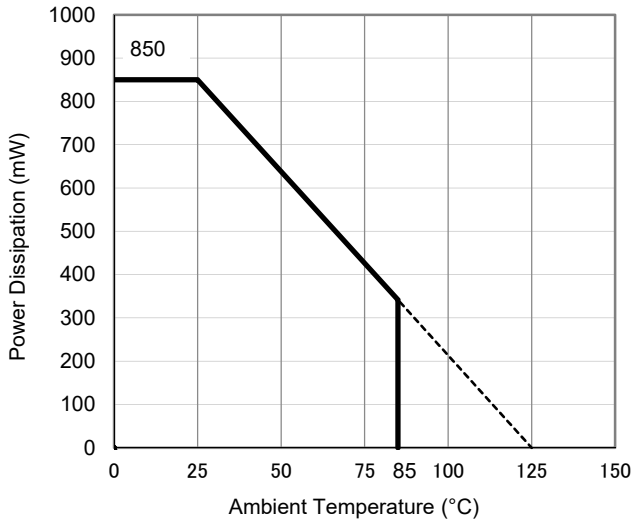
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 1.6 mm
Copper Ratio	Outer Layers (First and Fourth Layers): Approx. 10%, 60 mm square Inner Layers (Second and Third Layers): Approx. 100%, 74.2 mm square
Through-holes	ϕ 0.85 mm × 44 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

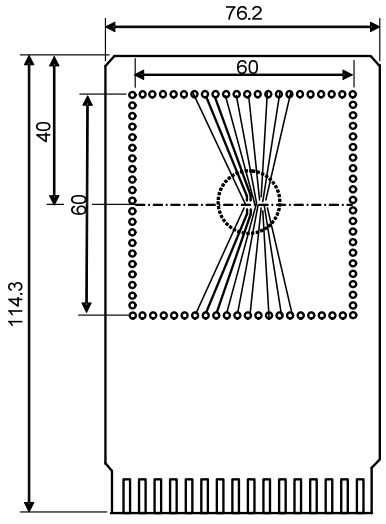
Item	Measurement Result
Power Dissipation	850 mW
Thermal Resistance (θja)	θja = 118 °C/W
Thermal Characterization Parameter (ψjt)	ψjt = 35 °C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter

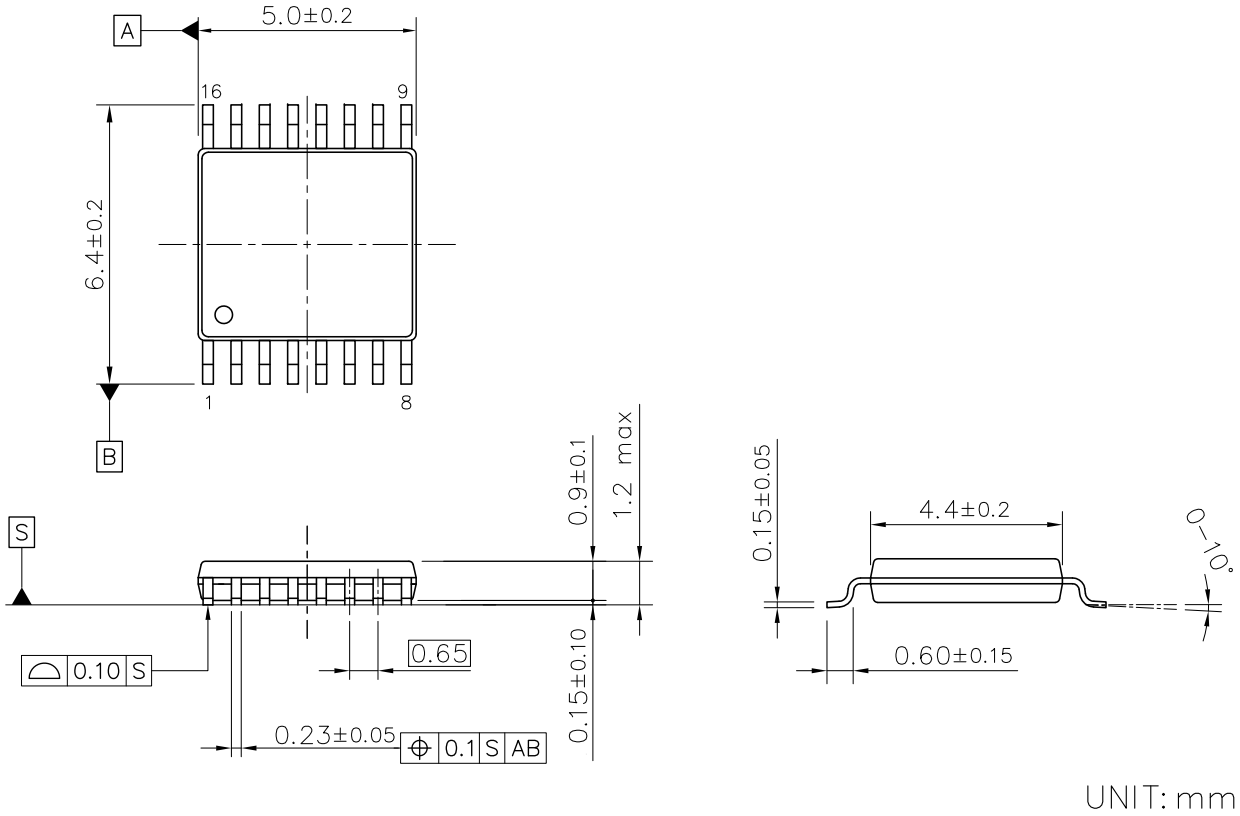


Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

RICOH



TSSOP-16 Package Dimensions

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