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WM8782-EV1M

Evaluation Board User Handbook

Rev 1.1

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INTRODUCTION

The WM8782 is a high performance, low cost stereo audio ADC designed for recordable media applications.

This evaluation platform and documentation should be used in conjunction with the latest version of the WM8782 datasheet. The datasheet gives device functionality information as well as timing and data format requirements.

This evaluation platform has been designed to allow the user ease of use and give optimum performance in device measurement.

GETTING STARTED

EVALUATION BOARD CHECKLIST

The following items are available from Wolfson:

- WM8782-EV1B Evaluation Board - 6125_SSOP20_EV1_REV1
- WM8782-EV1M User Handbook (download from <http://www.wolfsonmicro.com>)

CUSTOMER REQUIREMENTS

Minimum customer requirements are:

- D.C. Power supply of +5V
- D.C. Power supply of +2.7V to +3.6V

Minimum signal path requirements are:

- An analogue input source
- S/PDIF receiving unit
- An MCLK source

PCB MAIN CONNECTIONS

POWER SUPPLIES

Using appropriate power leads with 4mm connectors, supplies should be connected as described in Table 1 Power Supply Connections.

REF-DES	SOCKET NAME	SUPPLY
J4	AVDD	+2.7V to +5.5V
J3	DVDD	+2.7V to +3.6V
J1	+5V	+5V
J2	GND	0V
J5	GND	0V

Table 1 Power Supply Connections

Notes:

- J2 and J5 GND connections should be connected to a common GND on the supply.
- Refer to WM8782 datasheet for current limitations on individual supply voltages.

Important: Exceeding the recommended maximum voltage can damage EVB components. Under voltage may cause improper operation of some or all of the EVB components.

DIGITAL INPUT

There are two possible methods to input the required digital signal clocks (MCLK, BCLK and LRCLK) to the WM8782 evaluation board. An AES/EBU, UEC958, S/PDIF, EIAJ CP340/1201 signal from coaxial input via a standard phono connector (J8) or direct digital input is available via one side of a 2x6 pin header (H1).

A level shift IC (U5) has been included in the digital input interface path to provide signal buffering to the input signals; this allows an external clock source to be matched to the WM8782 requirements.

The WM8782 must always have an MCLK input for operation, which can be derived either from S/PDIF signal clock recovery or from an external MCLK source via a SMB connector (J12). Both sources can be used by the onboard multi-rate clock generator (U4) to produce suitable BCLK and LRC clocks.

If the WM8782 is configured for Master mode, only an MCLK source is required.

CONNECTOR REFERENCE	CONNECTOR TYPE	SIGNAL REFERENCE
J8	Phono Connector	SPDIF_IN
J12	SMB Connector	MCLK

Table 2 Digital Input connections

DIGITAL OUTPUT

The ADC output can be converted to an S/PDIF signal via the CS8427CS device (U3) and output from the WM8782 evaluation board via a standard phono connector (J6). Alternatively the ADC output data and clocks may be accessed via one side of a 2x6 pin header (H2).

A level shift IC (U5) has been included in the digital output interface path to provide signal buffering to the output signals; this allows external receiver requirements to be met.

CONNECTOR REFERENCE	CONNECTOR TYPE	SIGNAL REFERENCE
J6	Phono Connector	SPDIF_OUT

Table 3 Digital Output Connections

ANALOGUE INPUT

There are 2 analogue inputs via standard phono connectors; AINL (J9) and AINR (J10).

CONNECTOR REFERENCE	CONNECTOR TYPE	SIGNAL REFERENCE
J9	Phono Connector	AINL
J10	Phono Connector	AINR

Table 4 Analogue Input Connections

Analogue input is also possible via two test points (TP5) and (TP6).

The default configuration for the analogue inputs is for two single ended connections, AINL and AINR connectors referenced to ground. It is possible to configure the input stage of the WM8782 for pseudo-differential operation. This mode of operation will allow common noise on the input signal and common signal to be eliminated. Configuration for this mode is considered later in the user manual.

The input configuration of the WM8782 also allows the op-amp to be configured for different gains. The default of the evaluation board is for unity gain. By changing the input resistors (R9) and (R17) or the feedback resistors (R11) and (R22) the gain of the input can be controlled to suit the level of input signal. For example if the input signal is 2V_{rms} (Max input to WM8782 is 1V_{rms}) then R11 and R22 can be populated with 5K resistors to set the input gain to be 0.5.

All WM8782 device pins are accessible for easy measurement via the 10-pin headers (H3 and H4) running up the left and right sides of the device.

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INTERFACES

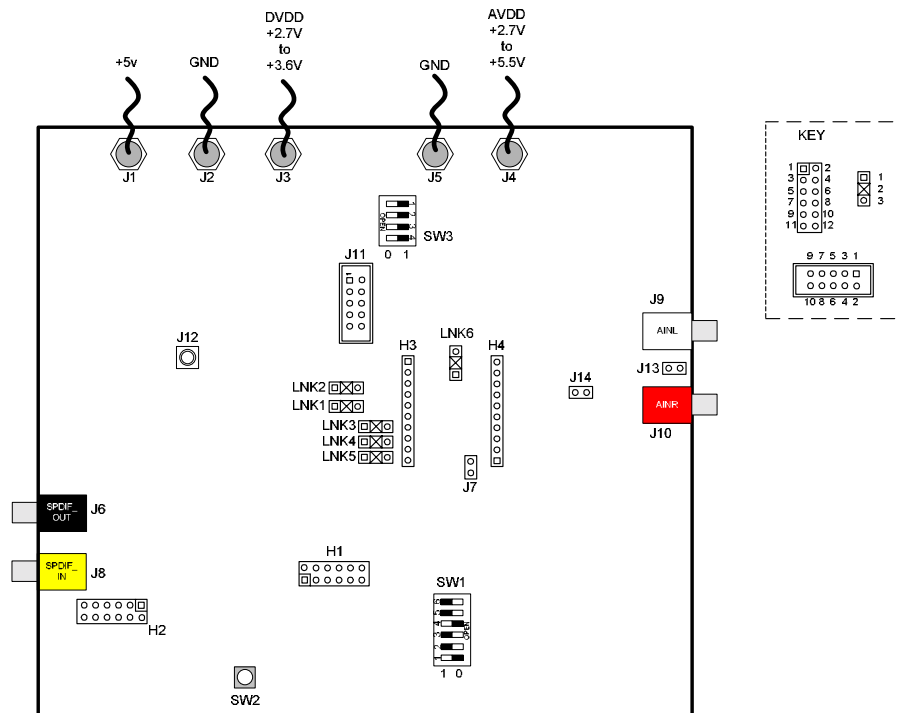


Figure 1 Interfaces

HEADERS

H3	WM8782	PIN NAME
1	1	MCLK
2	2	DOUT
3	3	LRCLK
4	4	DGND
5	5	DVDD
6	6	BCLK
7	7	IWL
8	8	FSAMPEN
9	9	FORMAT
10	10	VMID

Table 5 Headers

J12	WM8782	PIN NAME
1	11	VREFGND
2	12	VREFP
3	13	AVDD
4	14	AGND
5	15	AINOPR
6	16	AINR
7	17	COM
8	18	AINOPL
9	19	AINL
10	20	M/S

LINKS AND JUMPERS

LINKS AND JUMPERS	LINK STATUS	DESCRIPTION
LNK1 BCLK Config	1 and 2 SHORT 2 and 3 SHORT CENTRE	Slave Mode, BCLK From H1 [default setting] Slave Mode, BCLK From Multi BCLK (U4) Master Mode, BCLK from WM8782 (U7)
LNK2 LRCLK Config	1 and 2 SHORT 2 and 3 SHORT CENTRE	Slave Mode, LRCLK From H1 [default setting] Slave Mode, LRCLK From Multi LRCLK (U4) Master Mode, LRCLK from WM8782 (U7)
LNK3 Word Length	1 and 2 SHORT 2 and 3 SHORT CENTRE	20 bit 16 bit 24 bit [default setting]
LNK4 Fast Sampling Rate Enable	1 and 2 SHORT 2 and 3 SHORT CENTRE	96ken (64x OSR) 48ken (128x OSR) [default setting] 192ken (32x OSR)
LNK5 Audio Mode Select	1 and 2 SHORT 2 and 3 SHORT CENTRE	Left Justified Right Justified I2S [default setting]
LNK6 Master/Slave Selection	1 and 2 SHORT 2 and 3 SHORT CENTRE	Master Mode Slave Mode [default setting] No operation
J7	SHORT OPEN	COM to VMID 5K [default setting] COM to VMID 10K
J13	SHORT OPEN	Analogue inputs referenced to GND [default setting] Analogue inputs referenced to COM input
J14	SHORT OPEN	Connect COM to analogue input reference. Disconnect COM to analogue input reference [default setting]

Table 6 Links and Jumpers

SWITCHES

SWITCH	SWITCH POSITION	DESCRIPTION
SW1	<u>6</u> <u>5</u> <u>4</u> <u>3</u> <u>2</u> <u>1</u>	CS8427 format configuration
	0 0 1 0 0 1	I2S Compatible [default setting]
	0 0 0 0 0 1	Left Justified
	1 0 0 0 0 1	Right Justified
SW3	<u>4</u> <u>3</u> <u>2</u> <u>1</u>	Multi-rate conversion MCLK selection
	1 0 0 0	256fs [default setting]
	0 1 0 0	384fs
	0 0 1 0	512fs
SW2	0 0 0 1	768fs
		The CS8427 may be RESET by pressing and releasing switch SW2. This is required if the switches on SW1 are changed after the board is powered up.

Table 7 Switches

WM8782 BLOCK DIAGRAM

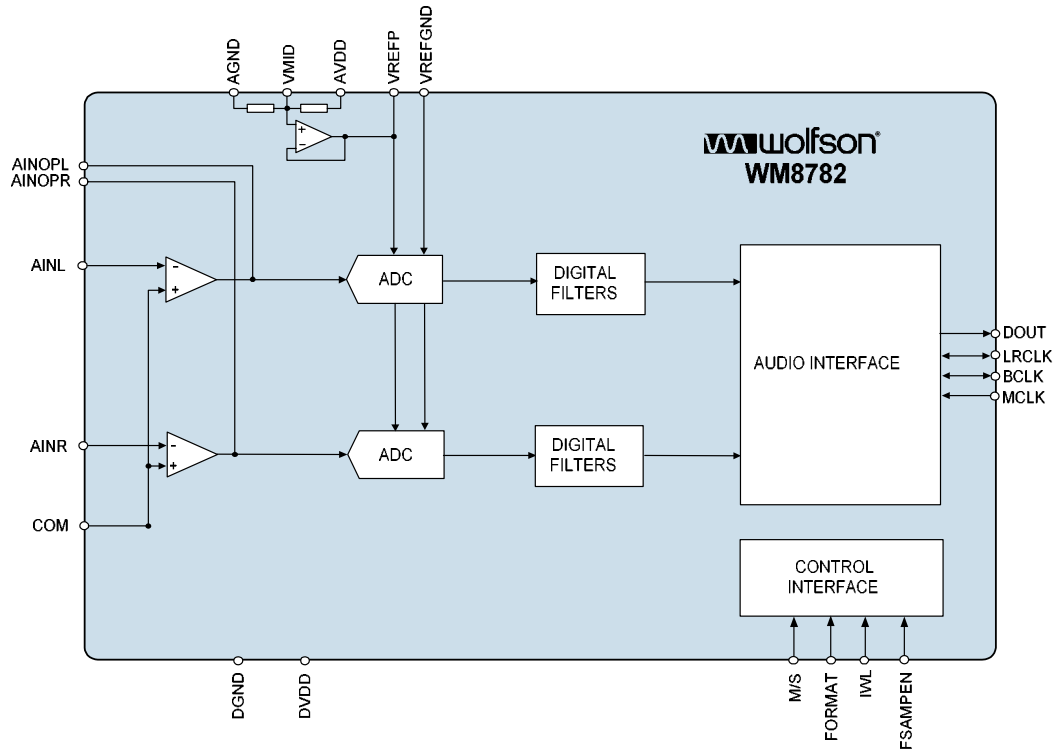


Figure 2 WM8782 Block Diagram

HARDWARE CONFIGURATIONS

DEFAULT CONFIGURATION

Functionality of the WM8782 is achieved through a hardware control interface; the evaluation board is fitted with 3 position switches to exercise the full control capability. The device can be configured as either master or slave using LNK6 (an MCLK clock must be supplied to the WM8782 in both configurations either through the SPDIF interface, header H1 or J12).

The default configuration is detailed in Figure 3. This configuration allows the connection of a stereo analogue signal to AINL/R. The MCLK source is applied via the SPDIF input J8, the digital output signal can then be taken from the SPDIF_OUT output J6.

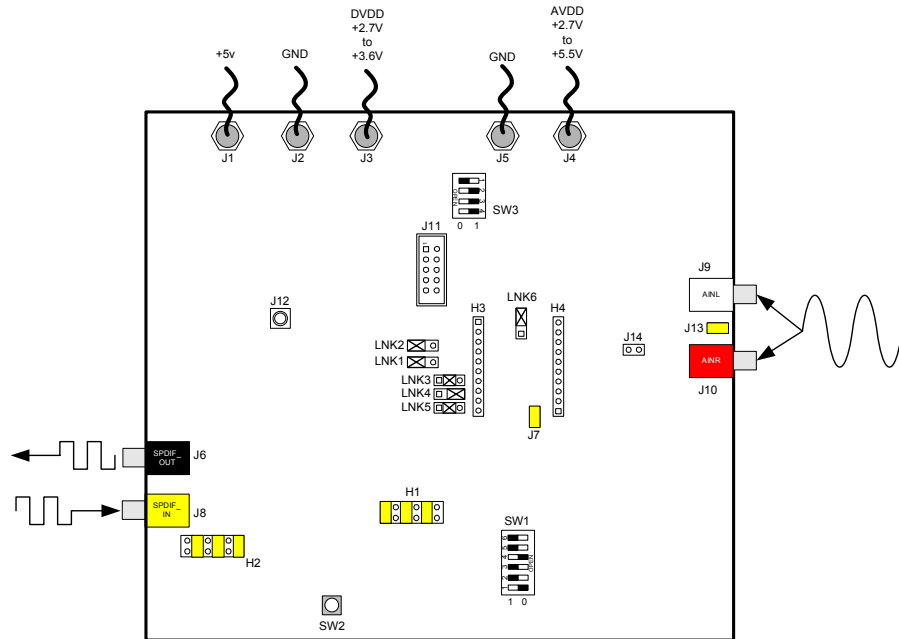


Figure 3 Default EVB Configuration

LINKS, JUMPERS AND SWITCHES	POSITION	DESCRIPTION												
H1	SHORT 1-2, 5-6 and 9-10	CS8427 supplies I2S interface clocks												
H2	SHORT 1-2, 5-6 and 9-10	CS8427 clock input												
SW1	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td> </tr> <tr> <td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td> </tr> </table>	6	5	4	3	2	1	0	0	1	0	0	1	Data Format I2S Compatible
6	5	4	3	2	1									
0	0	1	0	0	1									
SW3	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td>4</td><td>3</td><td>2</td><td>1</td> </tr> <tr> <td>1</td><td>0</td><td>0</td><td>0</td> </tr> </table>	4	3	2	1	1	0	0	0	MCLK rate 256fs Output not used with this EVB configuration				
4	3	2	1											
1	0	0	0											
SW2		Press once if SW1 settings changed.												
LNK1	SHORT 1-2	H1 I2S Interface BCLK												
LNK2	SHORT 1-2	H1 I2S Interface LRCLK												
LNK3	CENTRE	24 Bit data												
LNK4	SHORT 2-3	48K sample rate												
LNK5	CENTRE	I2S format												
LNK6	SHORT 2-3	Slave mode												
J7	SHORT	COM to VMID 5K												
J13	SHORT	Analogue input referenced to GND												
J14	OPEN	COM pin to analogue input open												

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MASTER MODE

Detailed in Figure 4 is an example of the WM8782 configured for Master mode and an external MCLK applied via J12. In this example an external clock source is used to supply the WM8782 MCLK, from which, the BCLK and LRCLK clocks are produced by the WM8782 device and then input to the CS8427 via H2.

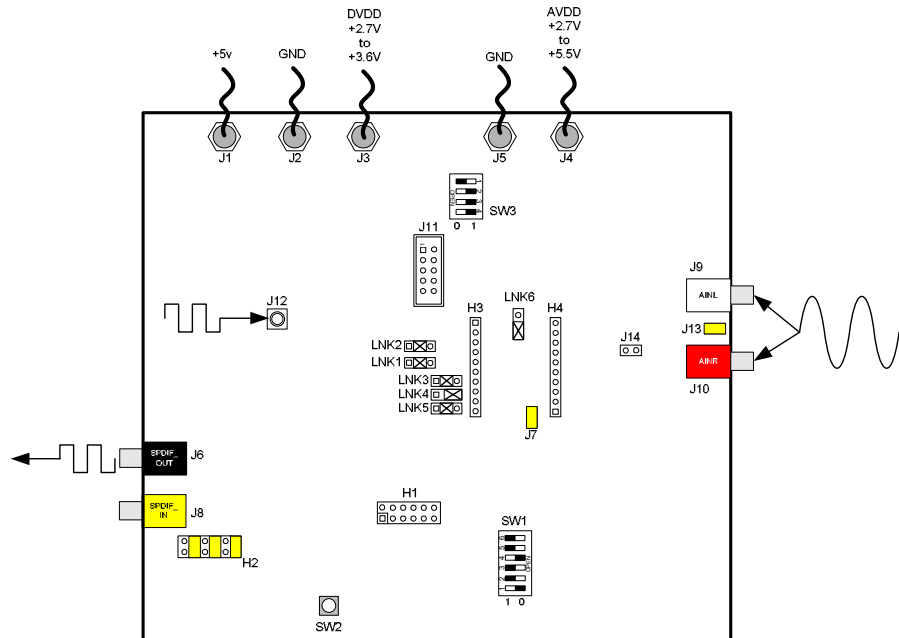


Figure 4 Master Mode Setup Example

LINKS AND JUMPERS	SWITCH POSITION	DESCRIPTION
H1	All Links OFF	CS8427 clock input not used
H2	SHORT 1-2, 5-6 and 9-10	CS8427 clock input from WM8782
SW1	6 5 4 3 2 1 0 0 1 0 0 1	Data Format I2S Compatible
SW3	4 3 2 1 1 0 0 0	MCLK rate 256fs Output not used with this EVB config.
SW2		Press once if SW1 settings changed.
LNK1	CENTRE	I2S Interface BCLK from WM8782
LNK2	CENTRE	I2S Interface LRCLK from WM8782
LNK3	CENTRE	24 Bit data
LNK4	SHORT 2-3	48K sample rate
LNK5	CENTRE	I2S format
LNK6	SHORT 1-2	Master mode
J7	SHORT	COM to VMID 5K
J13	SHORT	Analogue input referenced to GND
J14	OPEN	COM pin to analogue input open

Table 8 External MCLK, WM8782 Master Mode Example Settings

USING AN EXTERNAL MCLK AND ONBOARD MULTI-RATE CLOCK GENERATOR

Detailed in Figure 5 is the setup required if using an external MCLK in slave mode. In this example an external clock source is used to supply the WM8782 MCLK and to provide the multi-rate generator clock, from which, the BCLK and LRCLK clocks are produced. The digital output is taken from the SPDIF_OUT.

Note: The multi rate clock generator can also be used if the MCLK source is supplied via H1, either from the SPDIF input or a direct connection to H1.

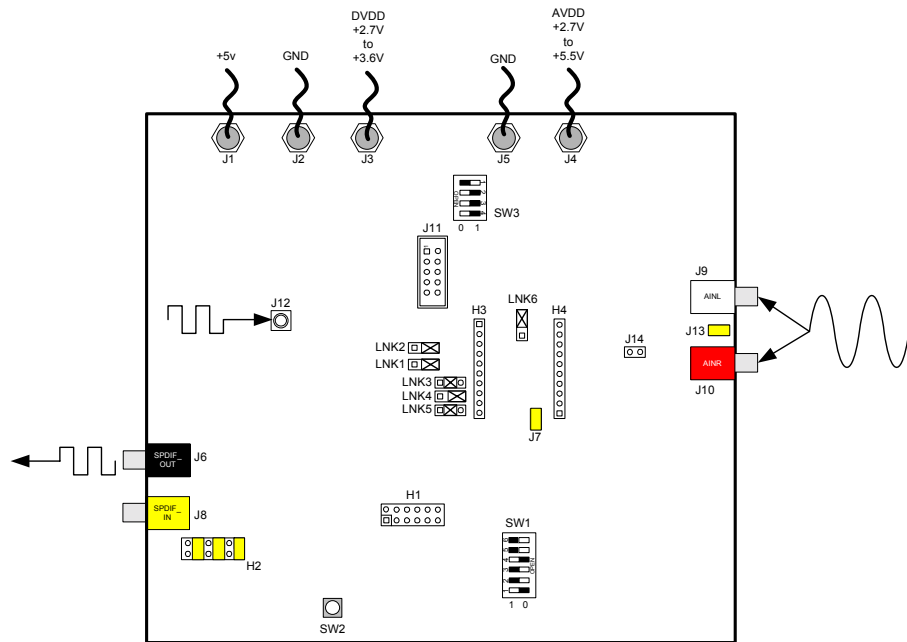
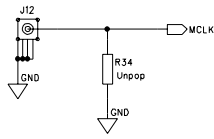


Figure 5 Using the Multi-rate Clock Generator Example

LINKS AND JUMPERS	SWITCH POSITION	DESCRIPTION
H1	All Links OFF	CS8427 clock input not used
H2	SHORT 1-2, 5-6 and 9-10	CS8427 clock input from Multi-rate gen.
SW1	6 5 4 3 2 1 0 0 1 0 0 1	Data Format I2S Compatible
SW3	4 3 2 1 1 0 0 0	MCLK rate 256fs
SW2		Press once if SW1 settings changed.
LNK1	SHORT 2-3	I2S Interface BCLK from Multi-rate
LNK2	SHORT 2-3	I2S Interface LRCLK from Multi-rate
LNK3	CENTRE	24 Bit data
LNK4	SHORT 2-3	48K sample rate
LNK5	CENTRE	I2S format
LNK6	SHORT 2-3	Slave mode
J7	SHORT	COM to VMID 5K
J13	SHORT	Analogue input referenced to GND
J14	OPEN	COM pin to analogue input open

Table 9 Using the Multi-rate Clock Generator Example



De-coupling for Level Shift U5

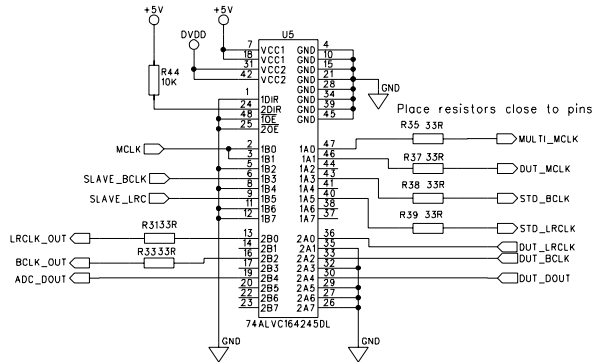
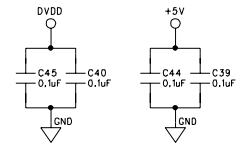


Figure 8 Clock Signals Buffer

WM8782-EV1M

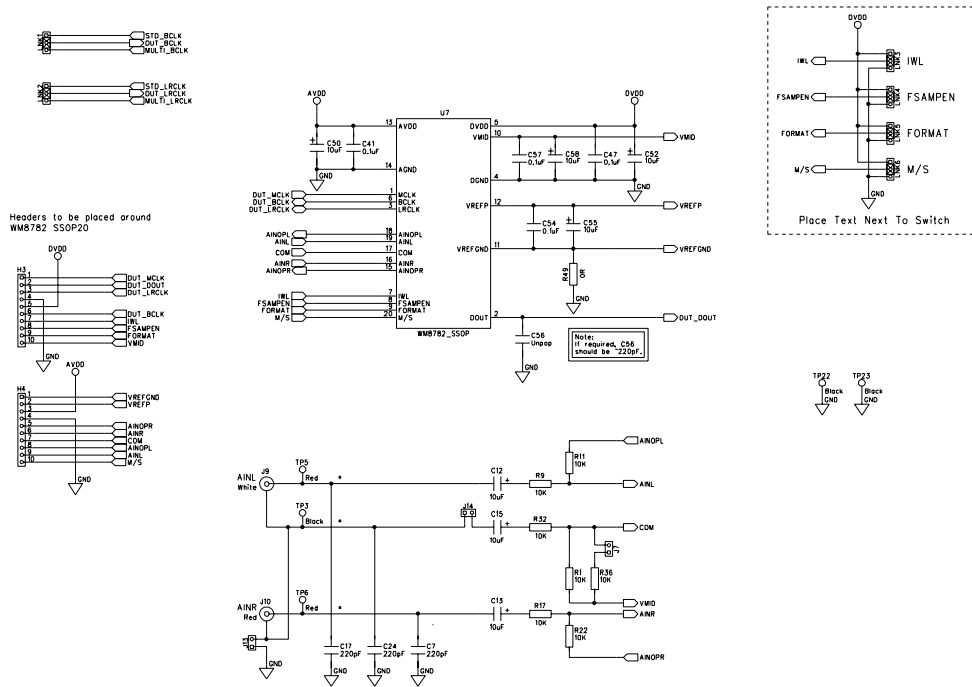


Figure 9 WM8782

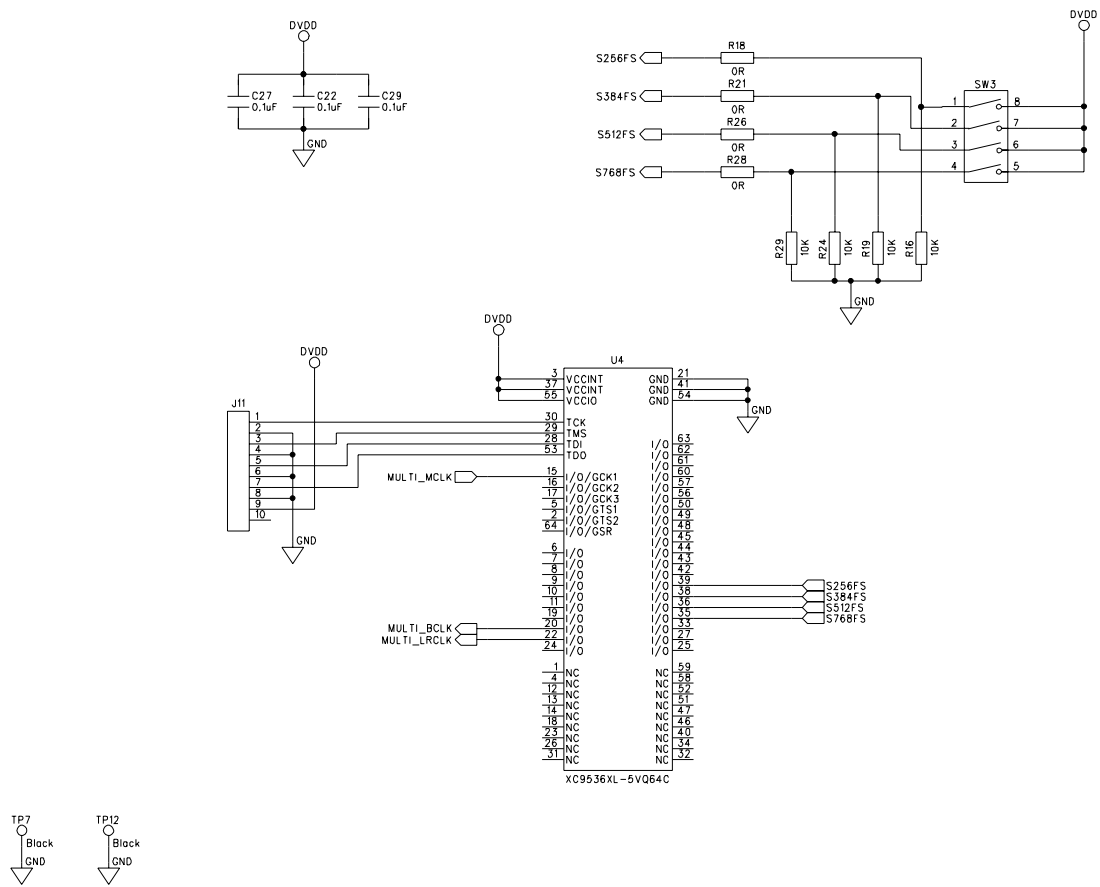


Figure 10 Multi-rate Clock Generator

WM8782-EV1M

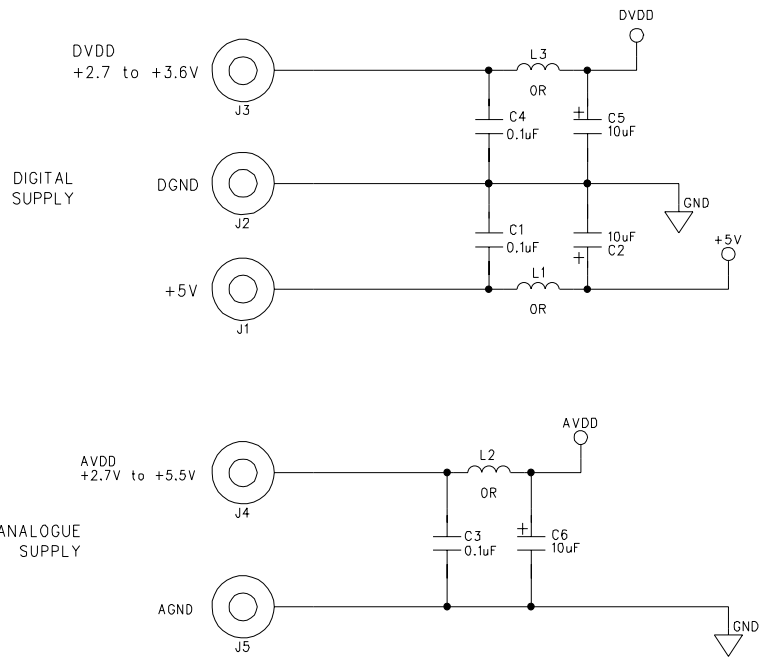
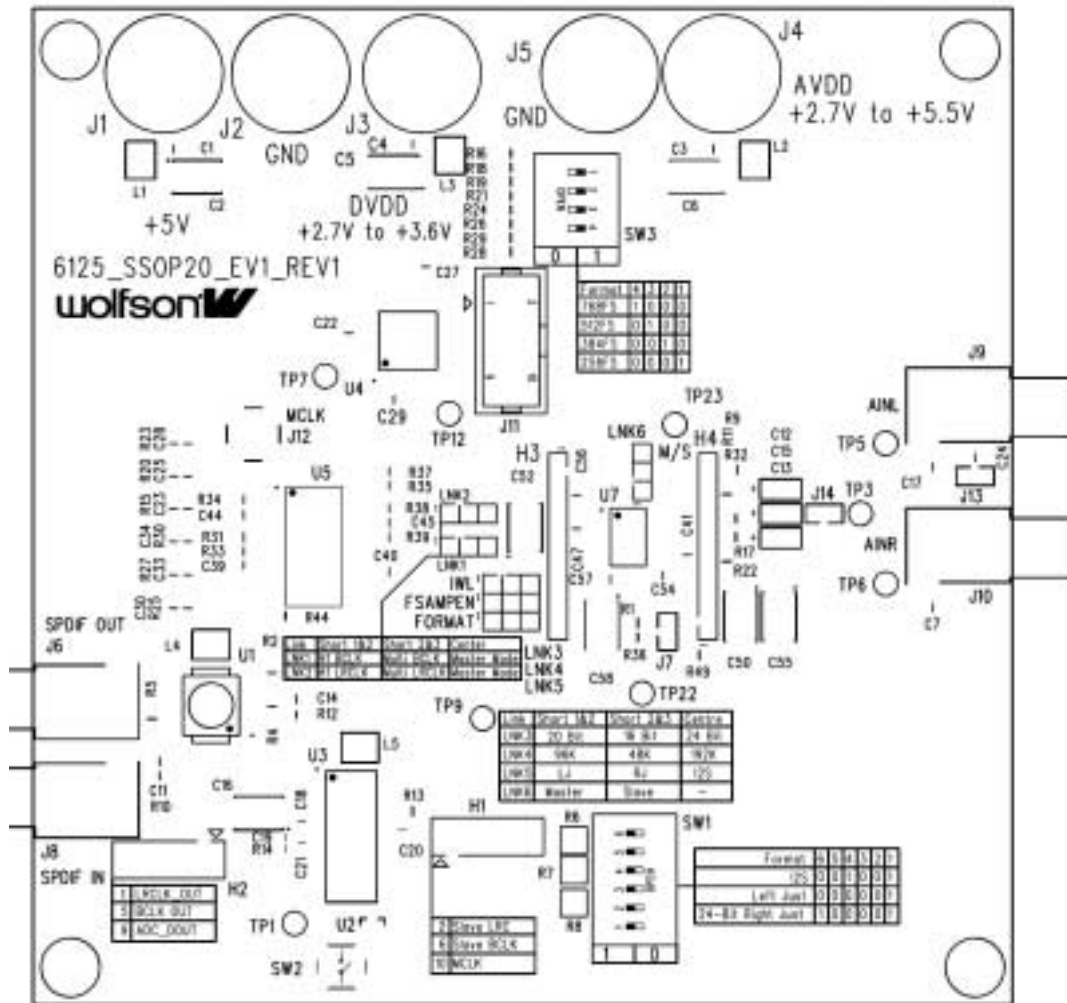


Figure 11 Power Supplies

PCB LAYOUT



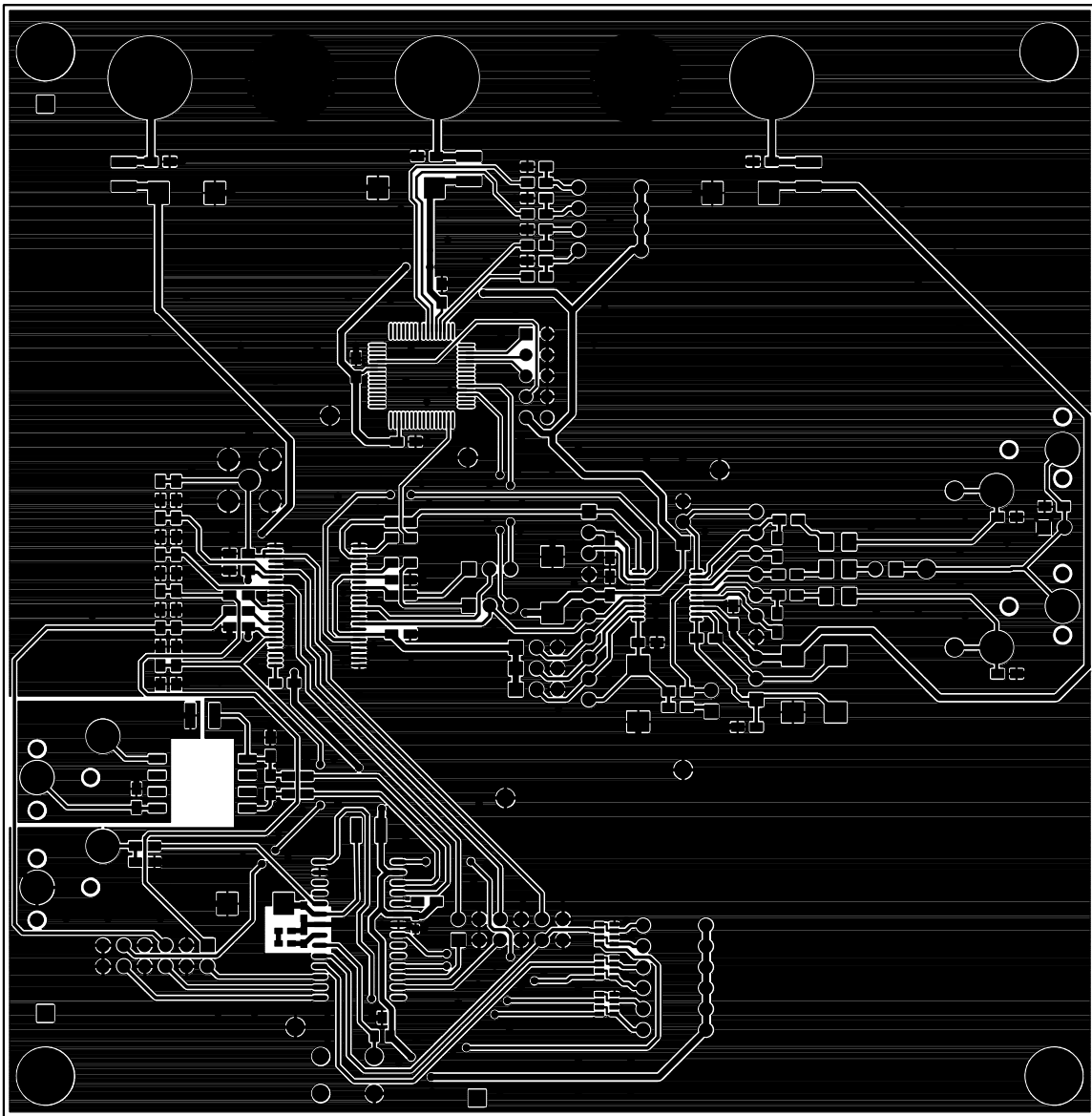


Figure 13 Top Layer

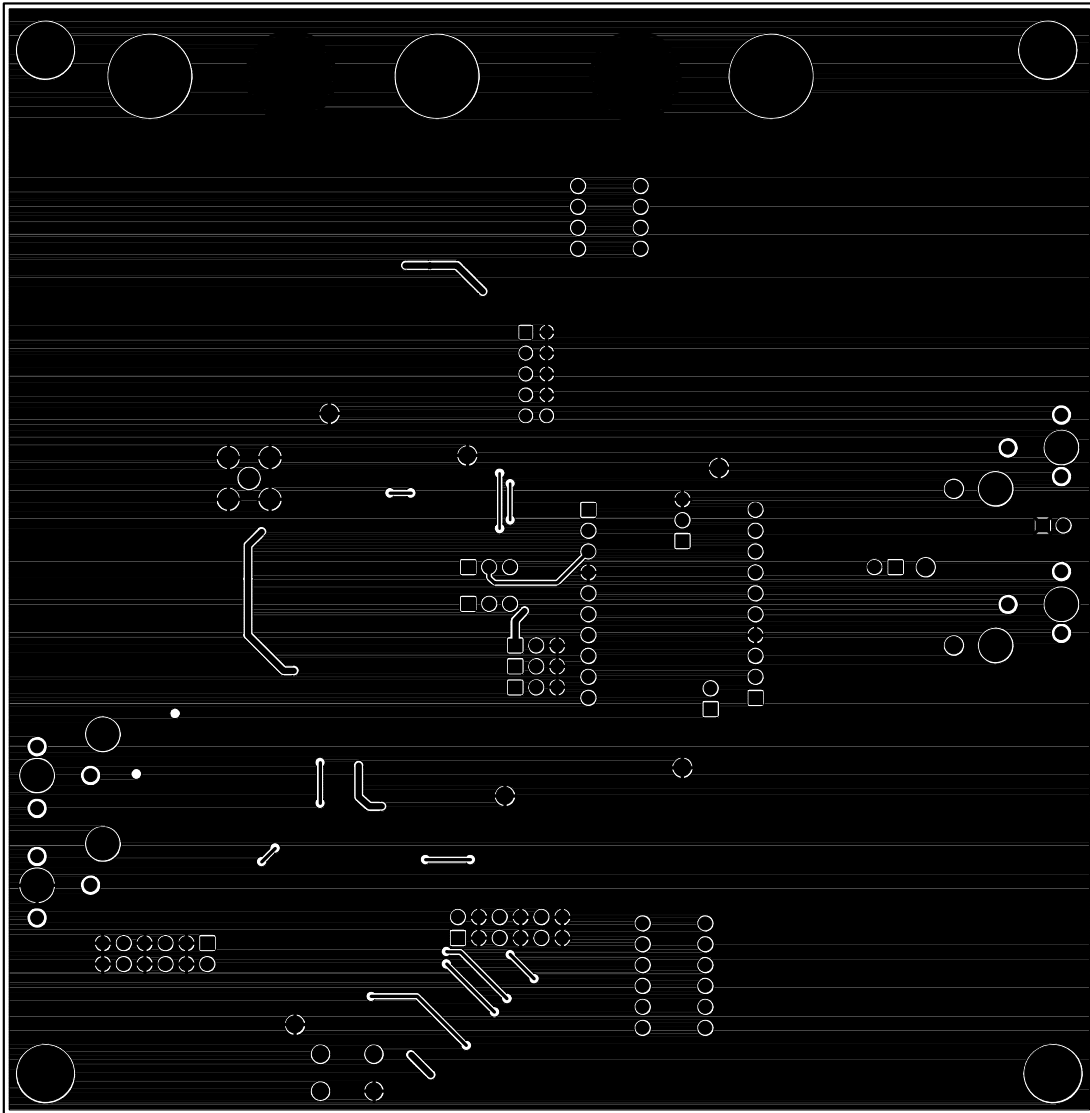


Figure 14 Bottom Layer

WM8782-EV1M

WM8782-EV1B BILL OF MATERIAL

DESCRIPTION	REFERENCE	QTY
SMB Connector PCB Mount 50 Ohm VERTICAL	J12	1
Phono Socket PCB mount RED	J10	1
Phono Socket PCB mount YELLOW	J8	1
Phono Socket PCB mount WHITE	J9	1
74ALVC164245 16 Bit Dual Supply Bus Transceiver SSO	U5	1
4.7nF 0603 SMD Ceramic Capacitor 50V X7R	C21	1
DIL Switch 4-Way Rocker	SW3	1
DIL Switch 6-Way Rocker	SW1	1
Phono Socket PCB mount BLACK	J6	1
B3F1000 SPNO PCB mount switch	SW2	1
47k 1206 SMD chip 4 resistor array 5% 0.063W	R6, R7, R8	3
1.32mm PCB Test Terminal BLACK	TP1, TP3, TP7, TP9, TP12, TP22, TP23	7
1.32mm PCB Test Terminal RED	TP5, TP6	2
220pF 0805 SMD Ceramic Capacitor 50V X7R	C7, C17, C24	3
0.01uF 0805 SMD Ceramic Capacitor 50V X7R	C11	1
0.1uF 0805 SMD Ceramic Capacitor 50V X7R	C1, C3, C4, C14, C22, C27, C29, C39, C40, C41, C44, C45, C47, C54, C57	15
2x5 2.54mm Male PCB Header LoPro VERTICAL	J11	1
620R 0805 SMD chip resistor 1% 0.1W	R12	1
0.1uF 0603 SMD Ceramic Capacitor 16V X7R	C18, C19, C20	3
4mm Non-Insulated Panel Socket 16A	J1, J2, J3, J4, J5	5
1x2 PCB Pin Header 0.1" VERTICAL	J7, J13, J14	3
1x10 2.54mm pitch PCB Pin Header VERTICAL	H3, H4	2
2x6 2.54mm pitch PCB Pin Header VERTICAL	H1, H2	2
3.3uH 1210 Surface Mount Inductor '1210A series'	L5	1
DS1813 5V active Low Power-On-Reset chip SOT	U2	1
0R 0805 SMD chip resistor 1% 0.1W	R5, R18, R21, R26, R28, R49	6
0R 1206 Resistor on 1210 Inductor site	L1, L2, L3	3
33R 0805 SMD chip resistor 1% 0.1W	R14, R31, R33, R35, R37, R38	6
1K2 0805 SMD chip resistor 1% 0.1W	R39	1
10K 0805 SMD chip resistor 1% 0.1W	R1, R9, R11, R16, R17, R19, R22, R24, R29, R32, R36, R44	12
100K 0805 SMD chip resistor 1% 0.1W	R13	1
XC9536XL-15 3.3V 36 macrocell CPLD	U4	1
75R 0805 SMD chip resistor 1% 0.125W	R10	1
10uF 10V SMD Tantalum Capacitor case A	C12, C13, C15	3
10uF 12.5V SMD Poly Aluminium Low ESR CD Series	C2, C5, C6, C16, C50, C52, C55, C58	8
2:1 Ratio 96KHz SPDIF Digital Audio transformer SOIC	U1	1
JSK9-16-G0 PCB 1x3 Jumper Switch 0.1" Center-off VERTICAL	LNK1, LNK2, LNK3, LNK4, LNK5, LNK6	6
CS8427 96KHz Audio Transceiver	U3	1
WM8782 24-bit 96kHz Stereo ADC	U7	1
Unpop 0805 SMD Ceramic Capacitor site	C23, C25, C28, C30, C33, C34, C56	7
Unpop 1210 Surface Mount Inductor site	L4	1
Unpopulated 0805 resistor site	R2, R4, R15, R20, R23, R25, R27, R30, R34	9

Table 10 WM8782-EV1M Bill of Materials

Note: ¹ The audio transformer used on this board is manufactured by Scientific Conversion Inc. (www.scientificconversion.com).

APPENDIX - EXTERNAL DSP CONNECTION TO THE WM8782-EV1B

The WM8782-EV1B evaluation board has been designed to allow it to be easily connected to an external DSP platform with error free operation.

The following information is provided to ease the connection process and ensure that all signals sent and received by the WM8782-EV1B are reliable and at the correct voltage levels.

AUDIO INTERFACE CONNECTIONS

It is recommended that twisted pair (signal twisted with GND) or shielded wires are used to make the audio interface connections between the DSP and WM8782-EV1B platforms. This is to ensure that no interference or noise is picked up by the clocks or data lines, thus reducing performance and reliability.

When the WM8782 is set in **Slave Mode**, the jumpers on H1 and H2 should be removed, disconnecting the digital input and output section of the WM8782 evaluation board. The DOUT data from the WM8782 should then be connected to the DSP via pin 2 of header strip H3 and the GND connection should be taken from pin 4 of header strip H3. The BCLK input clock signal to the WM8782 should be connected to the DSP via pin 6 and the LRCLK input clock should be connected via pin 3 of header strip H3. In this configuration LNK1 and LNK2 should be set to the centre position to isolate the output of the level shift IC (U5) from the DSP output clocks. The input MCLK should be connected to H1 pin 10 as detailed in Figure 16.

The DOUT signal should be taken direct from the WM8782 digital output because the output side of the level-shift IC (U5) from the WM8782 is pulled up to +5V which may overdrive and cause damage to the DSP inputs. The digital output levels of the WM8782 are Logic High (min) = $DBVDD * 0.9$; Logic Low (max) = $DBVDD * 0.1$ which should meet the input level requirements of most DSPs running at +3V supplies.

If the DSP is running with +5V supplies then the DOUT connection to it should be made from the output side of the level-shift IC (U5), connecting the signals as shown in Figure 15.

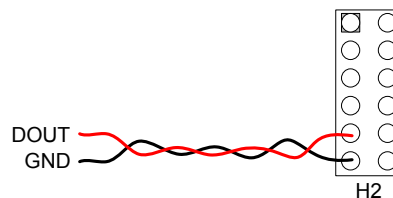


Figure 15 Data Connection to the DSP Platform (+5V tolerant input levels)

Also when the DSP is operating at +5V, the MCLK, BCLK and LRCLK input clock signals should be connected to the input side of the level-shift IC (U5) as detailed in Figure 16. For this configuration LNK1 and LNK2 should be set to short positions 1 and 2.

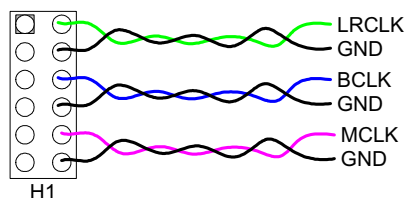


Figure 16 Clock Connection to the DSP Platform (+5V tolerant input levels)

When the WM8782 is set to **Master mode**, the jumpers on header H1 and H2 should be removed, disconnecting the digital input and output section of the evaluation board. If an external MCLK signal is being used (i.e. supplied by the DSP), then the DSP platform should be connected as shown in Figure 17. The signal should be connected to H1 and not on the header strip H3 running up the side of the device. Connecting the signal on the output side of the level-shift IC (U5) will cause drive contention between U5 and the DSP and could result in damage to either or both devices. In most cases, the DSP supplies will be set around +3V for low power portable applications. The inputs to the level-shift IC (74ALVC164245) have a TTL threshold (i.e. Logic High = +2V(min); Logic Low = +0.8V(max)) and low input current requirements (i.e. 15uA max) allowing most DSPs to connect directly.

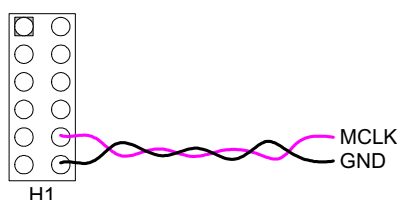


Figure 17 Timing Connections from DSP Platform

The digital inputs to the WM8782 have a CMOS threshold (i.e. Logic High (min) = $DBVDD * 0.7$; Logic Low (max) = $DBVDD * 0.3$). These are met directly by the level shift IC outputs.

Also in Master mode the jumpers on H2 should be removed, disconnecting the digital output section of the WM8782 evaluation board. The DOUT, BCLK and LRCLK signals from the WM8782 should then be connected to the DSP from headers H3 running up the side of the WM8782.

The DOUT, BCLK and LRCLK signals should be taken direct from the WM8782 digital output as the output side of the level-shift IC (U5) from the WM8782 is pulled up to +5V which may overdrive and cause damage to the DSP inputs. The digital output levels of the WM8782 are Logic High (min) = $DBVDD * 0.9$; Logic Low (max) = $DBVDD * 0.1$ which should meet the input level requirements of most DSPs running at +3V supplies.

If the DSP is running with +5V supplies (and +5V tolerant inputs) then the connections from the WM8782 evaluation board to the DSP should be made from H2 on the output side of the level-shift IC from the WM8782 as shown in Figure 18.

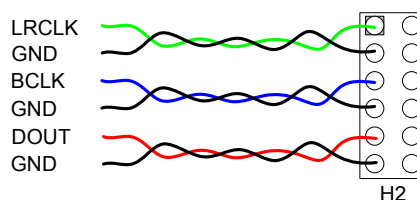


Figure 18 Connections to the DSP Platform (+5V tolerant input levels)

This will ensure that the DSP input level specifications are met.

EVALUATION SUPPORT

The aim of this evaluation kit is to help you to become familiar with the functionality and performance of the WM8782 ADC.

If you require more information or require technical support please contact Wolfson Microelectronics Applications group through the following channels:

Email: apps@wolfsonmicro.com

Telephone Apps: +44 (0)131 272 7070

Fax: +44 (0)131 272 7001

Mail: Applications Department at address on last page.

or contact your local Wolfson representative.

Additional information may be made available from time to time on our web site at:

<http://www.wolfsonmicro.com>

WM8782-EV1M

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