

## 24-bit 192kHz Stereo DAC

### DESCRIPTION

The WM8761 is a high performance stereo DAC designed for audio applications such as DVD, home theatre systems, and digital TV. The WM8761 supports data input word lengths from 16 to 24-bits and sampling rates up to 192kHz. The WM8761 consists of a serial interface port, digital interpolation filters, multi-bit sigma delta modulators and stereo DAC in a 14-pin SOIC package.

The WM8761 has a hardware control interface for selection of audio data interface format, mute and de-emphasis. The WM8761 supports I<sup>2</sup>S, right justified or DSP interfaces.

The WM8761 is an ideal device to interface to AC-3™, DTS™, and MPEG audio decoders for surround sound applications, or for use in DVD players, including supporting the implementation of 2 channels at 192kHz for high-end DVD-Audio applications.

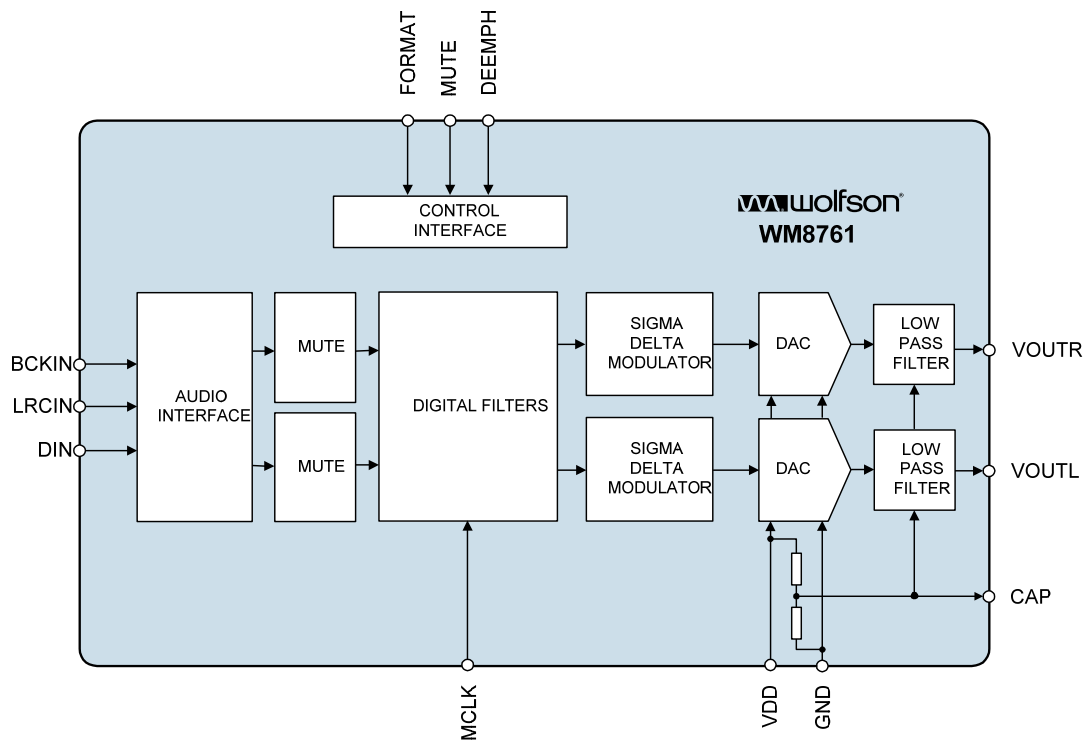
### FEATURES

- Stereo DAC
- Audio Performance
  - 100dB SNR ('A' weighted @ 48kHz)
  - -90dB THD
- DAC Sampling Frequency: 8kHz – 192kHz
- Pin Selectable Audio Data Interface Format
  - 16 to 24-bit I<sup>2</sup>S, 24-bit Right Justified or DSP
- 2.7V - 5.5V Supply Operation
- 14-pin SOIC Package
- Pin Compatible with WM8725 & WM8726

### APPLICATIONS

- DVD Players
- Home Theatre Systems
- Digital TV
- Digital Set Top Boxes

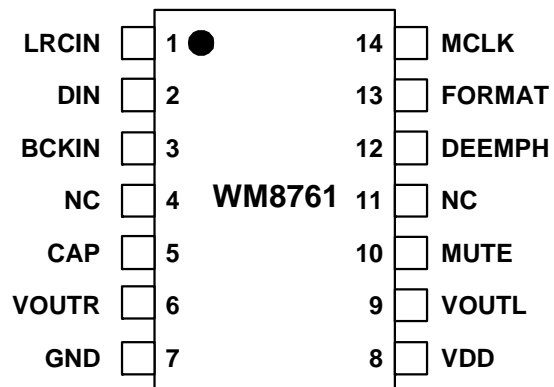
### BLOCK DIAGRAM



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## PIN CONFIGURATION



## ORDERING INFORMATION

| DEVICE       | TEMPERATURE RANGE | PACKAGE                                  | MOISTURE SENSITIVITY LEVEL | PEAK SOLDERING TEMPERATURE |
|--------------|-------------------|--|----------------------------|----------------------------|
| WM8761CGED   | -40 to +85°C      | 14-lead SOIC<br>(Pb-free)                | MSL1                       | 260°C                      |
| WM8761CGED/R | -40 to +85°C      | 14-lead SOIC<br>(Pb-free, tape and reel) | MSL1                       | 260°C                      |

**Note:**

Reel quantity = 3,000

**PIN DESCRIPTION**

| PIN | NAME   | TYPE            | DESCRIPTION  |
|-----|--------|-----------------|--|
| 1   | LRCIN  | Digital input   | Sample rate clock input  |
| 2   | DIN    | Digital input   | Serial audio data input  |
| 3   | BCKIN  | Digital input   | Bit clock input  |
| 4   | NC     | No connect      | No internal connection   |
| 5   | CAP    | Analogue output | Analogue internal reference  |
| 6   | VOUTR  | Analogue output | Right channel DAC output   |
| 7   | GND    | Supply          | Negative supply  |
| 8   | VDD    | Supply          | Positive supply  |
| 9   | VOUTL  | Analogue output | Left channel DAC output  |
| 10  | MUTE   | Digital input   | Soft mute control, Internal pull down<br>High Impedance = Automute<br>High = Mute ON<br>Low = Mute OFF                                       |
| 11  | NC     | No connect      | No internal connection   |
| 12  | DEEMPH | Digital input   | De-emphasis select, Internal pull up<br>High = de-emphasis ON<br>Low = de-emphasis OFF   |
| 13  | FORMAT | Digital input   | Data input format select, Internal pull up<br>Low = 24-bit right justified or DSP 'late'<br>High = 16-24-bit I <sup>2</sup> S or DSP 'early' |
| 14  | MCLK   | Digital input   | Master clock input   |

**Note:**

1. Digital input pins have Schmitt trigger input buffers.

## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <math> < 30^{\circ}\text{C}</math> / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <math> < 30^{\circ}\text{C}</math> / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <math> < 30^{\circ}\text{C}</math> / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

| CONDITION                           | MIN       | MAX       |
|-------------------------------------|-----------|-----------|
| Supply voltage                      | -0.3V     | +7V       |
| Voltage range digital inputs        | GND -0.3V | VDD +0.3V |
| Master Clock Frequency              |           | 50MHz     |
| Operating temperature range, $T_A$  | -40°C     | +85°C     |
| Storage temperature after soldering | -65°C     | +150°C    |

**DC ELECTRICAL CHARACTERISTICS**

| PARAMETER                   | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------|--------|-----------------|-----|-----|-----|------|
| Supply range                | VDD    |                 | 2.7 |     | 5.5 | V    |
| Ground                      | GND    |                 |     | 0   |     | V    |
| Supply current              |        | VDD = 5V        |     | 27  |     | mA   |
| Supply current              |        | VDD = 3.3V      |     | 23  |     | mA   |
| Power down current (note 4) |        | VDD=3.3V        |     | 0.5 |     | mA   |

**ELECTRICAL CHARACTERISTICS****Test Conditions**

VDD = 5V, GND = 0V, T<sub>A</sub> = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

| PARAMETER                                | SYMBOL           | TEST CONDITIONS                        | MIN        | TYP         | MAX        | UNIT             |
|--|------------------|--|------------|-------------|------------|------------------|
| <b>Digital Logic Levels (TTL Levels)</b> |                  |  |            |             |            |                  |
| Input LOW level                          | V <sub>IL</sub>  |  |            |             | 0.8        | V                |
| Input HIGH level                         | V <sub>IH</sub>  |  | 2.0        |             |            | V                |
| Output LOW                               | V <sub>OL</sub>  | I <sub>OL</sub> = 2mA                  |            |             | GND + 0.3V | V                |
| Output HIGH                              | V <sub>OH</sub>  | I <sub>OH</sub> = 2mA                  | VDD - 0.3V |             |            | V                |
| <b>Analogue Reference Levels</b>         |                  |  |            |             |            |                  |
| Reference voltage (CAP)                  |                  |  |            | VDD/2       |            | V                |
| Potential divider resistance             | R <sub>CAP</sub> | VDD to CAP and CAP to GND              |            | 50k         |            | Ω                |
| <b>DAC Output (Load = 10kΩ 50pF)</b>     |                  |  |            |             |            |                  |
| 0dBfs Full scale output voltage          |                  | At DAC outputs                         |            | 1.0 x VDD/5 |            | V <sub>rms</sub> |
| SNR (Note 1,2,3)                         |                  | A-weighted, @ fs = 48kHz               | 94         | 100         |            | dB               |
| SNR (Note 1,2,3)                         |                  | A-weighted @ fs = 96kHz                |            | 97          |            | dB               |
| SNR (Note 1,2,3)                         |                  | A-weighted @ fs = 192kHz               |            | 97          |            | dB               |
| SNR (Note 1,2,3)                         |                  | A-weighted, @ fs = 48kHz<br>VDD = 3.3V |            | 95          |            | dB               |
| SNR (Note 1,2,3)                         |                  | A-weighted @ fs = 96kHz<br>VDD = 3.3V  |            | 95          |            | dB               |
| SNR (Note 1,2,3)                         |                  | Non 'A' weighted @ fs = 48kHz          |            | 98          |            | dB               |
| THD (Note 3)                             |                  | 1kHz, 0dBfs                            |            | -90         | -85        | dB               |
| Dynamic Range (Note 2)                   |                  | 1kHz, THD+N @ -60dBfs                  | 90         | 100         |            | dB               |
| DAC channel separation                   |                  |  |            | 93          |            | dB               |

**Test Conditions**VDD = 5V, GND = 0V, T<sub>A</sub> = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

| PARAMETER                           | SYMBOL | TEST CONDITIONS                               | MIN | TYP   | MAX | UNIT             |
|-------------------------------------|--------|---|-----|-------|-----|------------------|
| <b>Analogue Output Levels</b>       |        |   |     |       |     |                  |
| Output level                        |        | Load = 10kΩ, 0dBFS                            |     | 1.1   |     | V <sub>RMS</sub> |
|                                     |        | Load = 10kΩ, 0dBFS,<br>(VDD = 3.3V)           |     | 0.72  |     | V <sub>RMS</sub> |
| Gain mismatch<br>channel-to-channel |        |   |     | ±1    |     | %FSR             |
| Minimum resistance load             |        | To midrail or a.c.<br>coupled                 |     | 1     |     | kΩ               |
|                                     |        | To midrail or a.c.<br>coupled<br>(VDD = 3.3V) |     | 1     |     | kΩ               |
| Maximum capacitance load            |        | 5V or 3.3V                                    |     | 100   |     | pF               |
| Output d.c. level                   |        |   |     | VDD/2 |     | V                |
| <b>Power On Reset (POR)</b>         |        |   |     |       |     |                  |
| POR threshold                       |        |   |     | 2.4   |     | V                |

**Notes:**

- Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted over a 20Hz to 20kHz bandwidth.
- All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
- CAP pin decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).
- Power down occurs 1.5μs after MCLK is stopped.

**TERMINOLOGY**

- Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
- Dynamic range (dB) - DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
- THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
- Stop band attenuation (dB) - Is the degree to which the frequency spectrum is attenuated (outside audio band).
- Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.

## MASTER CLOCK TIMING

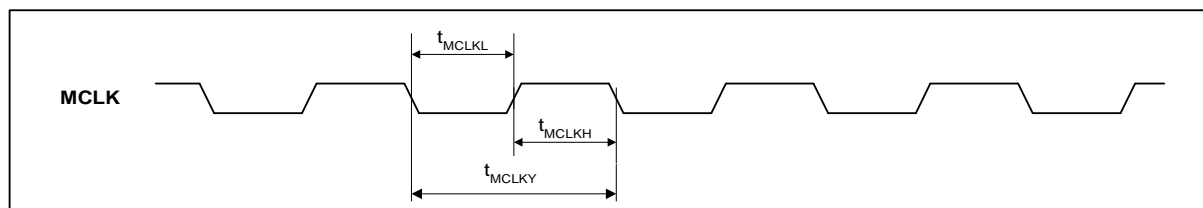


Figure 1 Master Clock Timing Requirements

### Test Conditions

VDD = 5V, GND = 0V, T<sub>A</sub> = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

| PARAMETER                              | SYMBOL      | TEST CONDITIONS | MIN   | TYP | MAX   | UNIT |
|--|-------------|-----------------|-------|-----|-------|------|
| <b>System Clock Timing Information</b> |             |                 |       |     |       |      |
| MCLK Master clock pulse width high     | $t_{MCLKH}$ |                 | 8     |     |       | ns   |
| MCLK Master clock pulse width low      | $t_{MCLKL}$ |                 | 8     |     |       | ns   |
| MCLK Master clock cycle time           | $t_{MCLKY}$ |                 | 20    |     |       | ns   |
| MCLK Duty cycle                        |             |                 | 40:60 |     | 60:40 |      |
| Time from MCLK stopping to power down. |             |                 | 1.5   |     | 12    | μs   |

## DIGITAL AUDIO INTERFACE

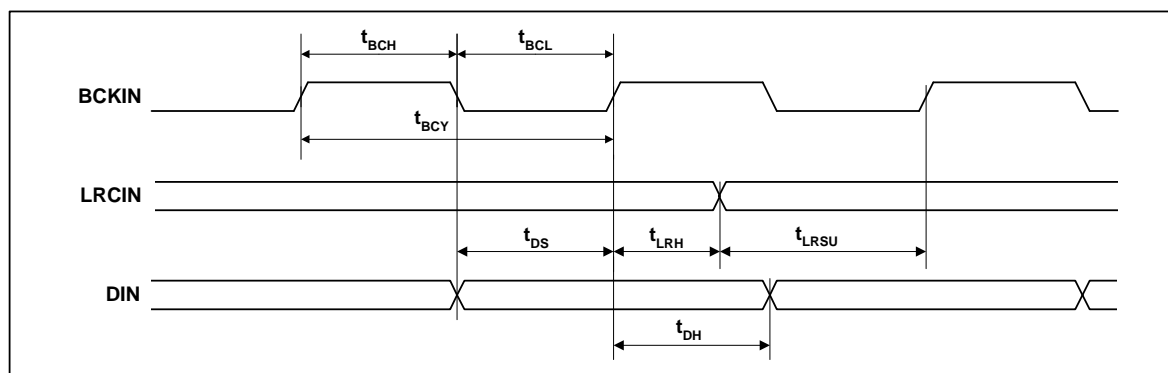


Figure 2 Digital Audio Data Timing

### Test Conditions

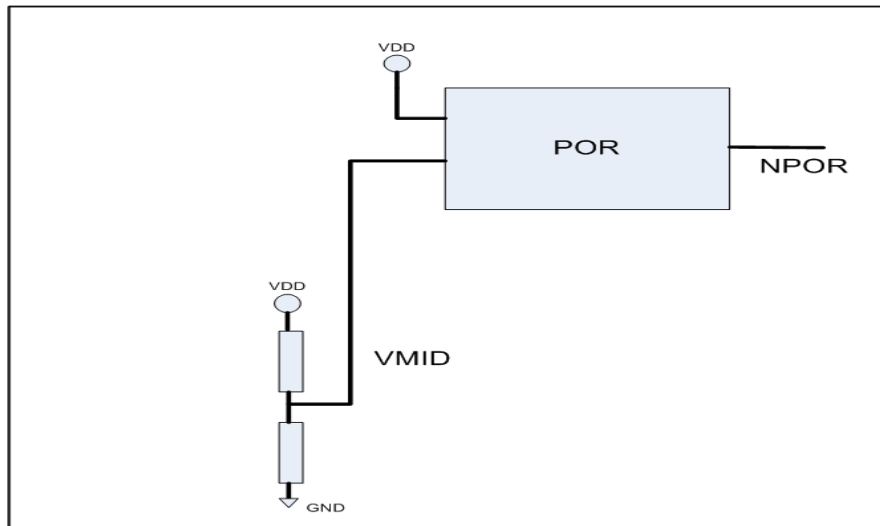
VDD = 5V, GND = 0V, T<sub>A</sub> = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

| PARAMETER                                  | SYMBOL     | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|------------|-----------------|-----|-----|-----|------|
| <b>Audio Data Input Timing Information</b> |            |                 |     |     |     |      |
| BCKIN cycle time                           | $t_{BCY}$  |                 | 40  |     |     | ns   |
| BCKIN pulse width high                     | $t_{BCH}$  |                 | 16  |     |     | ns   |
| BCKIN pulse width low                      | $t_{BCL}$  |                 | 16  |     |     | ns   |
| LRCIN set-up time to BCKIN rising edge     | $t_{LRSU}$ |                 | 8   |     |     | ns   |
| LRCIN hold time from BCKIN rising edge     | $t_{LRH}$  |                 | 8   |     |     | ns   |
| DIN set-up time to BCKIN rising edge       | $t_{DS}$   |                 | 8   |     |     | ns   |
| DIN hold time from BCKIN rising edge       | $t_{DH}$   |                 | 8   |     |     | ns   |



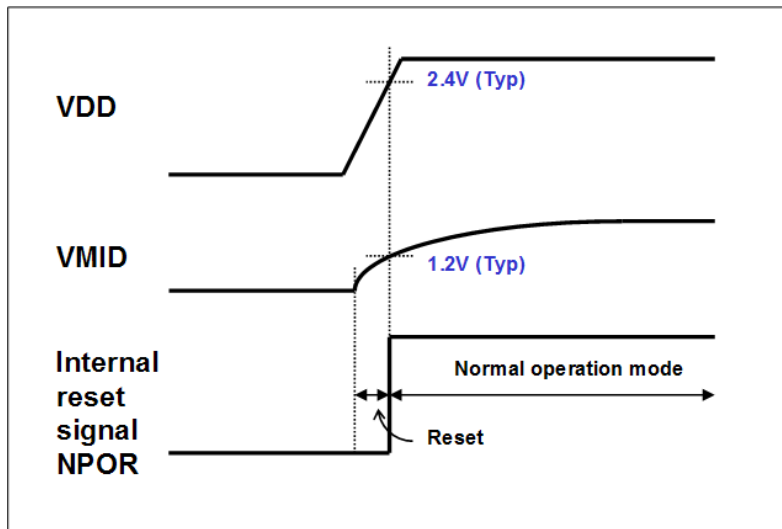
**POWER ON RESET (POR)**

The WM8761 has an internal power-on-reset (POR) circuit which is used to reset the digital logic into a default state after power up. A block diagram of the reset circuit is shown in Figure 3



**Figure 3 Block Diagram of Power-On-Reset**

The active low reset signal NPOR will be asserted low until VDD=2.4V, which means VMID rises to 1.2V. When this threshold has been reached, then the NPOR is released and the digital interface has been reset. This is illustrated in the diagram shown in Figure 4.



**Figure 4 Generation of Internal NPOR at Power-On-Reset**

Figure 5 illustrates the NPOR generation when the power is removed.

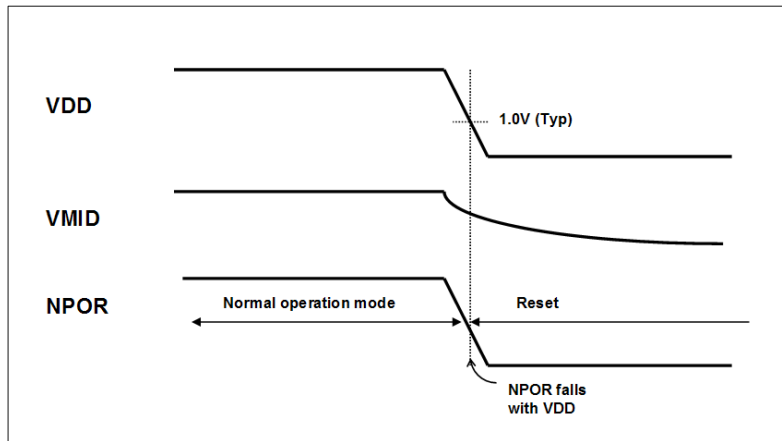


Figure 5 Generation of NPOR at Power-Off-Reset

## DEVICE DESCRIPTION

### GENERAL INTRODUCTION

The WM8761 is a high performance DAC designed for digital consumer audio applications. The range of features make it ideally suited for use in DVD players, AV receivers and other consumer audio equipment.

The WM8761 is a complete 2-channel stereo audio digital-to-analogue converter, including digital interpolation filter, multi-bit sigma delta with dither, and switched capacitor multi-bit stereo DAC and output smoothing filters. It is fully compatible and an ideal partner for a range of industry standard microprocessors, controllers and DSPs. A novel multi bit sigma-delta DAC design is used, utilising a 128x oversampling rate, to optimise signal to noise performance and offer increased clock jitter tolerance. (In 'high-rate' operation, the oversampling ratio is 64x for system clocks of 128fs).

Control of internal functionality of the device is provided by hardware control (pin programmed).

Operation using master clocks of 256fs, 512fs or 768fs is provided, selection between clock rates being automatically controlled. Sample rates (fs) from less than 8kHz to 96kHz are allowed, provided the appropriate system clock is input. Support is also provided for up to 192kHz using a master clock of 128fs.

The audio data interface supports 24-bit right justified or 16-24-bit I<sup>2</sup>S (Philips left justified, one bit delayed) interface formats. A DSP interface is also supported, enhancing the interface options for the user.

A single 2.7-5.5V supply may be used, the output amplitude scaling with absolute supply level. Low supply voltage operation and low current consumption combined with the low pin count small package make the WM8761 attractive for many consumer applications.

The device is packaged in a small 14-pin SOIC.

### DAC CIRCUIT DESCRIPTION

The WM8761 DAC is designed to allow playback of 24-bit PCM audio or similar data with high resolution and low noise and distortion. Sample rates up to 192kHz may be used, with much lower sample rates acceptable provided that the ratio of sample rate (LRCIN) to master clock (MCLK) is maintained at one of the required rates.

The two DACs on the WM8761 are implemented using sigma-delta oversampled conversion techniques. These require that the PCM samples are digitally filtered and interpolated to generate a set of samples at a much higher rate than the up to 192kHz input rate. This sample stream is then digitally modulated to generate a digital pulse stream that is then converted to analogue signals in a switched capacitor DAC. The advantage of this technique is that the DAC is linearised using noise shaping techniques, allowing the 24-bit resolution to be met using non-critical analogue components. A further advantage is that the high sample rate at the DAC output means that smoothing filters on the output of the DAC need only have fairly crude characteristics in order to remove the characteristic steps, or images on the output of the DAC. To ensure that generation of tones characteristic to sigma-delta convertors is not a problem, dithering is used in the digital modulator along with a higher order modulator. The multi-bit switched capacitor technique used in the DAC reduces sensitivity to clock jitter, and dramatically reduces out of band noise compared to switched current or single bit techniques used in other implementations.

The voltage on the CAP pin is used as the reference for the DACs. Therefore the amplitude of the signals at the DAC outputs will scale with the amplitude of the voltage at the CAP pin. An external reference could be used to drive into the CAP pin if desired, with a value typically of about mid-rail ideal for optimum performance.

The outputs of the 2 DACs are buffered out of the device by buffer amplifiers. These amplifiers will source load currents of several mA and sink current up to 1.5mA allowing significant loads to be driven. The output source is active and the sink is Class A, i.e. fixed value, so greater loads might be driven if an external 'pull-down' resistor is connected at the output.

Typically an external low pass filter circuit will be used to remove residual out of band noise characteristic of delta sigma converters. However, the advanced multi-bit DAC used in WM8761 produces far less out of band noise than single bit traditional sigma delta DACs, and so in many applications this filter may be removed, or replaced with a simple RC pole.

## CLOCKING SCHEMES

In a typical digital audio system there is only one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's Master Clock. The external master clock can be applied directly through the MCLK input pin with no configuration necessary for sample rate selection.

Note that on the WM8761, MCLK is used to derive clocks for the DAC path. The DAC path consists of DAC sampling clock, DAC digital filter clock and DAC digital audio interface timing. In a system where there are a number of possible sources for the reference clock it is recommended that the clock source with the lowest jitter be used to optimise the performance of the DAC.

The device can be powered down by stopping MCLK. In this state the power consumption is substantially reduced.

## DIGITAL AUDIO INTERFACE

Audio data is applied to the internal DAC filters via the Digital Audio Interface. Three interface formats are supported:

- Right Justified mode
- I<sup>2</sup>S mode
- DSP mode

All formats send the MSB first. The data format is selected with the FORMAT pin. When FORMAT is LOW, right justified data format is selected and word lengths up to 24-bits may be used. When the FORMAT pin is HIGH, I<sup>2</sup>S format is selected and word length of any value up to 24-bits may be used. (If a word length shorter than 24-bits is used, the unused bits will be padded with zeros). If LRCIN is 4 BCKINS or less duration, the DSP compatible format is selected. Early and Late clock formats are supported, selected by the state of the FORMAT pin.

'Packed' mode (i.e. only 32 or 48 clocks per LRCIN period) operation is also supported in I<sup>2</sup>S and right justified modes. If a 'packed' format of 16-bit word length is applied (16 BCKINS per LRCIN half period), the device auto-detects this mode and switches to 16-bit data length.

### I<sup>2</sup>S MODE

The WM8761 supports word lengths of 16-24 bits in I<sup>2</sup>S mode.

In I<sup>2</sup>S mode, the digital audio interface receives data on the DIN input. Audio Data is time multiplexed with LRCIN indicating whether the left or right channel is present. LRCIN is also used as a timing reference to indicate the beginning or end of the data words.

In I<sup>2</sup>S modes, the minimum number of BCKINS per LRCIN period is 2 times the selected word length. LRCIN must be high for a minimum of word length BCKINS and low for a minimum of word length BCKINS. Any mark to space ratio on LRCIN is acceptable provided the above requirements are met. In I<sup>2</sup>S mode, the MSB is sampled on the second rising edge of BCKIN following a LRCIN transition. LRCIN is low during the left samples and high during the right samples.

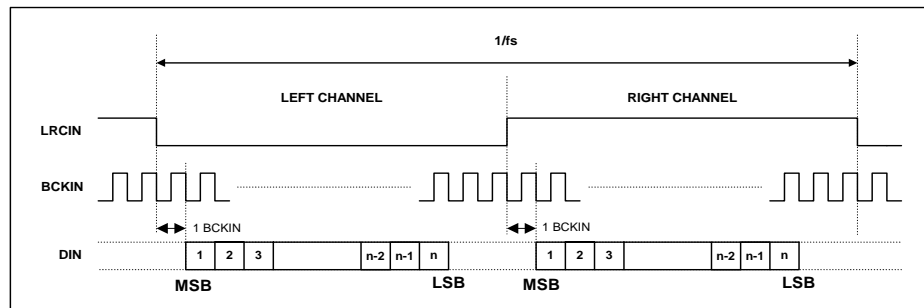


Figure 6 I<sup>2</sup>S Mode Timing Diagram

### RIGHT JUSTIFIED MODE

The WM8761 supports word lengths of 24-bits in right justified mode.

In right justified mode, the digital audio interface receives data on the DIN input. Audio Data is time multiplexed with LRCIN indicating whether the left or right channel is present. LRCIN is also used as a timing reference to indicate the beginning or end of the data words.

In right justified mode, the minimum number of BCKINs per LRCIN period is 2 times the selected word length. LRCIN must be high for a minimum of word length BCKINs and low for a minimum of word length BCKINs. Any mark to space ratio on LRCIN is acceptable provided the above requirements are met.

In right justified mode, the LSB is sampled on the rising edge of BCKIN preceding a LRCIN transition. LRCIN is high during the left samples and low during the right samples.

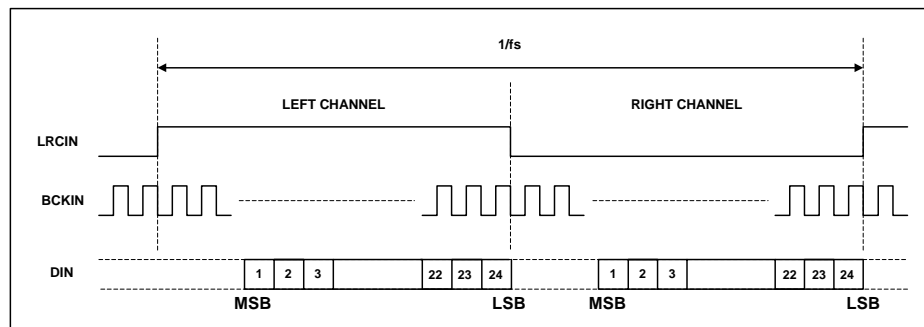


Figure 7 Right Justified Mode Timing Diagram

### DSP MODE

A DSP compatible, time division multiplexed format is also supported by the WM8761. This format is of the type where a 'synch' pulse is followed by two data words (left and right) of predetermined word length. (16-bits). The 'synch' pulse replaces the normal duration LRCIN, and DSP mode is auto-detected by the shorter than normal duration of the LRCIN. If LRCIN is of 4 BCKIN or less duration, the DSP compatible format is selected. Early and Late clock formats are supported, selected by the state of the FORMAT pin.

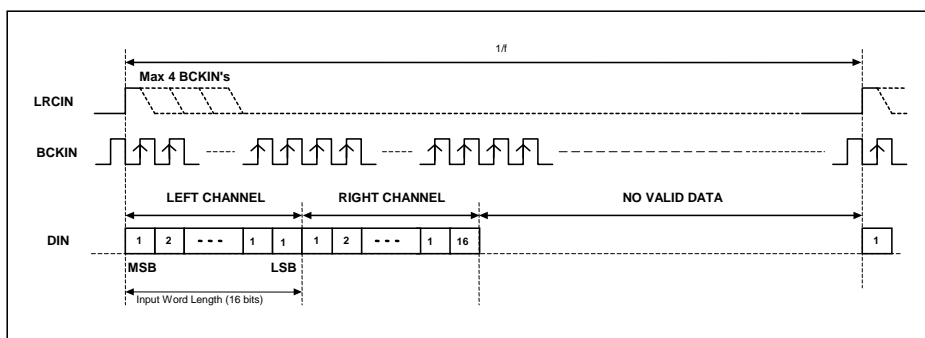


Figure 8 DSP 'Late' Mode Timing

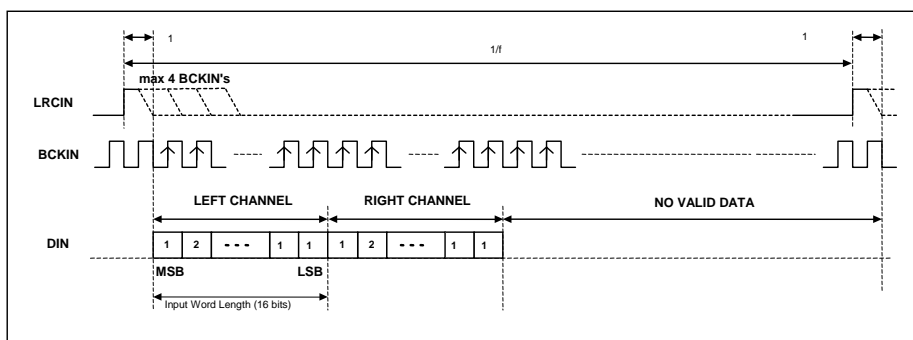


Figure 9 DSP 'Early' Mode Timing

## AUDIO DATA SAMPLING RATES

The master clock for WM8761 supports audio sampling rates from 128fs to 768fs, where fs is the audio sampling frequency (LRCIN) typically 32kHz, 44.1kHz, 48kHz, 96kHz or 192kHz. The master clock is used to operate the digital filters and the noise shaping circuits.

The WM8761 has a master clock detection circuit that automatically determines the relation between the master clock frequency and the sampling rate (to within +/- 8 master clocks). If there is a greater than 8 clocks error, the interface shuts down the DAC and mutes the output. The master clock should be synchronised with LRCIN, although the WM8761 is tolerant of phase differences or jitter on this clock.

| SAMPLING RATE (LRCIN) | MASTER CLOCK FREQUENCY (MHz) (MCLK) |             |             |             |
|-----------------------|-------------------------------------|-------------|-------------|-------------|
|                       | 128FS                               | 256fs       | 512fs       | 768fs       |
| 32kHz                 | 4.096                               | 8.192       | 16.384      | 24.576      |
| 44.1kHz               | 5.6448                              | 11.2896     | 22.5792     | 33.8688     |
| 48kHz                 | 6.144                               | 12.288      | 24.576      | 36.864      |
| 96kHz                 | 12.288                              | 24.576      | Unavailable | Unavailable |
| 192kHz                | 24.576                              | Unavailable | Unavailable | Unavailable |

Table 1 Master Clock Frequencies Versus Sampling Rate

For sample rate support of MCLK at 192fs and 384fs, please refer to the pin-compatible WM8761B device.

## HARDWARE CONTROL MODES

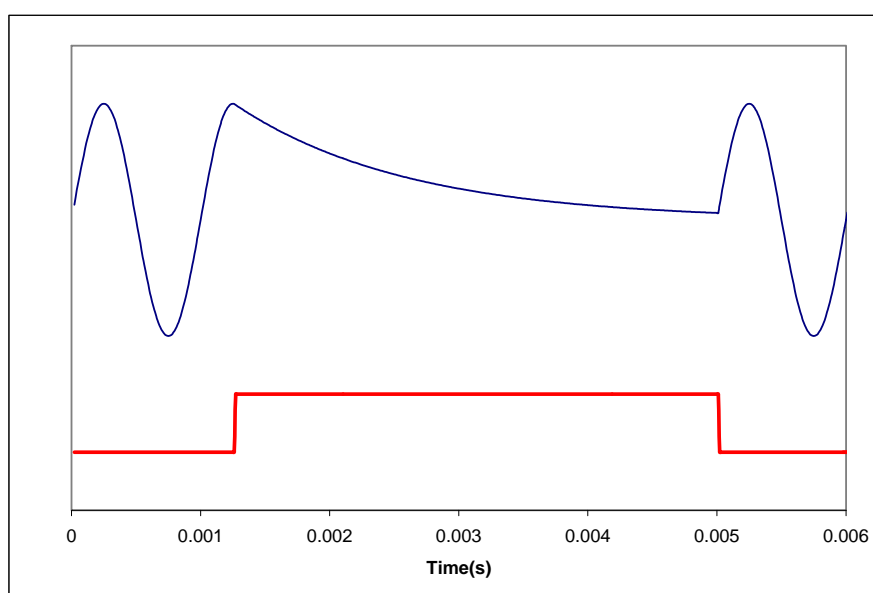
The WM8761 is hardware programmable providing the user with options to select input audio data format, de-emphasis and mute.

### MUTE AND AUTO MUTE OPERATION

Pin 10 (MUTE) controls selection of MUTE directly, and can be used to enable and disable the automute function, or as an output of the automuted signal.

| MUTE PIN | DESCRIPTION   |
|----------|---|
| 0        | Normal Operation, MUTE off                                      |
| 1        | Mute DAC channels   |
| Floating | Enable IZD, MUTE becomes an output to indicate when IZD occurs. |

**Table 2 Mute and Automute Control**



**Figure 10 Application and Release of MUTE**

The MUTE pin is an input to select mute or not mute. MUTE is active high; taking the pin high causes the filters to soft mute, ramping down the audio signal over a few milliseconds. Taking MUTE low again allows data into the filter. Refer to Figure 10.

The Infinite Zero Detect (IZD) function detects a series of zero value audio samples of 1024 samples long being applied to both channels. After such an event, a latch is set whose output (AUTOMUTED) is connected through a 10kohm resistor to the MUTE pin. Thus if the MUTE pin is not being driven, the automute function will assert mute.

If MUTE is tied low, AUTOMUTED is overridden and will not mute. If MUTE is driven from a bi-directional source, then both MUTE and automute functions are available. If MUTE is not driven, AUTOMUTED appears as a weak output (10k source impedance) so can be used to drive external mute circuits. AUTOMUTED will be removed as soon as any channel receives a non-zero input.

A diagram showing how the various Mute modes interact is shown below in Figure 11.

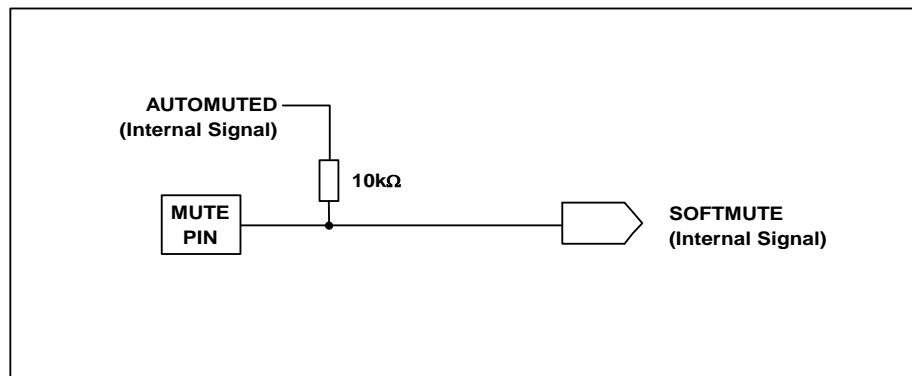


Figure 11 Selection Logic for MUTE Modes

### INPUT AUDIO FORMAT SELECTION

FORMAT (pin 13) controls the data input format.

| FORMAT | INPUT DATA MODE            |
|--------|----------------------------|
| 0      | 24 bit right justified     |
| 1      | 16–24 bit I <sup>2</sup> S |

Table 3 Input Audio Format Selection

#### Notes:

- In 16-24 bit I<sup>2</sup>S mode, any data from 16-24 bits or more is supported provided that LRCIN is high for a minimum of data width BCKINs and low for a minimum of data width BCKINs, unless Note 2. For data widths greater than 24 bits, the LSB's will be truncated and the most significant 24 bits will be used by the internal processing.
- If exactly 16 BCKIN cycles occur in both the low and high period of LRCIN the WM8761 will assume the data is 16-bit and accept the data accordingly.

### INPUT DSP FORMAT SELECTION

| FORMAT | 50% LRCIN DUTY CYCLE  | LRCIN of 4 BCKIN or Less Duration |
|--------|---|-----------------------------------|
| 0      | 24-bit (MSB-first, right justified)                                 | DSP format – 'late' mode          |
| 1      | Up to 24-bit I <sup>2</sup> S format (Philips serial data protocol) | DSP format – 'early' mode         |

Table 4 DSP Interface Formats

### DE-EMPHASIS CONTROL

DEM (pin 12) is an input control for selection of de-emphasis filtering to be applied.

| DEEMPH | DE-EMPHASIS |
|--------|-------------|
| 0      | Off         |
| 1      | On          |

Table 5 De-emphasis Control

### DAC OUTPUT PHASE

In the DAC to analogue output, the analogue output data VOUTL/R, is a phase inverted representation of the digital input signal.



**DIGITAL FILTER CHARACTERISTICS**

| PARAMETER            | SYMBOL | TEST CONDITIONS | MIN | TYP     | MAX        | UNIT |
|----------------------|--------|-----------------|-----|---------|------------|------|
| Passband Edge        |        | -3dB            |     | 0.487fs |            |      |
| Passband Ripple      |        | $f < 0.444fs$   |     |         | $\pm 0.05$ | dB   |
| Stopband Attenuation |        | $f > 0.555fs$   | -60 |         |            | dB   |

Table 6 Digital Filter Characteristics

**DAC FILTER RESPONSES**

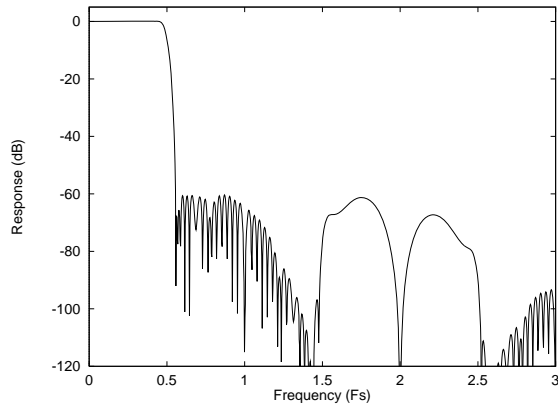


Figure 12 DAC Digital Filter Frequency Response for 256fs, 512fs & 768fs

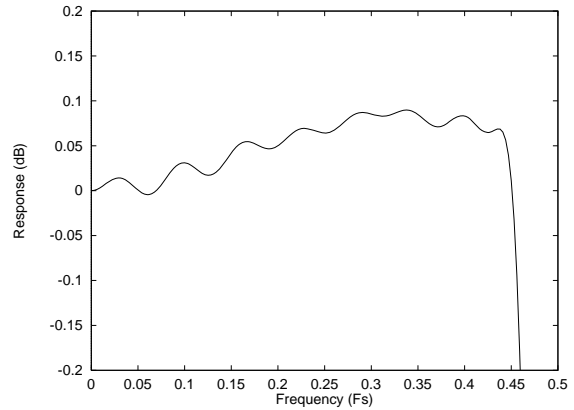


Figure 13 DAC Digital Filter Ripple for 256fs, 512fs & 768fs

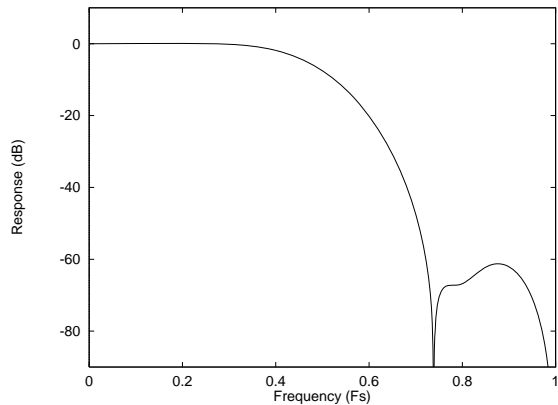


Figure 14 DAC Digital Filter Frequency Response for 128fs

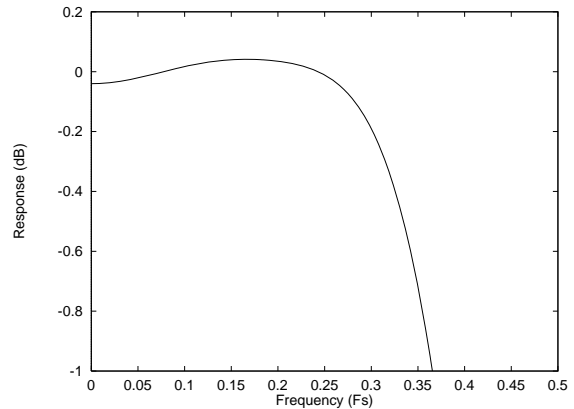


Figure 15 DAC Digital Filter Ripple for 128fs

### DIGITAL DE-EMPHASIS CHARACTERISTICS

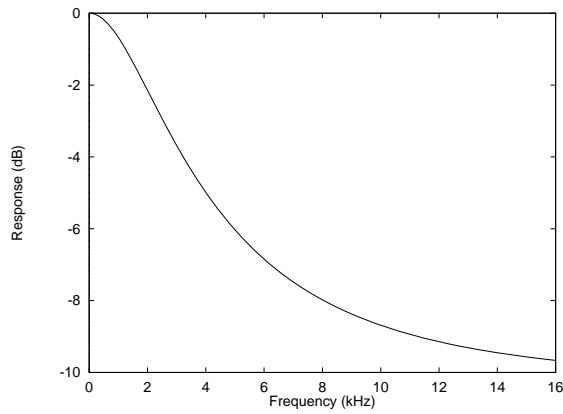


Figure 16 De-Emphasis Frequency Response (32kHz)

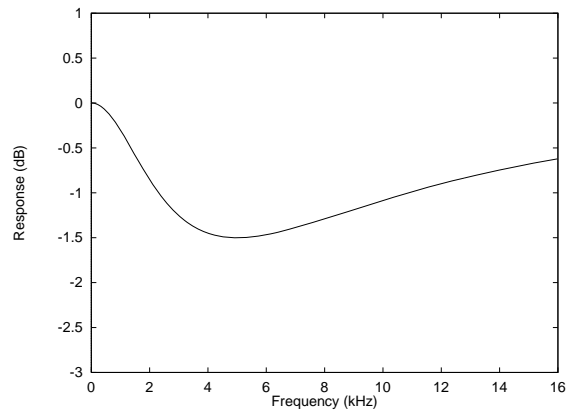


Figure 17 De-Emphasis Error (32kHz)

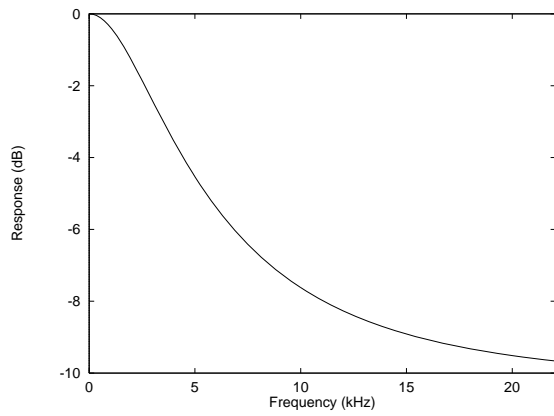


Figure 18 De-Emphasis Frequency Response (44.1kHz)

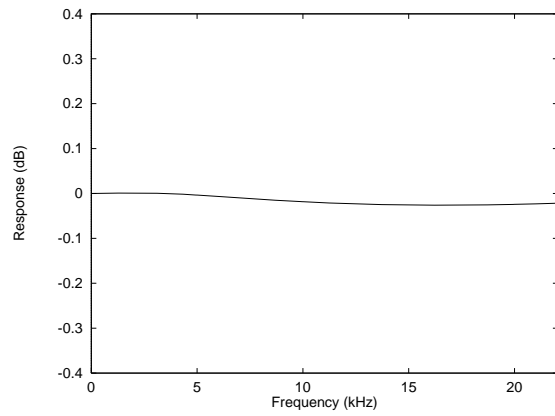


Figure 19 De-Emphasis Error (44.1kHz)

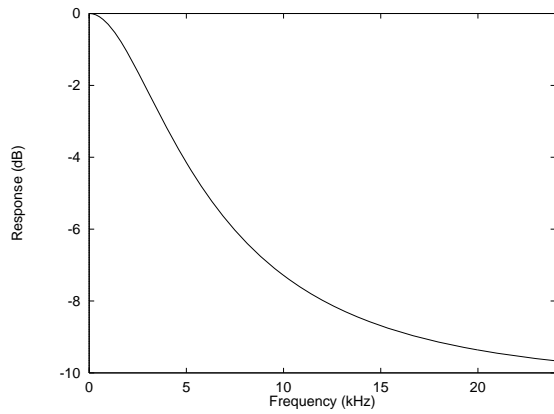


Figure 20 De-Emphasis Frequency Response (48kHz)

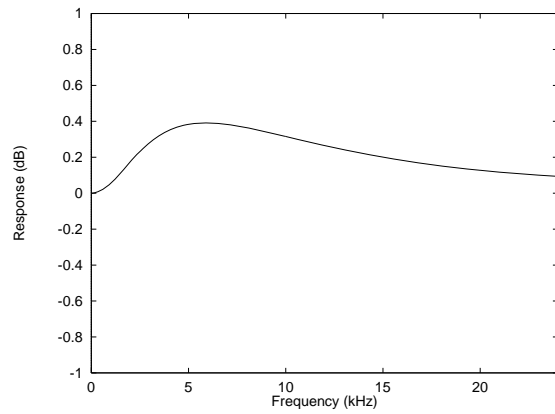


Figure 21 De-Emphasis Error (48kHz)

## APPLICATIONS INFORMATION

## RECOMMENDED EXTERNAL COMPONENTS

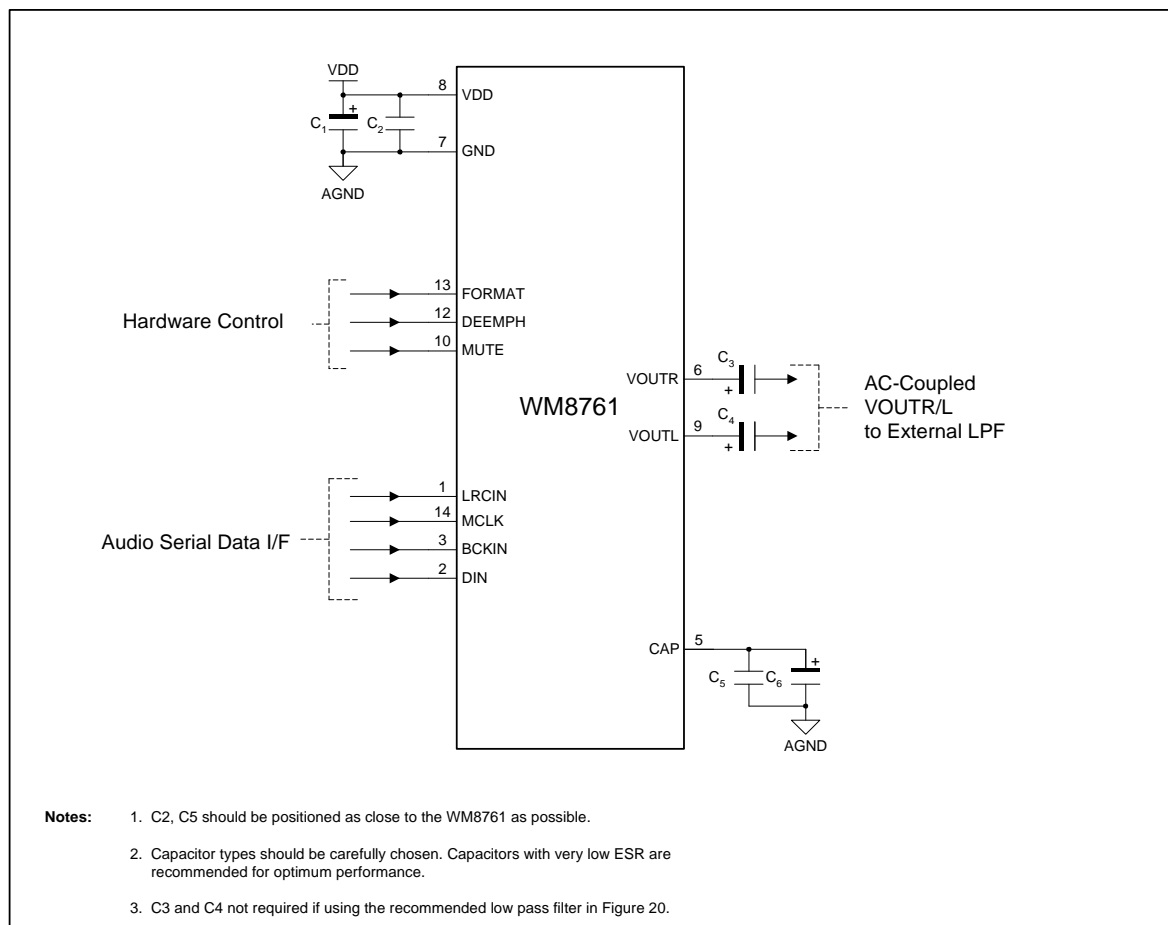


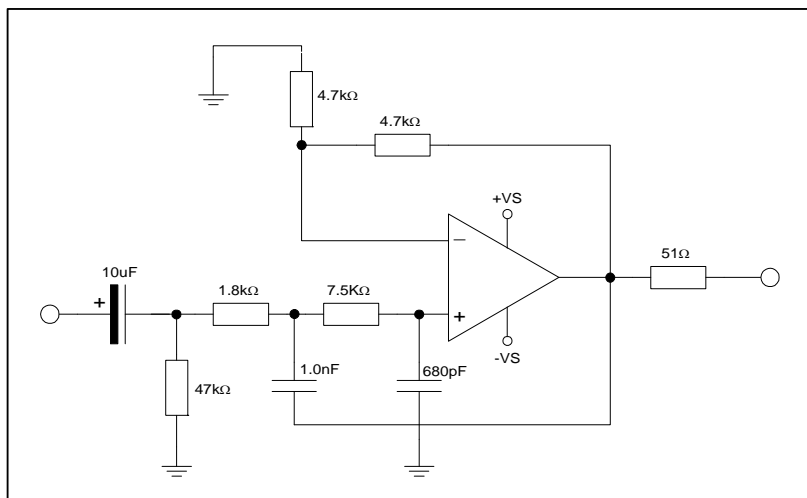
Figure 22 External Component Diagram

## RECOMMENDED EXTERNAL COMPONENTS VALUES

| COMPONENT REFERENCE | SUGGESTED VALUE | DESCRIPTION   |
|---------------------|-----------------|---|
| C1                  | 10 $\mu$ F      | De-coupling for VDD   |
| C2                  | 0.1 $\mu$ F     | De-coupling for VDD   |
| C3 and C4           | 10 $\mu$ F      | Output AC coupling caps to remove midrail DC level from outputs |
| C5                  | 0.1 $\mu$ F     | Reference de-coupling capacitors for CAP pin                    |
| C6                  | 10 $\mu$ F      |   |

Table 7 External Components Description

## RECOMMENDED ANALOGUE LOW PASS FILTER

Figure 23 Recommended 2<sup>nd</sup> Order Low Pass Filter

An external low pass filter is recommended (see Figure 20) if the device is driving a wideband amplifier. In some applications, a passive RC filter may be adequate.

## PCB LAYOUT RECOMMENDATIONS

Care should be taken in the layout of the PCB that the WM8761 is to be mounted to. The following notes will help in this respect:

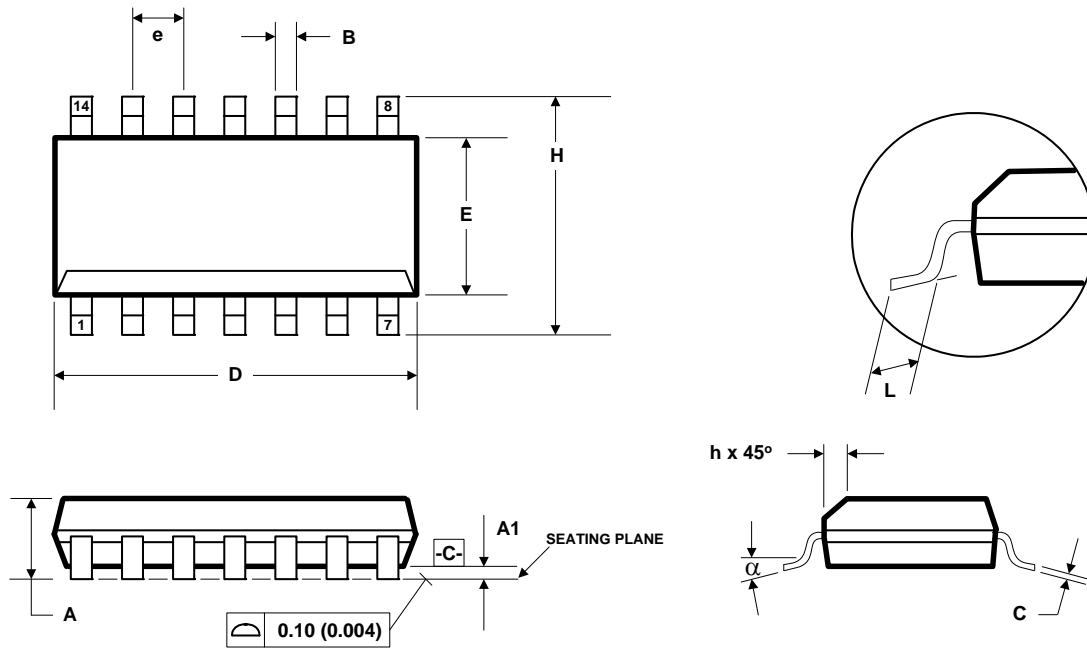
1. **The VDD supply to the device should be as noise free as possible.** This can be accomplished to a large degree with a 10uF bulk capacitor placed locally to the device and a 0.1uF high frequency decoupling capacitor placed as close to the VDD pin as possible. It is best to place the 0.1uF capacitor directly between the VDD and GND pins of the device on the same layer to minimize track inductance and thus improve device decoupling effectiveness.
2. **The CAP pin should be as noise free as possible.** This pin provides the decoupling for the on chip reference circuits and thus any noise present on this pin will be directly coupled to the device outputs. In a similar manner to the VDD decoupling described in 1. above, this pin should be decoupled with a 10uF bulk capacitor local to the device and a 0.1uF capacitor as close to the CAP pin as possible.
3. **Separate analogue and digital track routing from each other.** The device is split into analogue (pins 5 – 9) and digital (pins 1 – 4 & pins 10 – 14) sections that allow the routing of these signals to be easily separated. By physically separating analogue and digital signals, crosstalk from the PCB can be minimized.
4. **Use an unbroken solid GND plane.** To achieve best performance from the device, it is advisable to have either a GND plane layer on a multilayer PCB or to dedicate one side of a 2 layer PCB to be a GND plane. For double sided implementations it is best to route as many signals as possible on the device mounted side of the board, with the opposite side acting as a GND plane. The use of a GND plane greatly reduces any electrical emissions from the PCB and minimizes crosstalk between signals.

An evaluation board is available for the WM8761 that demonstrates the above techniques and the excellent performance achievable from the device. This can be ordered or the User manual downloaded from the Wolfson web site at [www.wolfsonmicro.com](http://www.wolfsonmicro.com)

PACKAGE DRAWING

D: 14 PIN SOIC 3.9mm Wide Body

DM001.C



| Symbols | Dimensions (MM)  |      | Dimensions (Inches) |        |
|---------|------------------|------|---------------------|--------|
|         | MIN              | MAX  | MIN                 | MAX    |
| A       | 1.35             | 1.75 | 0.0532              | 0.0688 |
| A1      | 0.10             | 0.25 | 0.0040              | 0.0098 |
| B       | 0.33             | 0.51 | 0.0130              | 0.0200 |
| C       | 0.19             | 0.25 | 0.0075              | 0.0098 |
| D       | 8.55             | 8.75 | 0.3367              | 0.3444 |
| E       | 3.80             | 4.00 | 0.1497              | 0.1574 |
| e       | 1.27 BSC         |      | 0.05 BSC            |        |
| H       | 5.80             | 6.20 | 0.2284              | 0.2440 |
| h       | 0.25             | 0.50 | 0.0099              | 0.0196 |
| L       | 0.40             | 1.27 | 0.0160              | 0.0500 |
| α       | 0°               | 8°   | 0°                  | 8°     |
| REF:    | JEDEC.95, MS-012 |      |                     |        |

NOTES:

- A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS (INCHES).
- B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
- C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM (0.010IN).
- D. MEETS JEDEC.95 MS-012, VARIATION = AB. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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**REVISION HISTORY**

| DATE     | REV | ORIGINATOR | CHANGES  |
|----------|-----|------------|--|
| 09/02/11 | 4.4 | WF         | Added WM8726 text, p1<br>Replaced sample rate text with fs ratio text for Figures 12-15, p18   |
| 13/06/11 | 4.5 | BT         | Removed reference to 192fs and 384fs support, placed reference to WM8761B device for 192fs and 384fs support in Audio Data Sampling Rates section. |
| 16/09/11 | 4.6 | JMacD      | Order codes changed from WM8761GED/V and WM8761GED/RV to WM8761CGED and WM8761CGED/R to reflect copper wire bonding and MSL change.                |
| 16/09/11 | 4.6 | JMacD      | MSL changed from MSL2 to MSL1.   |

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