CS4270

24-Bit, 192-kHz Stereo Audio CODEC

D/A Features

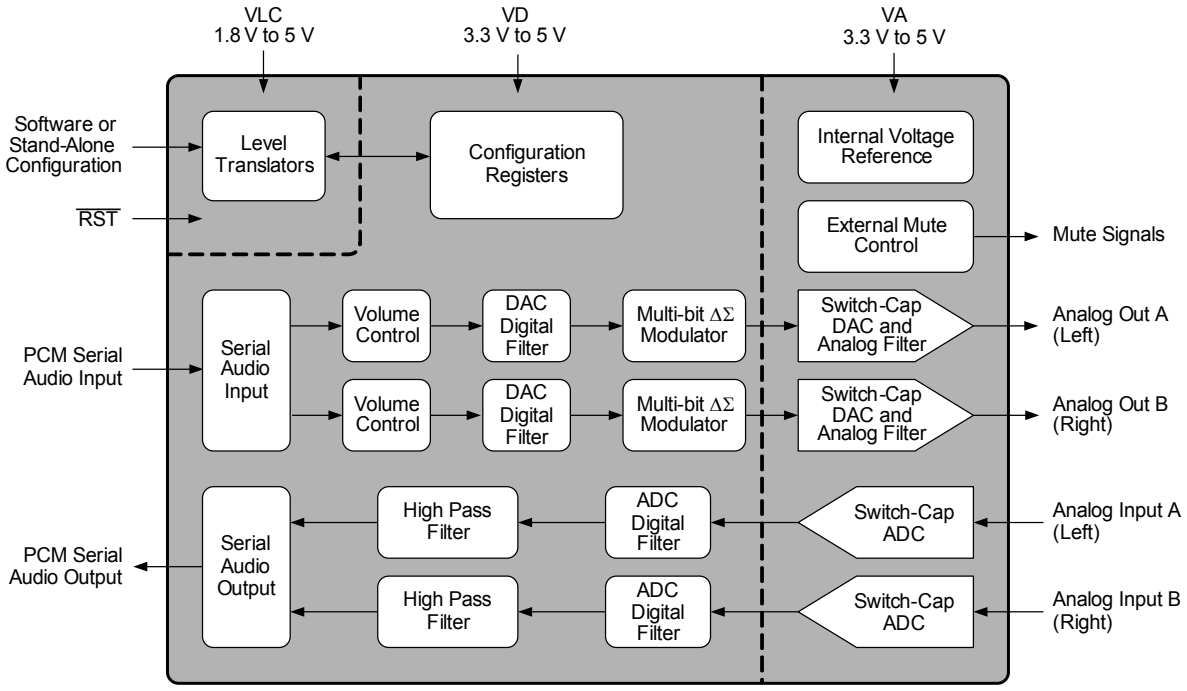
- High Performance
  - 105 dB Dynamic Range
  - -87 dB THD+N
- Selectable Serial Audio Interface Formats
  - Left-Justified up to 24 bits
  - I²S up to 24 bits
  - Right-Justified 16, and 24 bits
- Control Output for External Muting
- Digital De-Emphasis
- Popguard® Technology
- Multi-bit ΔΣ Conversion
- Digital Volume Control
- Single-Ended Output

A/D Features

- High Performance
  - 105 dB Dynamic Range
  - -95 dB THD+N
- Multi-bit ΔΣ Conversion
- High-Pass Filter to Remove DC Offsets
- Selectable Serial Audio Interface Formats
  - Left-Justified up to 24 bits
  - I²S up to 24 bits
- Single-Ended Input

System Features

- Direct Interface with Logic Levels 1.8 V to 5 V
- Internal Digital Loopback
- Stand-Alone or Serial Control Port Functionality
- Single-Ended Analog Architecture
- Supports all Audio Sample Rates from 4 kHz to 216 kHz
- 3.3- or 5-V Core Supply



Stand-Alone Mode Feature Set

- System Features
  - Master or Slave Serial Audio Interface
  - Single-, Double-, or Quad-Speed Operation
- D/A Features
  - Auto-Mute on Static Samples
  - 44.1 kHz 50/15 μs De-emphasis Available
  - Selectable Serial Audio Interface Formats
    - Left-Justified up to 24-bit
    - I²S up to 24-bit
- A/D Features
  - High-Pass Filter
  - Selectable Serial Audio Interface Formats
    - Left-Justified up to 24-bit
    - I²S up to 24-bit

Software Mode Feature Set

- System Features
  - Master or Slave Serial Audio Interface
  - Single-, Double-, or Quad-Speed Operation
  - Internal Digital Loopback Available
- D/A Features
  - Selectable Auto-mute
  - 44.1-kHz 50/15 μs De-emphasis Available
  - Configurable Muting Controls
  - Volume Control
  - Selectable Serial Audio Interface Formats
    - Left-Justified up to 24-bit
    - I²S up to 24-bit
    - Right-Justified 16, and 24-bit
- A/D Features
  - Selectable High-Pass Filter or DC Offset Calibration
  - Selectable Serial Audio Interface Formats
    - Left-Justified up to 24-bit
    - I²S up to 24-bit

General Description

The CS4270 is a high-performance, integrated audio CODEC. The CS4270 performs stereo analog-to-digital (A/D) and digital-to-analog (D/A) conversion of up to 24-bit serial values at sample rates up to 216 kHz.

Standard 50/15 μs de-emphasis is available for sampling rates of 44.1 kHz for compatibility with digital audio programs mastered using the 50/15 μs pre-emphasis technique.

Integrated level translators allow easy interfacing between the CS4270 and other devices operating over a wide range of logic levels.

Independently addressable high-pass filters are available for the right and left channel of the A/D. This allows the A/D to be used in a wide variety of applications where one audio channel and one DC measurement channel is desired.

The CS4270 is available in a 24-pin TSSOP package (-10° to +70° C). The CDB4270 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please refer to "Ordering Information" on page 44 for complete ordering information.

The CS4270's wide dynamic range, negligible distortion, and low noise make it ideal for applications such as DVD recorders, digital televisions, set-top boxes, and effects processors.

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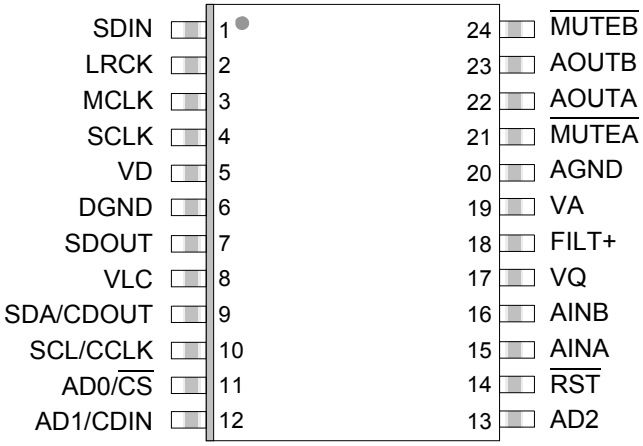
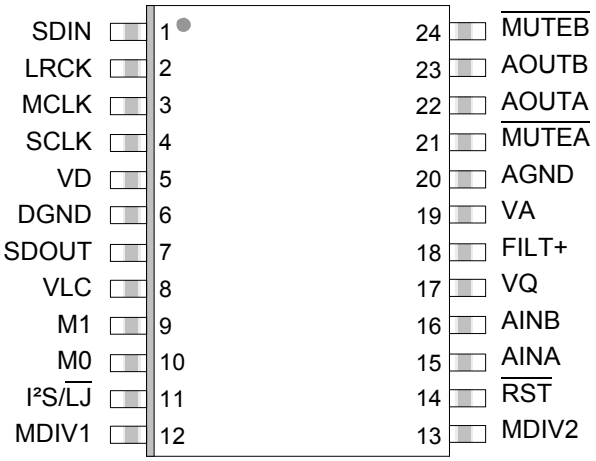
1. PIN DESCRIPTIONS

1.1 Software Mode



Pin Name	#	Pin Description
SDIN	1	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
LRCK	2	**Left Right Clock** *(Input/Output)* - Determines which channel, left or right, is currently active on the serial audio data line. The frequency of the left/right clock must be at the audio sample rate, Fs.
MCLK	3	**Master Clock** (*Input*) - Clock for the delta-sigma modulator and the digital filters.
SCLK	4	**Serial Bit Clock** *(Input/Output)* - Serial bit clock for the serial audio interface.
VD	5	**Digital Power** (*Input*) - Positive power for the digital section.
DGND	6	**Digital Ground** (*Input*) - Ground reference for the digital section.
SDOUT	7	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data.
VLC	8	**Serial Control Port Power** (*Input*) - Positive power for the Serial Control Port.
SDA/CDOUT	9	**Serial Control Data** (*Input/Output*) - SDA is a data I/O line in I²C Mode. CDOUT is the output data line for the Serial Control Port in SPI format.
SCL/CCLK	10	**Serial Control Port Clock** (*Input*) - SCL is the serial input Clock for the Serial Control Port in I²C format. CCLK is the serial input Clock for the Serial Control Port in SPI format.
AD0/$\overline{CS}$	11	**Address Bit 0 (I²C)/Serial Control Port Chip Select (SPI)** *(Input)* - AD0 is a chip address pin in I²C format. CS is the chip select signal for SPI format.
AD1/CDIN	12	**Address Bit 1 (I²C)/Serial Control Data** (*Input*) - AD1 is a chip address pin in I²C Mode. CDIN is the input data line for the Serial Control Port in SPI format.
AD2	13	**Address Bit 2 (I²C)** (*Input*) - AD2 is a chip address pin in I²C format.
$\overline{RST}$	14	**Reset** (*Input*) - Input for resetting all internal registers to their default settings and for placing the device in a low-power mode.
AINA AINB	15 16	**Analog Audio Input** (*Input*) - Analog inputs to the ADC.
VQ	17	**Quiescent Voltage** (*Output*) - Filter connection for the internal quiescent voltage.
FILT+	18	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits.
VA	19	**Analog Power** (*Input*) - Positive power for the analog section.
AGND	20	**Analog Ground** (*Input*) - Ground reference for the analog section.
$\overline{MUTEA}$ $\overline{MUTEB}$	21 24	**Mute Control** *(Output)* - Mute control signal used to control the state of the optional external analog muting circuitry. See Section 5.6 on page 27.
AOUTA AOUTB	22 23	**Analog Audio Output** (*Output*) - Analog outputs from the DAC.

1.2 Stand-Alone Mode



Pin Name	#	Pin Description
SDIN	1	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
LRCK	2	**Left Right Clock** *(Input/Output)* - Determines which channel, Left or Right, is currently active on the serialaudio data line. The frequency of the left/right clock must be at the audio sample rate, Fs.
MCLK	3	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
SCLK	4	**Serial Bit Clock** *(Input/Output)* - Serial bit clock for the serial audio interface.
VD	5	**Digital Power** (*Input*) - Positive power for the digital section.
DGND	6	**Digital Ground** (*Input*) - Ground reference for the digital section.
SDOUT (M/$\overline{S}$)	7	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data. This pin must be pulled up or down through a 47-kΩ resistor to select Master or Slave Mode.
VLC	8	**Serial Control Port Power** (*Input*) - Positive power for the Serial Control Port.
M1 M0	9 10	**Mode Selection** (*Input*) - Determines the system sampling frequency range of the device.
I²S/$\overline{LJ}$	11	**Serial Audio Interface Select** *(Input)* - Selects either the Left-Justified or I²S format for the Serial Audio Interface.
MDIV1 MDIV2	12 13	**MCLK Divide** (*Input*) - Configures the device to divide MCLK by 1, 1.5, 2, or 4.
$\overline{RST}$	14	**Reset** (*Input*) - Input for resetting all internal registers to their default settings and for placing the device in a low-power mode.
AINA AINB	15 16	**Analog Input** (*Input*) - Analog inputs to the ADC.
VQ	17	**Quiescent Voltage** (*Output*) - Filter connection for the internal quiescent voltage
FILT+	18	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits.
VA	19	**Analog Power** (*Input*) - Positive power for the analog section.
AGND	20	**Analog Ground** (*Input*) - Ground reference for the analog section.
$\overline{MUTEA}$ $\overline{MUTEB}$	21 24	**Mute Control** *(Output)* - Mute control signal used to control the state of the optional external analog muting circuitry. See Section 5.6 on page 27.
AOUTA AOUTB	22 23	**Analog Audio Output** (*Output*) - Analog outputs for the DAC.

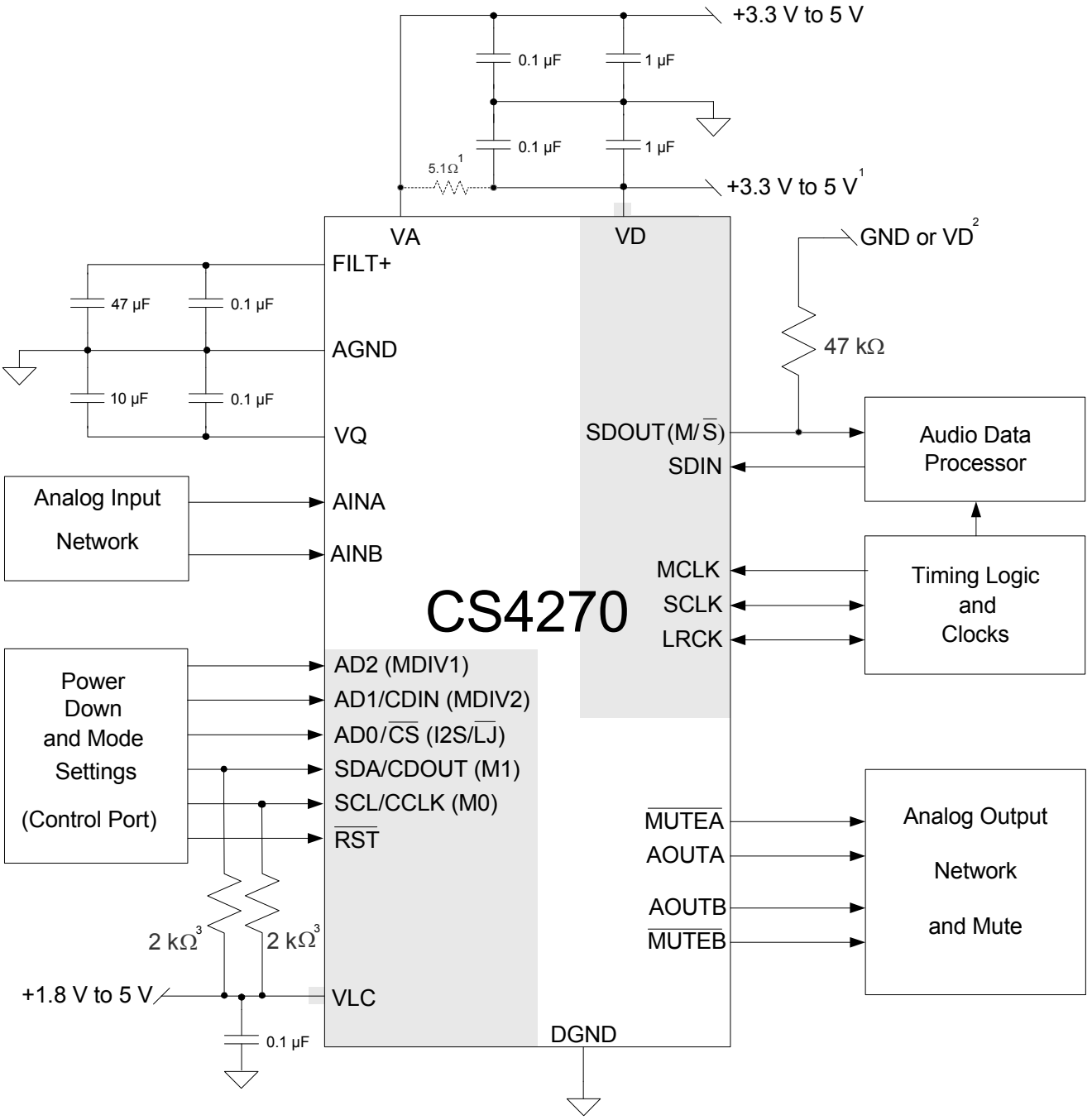
2. DIGITAL I/O PIN CHARACTERISTICS

The level for each input is set by its corresponding power supply and should not exceed the maximum ratings.

Power Supply	Pin Number	Pin Name	I/O	Driver	Receiver
Software Mode					
VLC	9	SDA/CDOUT	Input/Output	1.8 V-5.0 V, Open Drain	1.8 V-5.0 V, with hysteresis
	10	SCL/CCLK	Input	-	1.8 V-5.0 V, with hysteresis
	11	AD0/$\overline{CS}$	Input	-	1.8 V-5.0 V
	12	AD1/CDIN	Input	-	1.8 V-5.0 V
	13	AD2	Input	-	1.8 V-5.0 V
Stand-Alone Mode					
VLC	9	M1	Input	-	1.8 V-5.0 V
	10	M0	Input	-	1.8 V-5.0 V
	11	I²S/$\overline{LJ}$	Input	-	1.8 V-5.0 V
	12	MDIV1	Input	-	1.8 V-5.0 V
	13	MDIV2	Input	-	1.8 V-5.0 V
All Modes					
VD	1	SDIN	Input	-	3.3 V-5.0 V
	2	LRCK	Input/Output	3.3 V-5.0 V, CMOS	3.3 V-5.0 V
	3	MCLK	Input	-	3.3 V-5.0 V
	4	SCLK	Input/Output	3.3 V-5.0 V, CMOS	3.3 V-5.0 V
	7	SDOUT	Output	3.3 V-5.0 V, CMOS	-
VA	14	$\overline{RST}$	Input	-	1.8 V-5.0 V
	21	$\overline{MUTEA}$	Output	3.3 V-5.0 V, CMOS	-
	24	$\overline{MUTEB}$	Output	3.3 V-5.0 V, CMOS	-

Table 1. Digital I/O Pin Power Rails

3. TYPICAL CONNECTION DIAGRAM



1. If using separate supplies for VA and VD, 5.1Ω resistor not needed. See "Grounding and Power Supply Decoupling."

2. In Stand-Alone mode, use a 47 kO pull-down to select Slave Mode or 47 kO pull-up to VD to select Master Mode. See "Master/Slave Mode Selection."

3. Use pull-up resistors in Software Mode. In Stand-Alone Mode, use pull-up or pull-down. See "Mode Selection & De-Emphasis."

Figure 1. CS4270 Typical Connection Diagram

4. CHARACTERISTICS AND SPECIFICATIONS

SPECIFIED OPERATING CONDITIONS

AGND = DGND= 0 V; all voltages with respect to ground.

Parameters		Symbol	Min	Nom	Max	Units
DC Power Supplies:	Analog	VA	3.14	5.0	5.25	V
	Digital	VD	3.14	3.3	5.25	V
	Serial Control Port	VLC	1.71	3.3	5.25	V
Ambient Operating Temperature (Power Applied)		T_A	-40	-	+85	°C

ABSOLUTE MAXIMUM RATINGS

AGND = DGND = 0 V, All voltages with respect to ground.(Note 1)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Analog	VA	-0.3	-	+6.0	V
	Digital	VD	-0.3	-	+6.0	V
	Serial Control Port	VLC	-0.3	-	+6.0	V
Input Current	(Note 2)	I_{in}	-10	-	+10	mA
Analog Input Voltage		V_{IN}	AGND-0.7	-	VA+0.7	V
Digital Input Voltage	Serial Control Port	V_{IND-C}	-0.3	-	VLC+0.3	V
	Digital	V_{IND-D}	-0.3	-	VD+0.3	V
Ambient Operating Temperature (Power Applied)		T_{AC}	-50	-	+95	°C
Storage Temperature		T_{stg}	-65	-	+150	°C

Notes: 1. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

DAC ANALOG CHARACTERISTICS

Test Conditions (unless otherwise specified): VD = VL = 3.3 V, AGND = DGND = 0 V; T_A = +25° C; Full-Scale Output Sine Wave, 997 Hz (Note 3). Decoupling capacitors, filter capacitors, and recommended output filter as shown in Figure 1 on page 7. Fs = 48/96/192 kHz; Synchronous Mode; Test load R_L = 3 kΩ, C_L = 10 pF (see Figure 2). Measurement Bandwidth 10 Hz to 20 kHz.

Parameter			Symbol	VA = 5 V Min	VA = 5 V Typ	VA = 5 V Max	VA = 3.3 V Min	VA = 3.3 V Typ	VA = 3.3 V Max	Unit
Dynamic Range	18 to 24 bit	A-weighted	DR	99	105	-	97	103	-	dB
		unweighted		96	102	-	94	100	-	dB
	16 Bit	A-weighted		90	96	-	90	96	-	dB
		unweighted		87	93	-	87	93	-	dB
Total Harmonic Distortion + Noise										
	18 to 24 bit	0 dB	THD+N	-	-87	-83	-	-83	-79	dB
		-20 dB		-	-82	-	-	-80	-	dB
		-60 dB		-	-42	-	-	-40	-	dB
	16 Bit	0 dB		-	-85	-81	-	-81	-77	dB
		-20 dB		-	-76	-	-	-76	-	dB
		-60 dB		-	-36	-	-	-36	-	dB

DAC Performance across Full VA Range

Parameter		Symbol	Min	Typ	Max	Unit
Interchannel Isolation	(1 kHz)		-	100	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	0.25	dB
Gain Drift			-100	-	+100	ppm/°C
Analog Output						
Full Scale Output Voltage			0.6•VA	0.65•VA	0.7•VA	Vpp
Max DC Current draw from AOUTA or AOUTB		I_{OUTmax}	-	10	-	µA
Max AC-Load Resistance (see Figure 3)		R_L	-	3	-	kΩ
Max Load Capacitance (see Figure 3)		C_L	-	100	-	pF
Output Impedance of AOUTA and AOUTB		Z_{OUT}	-	100	-	Ω

Note: 3. One LSB of triangular PDF dither added to data.

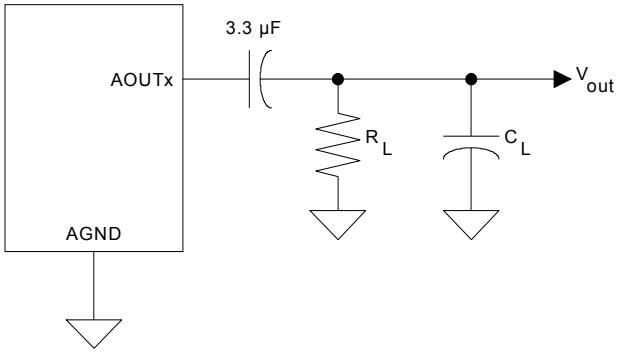


Figure 2. Output Test Load

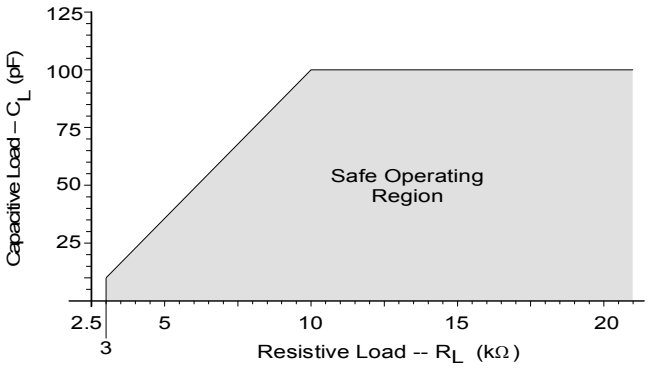


Figure 3. Maximum Loading

DAC COMBINED INTERPOLATION & ANALOG FILTER RESPONSE

The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs. (See Note 4)

Parameter		Symbol	Min	Typ	Max	Unit
Single-Speed Mode						
Passband (Note 5)	to -0.1 dB corner to -3 dB corner		0 0	- -	.35 .4992	Fs Fs
Frequency Response 10 Hz to 20 kHz			-.175	-	+.01	dB
StopBand			.5465	-	-	Fs
StopBand Attenuation	(Note 6)		50	-	-	dB
Group Delay		tgd	-	10/Fs	-	s
De-emphasis Error (Note 8)	Fs = 32 kHz Fs = 44.1 kHz Fs = 48 kHz		- - -	- - -	+1.5/+0 +.05/-.25 -.2/-.4	dB dB dB
Double-Speed Mode						
Passband (Note 5)	to -0.1 dB corner to -3 dB corner		0 0	- -	.22 .501	Fs Fs
Frequency Response 10 Hz to 20 kHz			-.15	-	+.15	dB
StopBand			.5770	-	-	Fs
StopBand Attenuation	(Note 6)		55	-	-	dB
Group Delay		tgd	-	5/Fs	-	s
Quad-Speed Mode						
Passband (Note 5)	to -0.1 dB corner to -3 dB corner		0 0	- -	0.110 0.469	Fs Fs
Frequency Response 10 Hz to 20 kHz			-.12	-	+0	dB
StopBand			0.7	-	-	Fs
StopBand Attenuation	(Note 6)		51	-	-	dB
Group Delay		tgd	-	2.5/Fs	-	s

Notes: 4. Amplitude vs. Frequency plots of this data are available in Section 9. “Filter Plots” on page 38. See Figures 23 through 46.

5. Response is clock dependent and will scale with Fs.

6. For Single-Speed Mode, the Measurement Bandwidth is 0.5465 Fs to 3 Fs.
For Double-Speed Mode, the Measurement Bandwidth is 0.577 Fs to 1.4 Fs.
For Quad-Speed Mode, the Measurement Bandwidth is 0.7 Fs to 1 Fs.

7. De-emphasis is available only in Single-Speed Mode.

ADC ANALOG CHARACTERISTICS

Test Conditions (unless otherwise specified): VD = VL = 3.3 V, DGND = AGND = 0 V; T_A = 25° C; 997 Hz Input Sine Wave. Figure 15 on page 26 shows the test circuit; Fs = 48/96/192 kHz; Synchronous Mode; Measurement Bandwidth 10 Hz to 20 kHz.

Dynamic Performance			**VA = 5 V**			**VA = 3.3 V**			
Single-Speed Mode	Fs = 48 kHz	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Dynamic Range	A-weighted		99	105	-	96	102	-	dB
	unweighted		96	102	-	93	99	-	dB
Total Harmonic Distortion + Noise	(Note 8)								
	-1 dB	THD+N	-	-95	-90	-	-92	-87	dB
	-20 dB		-	-82	-	-	-79	-	dB
	-60 dB		-	-42	-	-	-39	-	dB
Double-Speed Mode	Fs = 96 kHz								
Dynamic Range	A-weighted		99	105	-	96	102	-	dB
	unweighted		96	102	-	93	99	-	dB
	40 kHz bandwidth unweighted		-	99	-	-	96	-	dB
Total Harmonic Distortion + Noise	(Note 8)								
	-1 dB		-	-95	-90	-	-92	-87	dB
	-20 dB	THD+N	-	-82	-	-	-79	-	dB
	-60 dB		-	-42	-	-	-39	-	dB
	40 kHz bandwidth unweighted		-	-93	-	-	-89	-	dB
Quad-Speed Mode	Fs = 192 kHz								
Dynamic Range	A-weighted		99	105	-	96	102	-	dB
	unweighted		96	102	-	93	99	-	dB
	40 kHz bandwidth unweighted		-	99	-	-	96	-	dB
Total Harmonic Distortion + Noise	(Note 8)								
	-1 dB		-	-95	-90	-	-92	-87	dB
	-20 dB	THD+N	-	-82	-	-	-79	-	dB
	-60 dB		-	-42	-	-	-39	-	dB
40 kHz bandwidth	-1 dB		-	-93	-	-	-89	-	dB

Dynamic Performance - All Sampling Speed Modes					
Parameter		**Min**	**Typ**	**Max**	**Unit**
Interchannel Isolation		-	100	-	dB
DC Accuracy					
Interchannel Gain Mismatch		-	0.1	-	dB
Gain Error		-3	-	+3	%
Gain Drift		-	±100	-	ppm/°C
Analog Input Characteristics					
Full-Scale Input Voltage		0.53*VA	0.56*VA	0.58*VA	Vpp
Input Impedance		-	300	-	kΩ

Note: 8. Referred to the typical full-scale input voltage.

ADC DIGITAL FILTER CHARACTERISTICS

Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. (Note 9)

Parameter			Symbol	Min	Typ	Max	Unit
Single-Speed Mode							
Passband	(-0.1 dB)	(Note 10)		0	-	0.49	Fs
Passband Ripple				-	-	0.035	dB
Stopband		(Note 10)		0.57	-	-	Fs
Stopband Attenuation				70	-	-	dB
Group Delay			t_{gd}	-	12/Fs	-	s
Double-Speed Mode							
Passband	(-0.1 dB)	(Note 10)		0	-	0.49	Fs
Passband Ripple				-	-	0.05	dB
Stopband		(Note 10)		0.56	-	-	Fs
Stopband Attenuation				69	-	-	dB
Group Delay			t_{gd}	-	9/Fs	-	s
Quad-Speed Mode							
Passband	(-0.1 dB)	(Note 10)		0	-	0.26	Fs
Passband Ripple				-	-	0.05	dB
Stopband		(Note 10)		0.50	-	-	Fs
Stopband Attenuation				60	-	-	dB
Group Delay			t_{gd}	-	5/Fs	-	s
High-Pass Filter Characteristics							
Frequency Response	-3.0 dB -0.13 dB	(Note 11)		- -	1 20	- -	Hz Hz
Phase Deviation	@ 20 Hz	(Note 11)		-	10	-	deg
Passband Ripple				-	-	0	dB

Notes: 9. Plots of this data are contained in Section 9. “Filter Plots” on page 38. See Figures 23 through 46.

10. The filter frequency response scales precisely with Fs.

11. Response shown is for Fs equal to 48 kHz. Filter characteristics scale with Fs.

DC ELECTRICAL CHARACTERISTICS

T_A = 25° C; AGND = DGND = 0 V, all voltages with respect to 0 V; MCLK = 12.288 MHz; Master Mode).

Parameter		Symbol	Min	Typ	Max	Unit
Power Supply						
Power Supply Current	VA = 5 V	I_A	-	37	42	mA
(Normal Operation)	VA = 3.3 V	I_A	-	24	30	mA
	VD, VLC = 5 V	I_D	-	32	38	mA
	VD, VLC = 3.3 V	I_D	-	13	20	mA
Power Supply Current	VA = 5 V	I_A	-	70	-	µA
(Power-Down Mode) (Note 12)	VD, VLC = 5 V	I_D	-	3	-	µA
Power Consumption						
VA = 5 V, VD = VLC= 3.3 V	Normal Operation	-	-	224	270	mW
VA = 5 V, VD = VLC = 5 V	Normal Operation	-	-	345	400	mW
	Power-Down Mode (Note 12)	-	-	365	-	µW
Power Supply Rejection Ratio(1 kHz)	(Note 13)	PSRR	-	55	-	dB
Common Mode Voltage						
Nominal Common Mode Voltage		VQ	-	VA/2	-	VDC
Maximum DC Current Source/Sink from VQ			-	1	-	µA
VQ Output Impedance			-	25	-	kΩ
Positive Voltage Reference						
FILT+ Nominal Voltage		FILT+	-	VA	-	VDC
Maximum DC Current Source/Sink from FILT+			-	10	-	µA
FILT+ Output Impedance			-	10	-	kΩ
Mute Control						
Maximum MUTEA & MUTEB Drive Current			-	3	-	mA

Notes: 12. Power Down Mode is defined as $\overline{RST}$ = Low with all clocks and data lines held static.

13. Valid with the recommended capacitor values on FILT+ and VQ as shown in the Typical Connection Diagram.

DIGITAL SWITCHING CHARACTERISTICS

Parameter (Note 14)		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	Serial Audio Interface	V_{IH}	0.7xVD	-	-	V
	Serial Control Port		0.7xVLC	-	-	V
Low-Level Input Voltage	Serial Audio Interface	V_{IL}	-	-	0.2xVD	V
	Serial Control Port		-	-	0.2xVLC	V
High-Level Output Voltage at I_o = 2 mA	Serial Audio Interface	V_{OH}	VD - 1.0	-	-	V
	Serial Control Port		VLC - 1.0	-	-	V
	$\overline{MUTEA}$, $\overline{MUTEB}$		VA - 1.0	-	-	V
Low-Level Output Voltage at I_o = 2 mA		V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-10	-	10	µA

Notes: 14. Serial Audio Port signals include: SCLK, LRCK, SDOUT, SDIN
Serial Control Port signals include: SDA/CDOUT, SCL/CCLK, AD1/CDIN, AD0/$\overline{CS}$, $\overline{RST}$

SWITCHING CHARACTERISTICS - SERIAL AUDIO INTERFACE

Logic "0" = DGND = AGND = 0 V; Logic "1" = VD, C_L = 20 pF.

Parameter	Symbol	Min	Typ	Max	Unit
Sample Rate Single-Speed Mode	Fs	4	-	54	kHz
Double-Speed Mode	Fs	50	-	108	kHz
Quad-Speed Mode	Fs	100	-	216	kHz
MCLK Specifications					
MCLK Frequency Stand-Alone Mode	fmclk	1.024	-	55.296	MHz
(Note 15) Serial Control Port Mode	fmclk	1.024	-	55.296	MHz
MCLK Duty Cycle		40	50	60	ns
Master Mode					
LRCK Duty Cycle		-	50	-	%
SCLK Period (Note 16)	t_{sclkw}	-	$\frac{1}{(64)Fs}$	-	s
SCLK Duty Cycle		-	50	-	%
SCLK falling to LRCK edge	t_{mslr}	-20	-	20	ns
SCLK falling to SDOUT valid	t_{sdo}	-	-	32	ns
SDIN valid to SCLK rising setup time	t_{sdis}	16	-	-	ns
SCLK rising to SDIN hold time	t_{sdih}	20	-	-	ns
Slave Mode					
LRCK Duty Cycle		40	50	60	%
SCLK Period (Note 15) Single-Speed Mode	t_{sclkw}	$\frac{1}{(128)Fs}$	-	-	s
Double-Speed Mode	t_{sclkw}	$\frac{1}{(64)Fs}$	-	-	s
Quad-Speed Mode	t_{sclkw}	$\frac{1}{(64)Fs}$	-	-	s
SCLK Duty Cycle		45	50	55	ns
SCLK falling to LRCK edge	t_{slrd}	-20	-	20	ns
SDOUT valid before SCLK rising	t_{stp}	10	-	-	ns
SDOUT valid after SCLK rising	t_{hld}	5	-	-	ns
SDIN valid to SCLK rising setup time	t_{sdis}	16	-	-	ns
SCLK rising to SDIN hold time	t_{sdih}	20	-	-	ns

Notes: 15. In Control Port Mode, MCLK Frequency, and Functional Mode Select bits must be configured according to Table 7 on page 22, Table 9 on page 33, and Table 13 on page 35.

16. $t_{sclkw} = t_{sclkh} + t_{sclkl}$ in Figures 5 and 7.

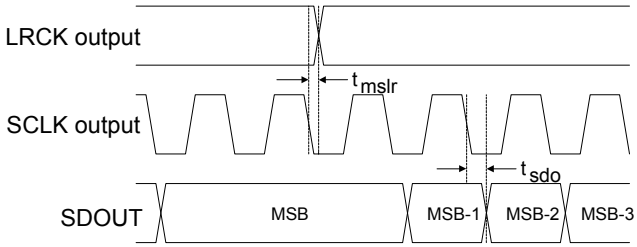


Figure 4. Master Mode, Left-Justified SAI

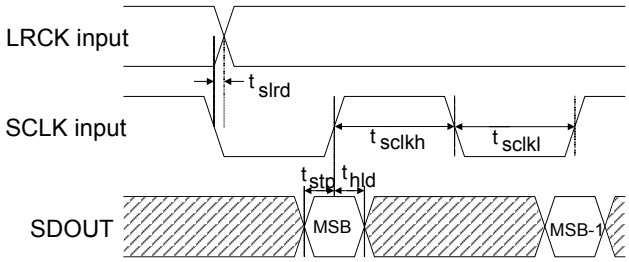


Figure 5. Slave Mode, Left-Justified SAI

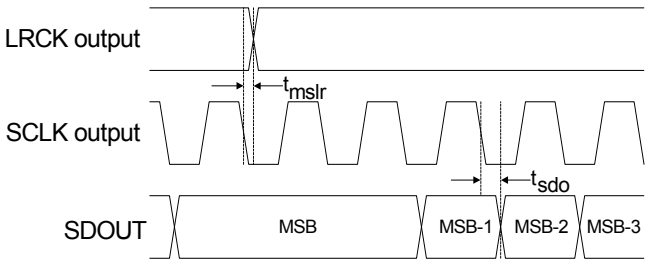


Figure 6. Master Mode, I²S SAI

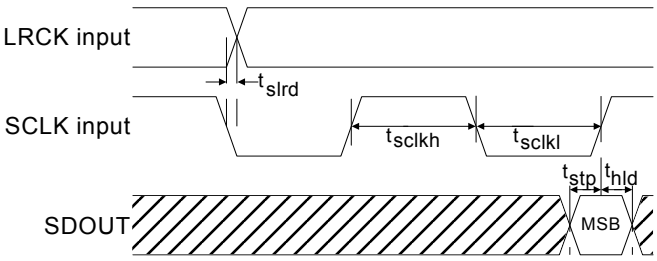


Figure 7. Slave Mode, I²S SAI

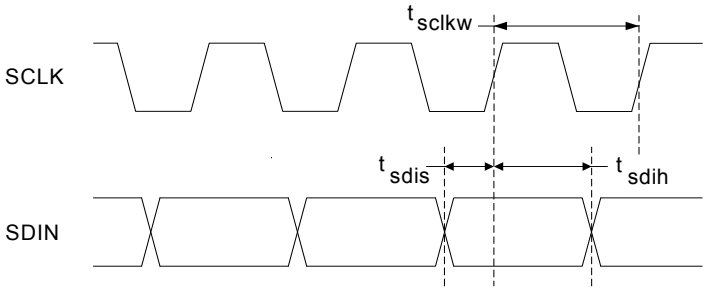


Figure 8. Master and Slave Mode, SCLK/SDIN

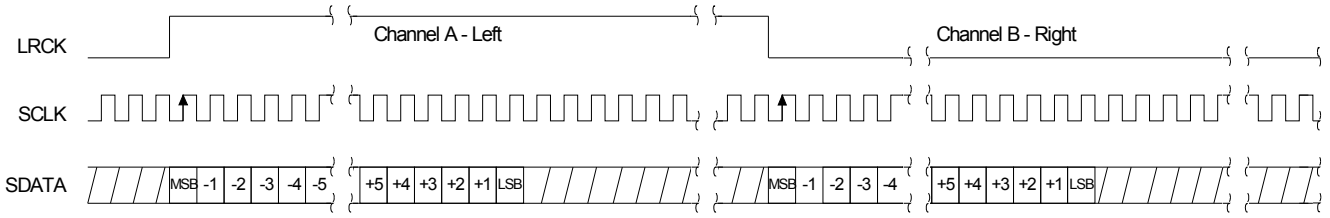


Figure 9. Format 0, Left-Justified up to 24-Bit Data

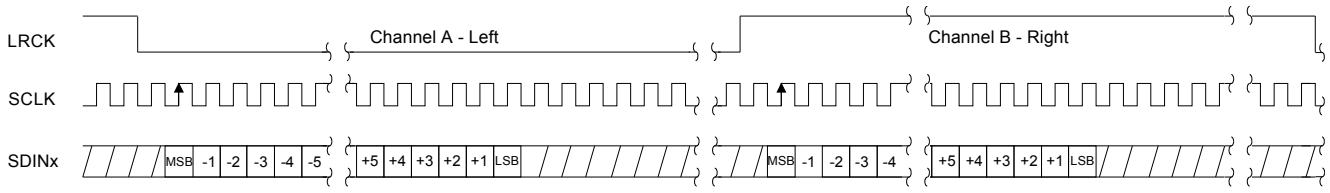


Figure 10. Format 1, I²S up to 24-Bit Data

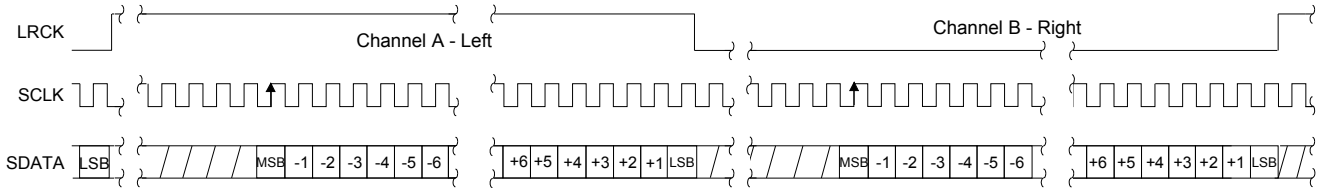


Figure 11. Format 2 or 3, Right-Justified 16-Bit or 24-Bit Data (Serial Control Port Mode Only)

SWITCHING CHARACTERISTICS - SOFTWARE MODE - I²C FORMAT

Inputs: Logic '0' = AGND = DGND = 0 V, Logic '1' = VLC, C_L = 30 pF

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{RST}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 17)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}	-	1	µs
Fall Time SCL and SDA	t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns

Note: 17. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

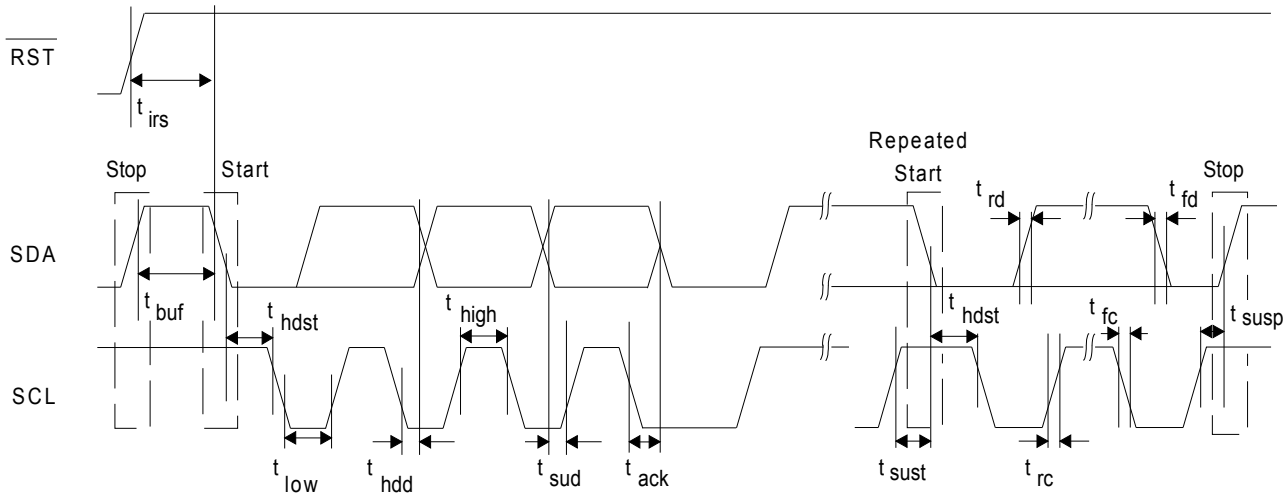


Figure 12. Software Mode Timing - I²C Format

SWITCHING CHARACTERISTICS - SOFTWARE MODE - SPI FORMAT

Inputs: Logic '0' = AGND = DGND = 0 V; Logic '1' = VLC; C_L = 20 pF.

Parameter	Symbol	Min	Max	Unit
CCLK Clock Frequency	f_{sclk}	-	6	MHz
$\overline{RST}$ Rising Edge to $\overline{CS}$ Falling	t_{srs}	500	-	ns
CCLK Edge to $\overline{CS}$ Falling (Note 18)	t_{spi}	500	-	ns
$\overline{CS}$ High Time Between Transmissions	t_{csh}	1.0	-	µs
$\overline{CS}$ Falling to CCLK Edge	t_{css}	20	-	ns
CCLK Low Time	t_{scl}	66	-	ns
CCLK High Time	t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time	t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time (Note 19)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN (Note 20)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN (Note 20)	t_{f2}	-	100	ns
Transition Time from CCLK to CDOUT Valid (Note 21)	t_{scdov}	-	100	ns
Time from $\overline{CS}$ rising to CDOUT High-Z	t_{cscdo}	-	100	ns

Notes: 18. t_{spi} only needed before first falling edge of $\overline{CS}$ after $\overline{RST}$ rising edge. t_{spi} = 0 at all other times.

19. Data must be held for sufficient time to bridge the transition time of CCLK.

20. For F_{SCK} < 1 MHz.

21. CDOUT should not be sampled during this time.

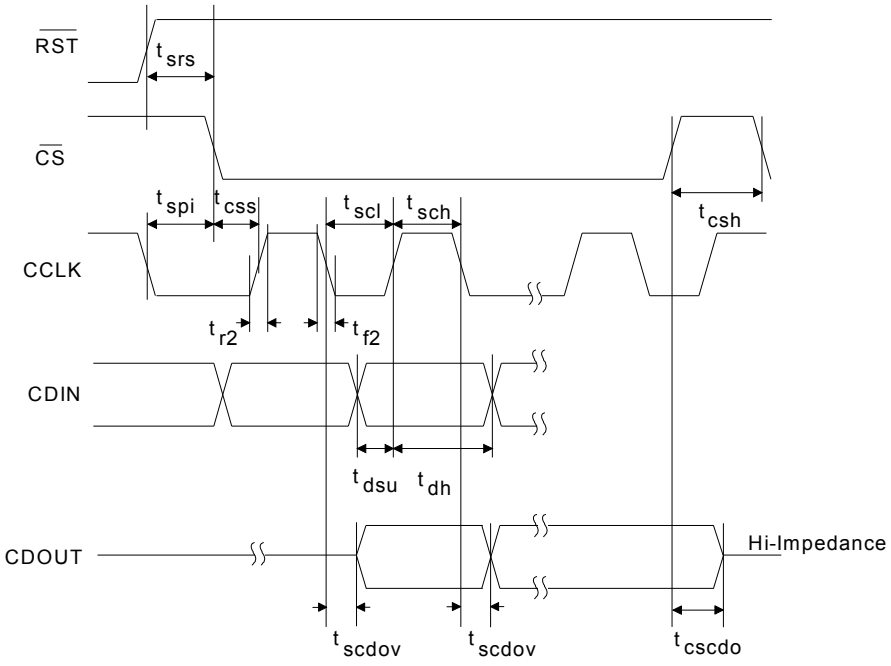


Figure 13. SPI Control Port Timing

5. APPLICATIONS

5.1 Stand-Alone Mode

5.1.1 Access to Stand-Alone Mode

Reliable power-up is achieved by keeping the device in reset until the power supplies, clocks and configuration pins are stable. It is also recommended that $\overline{RST}$ be asserted if the analog or digital supplies drop below the minimum specified operating voltages to prevent power glitch related issues.

The delay time from the release of reset until the device enters Stand-Alone Mode is 1,045 sample periods. Table 2 lists the approximate wait time for each sampling mode.

Speed Mode	Approximate Delay Time
Single-Speed	21.8 ms (48 kHz)
Double-Speed	10.9 ms (96 kHz)
Quad-Speed	5.4 ms (192 kHz)

Table 2. Approximate Delay Time from Release of $\overline{RST}$ to Entering Standalone Mode

5.1.2 Access to Master/Slave Mode

The CS4270 supports operation in either Master Mode or Slave Mode.

In Master Mode, LRCK and SCLK are outputs and are synchronously generated by the device. The LRCK frequency is equal to Fs and the SCLK frequency is equal to 64x Fs.

In Slave Mode, LRCK and SCLK are inputs, requiring external generation that is synchronous to MCLK. SCLK must be 48x or 64x Fs to maximize system performance.

In Stand-Alone Mode, the CS4270 enters Slave Mode when SDOUT (M/$\overline{S}$) is pulled low through a 47 kΩ resistor. Master Mode is accessed by placing a 47 kΩ pull-up to VD on the SDOUT (M/$\overline{S}$) pin.

Configuration of clock ratios in each of these modes is outlined in Table 4.

5.1.3 System Clocking

The CS4270 operates at sampling frequencies from 4 kHz to 216 kHz. This range is divided into three speed modes, as shown in Table 3.

Mode	Sampling Frequency
Single-Speed	4-54 kHz
Double-Speed	50-108 kHz
Quad-Speed	100-216 kHz

Table 3. Speed Modes

5.1.4 Clock Ratio Selection

Depending on whether the CS4270 is in Master or Slave Mode, different MCLK/LRCK and SCLK/LRCK ratios may be used. These ratios are shown in the Table 4. '0' = DGND, '1' = VLC.

Master Mode					
	MCLK/LRCK	SCLK/LRCK	LRCK	MDIV2	MDIV1
Single-Speed	256	64	Fs	0	0
	384 (Note 22)	64	Fs	0	1
	512	64	Fs	1	0
	1,024	64	Fs	1	1
Double-Speed	128	64	Fs	0	0
	192 (Note 22)	64	Fs	0	1
	256	64	Fs	1	0
	512	64	Fs	1	1
Quad-Speed	64	64	Fs	0	0
	96 (Note 22)	64	Fs	0	1
	128	64	Fs	1	0
	256	64	Fs	1	1
Slave Mode					
	MCLK/LRCK	SCLK/LRCK	LRCK	MDIV2	MDIV1
Single-Speed	256	32, 48, 64, 128	Fs	0	0
	384 (Note 22)	32, 48, 64, 96	Fs	0	1
	512	32, 48, 64, 128	Fs	1	0
	1,024	32, 48, 64, 96	Fs	1	1
Double-Speed	128	32, 48, 64	Fs	0	0
	192 (Note 22)	32, 48, 64	Fs	0	1
	256	32, 48, 64	Fs	1	0
	512	32, 48, 64	Fs	1	1
Quad-Speed	64	32, 48, 64	Fs	0	0
	96 (Note 22)	32, 48, 64	Fs	0	1
	128	32, 48, 64	Fs	1	0
	256	32, 48, 64	Fs	1	1

Table 4. Clock Ratios - Stand-Alone Mode

Note: 22. Once the MDIVx pins have been configured for this setting, $\overline{\text{RST}}$ must be asserted and then deasserted before normal operation can begin. During startup, $\overline{\text{RST}}$ should remain asserted until after this selection is made and then deasserted.

5.1.5 Interpolation Filter

In Stand-Alone Mode, the fast roll-off interpolation filter is used. Filter specifications can be found in Section 4. Plots of the data are contained in Section 9. "Filter Plots" on page 38.

5.1.6 High-Pass Filter

At the system level, the input circuitry driving the CS4270 may generate a small DC offset into the ADC. The CS4270 includes one high-pass filter per channel after the decimator to remove any DC offset, which

could result in recording a DC level, possibly yielding "clicks" when switching between devices in a multi-channel system. In Stand-Alone Mode, the high-pass filter is always active and continuously subtracts a measure of the DC offset from the output of the decimation filter.

5.1.7 Mode Selection & De-Emphasis

The sample rate, Fs, can be adjusted from 4 kHz to 216 kHz and De-emphasis, optimized for 44.1 kHz, is available in Single-Speed Mode. In Stand-Alone Master Mode, the CS4270 must be set to the proper mode via the mode pins, M1 and M0. In Slave Mode, the CS4270 auto-detects Speed Mode and the M0 pin becomes De-emphasis select. Stand-alone definitions of the mode pins in Master Mode are shown in Table 5.

Mode 1	Mode 0	Mode	Sample Rate (Fs)	De-Emphasis
0	0	Single-Speed	4 kHz - 54 kHz	Off
0	1	Single-Speed	4 kHz - 54 kHz	44.1 kHz
1	0	Double-Speed	50 kHz - 108 kHz	Off
1	1	Quad-Speed	100 kHz - 216 kHz	Off

Table 5. CS4270 Stand-Alone Mode Control

5.1.8 Access to Serial Audio Interface Format

Either I²S or Left-Justified serial audio data format may be selected in Stand-Alone Mode. To use the I^2S format, tie the I²S/$\overline{LJ}$ pin to VLC during power up. To use $\overline{LJ}$ format, tie I²S/$\overline{LJ}$ to DGND during power up.

5.2 Serial Control Port Mode

5.2.1 Access to Serial Control Port Mode

Reliable power-up is achieved by keeping the device in reset until the power supplies, clocks, and configuration pins are stable. It is also recommended that $\overline{RST}$ be asserted if the analog or digital supplies drop below the minimum specified operating voltages to prevent power glitch related issues.

After $\overline{RST}$ is released, the device is put into Serial Control Port Mode by setting the power down bit through a SPI or I²C transaction, as described in Section 6.1 and Section 6.2.

If the transaction is not completed within 1,045 sample periods after the release of reset, the device enters Stand-Alone Mode.

If the first Serial Control Port transaction is ongoing while the device is executing pop control, there is a chance of generating audio transients. The details of the duration of pop control is outlined in Section 5.3.1 “Power-Up” on page 24.

When the device is Serial Control Port Mode, it can be programmed as desired. After clearing the power-down bit, desired device functioning can start.

5.2.2 Access to Master/Slave Mode

The CS4270 supports operation in either Master Mode or Slave Mode.

- In Master Mode, LRCK and SCLK are outputs and are synchronously generated by the device. LRCK is equal to Fs and SCLK is equal to 64x Fs.
- In Slave Mode, LRCK and SCLK are inputs, requiring external generation that is synchronous to MCLK. It is recommended that SCLK be 48x or 64x Fs to maximize system performance.

Clock-ratio configuration for each mode is outlined in the Table 11 on page 34 and Table 10 on page 33.

In Serial Control Port Mode, the CS4270 defaults to Slave Mode. The user may change this default setting by changing the status of the FM bits in the Mode Control Register (03h).

5.2.3 System Clocking

The CS4270 operates at sampling frequencies from 4 kHz to 216 kHz. This range is divided into three speed modes as shown in Table 6.

Mode	Sampling Frequency
Single-Speed	4-54 kHz
Double-Speed	50-108 kHz
Quad-Speed	100-216 kHz

Table 6. Speed Modes

5.2.4 Clock Ratio Selection

In Serial Control Port Master Mode, the user must configure the mode bits (MCLK_FREQ[2:0]) to set the speed mode and select the appropriate clock ratios. Changes to these bits should only be done while the PDN bit is set. Depending on whether the CS4270 is in Master or Slave Mode, different MCLK/LRCK and SCLK/LRCK ratios may be used. These ratios as well as the Serial Control Port Register Bits are shown in Table 7, Table 10 on page 33, and Section 8.3 on page 33. '0' = DGND, '1' = VLC.

Master Mode						
Speed Mode	MCLK/LRCK	SCLK/LRCK	LRCK	MCLK_FREQ2	MCLK_FREQ1	MCLK_FREQ0
Single-Speed	256	64	Fs	0	0	0
	384	64	Fs	0	0	1
	512	64	Fs	0	1	0
	768	64	Fs	0	1	1
	1,024	64	Fs	1	0	0
Double-Speed	128	64	Fs	0	0	0
	192	64	Fs	0	0	1
	256	64	Fs	0	1	0
	384	64	Fs	0	1	1
	512	64	Fs	1	0	0
Quad-Speed	64	64	Fs	0	0	0
	96	64	Fs	0	0	1
	128	64	Fs	0	1	0
	192	64	Fs	0	1	1
	256	64	Fs	1	0	0

Table 7. Clock Ratios - Serial Control Port Mode

Slave Mode						
Speed Mode	MCLK/LRCK	SCLK/LRCK	LRCK	MCLK_FREQ2	MCLK_FREQ1	MCLK_FREQ0
Single-Speed	256	32, 48, 64, 128	Fs	0	0	0
	384	32, 48, 64, 96, 128	Fs	0	0	1
	512	32, 48, 64, 128	Fs	0	1	0
	768	32, 48, 64, 96, 128	Fs	0	1	1
	1,024	32, 48, 64, 96, 128	Fs	1	0	0
Double-Speed	128	32, 48, 64	Fs	0	0	0
	192	32, 48, 64	Fs	0	0	1
	256	32, 48, 64	Fs	0	1	0
	384	32, 48, 64	Fs	0	1	1
	512	32, 48, 64	Fs	1	0	0
Quad-Speed	64	32, 48, 64	Fs	0	0	0
	96	32, 48, 64	Fs	0	0	1
	128	32, 48, 64	Fs	0	1	0
	192	32, 48, 64	Fs	0	1	1
	256	32, 48, 64	Fs	1	0	0

Table 7. Clock Ratios - Serial Control Port Mode (Continued)

5.2.5 Internal Digital Loopback

In Serial Control Port Mode, the CS4270 supports an internal digital loopback mode in which the output of the ADC is routed to the input of the DAC. This mode may be activated by setting the DIG_LOOPBK bit in the ADC and DAC Control register (04h).

When this bit is set, the CS4270 ignores the status of the DAC_DIF(4:3) bits in register 04h. Any changes made to the DAC_DIF(4:3) bits while the DIG_LOOPBK bit is set will have no impact on operation until the DIG_LOOPBK bit is released, at which time the Digital Interface Format of the DAC will operate according to the format selected in the DAC_DIF(4:3) bits. While the DIG_LOOPBK bit is set, data will be present on the SDOUT pin in the format selected in the ADC_DIF(0) bit in register 04h.

5.2.6 Auto-Mute

The Auto-Mute function is controlled by the status of the Auto Mute bit in the Mute register. When set, the DAC output will mute following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. Detection and muting are done independently for each channel. The common mode on the output will be retained and the Mute Control pin for that channel will become active during the mute period. The muting function is affected, similar to volume control changes, by the Soft and Zero Cross bits in the Transition and Control register. The Auto Mute bit is set by default.

5.2.7 DC Offset Calibration Using the High-Pass Filter

At the system level, the input circuitry driving the CS4270 may generate a small DC offset level into the A/D converter which could result in possibly yielding "clicks" when switching between devices in a multi-channel system. The CS4270 includes one high-pass filter per channel (see “ADC High Pass Filter Freeze for CH A (Bit 7)” on page 34 and “ADC High Pass Filter Freeze for CH A (Bit 7)” on page 34) to alleviate this system problem.

Running the CS4270 with the high-pass filter enabled, then freezing the stored DC offset value eliminates offsets anywhere in the signal path between the calibration point and the CS4270.

5.2.8 Oversampling Modes

The CS4270 operates in one of three oversampling modes based on the input sample rate. Mode selection is determined by the FM bits in the Mode Control Register (03h). Single-Speed Mode supports input sample rates from 4 to 54 kHz and uses a 128x oversampling ratio. Double-Speed Mode supports input sample rates from 50 to 108 kHz and uses an oversampling ratio of 64x. Quad-Speed Mode supports input sample rates from 100 to 216 kHz and uses an oversampling ratio of 32x. See Table 7 on page 22.

5.3 Popguard Transient Control

The CS4270 uses a novel technique to minimize the effects of output transients during power-up and power-down. This technology, when used with external DC-blocking capacitors in series with the audio outputs, minimizes the audio transients commonly produced by single-ended single-supply converters. The Popguard Transient Control is activated inside the DAC when $\overline{\text{RST}}$ is toggled and requires no other external control, aside from choosing the appropriate DC-blocking capacitor. See Section 8.3.3 for information about configuration.

5.3.1 Power-Up

When the device is initially powered-up, the audio outputs, AOUTA and AOUTB, are clamped to AGND.Following a delay of 1,045 sample periods, each output begins to ramp toward the quiescent voltage. Approximately 0.4 seconds later, the outputs reach VQ and audio output begins.This gradual voltage ramping allows time for the external DC-blocking capacitors to charge to the quiescent voltage, minimizing audible power-up transients.

5.3.2 Power-Down

To prevent audible transients at power-down, the device must first enter its power-down state. When this occurs, audio output ceases and the internal output buffers are disconnected from AOUTA and AOUTB. In their place, a soft-start current sink is substituted which allows the DC-blocking capacitors to slowly discharge. Once this charge is dissipated, the power to the device may be turned off and the system is ready for the next power-on.

5.3.3 Discharge Time

To prevent an audio transient at the next power-on, the DC-blocking capacitors must fully discharge before turning on the power or exiting the power-down state. If full discharge does not occur, a transient will occur when the audio outputs are initially clamped to AGND. The time that the device must remain in the power-down state is related to the value of the DC-blocking capacitance and the output load. For example, with a 3.3 μF capacitor, the minimum power-down time will be approximately 0.4 seconds.

5.4 De-Emphasis Filter (Single-Speed Mode Only)

The CS4270 includes a digital de-emphasis filter. Figure 14 shows the de-emphasis curve for Fs equal to 44.1 kHz. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs. Please see Section 5.1.7 for the desired de-emphasis control for Stand-Alone Mode and Section 5.2 for Serial Control Port Mode.

The de-emphasis feature is included to accommodate audio recordings that use 50/15 μs pre-emphasis equalization as a means of noise reduction.

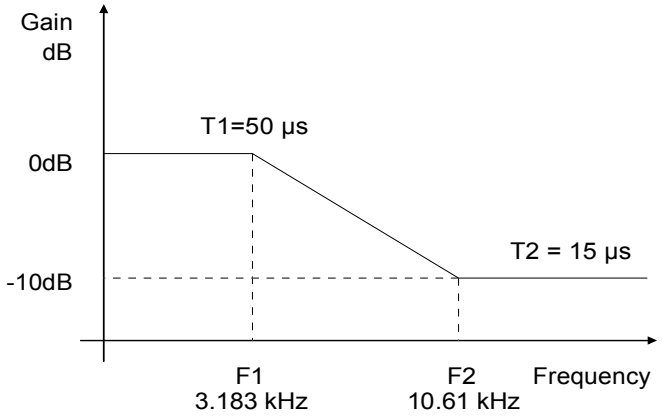


Figure 14. De-Emphasis Curve

5.5 Analog Connections

The analog modulator samples the input at 6.144 MHz for Fs = 48, 96, and 128 kHz and scales proportionally for all other sampling speeds.The digital filter rejects signals within the stopband of the filter. However, there is no rejection for input signals that are multiples of the input sampling frequency (e.g., n × 6.144 MHz), where n = 0, 1, 2, ... Figure 15 shows the recommended topology of the analog input network. The capacitor values are chosen not only provide the appropriate filtering of noise at the modulator sampling frequency, but to act as a charge source for the internal sampling circuits. The use of capacitors with a large voltage coefficient (such as general-purpose ceramics) can degrade signal linearity.

5.5.1 Input Component Values

Table 8 shows the three parameters (source impedance, attenuation, and input impedance) that determine the values of resistors R1 and R2, as seen in Figure 15, and shows the design equations used to determine these values.

Parameter	Equation
Source Impedance: The impedance as seen from the ADC looking back into the signal network. The ADC achieves optimal THD+N performance when source impedance less than or equal to 1.0 kΩ. See Figure 16 and 17.	$\frac{(R1 \times R2)}{R1 + R2}$
Attenuation: The required attenuation factor depends on the magnitude of the input signal. For VA = 5 V, the full-scale input voltage equals 0.56*VA (1 Vrms). See ADC Analog Characteristics on page 11. The user should select values for R1 and R2 such that the magnitude of the incoming signal multiplied by the attenuation factor is less than or equal to the full-scale input voltage of the device.	$\frac{(R2)}{(R1 + R2)}$
Input Impedance: Input impedance is the impedance from the signal source to the ADC analog input pins. Table 8 shows the input parameters and the associated design equations.	$(R1 + R2)$

Table 8. Analog Input Design Parameters

Figure 15 illustrates an example configuration using two 2-kΩ resistors in place of R1 and R2. This circuit will attenuate a typical line level voltage, 2 Vrms, to the full-scale input of the ADC, 0.56*VA (1 Vrms) when VA = 5 V.

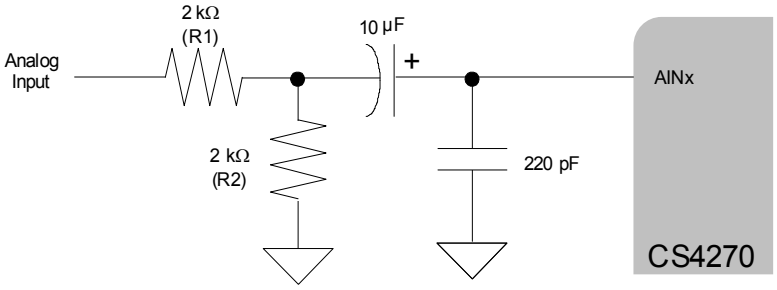


Figure 15. CS4270 Example Analog Input Network

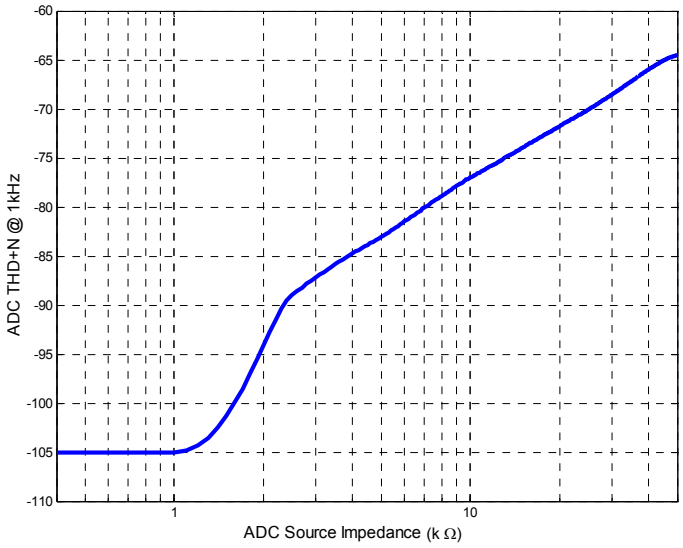


Figure 16. A/D THD+N Performance vs. Input Source Impedance

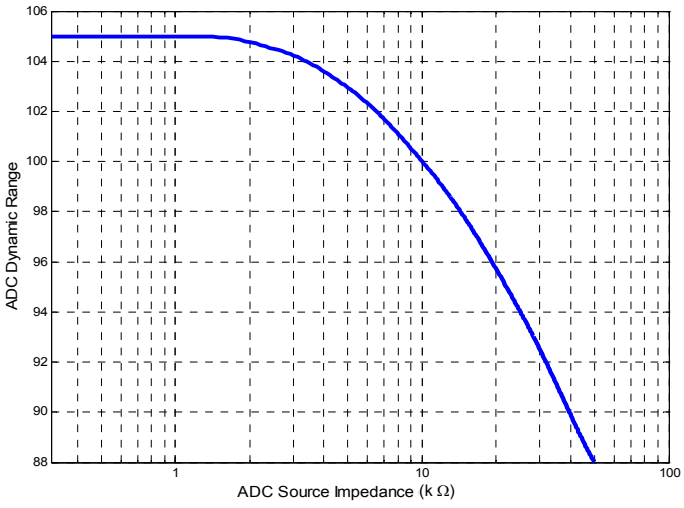


Figure 17. A/D Dynamic Range vs. Input Source Impedance

5.5.2 Output Connections

The analog output filter present in the CS4270 is a switched-capacitor low pass filter. Its response, combined with that of the digital interpolator, is given in Figures 23 - 46. The recommended external analog circuitry is shown in Figure 18.

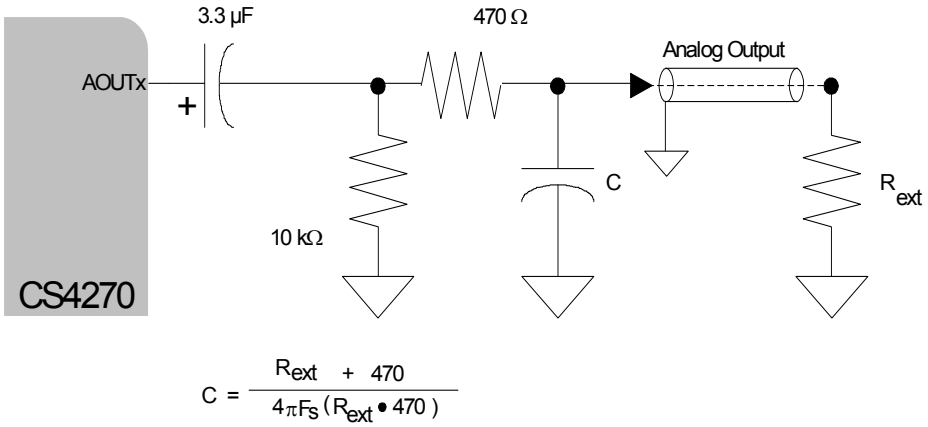


Figure 18. CS4270 Recommended Analog Output Filter

5.6 Mute Control

The Mute Control pins become active during power-up initialization, reset, muting, when the MCLK to LRCK ratio is incorrect, and during power-down. The MUTE pins are intended to be used as control for an external mute circuit in order to add device mute capability.

The CS4270 also features Auto-Mute, which is enabled by default. The Auto-Mute function causes the MUTE pin corresponding to an individual channel to activate following the reception of 8192 consecutive static-level audio samples on the respective channel. A single transition of data on the channel will cause the corresponding MUTE pin to deactivate.

Use of the Mute Control function is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute Control function can enable the system designer to achieve idle channel noise/signal-to-noise ratios which are only limited by the external mute circuit. The MUTE pins are active-low. See Figure 19 for a suggested active-low mute circuit.

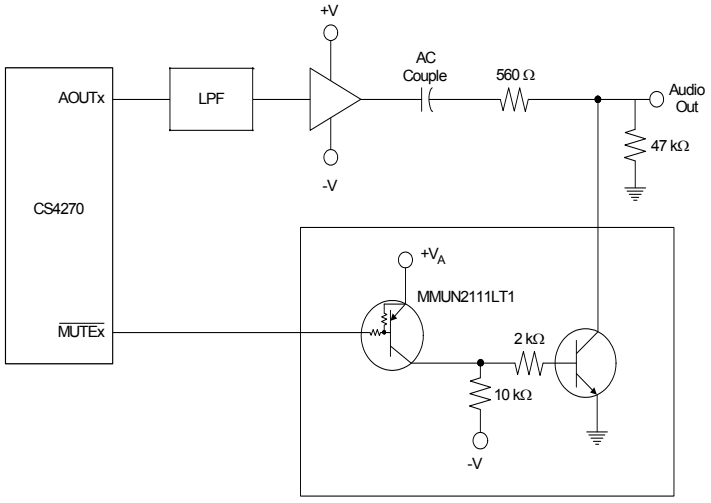


Figure 19. Suggested Active-Low Mute Circuit

5.7 Synchronization of Multiple Devices

In systems where multiple ADCs are required, care must be taken to achieve simultaneous sampling. To ensure synchronous sampling, the MCLK and LRCK must be the same for all of the CS4270s in the system. If only one MCLK source is needed, one solution is to place one CS4270 in Master Mode, and slave all of the other CS4270s to the one master. If multiple MCLK sources are needed, a possible solution would be to supply all clocks from the same external source and time the CS4270 reset with the inactive edge of MCLK. This will ensure that all converters begin sampling on the same clock edge.

5.8 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS4270 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 on page 7 shows the recommended power arrangements, with VA, VD and VLC connected to clean supplies. VD, which powers the digital filter, may be run from the system digital supply or may be powered from the analog supply via a resistor. In the latter case, no additional devices should be powered from VD. See Figure 1 on page 7 for an example. Power supply decoupling capacitors should be as near to the CS4270 as possible, with the low value ceramic capacitor being the nearest. All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The FILT+ and VQ decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path to AGND. The CDB4270 evaluation board demonstrates the optimum layout and power supply arrangements. To minimize digital noise, connect the CS4270 digital outputs only to CMOS inputs.

6. SOFTWARE MODE

6.1 Software Mode - I²C Control Port

Software Mode is used to access the registers, allowing the CS4270 to be configured for the desired operational modes and formats. The operation in Software Mode may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the I²C pins should remain static if no operation is required. Software Mode supports the I²C interface, with the CS4270 acting as a slave device.

SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL. Pin AD0 forms the least significant bit of the chip address and should be connected through a resistor to VL or GND as desired. The state of the pin is sensed while the CS4270 is being reset.

The signal timings for a read and write cycle are shown in Figure 20 and Figure 21. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS4270 after a Start condition consists of a 7-bit chip address field and a R/$\overline{W}$ bit (high for a read, low for a write). The upper 5 bits of the 7-bit address field are fixed at 10011. To communicate with a CS4270, the chip address field, which is the first byte sent to the CS4270, should match 10011 followed by the settings of AD0. The eighth bit of the address is the R/$\overline{W}$ bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS4270 after each input byte is read, and is input to the CS4270 from the microcontroller after each transmitted byte.

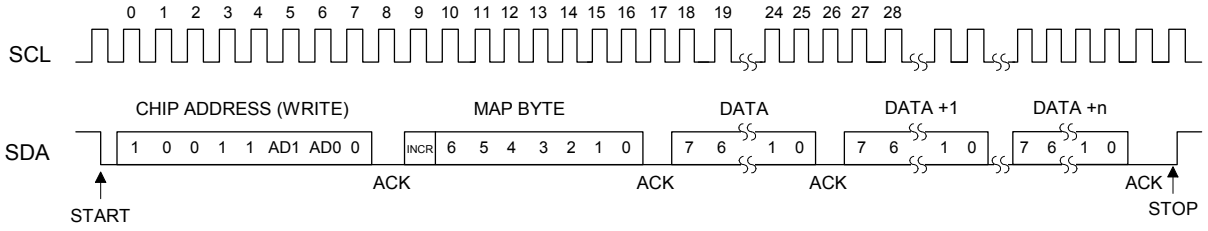


Figure 20. Software Mode Timing, I²C Write

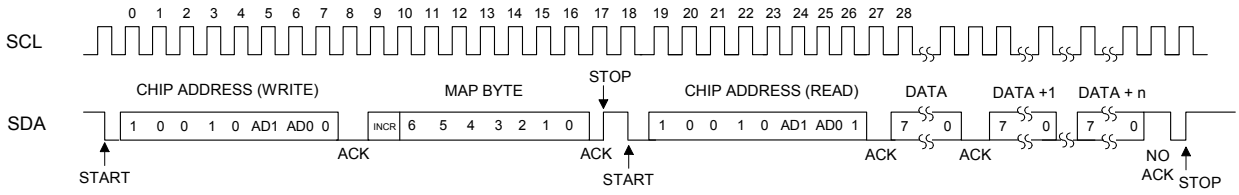


Figure 21. Software Mode Timing, I²C Read

Since the read operation can not set the MAP, an aborted write operation is used as a preamble. As shown in Figure 21, the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

```
Send start condition.
Send 10011xx0 (chip address & write operation).
Receive acknowledge bit.
Send MAP byte, auto increment off.
Receive acknowledge bit.
Send stop condition, aborting write.
Send start condition.
Send 10011xx1(chip address & read operation).
Receive acknowledge bit.
Receive byte, contents of selected register.
Send acknowledge bit.
Send stop condition.
```

Setting the auto increment bit in the MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

6.2 Software Mode - SPI Control Port

In SPI Mode, data is clocked into the serial control data line, CDIN, by the serial clock, CCLK (see Figure 22 for the clock to data relationship). There are no AD0 or AD1 pins. Pin $\overline{CS}$ is the chip select signal and is used to control SPI writes to the registers. When the device detects a high-to-low transition on the AD0/$\overline{CS}$ pin after power-up, SPI Mode will be selected. All signals are inputs and data is clocked in on the rising edge of CCLK.

6.2.1 SPI Write

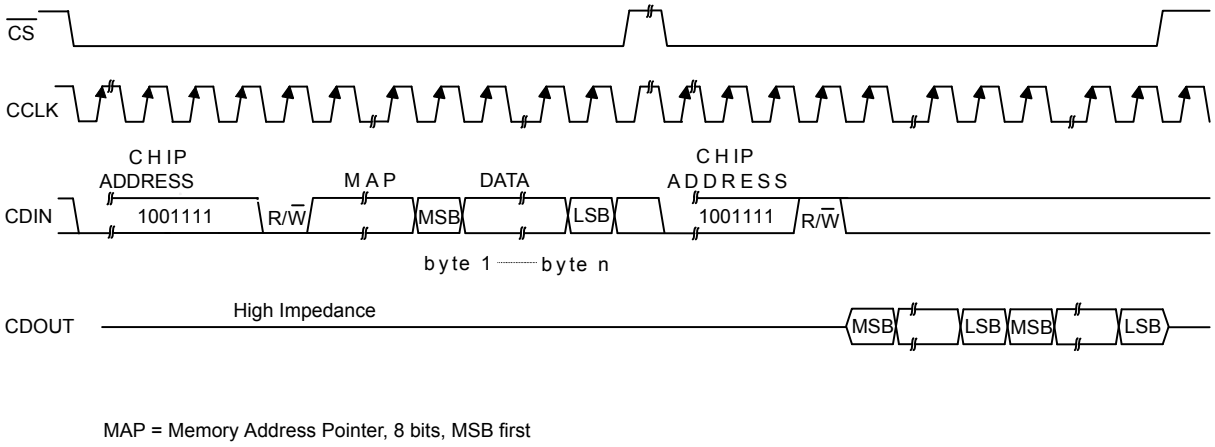
To write to the device, use the following procedure while adhering to the Software Mode switching specifications in "Switching Characteristics - Software Mode - SPI Format" section on page 18.

1. Bring $\overline{CS}$ low.
2. The address byte on the CDIN pin must then be 10011110 (R/$\overline{W}$ = 0).
3. Write to the memory address pointer, MAP. This byte points to the register to be written.
4. Write the desired data to the register pointed to by the MAP.
5. If the INCR bit (see Section 6.2.3.1) is set to 1, repeat the previous step until all the desired registers are written, then bring CS high.
6. If the INCR bit is set to 0 and further SPI writes to other registers are desired, it is necessary to bring $\overline{CS}$ high, and follow the procedure detailed from step 1. If no further writes to other registers are desired, bring $\overline{CS}$ high

6.2.2 SPI Read

To read from the device, use the following procedure while adhering to the values specified in "Switching Characteristics - Software Mode - SPI Format" section on page 18.

1. Bring $\overline{CS}$ low.
2. The address byte on the CDIN pin must then be 10011111 (R/$\overline{W}$ = 1).
3. CDOUT pin will then output the data from the register pointed to by the MAP, which is set during the SPI write operation.
4. If the INCR bit (see Section 6.2.3.1) is set to 1, keep $\overline{CS}$ low and continue providing clocks on CCLK to read from multiple consecutive registers. Bring $\overline{CS}$ high when reading is complete.
5. If the INCR bit is set to 0 and further SPI reads from other registers are desired, it is necessary to bring $\overline{CS}$ high, and follow the procedure detailed from step 1. If no further reads from other registers are desired, bring $\overline{CS}$ high.



MAP = Memory Address Pointer, 8 bits, MSB first

Figure 22. Software Mode Timing, SPI Mode

6.2.3 Memory Address Pointer (MAP)

The MAP byte comes after the address byte and selects the register to be read or written. Refer to Figures 20 and 21 on page 29, and Figure 22 on page 30.

6.2.3.1 Map Increment (INCR)

The device has MAP auto increment capability enabled by the INCR bit (the MSB) of the MAP. If INCR is set to 0, MAP will stay constant for successive I²C writes or reads and SPI writes. If INCR is set to 1, MAP will auto increment after each byte is written, allowing block reads or writes of successive registers.

7. REGISTER QUICK REFERENCE

This table shows the register and register bit names and their associated default values.

Addr	Function	7	6	5	4	3	2	1	0
01h	Device ID	ID3	ID2	ID1	ID0	REV3	REV2	REV1	REV0
p 32		1	1	0	0	0	0	0	1
02h	Power Control	Freeze	Reserved	PDN_ADC	Reserved	Reserved	Reserved	PDN_DAC	PDN
p 32		0	0	0	0	0	0	0	0
03h	Mode Control	Reserved	Reserved	FM1	FM0	MCLK_ FREQ2	MCLK_ FREQ1	MCLK_ FREQ0	POPG
p 33		0	0	1	1	0	0	0	0
04h	ADC and DAC Control	ADC_HPF_ FRZ_A	ADC_HPF_ FRZ_B	DIG_ LOOPBK	DAC_DIF1	DAC_DIF0	Reserved	Reserved	ADC_DIF0
p 34		0	0	0	0	0	0	0	0
05h	Transition Control	DAC_SNGL_ VOL	DAC_SOFT	DAC_ZC	ADC_INV_ B	ADC_INV_ A	DAC_INV_ B	DAC_INV_A	DE_EMPH
p 35		0	1	1	0	0	0	0	0
06h	Mute Control	Reserved	Reserved	AUTO_ MUTE	MUTE_ ADC_CHB	MUTE_ ADC_CH A	MUTE_ POL	MUTE_DAC_ CHB	MUTE_DAC_ CHA
p 36		0	0	1	0	0	0	0	0
07h	DAC Channel A Volume Control	DACA_ VOL7	DACA_ VOL6	DACA_ VOL5	DACA_ VOL4	DACA_ VOL3	DACA_ VOL2	DACA_ VOL1	DACA_ VOL0
p 36		0	0	0	0	0	0	0	0
08h	DAC Channel B Volume Control	DACB_ VOL7	DACB_ VOL6	DACB_ VOL5	DACB_ VOL4	DACB_ VOL3	DACB_ VOL2	DACB_ VOL1	DACB_ VOL0
p 37		0	0	0	0	0	0	0	0

8. REGISTER DESCRIPTION

** All registers are read/write in I²C Mode and SPI Mode, unless otherwise noted**

8.1 Device ID - Address 01h

7	6	5	4	3	2	1	0
ID3	ID2	ID1	ID0	REV3	REV2	REV1	REV0

Function:

This register is read only. Bits 7 through 4 are the device ID, which is 1100b (0Ch) and the remaining bits REV[3:0] are for the device revision.

8.2 Power Control - Address 02h

7	6	5	4	3	2	1	0
Freeze	Reserved	PDN_ADC	Reserved	Reserved	Reserved	PDN_DAC	PDN

8.2.1 Freeze (Bit 7)

Function:

This function allows changes to registers 05h–08h without the changes taking effect until the Freeze bit is cleared. To make multiple changes to these bits take effect simultaneously, set the Freeze bit, make all changes, then clear the Freeze bit.

8.2.2 PDN_ADC (Bit 5)

Function:

The ADC portion of the device will enter a low-power state whenever this bit is set.

8.2.3 PDN_DAC (Bit 1)

Function:

The DAC portion of the device enters a low-power state when this bit is set.

8.2.4 Power Down (Bit 0)

Function:

The device enters a low-power state when this bit is set. The contents of all registers are retained when the device is in power-down.

8.3 Mode Control - Address 03h

7	6	5	4	3	2	1	0
Reserved	Reserved	FM1	FM0	MCLK_FREQ2	MCLK_FREQ1	MCLK_FREQ0	POPG

8.3.1 ADC Functional Mode & Master/Slave Mode (Bits 5:4)

Function:

In Master Mode, the user must configure the CS4270 Speed Mode with these bits. In Slave Mode, the CS4270 auto-detects the speed mode.

FM1	FM0	Mode
0	0	Single-Speed Master Mode: 4 to 54 kHz sample rates
0	1	Double-Speed Master Mode: 50 to 108 kHz sample rates
1	0	Quad-Speed Master Mode: 100 to 216 kHz sample rates
1	1	Slave Mode (default)

Table 9. Functional Mode Selection

8.3.2 Ratio Select (Bits 3:1)

Function:

These bits are used to select the clocking ratios. The PDN bit should be set before, and cleared after, any changes to these bits.

MCLK_FREQ2	MCLK_FREQ1	MCLK_FREQ0	Mode
0	0	0	Divide by 1 (default)
0	0	1	Divide by 1.5
0	1	0	Divide by 2
0	1	1	Divide by 3
1	0	0	Divide by 4

Table 10. MCLK Divider Configuration

8.3.3 Popguard Transient Control (Bit 0)

Function:

When set, the Popguard Transient Control allows the quiescent voltage to slowly ramp to and from AGND to the quiescent voltage during power-on or power-off when this function is set. When cleared (default), this function is disabled. See Section 5.3 for additional details about Popguard.

8.4 ADC and DAC Control - Address 04h

7	6	5	4	3	2	1	0
ADC_HPF_FRZ_A	ADC_HPF_FRZ_B	DIG_LOOPBK	DAC_DIF1	DAC_DIF0	Reserved	Reserved	ADC_DIF0

8.4.1 ADC High Pass Filter Freeze for CH A (Bit 7)

Function:

When this bit is set, the internal high-pass filter DC offset value for channel A are frozen.This value is continuously subtracted from the conversion result. To recalibrate ADC channel A and obtain a new or continuous value for the system DC offset, clear this bit. See "DC Offset Calibration Using the High-Pass Filter" on page 23.

8.4.2 ADC High Pass Filter Freeze for CH B (Bit 6)

Function:

When this bit is set, the internal high-pass filter for channel B are frozen.The current DC offset value will be static and continuously subtracted from the conversion. To recalibrate ADC channel A and obtain a new or continuous value for the system DC offset, clear this bit. See "DC Offset Calibration Using the High-Pass Filter" on page 23.

8.4.3 Digital Loopback (Bit 5)

Function:

When this bit is set, an internal digital loopback from the ADC to the DAC will be enabled. See Section 5.2.5 "Internal Digital Loopback" on page 23.

8.4.4 DAC Digital Interface Format (Bits 4:3)

Function:

The DAC_Digital_Interface_Format and the options are detailed in Table 11 and Figures 9–11.

DAC_DIF1	DAC_DIF0	Description	Format	Figure
0	0	Left Justified, up to 24-bit data (default)	0	9
0	1	I²S, up to 24-bit data	1	10
1	1	Right-Justified, 16-bit Data	2	11
1	0	Right-Justified, 24-bit Data	3	11

Table 11. DAC Digital Interface Formats

8.4.5 ADC Digital Interface Format (Bit 0)

Function:

The required relationship between LRCK, SCLK, and SDOUT for the ADC is defined by the ADC Digital Interface Format. The options are detailed in Table 12 and may be seen in Figures 9 and 10.

ADC_DIF	Description	Format	Figure
0	Left Justified, up to 24-bit data (default)	0	9
1	I²S, up to 24-bit data	1	10

Table 12. ADC Digital Interface Formats

8.5 Transition Control - Address 05h

7	6	5	4	3	2	1	0
DAC_SNGL_VOL	DAC_SOFT	DAC_ZC	ADC_INV_CHB	ADC_INV_CHA	DAC_INV_CHB	DAC_INV_CHA	DE_EMPH

8.5.1 DAC Single Volume (Bit 7)

Function:

The AOUTA and AOUTB volume levels are independently controlled by the DAC Channel A & B Volume Control Registers when this bit is cleared.

The volumes on AOUTA and AOUTB are locked together and determined by the DAC Channel A Volume Control Register (07h) when this bit is set.

8.5.2 Soft Ramp and Zero Cross Enable (Bits 6:5)

Function:

Soft Ramp Enable

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods. See Table 13 on page 35.

Zero Cross Enable

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a time-out period between 512 and 1,024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Soft Ramp and Zero Cross Enable

Soft Ramp and Zero Cross Enable dictate that signal level changes, either by attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a time-out period between 512 and 1,024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel. See Table 10 on page 33.

DAC_SOFT	DAC_ZC	Mode
0	0	Changes take effect immediately
0	1	Zero Cross enabled
1	0	Soft Ramp enabled
1	1	Soft Ramp and Zero Cross enabled (default)

Table 13. Soft Cross or Zero Cross Mode Selection

8.5.3 Invert Signal Polarity (Bits 4:1)

Function:

When set, this bit activates an inversion of the signal polarity for the appropriate channel. This is useful if a board layout error has occurred or in other situations where a 180° phase shift is desirable.

8.5.4 De-Emphasis Control (Bit 0)

Function:

When this bit is set, the standard 50/15 μs digital de-emphasis filter is applied on the DAC output. Figure 14 on page 25 shows the filter response. **NOTE:** De-emphasis is available only in Single-Speed Mode.

When this bit is cleared, no de-emphasis is applied to the DAC outputs.

8.6 Mute Control - Address 06h

7	6	5	4	3	2	1	0
Reserved	Reserved	AUTO_MUTE	MUTE_ADC_CHB	MUTE_ADC_CHA	MUTE_POL	MUTE_DAC_CHB	MUTE_DAC_CHA

8.6.1 Auto-Mute (Bit 5)

Function:

When set, enables the Auto-Mute function. Section 5.2.6 “Auto-Mute” on page 23.

8.6.2 ADC Channel A & B Mute (Bits 4:3)

Function:

When this bit is set, the output of the ADC for the selected channel will be muted.

8.6.3 Mute Polarity (Bit 2)

Function:

The $\overline{\text{MUTEA}}$ and $\overline{\text{MUTEB}}$ pins (pins 24 and 21) are active low by default. When this bit is set, these pins are active high.

8.6.4 DAC Channel A & B Mute (Bits 1:0)

Function:

When this bit is set, the output of the DAC for the selected channel will be muted.

8.7 DAC Channel A Volume Control - Address 07h

7	6	5	4	3	2	1	0
DACA_VOL7	DACA_VOL6	DACA_VOL5	DACA_VOL4	DACA_VOL3	DACA_VOL2	DACA_VOL1	DACA_VOL0

Function:

See Section 8.8 DAC Channel B Volume Control - Address 08h.

8.8 DAC Channel B Volume Control - Address 08h

7	6	5	4	3	2	1	0
DACB VOL7	DACB VOL6	DACB VOL5	DACB VOL4	DACB VOL3	DACB VOL2	DACB VOL1	DACB VOL0

Function:

The digital volume control allows the user to attenuate the signal in 0.5 dB increments from 0 to -127 dB. VOL0 activates a 0.5 dB attenuation when set, and no attenuation when cleared. VOL[7:0] activates attenuation equal to their decimal value (in dB). Example volume settings are decoded as shown in Table 14. The volume changes are implemented as dictated by the DAC_SOFT and DAC_ZC bits in the Transition Control register (see Section 8.5.2).

Binary Code	Volume Setting
00000000	0 dB
00000001	-0.5 dB
00101000	-20 dB
00101001	-20.5 dB
11111110	-127 dB
11111111	-127.5 dB

Table 14. Digital Volume Control

9. FILTER PLOTS

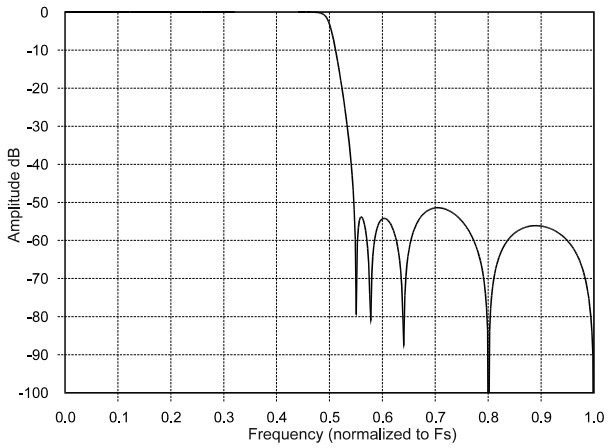


Figure 23. DAC Single-Speed Stopband Rejection

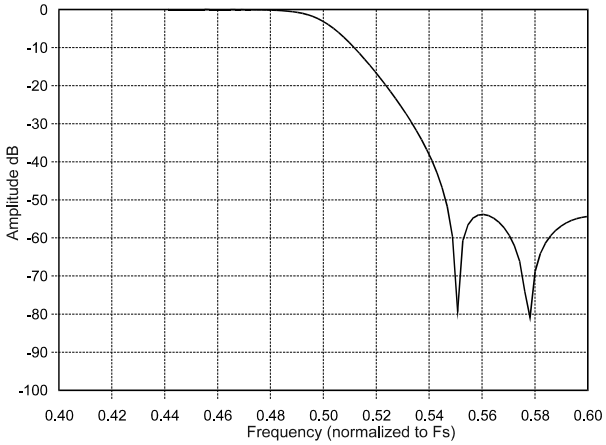


Figure 24. DAC Single-Speed Transition Band

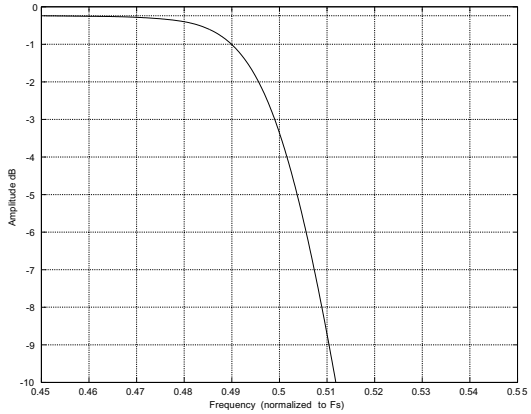


Figure 25. DAC Single-Speed Transition Band (detail)

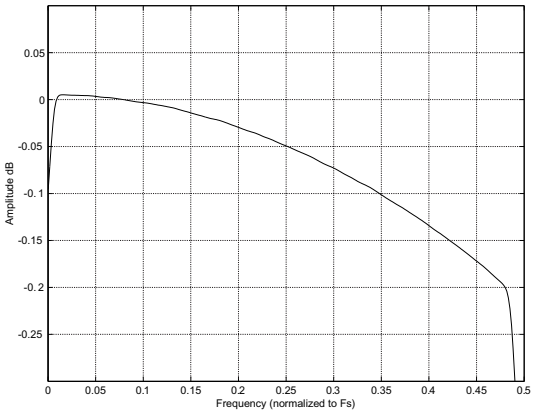


Figure 26. DAC Single-Speed Passband Ripple

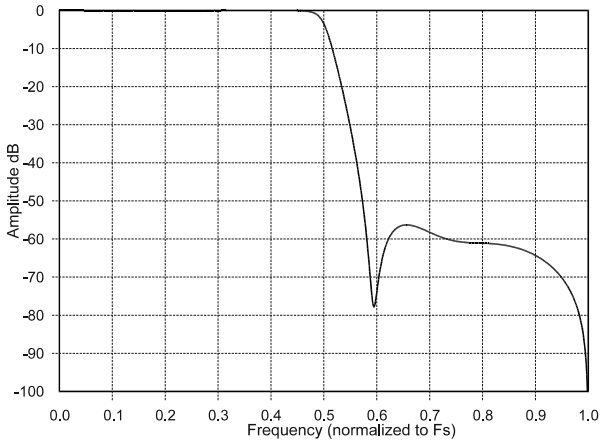


Figure 27. DAC Double-Speed Stopband Rejection

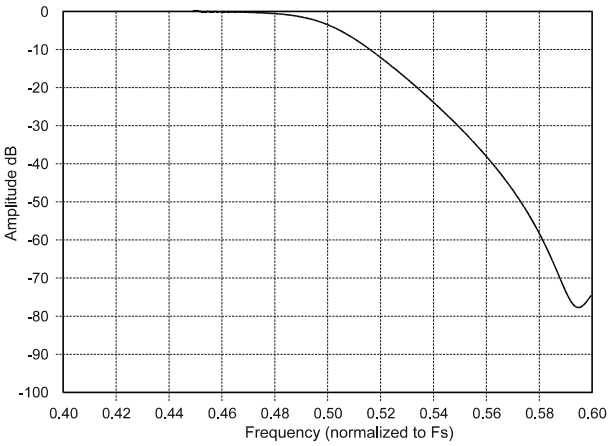


Figure 28. DAC Double-Speed Transition Band

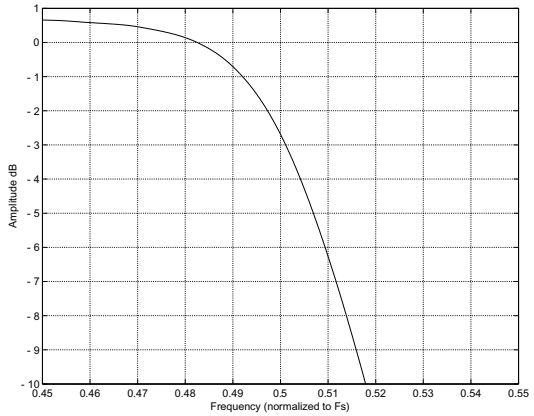


Figure 29. DAC Double-Speed Transition Band (detail)

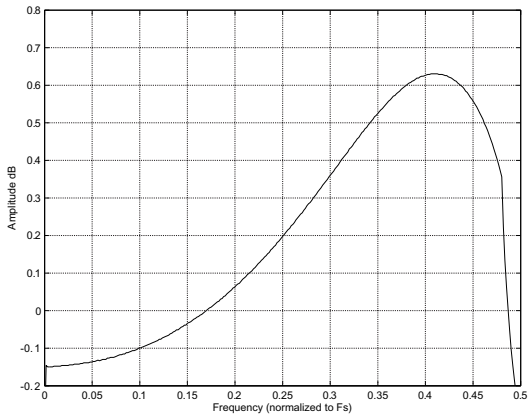


Figure 30. DAC Double-Speed Passband Ripple

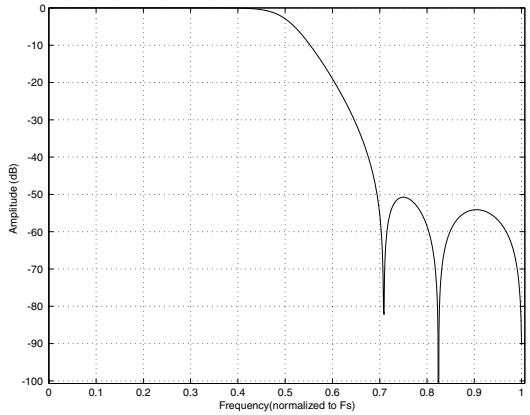


Figure 31. DAC Quad-Speed Stopband Rejection

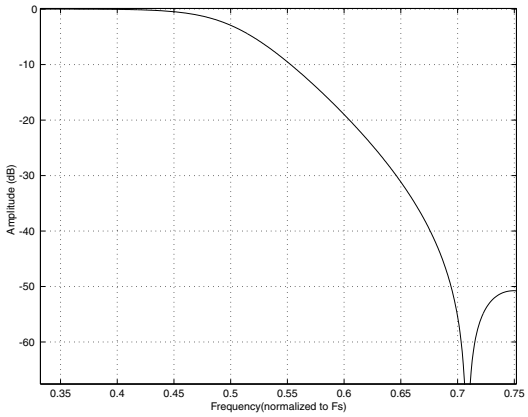


Figure 32. DAC Quad-Speed Transition Band

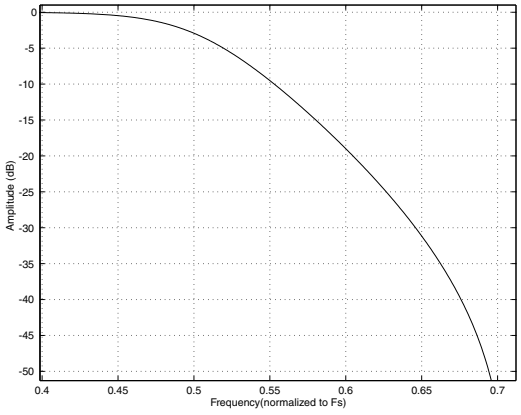


Figure 33. DAC Quad-Speed Transition Band (detail)

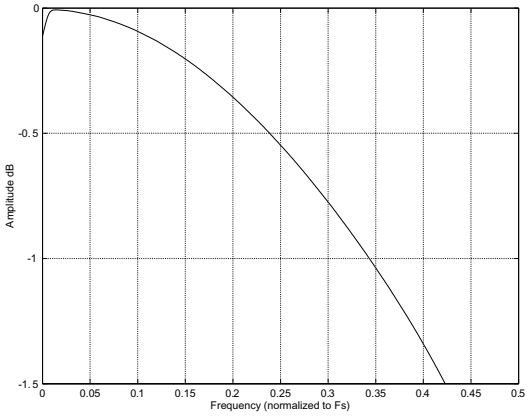


Figure 34. DAC Quad-Speed Passband Ripple

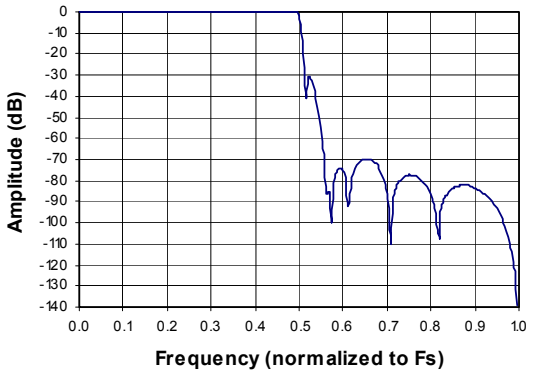


Figure 35. ADC Single-Speed Stopband Rejection

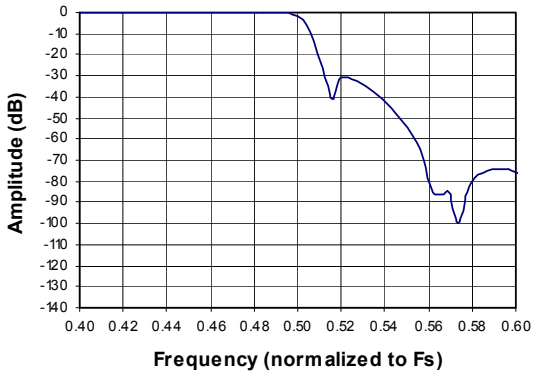


Figure 36. ADC Single-Speed Stopband (detail)

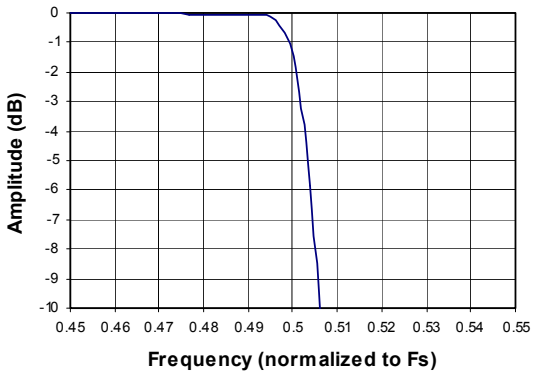


Figure 37. ADC Single-Speed Transition Band (detail)

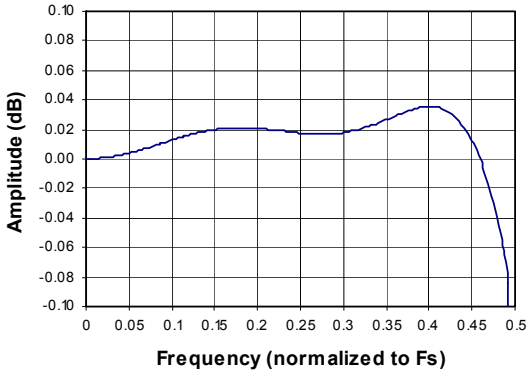


Figure 38. ADC Single-Speed Passband Ripple

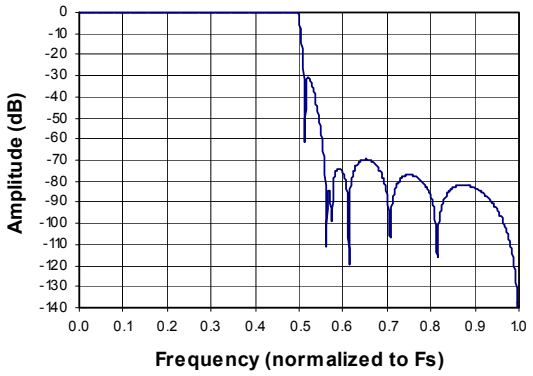


Figure 39. ADC Double-Speed Stopband Rejection

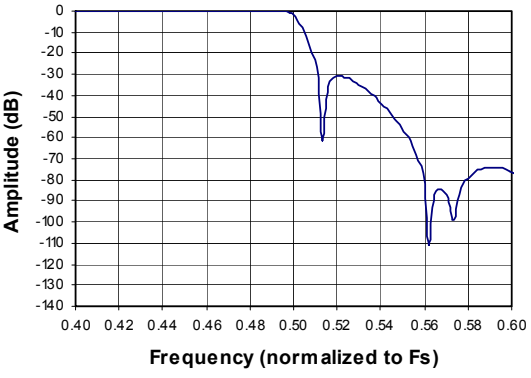


Figure 40. ADC Double-Speed Stopband (detail)

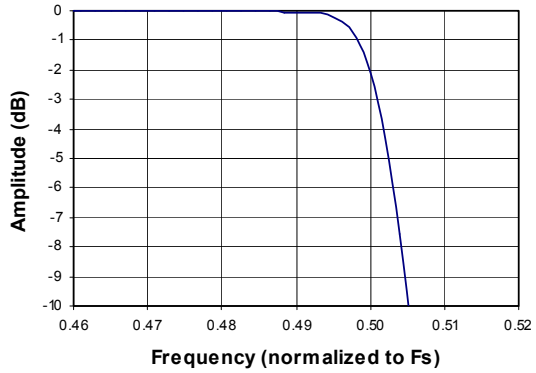


Figure 41. ADC Double-Speed Transition Band (detail)

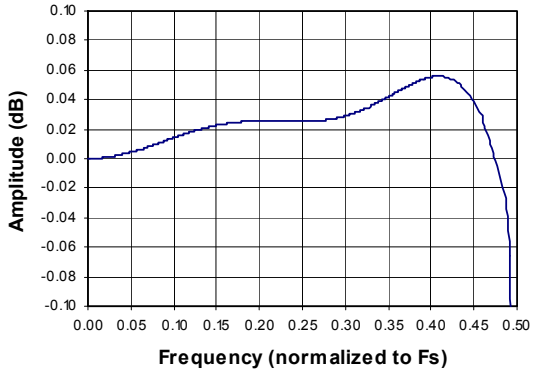


Figure 42. ADC Double-Speed Passband Ripple

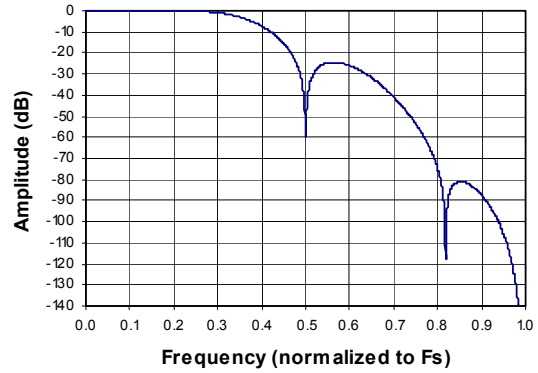


Figure 43. ADC Quad-Speed Stopband Rejection

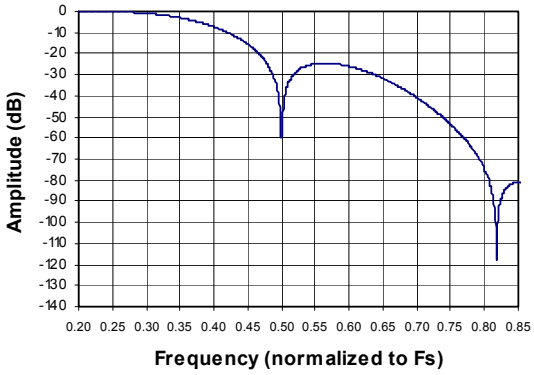


Figure 44. ADC Quad-Speed Stopband (detail)

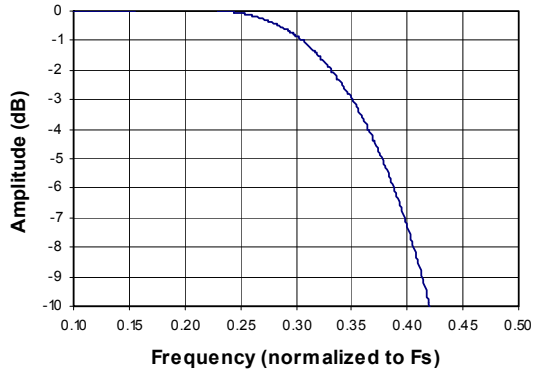


Figure 45. ADC Quad-Speed Transition Band (detail)

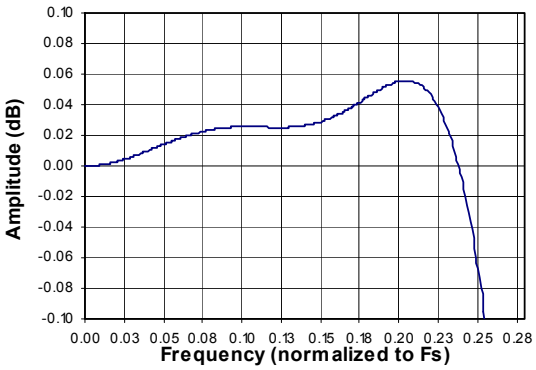


Figure 46. ADC Quad-Speed Passband Ripple

10.PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. For ADCs, measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A. For DACs, measured at 0 dB relative to full scale.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

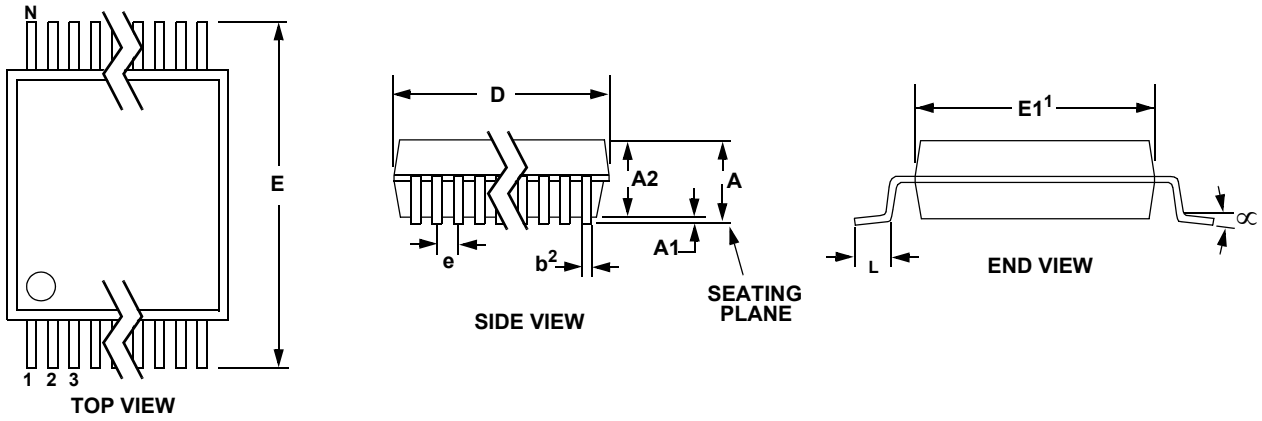
The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

11.PACKAGE DIMENSIONS

24L TSSOP (4.4 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.47	--	--	1.20	
A1	0.00197	0.00394	0.00591	0.05	0.10	0.15	
A2	0.03150	0.0394	0.04137	0.80	1.00	1.05	
b	0.00748	0.00965	0.01182	0.19	0.245	0.30	2,3
D	0.30338 BSC	0.30732 BSC	0.31126 BSC	7.70 BSC	7.80 BSC	7.90 BSC	1
E	0.24822	0.25216	0.25610	6.30	6.40	6.50	
E1	0.16942	0.17336	0.17730	4.30	4.40	4.50	1
e	--	0.026 BSC	--	--	0.65 BSC	--	
L	0.01970	0.02364	0.02955	0.50	0.60	0.75	
µ	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-153

Controlling Dimension is Millimeters.

1. "D" and "E1" are reference datums and do not include mold flash or protrusions, but do include mold mismatch and are measured at the parting line. Mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

THERMAL CHARACTERISTICS

Parameters	Symbol	Min	Typ	Max	Units
Allowable Junction Temperature		-	-	135	°C
Junction to Ambient Thermal Impedance (Note 4)					
(Multi-layer PCB) TSSOP	θ_{JA-M}	-	70	-	°C/W
(Single-layer PCB) TSSOP	θ_{JA-S}	-	105	-	°C/W

4. θ_{JA} is specified according to JEDEC specifications for multi-layer PCBs.

12.ORDERING INFORMATION

Product	Description	Package	Pb-Free	Temp Range	Container	Order #
CS4270	24-Bit 192 kHz Stereo Audio CODEC	24-TSSOP	YES	-10° to +70° C	Rail	CS4270-CZZ
					Tape & Reel	CS4270-CZZR
CDB4270	CS4270 Evaluation Board	-	-	-	-	CDB4270

13.REVISION HISTORY

Release	Changes

F1	– Deleted automotive grade content and references to grade throughout.
	– Formatting changes throughout.
	– Updated several "Pin Descriptions" on page 4.
	– Added "Digital I/O Pin Characteristics" on page 6.
	– Added decoupling cap to VLC on Typical Connection Diagram, Figure 1 on page 7.
	– Performance specifications updated per measured data in Section 4. "Characteristics and Specifications" on page 8:
	  – Min Specified Operating Conditions for "DC Power Supplies:" on page 8.
	  – Typ and Max DAC Analog Characteristics for "Total Harmonic Distortion + Noise" on page 9.
	  – Max ADC Analog Characteristics for "Total Harmonic Distortion + Noise" on page 11.
	  – Typ ADC Analog Characteristics for "Interchannel Isolation" on page 11.
	  – Typ and Max DC Electrical Characteristics for "Power Supply Current" on page 13.
	  – Typ and Max DC Electrical Characteristics for "Power Consumption VA = 5 V, VD = VLC= 3.3 V" on page 13.
	  – Typ DC Electrical Characteristics for "FILT+ Output Impedance" on page 13.
	  – Min Switching Characteristics - Software Mode - SPI Format for "CCLK High Time" and "CCLK Low Time" on page 18.
	– Added "Acknowledge Delay from SCL Falling" on page 17.
	– Added Transition Time from CCLK to CDOUT Valid (Note 21) and Time from CS rising to CDOUT High-Z to "Switching Characteristics - Software Mode - SPI Format" on page 18.
	– Added CDOUT to Figure 13 on page 18.
	– Added Table 2 on page 19 and associated text in Section 5.1.1 Access to Stand-Alone Mode.
	– Added Note 22 on page 20.
	– Updated descriptions of recommended power-up sequences in "Serial Control Port Mode" on page 21.
	– Updated "Clock Ratio Selection" on page 22 (added all SCLK/LRCK ratios to the serial control port mode table).
	– Updated Section 5.2.7 "DC Offset Calibration Using the High-Pass Filter" on page 23.
	– Added Section 5.3 "Popguard Transient Control" on page 24.
	– Updated Section 5.5.1 "Input Component Values" on page 25.
	– Updated presentation of input source resistance plots (Figure 16 and Figure 17 on page 26).
	– Added Section 6.2.2 SPI Read on page 30.
	– Updated bit names in Section 7. "Register Quick Reference" on page 31.
	– Updated Section 8.3.2 "Ratio Select (Bits 3:1)" on page 33.
	– Updated Section 8.3.3 "Popguard Transient Control (Bit 0)" on page 33.
	– Updated Section 8.4.1 and Section 8.4.2 on page 34.
	– Updated Section 8.5.4 "De-Emphasis Control (Bit 0)" on page 36.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com.

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