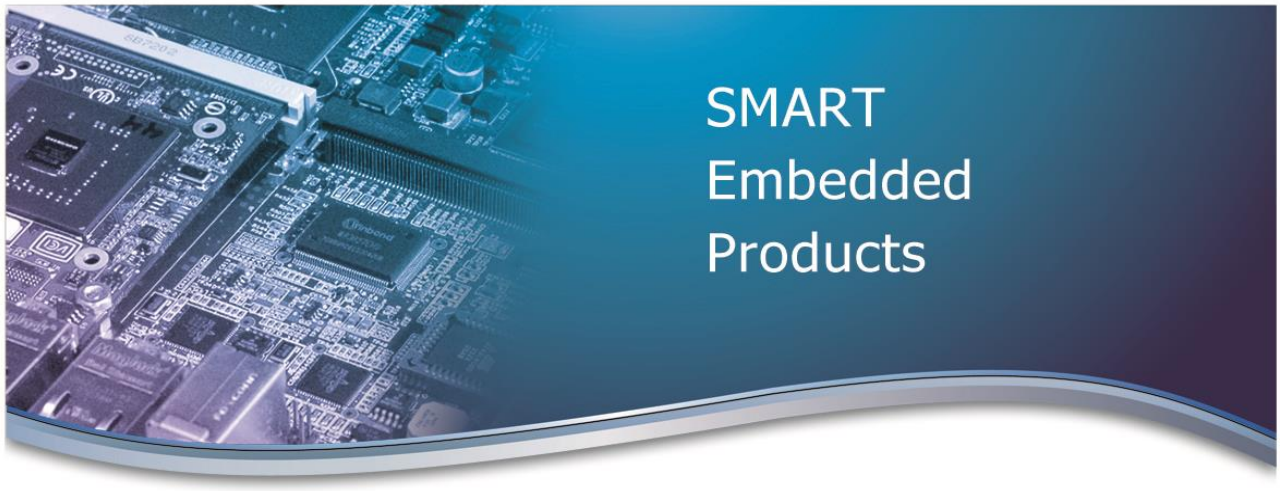

Product Specification

SMART MODULAR microSD™ MEMORY CARDS 8GB - 32GB SDHC and 64GB SDXC

SS9UDxxxGPHECMx21

January 2016
DSUD262-AA

www.smartm.com

REVISION HISTORY

Date	Revision	Section(s)	Description
January 2016	A	All	Initial release

ESD Caution – Handling
Static electricity may be discharged through this disk subsystem. In extreme cases, this may temporarily interrupt the operation or damage components. To prevent this, make sure you are working in an ESD-safe environment. For example, before handling the disk subsystem, touch a grounded device, such as a computer case, prior to handling.

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TABLE OF CONTENTS

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Flash Design Center: 2 Highwood Dr, Suite 101, Tewksbury, MA 01876 USA • Tel:(978) 221-3500 • Fax:(978) 303-8757
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LIST OF FIGURES

Corporate Headquarters: 39870 Eureka Dr, Newark, CA 94560, USA • Tel:(510) 623-1231 • Fax:(510) 623-1434 • E-mail: info@smartm.com
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Asia: Plot 18, Lrg Jelawat 4, Kawasan Perindustrian Seberang Jaya 13700, Prai, Penang, Malaysia • Tel: +604-3992909 • Fax: +604-3992903

LIST OF TABLES

Corporate Headquarters: 39870 Eureka Dr, Newark, CA 94560, USA • Tel:(510) 623-1231 • Fax:(510) 623-1434 • E-mail: info@smartm.com
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1. GENERAL DESCRIPTION

1.1. Overview

SMART's v3.0 microSD card is fully compliant with the SD Card Association specification. The Command List complies with Part 1 Physical Layer Specification v3.01 final definitions, Card Capacity of Non-secure Area, and v3.00 of the Secure Area Part 3 Security Specification.

The microSD card comes with 8-pin interface, designed to operate at operating frequencies of 25 MHz to 208MHz. It can alternate communication protocol between the SD mode and SPI mode. It performs data error detection and correction with very low power consumption.

SMART's microSD card is suitable for hand-held applications in semi-industrial/medical markets and is one of the most popular cards today based on its high performance, good reliability and wide compatibility.

SMART has built its foundation by providing proven technology and quality products to the most demanding Fortune 100 OEMs. SMART engineers its products to perform at the highest degree of reliability & compatibility while backing these products with outstanding services and technology expertise.

About SMART

SMART is a leading independent manufacturer of memory and embedded modular sub-systems inclusive of board-level through system-level design, manufacturing, test, and fulfillment services. We offer more than 500 standard and custom products to leading OEMs in the computer, industrial, networking and telecommunications industries worldwide.

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1.2. Features

- **Form Factor:** microSD
- **Interface:** Industry standard SD [Part 1 Physical Layer Specification Ver3.01 Final]
- **Supports SD SPI Mode**
- **Bus Widths Supported:** x1 and x4
- **Supported Bus Speed Modes (using x4 bus width)**
  - **DS:** Default Speed Mode up to 25 MHz, 3.3 V signaling
  - **HS:** High Speed Mode up to 50 MHz, 3.3 V signaling
  - **SDR12:** SDR up to 25 MHz, 1.8 V signaling
  - **SDR25:** SDR up to 50 MHz, 1.8 V signaling
  - **SDR50:** SDR up to 100 MHz, 1.8 V signaling
  - **SDR104:** SDR up to 208 MHz, 1.8 V signaling
  - **DDR50:** DDR up to 50 MHz, 1.8 V signaling

    NOTE: 1.8 V signal timing are different from those of 3.3 V.
- **NAND Technology:** Multi Level Cell (MLC)
- **Capacity:**
  - SDHC: 4-32Gbytes
  - SDXC: 64Gbytes
- **Operating Temperature:**
  - **Commercial Temperature:** 0ºC to +70ºC
  - **Industrial Temperature:** -40°C~85°C
- **Input Power:** 2.7 V – 3.6 V
- **Dimensions**: 15mm(L) x 11mm(W) x 1mm(H)

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1.3. Unique Features

- Implements Static and Dynamic Wear Leveling for longer life
- Bad Block Management improves the SD content reliability
- Supports 43 bits per 1K Bytes Advanced Error Detection/Correction for superior data reliability
- Device health information (erase count, bad block and spare count) is available via vendor specific command (Application Note available upon request)
- Command list supports [Part 1 Physical Layer Specification Ver3.01 Final] definitions
- Copyright Protection Mechanism: fully-compliant to the highest security SDMI Standard
- Supports CPRM (Content Protection for Recordable Media) for recorded content
- Password Protection of cards (optional)
- Built-in write protection features (permanent and temporary)

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2. OPERATIONAL CHARACTERISTICS

All listed values are typical unless otherwise stated.

2.1 Performance

Table 1: Performance Characteristics

Drive	Configuration	Sequential Read (MB/s)	Sequential Write (MB/s)
8 GB	SDR104 (UHS-I, 1.8V, 208MHz)	98	27
16 GB		97	54
32 GB		97	90
64 GB		99	91

Note: Performance measured using Testmetrix VTE-4100.

2.2 Operating Power Consumption

Table 2: MicroSD Card Power Consumption

Parameter	8GB	16GB	32GB	64GB	Unit
Read Current	79	87	89	98	mA
Write Current	64	104	143	150	mA
Standby Current	115	188	199	250	µA

Note**:** Current measured with multi-meter (maximum value), under SDR104 mode operation.

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2.3 Reliability

Table 3: Reliability Characteristics

Item		Value
Mean Time Between Failures (MTBF)		> 3 Million hours
Data Reliability		< 1 Non-Recoverable Error in 10^{14} bits read
Data Retention (@ 40˚C)		10 years > 90% life remaining
		1 year < 10% life remaining
Endurance[1]	8GB	23 TBW (7GB under sequential write)
	16GB	46 TBW (14GB under sequential write)
	32GB	93 TBW (29GB under sequential write)
	64GB	186 TBW(59GB under sequential write)
Error Correction / Error Detection		Up to 43 bits for every 1024 bytes of data

[1] The device level endurance is directly related to the application specific workload and the application's data retention requirement. Endurance can be increased by trading off data retention.

2.4 Endurance

- **Static & Dynamic Wear Leveling:** This feature eliminates overstressing Flash media by spreading the data writes across all Flash physical address space, including logical areas that are not written by the user. The data is wear leveled across the entire drive.

- **ECC:** SD products utilize BCH ECC to provide correction of up to 43 random single-bit errors per 1024 bytes of user data.

- **Bad Block Management:** This feature tracks all manufacturing and run-time bad blocks of flash media and replaces them with new ones from the spare pool.

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2.5 Environmental Conditions

Table 4: Environmental Conditions and Test Conditions (Commercial)

Parameter	Value
Shock	Plus with Half-Sine, 500G/2ms. 6 faces, 5 times/face
Bending Test	Force: 10N, hold 1 min for 5 times
Vibration	Displacement: 20-80Hz/1.52mm Acceleration: 80-2000HZ/20G 30mins/axis
Temperature and Humidity storage	40ºC/93%RH@500hrs
Operating Temperature	0ºC to 70ºC
Storage Temperature	-25ºC to 85ºC

Table 1: Environmental Conditions and Test Conditions (Industrial)

Parameter	Value
Shock	Plus with Half-Sine, 1500G/2ms. 6 faces, 5 times/face
Bending Test	Force: 10N, hold 1 min for 5 times
Vibration	Displacement: 20-80Hz/1.52mm Acceleration: 80-2000HZ/20G 60mins/axis
Temperature and Humidity storage	55ºC/95%RH@500hrs
Operating Temperature	-40ºC to 85ºC
Storage Temperature	-40ºC to 85ºC

2.6 Physical Characteristics

Table 6: Physical Characteristics

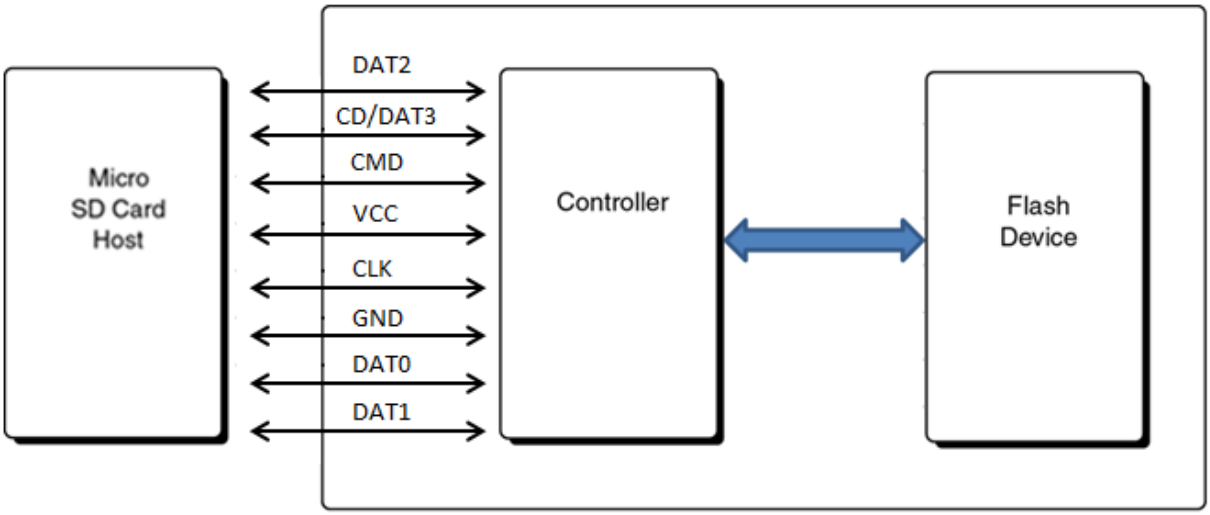
Parameter	Value
Length	15.0 mm [0.590 in]
Width	11.0 mm [0.433 in]
Thickness	1.0 mm [0.039 in]
Weight	0.4 g [0.014 oz]

3. PRODUCT DESCRIPTION

SMART's MicroSD Memory Card product line is offered in a UL approved housing with an advanced 8-pin connector. It contains a controller and a flash memory device. The on-board controller interfaces with a microSD Card Host allowing data to be written to and read from the flash memory device.

3.1 Functional Block Diagram

Figure 1: Functional Block Diagram (microSD Memory Card)



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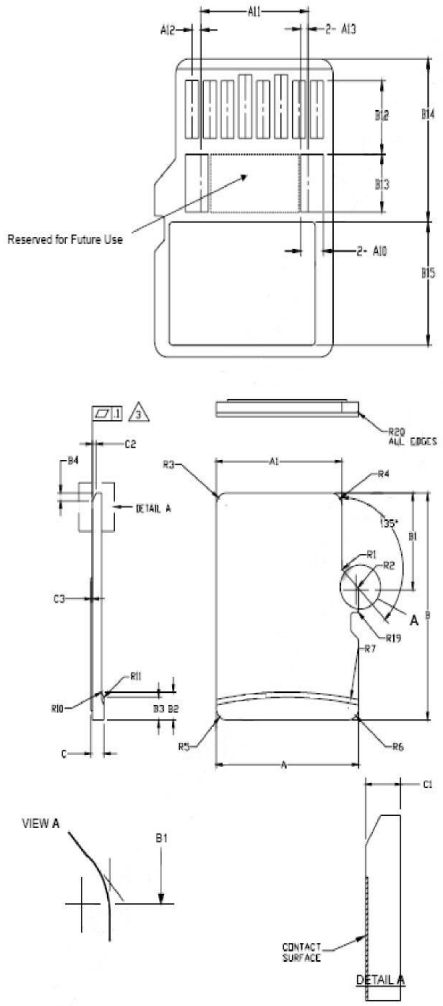
4. MECHANICAL SPECIFICATION

Figure 2: Mechanical Specification



	COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX	NOTE
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.80	-	-	
A10	1.35	1.40	1.45	
A11	6.50	6.60	6.70	
A12	0.50	0.55	0.60	
A13	0.40	0.45	0.50	
B	14.90	15.00	15.10	
B1	6.30	6.40	6.50	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50	-	-	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	-	-	9.00	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
B12	3.60	3.70	3.80	
B13	2.80	2.90	3.00	
B14	8.20	-	-	
B15	-	-	6.20	
C	0.90	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
D1	1.00	-	-	
D2	1.00	-	-	
D3	1.00	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.70	0.80	0.90	
R6	0.70	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	
R20	0.02	-	0.15	

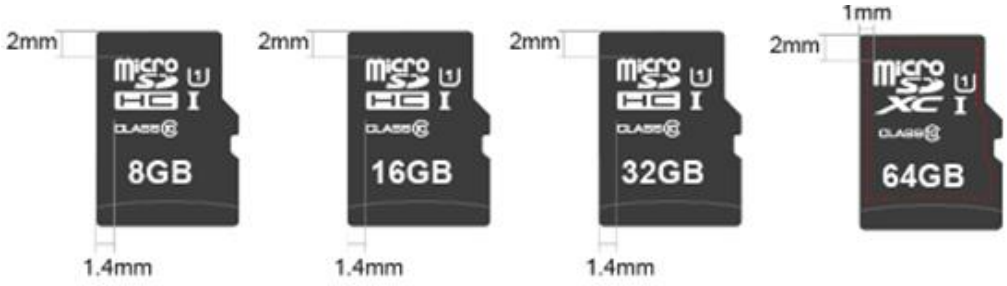
Notes:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. COPLANARITY IS ADDITIVE TO C1 MAX THICKNESS.

4.1 Label and Marking

Below are some examples of the standard laser mark for the SMART XL microSD card.

Figure 3: Label and Marking of microSD Card



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5. ELECTRICAL SPECIFICATION

5.1 Electrical Interface

The SMART microSD Memory Cards are fully compliant with the microSD specification (V1.1 and V1.01). Table 7 describes the I/O signals of the card. Signals whose source is the Host are designated as inputs (I) while signals that the microSD Card sources are outputs (O). Bi-directional signals are designated as Input/Output (I/O) or Input/Output using push-pull drivers (PP).

Table 7: Pin Assignments and Pin Types

Pin	Signal Name	Type	Signal Description
1	DAT2	I/O / PP	Data Line [bit2]
2	CD/DAT3	I/O / PP	Card Detect / Data Line [bit3]
3	CMD	PP	Command / Response
4	VCC	S	Supply Voltage
5	CLK	I	Clock
6	GND	S	Supply Voltage Ground
7	DAT0	I/O / PP	Data Line [bit0]
8	DAT1	I/O / PP	Data Line [bit1]

5.2 Absolute Maximum Ratings

Table 8: Absolute Maximum Ratings*

Parameter	MIN	MAX	Unit
DC Power Supply	-0.3	+3.6	V
Input Voltage	V_{SS} - 0.3	V_{DD} + 0.3	V
Operating Current	-	400	mA
Standby Current	-	1000	µA
Operating Temperature – (Commercial)	0	+70	°C
Operating Temperature – (Industrial)	-40	+85	°C
Storage Temperature – (Commercial)	-25	+85	°C
Storage Temperature– (Industrial)	-40	+85	°C

* Stress beyond the Absolute Maximum Rating conditions may result in permanent damage to the device. These are stress ratings only and functional operation should be restricted to those indicated in the operational sections of this specification. Exposure to conditions beyond recommended, up to and including the Absolute Maximum Rating conditions, for extended periods may affect device reliability.

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5.3 DC Characteristics

5.3.1 Bus Operation Conditions for 3.3 V Signaling

Table 9: Threshold Level for High Voltage Range

Symbol	Parameter	Min	Max	Unit	
V_{DD}	Supply Voltage	2.7	3.6	V	
V_{OH}	Output High Voltage	0.75*V_{DD}	-	V	(I_{OH}= 2mA V_{DD} Min)
V_{OL}	Output Low Voltage	-	0.125*V_{DD}	V	(I_{OL} = 2mA V_{DD} Min)
V_{IH}	Input High Voltage	0.625*V_{DD}	V_{DD}+0.3	V	
V_{IL}	Input Low Voltage	V_{SS}-0.3	0.25*V_{DD}	V	
-	Power Up Time	-	250	ms	(0V to V_{DD} Min)

Table 10: Peak Voltage and Leakage Current

Parameter	Min	Max	Unit
Peak voltage on all lines	-0.3	V_{DD}+0.3	V
All Inputs			
Input Leakage Current	-10	10	µA
All Outputs			
Output Leakage Current	-10	10	µA

5.3.2 Bus Operation Conditions for 1.8 VSignaling

Table 11: Threshold Level for 1.8 V Signaling

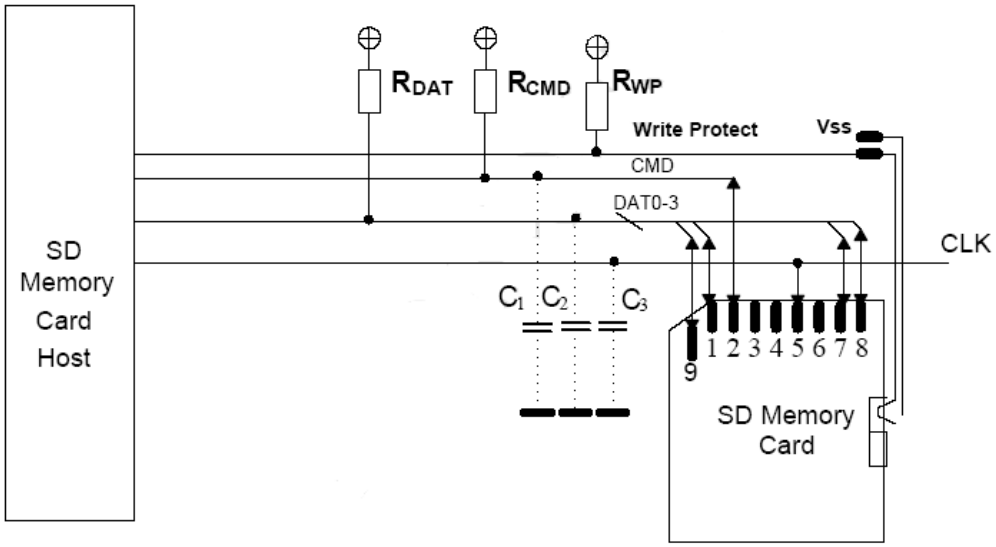
Symbol	Parameter	Min	Max	Unit	Conditions
V_{DD}	Supply Voltage	2.7	3.6	V	
V_{DDIO}	Regulator Voltage	1.7	1.95	V	Generated by VDD
V_{OH}	Output High Voltage	1.4	-	V	I_{OH} = 2mA
V_{OL}	Output Low Voltage	-	0.45	V	I_{OL} = 2mA
V_{IH}	Input High Voltage	1.27	2.00	V	
V_{IL}	Input Low Voltage	VSS-0.3	0.58	V	

Table 12: Input Leakage Current for 1.8V Signaling

Parameter	Min	Max	Unit	Conditions
Input Leakage Current	-2	2	µA	DAT3 pull-up is disconnected.

5.3.3 Bus Signal Line Load

Figure 4: Bus Circuitry Diagram



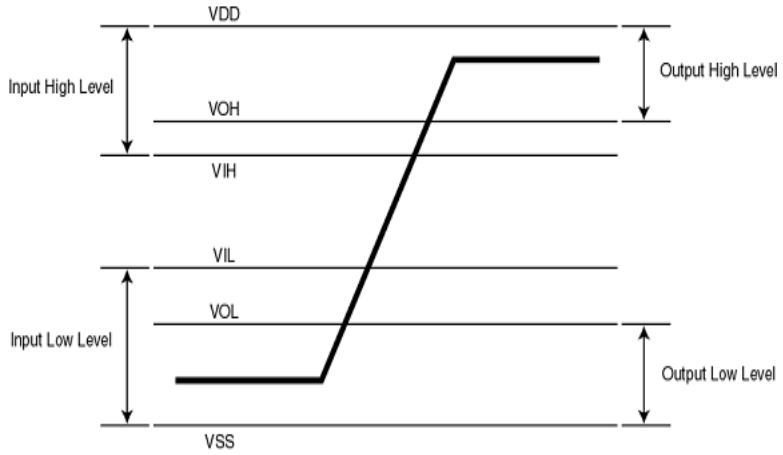
5.3.4 Bus Signal Line Loading (Recommended)

Table 13: Bus Signal Line Loading (recommended)

Symbol	Parameter	Min	Max	Units	Remark
R_{CMD}	Pull-up Resistor for CMD Signal	10	100	kΩ	to prevent bus floating
R_{DAT}	Pull-up Resistor for DAT Signals	10	100	kΩ	to prevent bus floating
C_L	Total bus capacitance for each signal line		40	pF	1 card CHOST+CBUS shall not exceed 30 pF
CCARD	Card Capacitance for each signal pin		10	pF	
-	Maximum signal line inductance		16	nH	
RDAT3	Pull-up resistance inside card	10	90	kΩ	May be used for card detection
CC	Capacity Connected to Power Line		5	µF	To prevent inrush current

6. AC CHARACTERISTICS

Figure 5: Bus Signal Levels



6.1 SD Interface timing (Default Mode)

Figure 6: Card Input Timing (Default Speed Card)

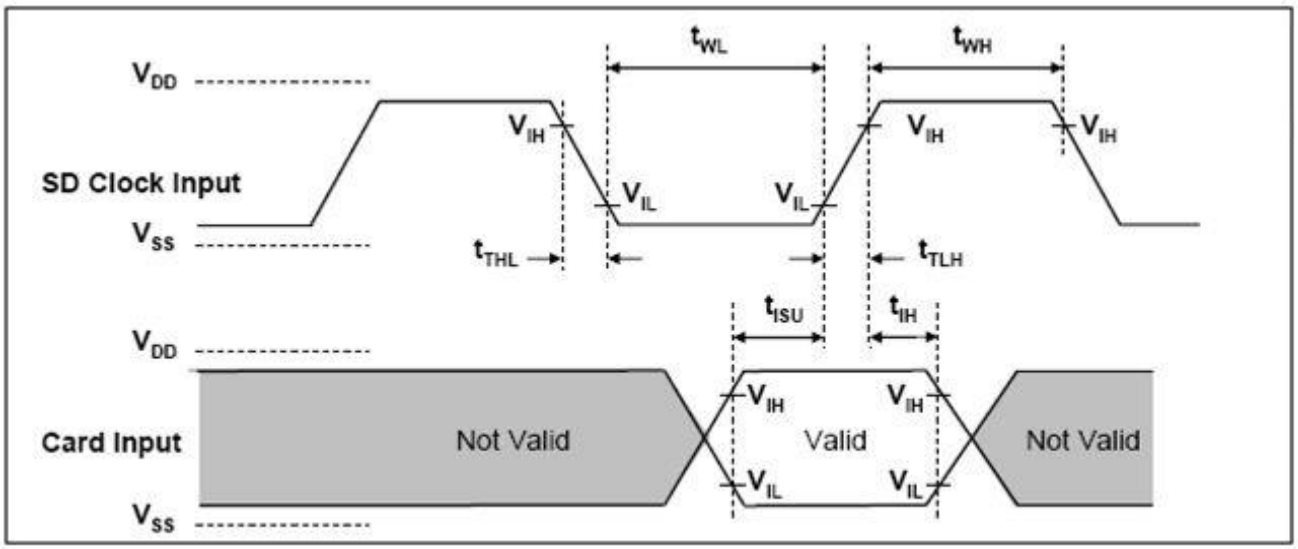


Figure 7: Card Output Timing (Default Speed Card)

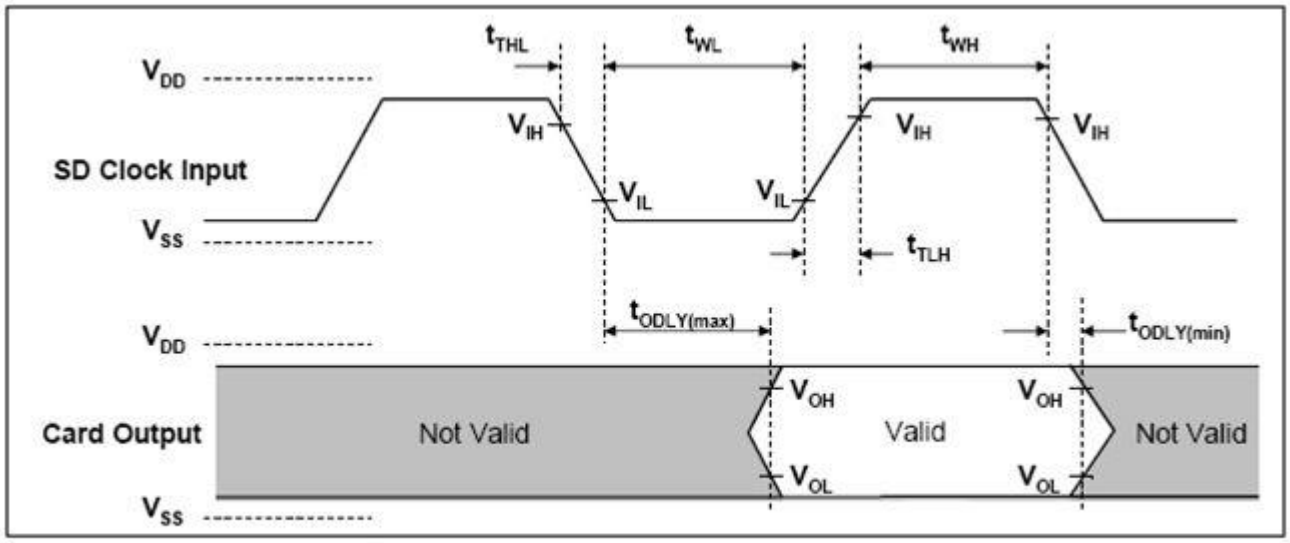


Table 14: Card Output Timing (Default Speed Mode)

Symbol	Parameter	Min	Max	Unit	Remark(1)
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
f_{PP}	Clock frequency data transfer mode	0	25	MHz	Ccard ≤ 10 pF
f_{OD}	Clock	0(2)/100	400	kHz	
t_{WL}	Clock low time	10		ns	Ccard ≤ 10 pF
t_{WH}	Clock high time	10		ns	Ccard ≤ 10 pF
t_{TL}	Clock rise time		10	ns	Ccard ≤ 10 pF
t_{TH}	Clock fall time		10	ns	Ccard ≤ 10 pF
Inputs CMD, DAT (referenced to CLK)					
t_{IS}	Input setup time	5		ns	Ccard ≤ 10 pF
t_{IH}	Input hold time	5		ns	Ccard ≤ 10 pF
Outputs CMD, DAT (reference to CLK)					
t_{ODLY}	Output delay time during Data Transfer	0	14	ns	C_L ≤ 40 pF
t_{ODLY}	Output delay time during Data Identification mode	0	50	ns	C_L ≤ 40 pF

(1) Values are for 1 card.

(2) 0Hz means to stop the clock. The given minimum frequency range is for cases where continuous clock is required.

6.2 SD Interface timing (High Speed Mode)

Figure 8: Interface Timing (High Speed Mode)

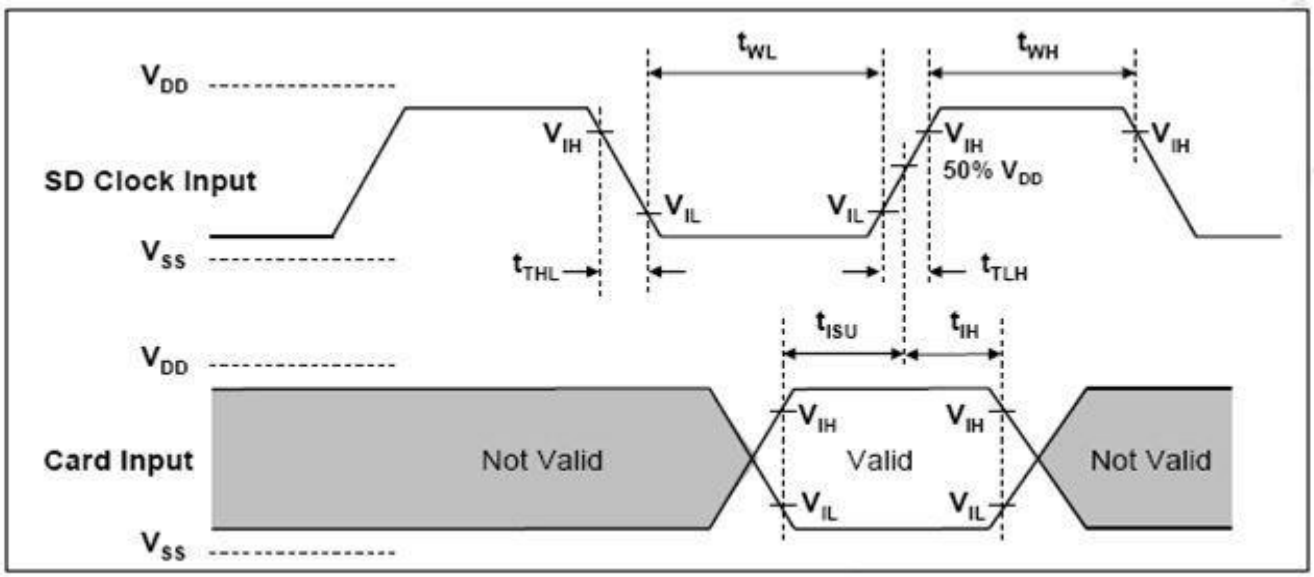


Figure 9: Card Output Timing (High Speed Mode)

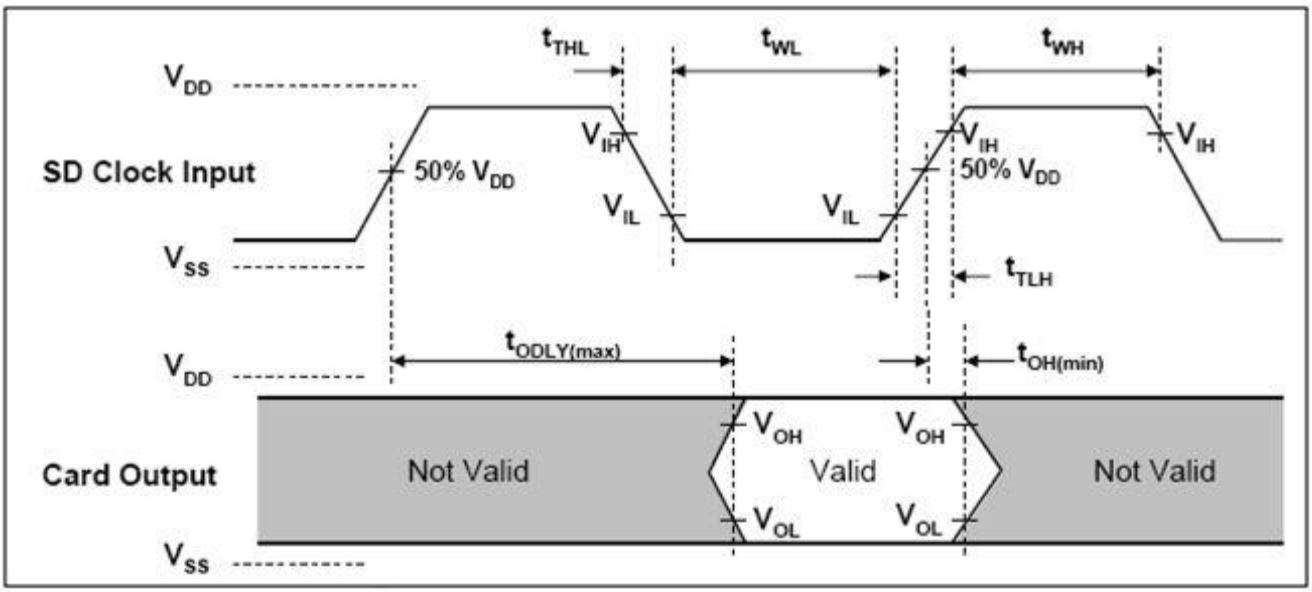


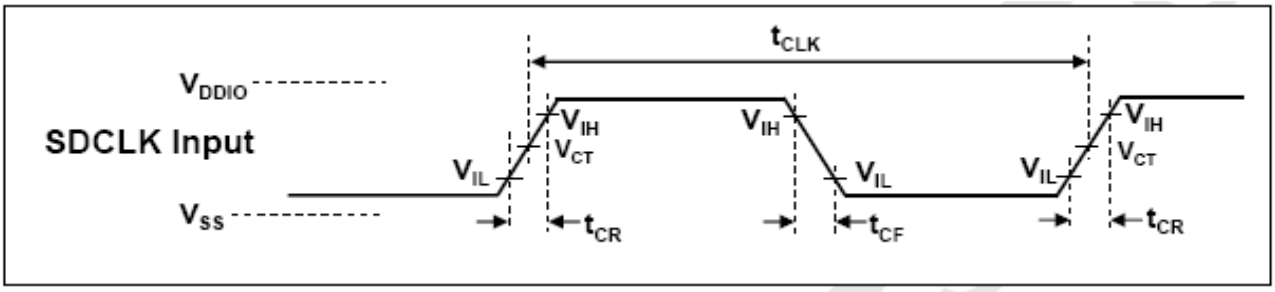
Table 15: SD Interface Timing Clock Values (High Speed Mode)

Symbol	Parameter	Min	Max	Unit	Remark[1]
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
f_{PP}	Clock frequency data transfer mode	0	50	MHz	Ccard ≤ 10 pF
t_{WL}	Clock low time	7	-	ns	Ccard ≤ 10 pF
t_{WH}	Clock high time	7	-	ns	Ccard ≤ 10 pF
t_{TLH}	Clock rise time	-	3	ns	Ccard ≤ 10 pF
t_{THL}	Clock fall time	-	3	ns	Ccard ≤ 10 pF
Inputs CMD, DAT (referenced to CLK)					
t_{IS}	Input setup time	6	-	ns	Ccard ≤ 10 pF
t_{IH}	Input hold time	2	-	ns	Ccard ≤ 10 pF
Outputs CMD, DAT (reference to CLK)					
t_{ODLY}	Output delay time during Data Transfer Mode	-	14	ns	C_L ≤ 40 pF
t_{OH}	Output Hold Time	2.5	-	ns	C_L ≤ 40 pF
c_L	Total System Capacitance of each line	-	40	pF	C_L ≤ 15 pF

(1) In order to satisfy server timing, host shall drive only one card.

6.3 SD Interface timing (SDR12, SDR25, SDR50, and SDR104 Modes)

Figure 10: Input Clock Signal Timing



Symbol	Min	Max	Unit	Remark
t_{CLK}	4.80	-	ns	208MHz (Max), Between rising edge, V_{CT} = 0.975V
t_{CR}, t_{CF}	-	0.2 * t_{CLK}	ns	t_{CR}, t_{CF} < 2.00ns (max) at 100 MHz, C_{CARD} = 10pF
Clock Duty	30	70	%	

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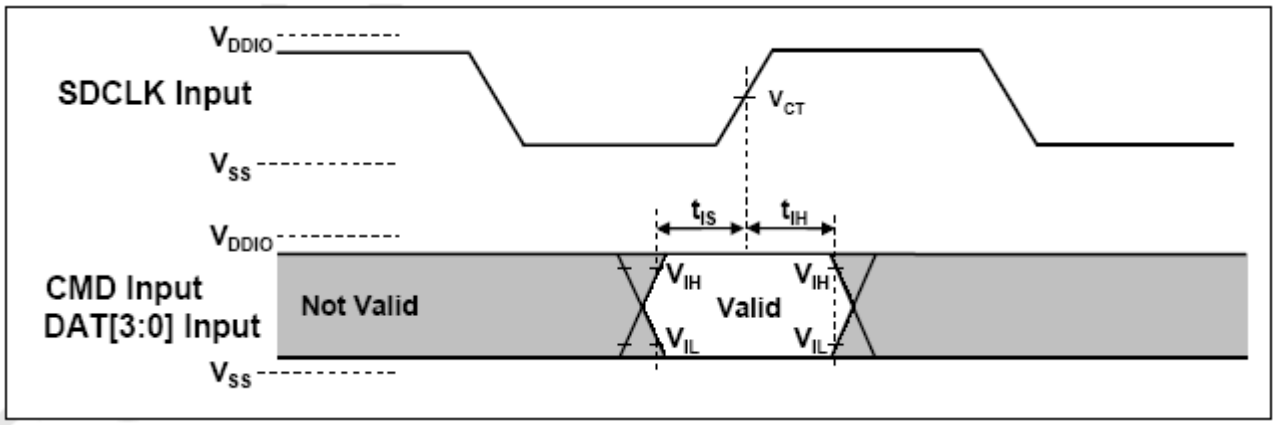
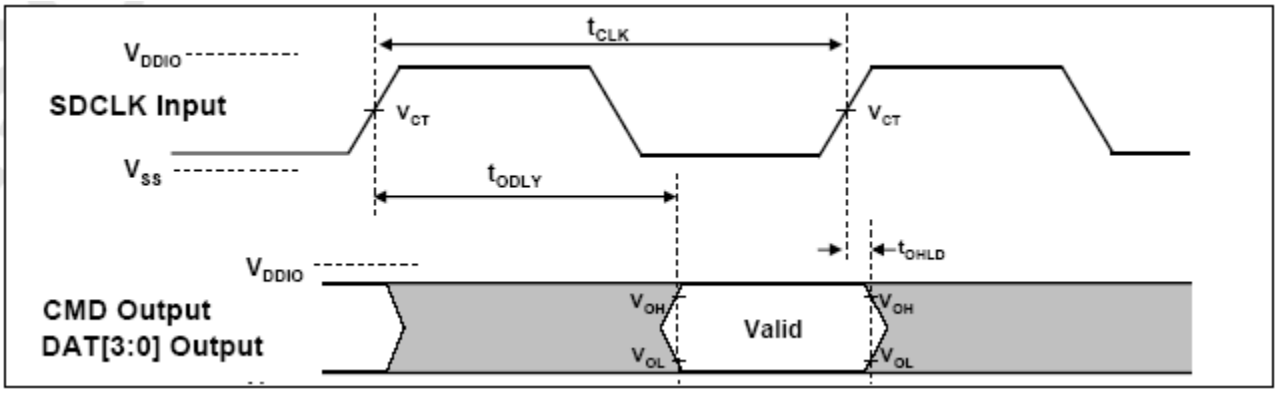
Figure 11: Card Input Timing (SDR50 and SDR104)



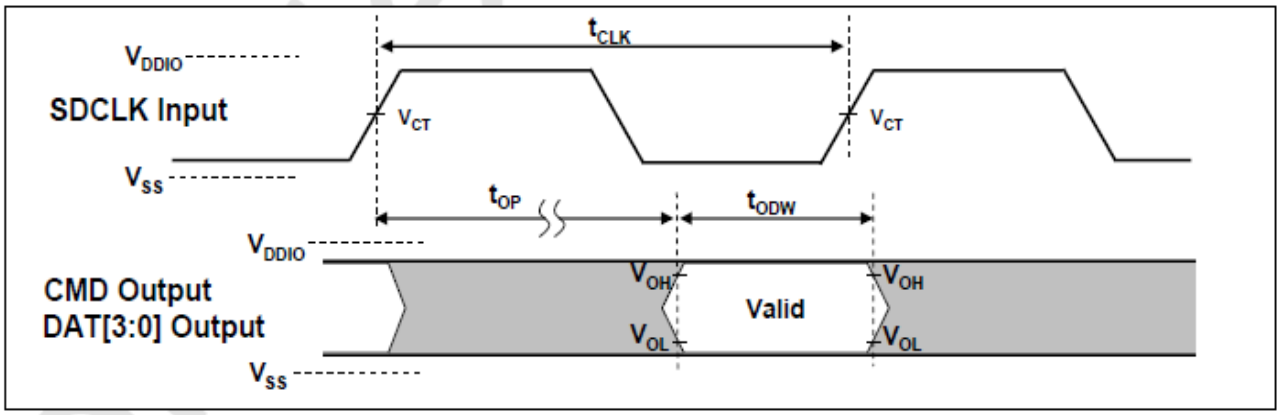
Symbol	Min	Max	Unit	SDR104 mode
t_{IS}	1.40	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5pF, V_{CT} = 0.975V
Symbol	**Min**	**Max**	**Unit**	**SDR50 mode**
t_{IS}	3.00	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5pF, V_{CT} = 0.975V

Figure 12: Output Timing - Fixed Data Window (SDR12, SD25, SDR50)



Symbol	Min	Max	Unit	Remark
t_{ODLY}	-	7.5	ns	tCLK>=10.0ns, CL=30pF, using driver Type B, for SDR50
t_{ODLY}	-	14	ns	tCLK>=20.0ns, CL=40pF, using driver Type B, for SDR25 and SDR12,
t_{OH}	1.5	-	ns	Hold time at the tODLY (min.), CL=15pF

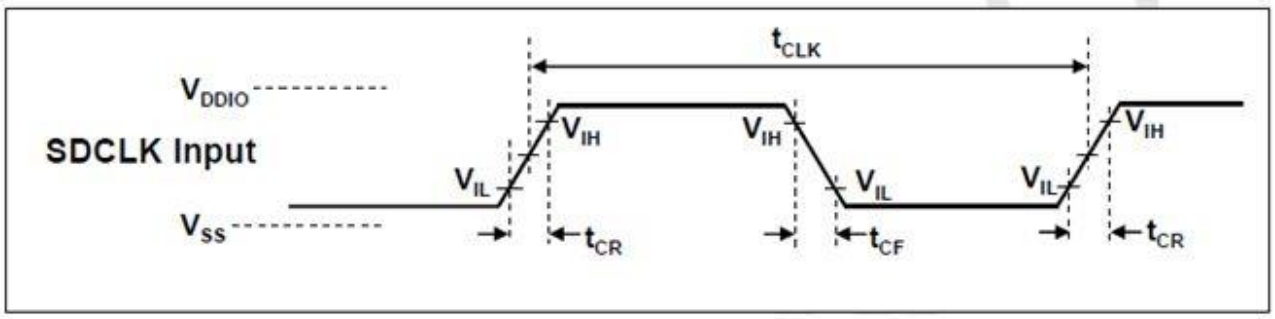
Figure 13: Output Timing - Variable Window (SDR104)



Symbol	Min	Max	Unit	Remark
t_{OP}	0	2	UI	Card Output Phase
Δt_{OP}	-350	+1550	ps	Delay variation due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW} = 2.88ns at 208MHz

6.4 SD Interface timing (DDR50 Modes)

Figure 14: SD Interface Timing (DDR50 Modes)



Symbol	Min	Max	Unit	Remark
t_{CLK}	20	-	UI	50MHz (Max) Between rising edge
t_{CR}	-	0.2 * t_{CLK}	ns	t_{CR}, t_{CF} < 4.00ns (max) at 50MHz, CCARD = 10pF
Clock Duty	45	55	%	

Figure 15: DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

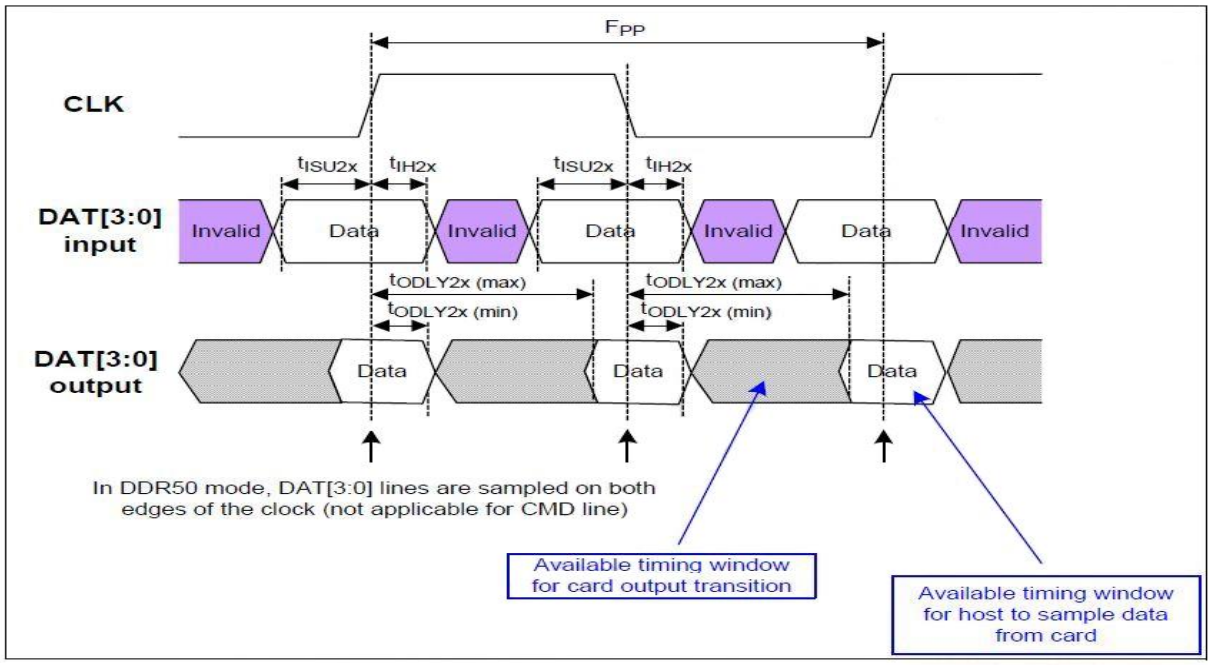


Table 16: Bus Timings – Parameters Values (DDR50 Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	6	-	ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	13.7	ns	C_L≤30 pF (1 card)
Output Hold time	t_{OH}	1.5	-	ns	C_L≥15 pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2x}	3	-	ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	C_L≤25 pF (1 card)
Output Hold time	t_{OH2x}	1.5	-	ns	C_L≥15 pF (1 card)

7. REGISTERS

The supported microSD registers used in the SMART MicroSD cards are shown in the table below. CID, RCA, CSD, SDR, and OCR registers are described in detail in the sections that follow.

Table 17: Supported microSD Registers

Name	Width	Description
CID	128	Card Identification
RCA	16	Relative Card Address
CSD	128	Card Specific Data
SCR	64	SD Configuration Register
OCR	32	Operation Condition Register
SSR	512	SD Status Register

7.1 Card Identification Register (CID)

The Card Identification (CID) register is 128 bits wide. It contains the information used during the card identification phase. Every individual flash card will have a unique identification number. The fields for the CID register are presented in the following table.

Table 18: Card Identification Register (CID) Fields

Bits	Width	Name	Field	Value	
[127:120]	8	Manufacturer ID	MID	0x27	
[119:104]	16	OEM/Application ID	OID	0x5048	
[103:64]	40	Product Name	PNM	8GB	SD08G
				16GB	SD16G
				32GB	SD32G
				64GB	SD64G
[63:56]	8	Product Revision	PRV	3.0 (0x30)(1)	
[55:24]	32	Product Serial Number	PSN	--(2)	
[23:20]	4	Reserved	--	--	
[19:8]	12	Manufacturing Date	MDT	--(2)	
[7:1]	7	CRC7 Checksum	CRC	--	
[0]	1	Not used, Always 1	-	1b	

(1)Support SD 3.0 spec, 0x30
(2)Defined by the Card Initialization Tool

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7.2 Relative Card Address (RCA)

The relative card address (RCA) register is 16 bits wide. It contains the card address assigned by the host during the card identification. This address is used for the addressed host-card communication after the identification procedure. The default value of the RCA register is 0x0000.

7.3 Card Specific Data (CSD)

The Card Specific Data (CSD) register is 128 bits wide. It provides information on how to access the card contents. The fields for the CSD register are presented in the following table.

Table 19: Card Specific Data (CSD) Fields

Bits	Width	Name	Field		Value
[127:126]	2	CSD Structure	CSD_STRUCTURE		01b
[125:120]	6	Reserved	---		00 0000b
[119:112]	8	Data Read Access Time 1	TAAC		0x0E
[111:104]	8	Data Read Access Time 2	NSAC		0x00
[103:96]	8	Max. Bus Clock Frequency	TRAN_SPEED(1)		0x32
[95:84]	12	Card Command Classes	CCC(2)		0x5B5
[83:80]	4	Max Read Block Data Length	READ_BL_LEN(3)		0x9
[79]	1	Partial Block Read Allowed	READ_BL_PARTIAL		0b
[78]	1	Write Block Misalignment	WRITE_BLK_MISALIGN		0b
[77]	1	Read Block Misalignment	READ_BLK_MISALIGN		0b
[76]	1	DSR implemented	DSR_IMP		0b
[75:70]	6	Reserved	---		00 0000b
[69:48]	22	Device Size	C_SIZE	8GB	00 0011 1011 0101 1111 b
				16GB	00 0111 0111 0101 1111b
				32GB	00 1110 1111 0011 1111b
				64GB	01 1101 1110 0111 1111b
[47]	1	Reserved	---		0b
[46]	1	Erase Single Block Enable	ERASE_BLK_EN		1b
[45:39]	7	Erase Sector Size	SECTOR_SIZE		111 1111b
[38:32]	7	Write Protect Group Size	WP_GRP_SIZE		000 0000b
[31]	1	Write Protect Group Enable	WP_GRP_ENABLE		0b
[30:29]	2	Reserved	---		00b
[28:26]	3	Write Speed Factor	R2W_FACTOR		010b
[25:22]	4	Max Write Data Block Length	WRITE_BL_LEN(3)		0x9
[21]	1	Partial Block Write Allowed	WRITE_BL_PARTIAL		0b

Bits	Width	Name	Field	Value
[20:16]	5	Reserved	---	0 0000b
[15]	1	File Format Group	FILE_FORMAT_GRP	0b
[14]	1	Copy Flag	COPY	0b
[13]	1	Permanent Write Protection	PERM_WRITE_PROTECT	0b
[12]	1	Temporary Write Protection	TMP_WRITE_PROTECT	0b
[11:10]	2	File Format	FILE_FORMAT	00b
[9:8]	2	Reserved	---	00b
[7:1]	7	CRC	CRC	--
[0]	1	Not used, Always '1'	---	1

(1) Value depends on the Card Type and mode.
(2) Support command class: 0, 2, 4, 5, 6, 7, 8 and 10. (Including Basic, Block Read/Write, Erase, Lock Card, Application specific and switch. Not supported command class: 1, 3, 6 and 9 (Including Write-Protection, I/O mode).
(3) This field is fixed to 9h, which indicates READ_BL_LEN / WRITE_BL_LEN = 512 Byte.

7.4 SD Configuration Register (SCR)

The SD Configuration Register (SCR) is 64 bits wide. It is another configuration register. SCR provides information about the SD card's special features that were configured into the given card. The fields for the SDR register are presented in the following table.

Table 20: SD Configuration Register (SCR) Fields

Bits	Width	Name	Field		Value (Binary)
[63:60]	4	SCR Structure	SCR_STRUCTURE		0000
[59:56]	4	SD Card Spec. Version	SD_SPEC		0010
[55]	1	Data Status After Erase	DATA_STAT_AFTER_ERASE		0
[54:52]	3	SD Security Support	SD_SECURITY	8GB - 32GB	011
				64GB	100
[51:48]	4	DAT Bus Width Support	SD_BUS_WIDTHS		0101
[47]	1	Spec. Version 3.00 or Higher	SD_SPEC3		1
[46:43]	4	Extended Security Support	EX_SECURITY		0000
[42:34]	9	Reserved	-		-
[33:32]	2	Command Support bits	CMD_SUPPORT	8GB - 32GB	10
				64GB	11
[31:0]	32	Reserved	-		-

7.5 Operation Condition Register (OCR)

The Operation Condition Register (OCR) register is 32 bits wide. The fields for the OCR register are presented in the following table.

Table 21: Operation Condition Register (OCR) Fields

OCR Bit position	Width	OCR Fields Defintion	Value (Binary)
[0:6]	7	Reserved	000 0000
[7]	1	Reserved for Low Voltage Range	0
[8:14]	7	Reserved	000 0000
[15]	1	2.7-2.8	1
[16]	1	2.8-2.9	1
[17]	1	2.9-3.0	1
[18]	1	3.0-3.1	1
[19]	1	3.1-3.2	1
[20]	1	3.2-3.3	1
[21]	1	3.3-3.4	1
[22]	1	3.4-3.5	1
[23]	1	3.5-3.6	1
[24]	1	Switching to 1.8V Accepted (S18A) (1)	--
[25:29]	5	Reserved	0 0000
[30]	1	Card Capacity Status (CCS) (2)	1
[31]	1	Card Power Up Status Bit(3)	1

(1) Only UHS-I card supports this bit.
(2) This bit is valid only when the card power up status bit is set.
(3) This bit is set to LOW if the card has not finished the power up routine.

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7.6 SD Status Register

The SD Status Register (SSR) is 512 bits wide and provides information about the SD card's proprietary features and may be used for application-specific usage. The fields for the SSR register are presented in the following table.

Table 22: SD Status Register (SSR) Fields

Bits	Width	Field	Value	
[511:510]	2	DAT_BUS_WIDTH	10b	
[509]	1	SECURED_MODE	0b	
[508:502]	7	Reserved	--	
[501:496]	6	Reserved	--	
[495:480]	16	SD_CARD_TYPE	0x0000	
[479:448]	32	SIZE_OF_PROTECTED_AREA(1)	8GB	0x03000000
			16GB	0x04000000
			32GB	0x05000000
			64GB	0x08000000
[447:440]	8	SPEED_CLASS	0x04	
[439:432]	8	PERFORMANCE_MOVE	0x00	
[431:428]	4	AU_SIZE	8GB - 32GB	0x9
			64GB	0xF
[427:424]	4	Reserved	--	
[423:408]	16	ERASE_SIZE	0x0200	
[407:402]	6	ERASE_TIMEOUT	10 1010b	
[401:400]	2	ERASE_OFFSET	10b	
[399:396]	4	UHS_SPEED_GRADE(2)	0x1	
[395:392]	4	UHS_AU_SIZE	0xF	
[391:312]	80	Reserved	--	
[311:0]	312	Reserved	Reserved for manufacturer	

(1) Value depends on the Card Type and mode
(2) Internal device performance exceeds SD spec. v3.01 UHS Speed Grade 1 criteria

8. PART NUMBERS

8.1 Part Numbering Information

Table 23: Part Number Information

SMART Part Number*	Drive Capacity	Formatted FAT Capacity (Bytes)	Unformatted Capacity (C_Size correlated) (Bytes)
SS9UD008GPHECMx21	8GB	7,960,788,992	7,969,177,600
SS9UD016GPHECMx21	16GB	16,013,852,672	16,022,241,280
SS9UD032GPHECMx21	32GB	32,099,008,512	32,111,591,424
SS9UD064GPHECMx21	64GB	64,189,628,416	64,223,182,848

* x = I for Industrial Temperature, C for Commercial Temperature

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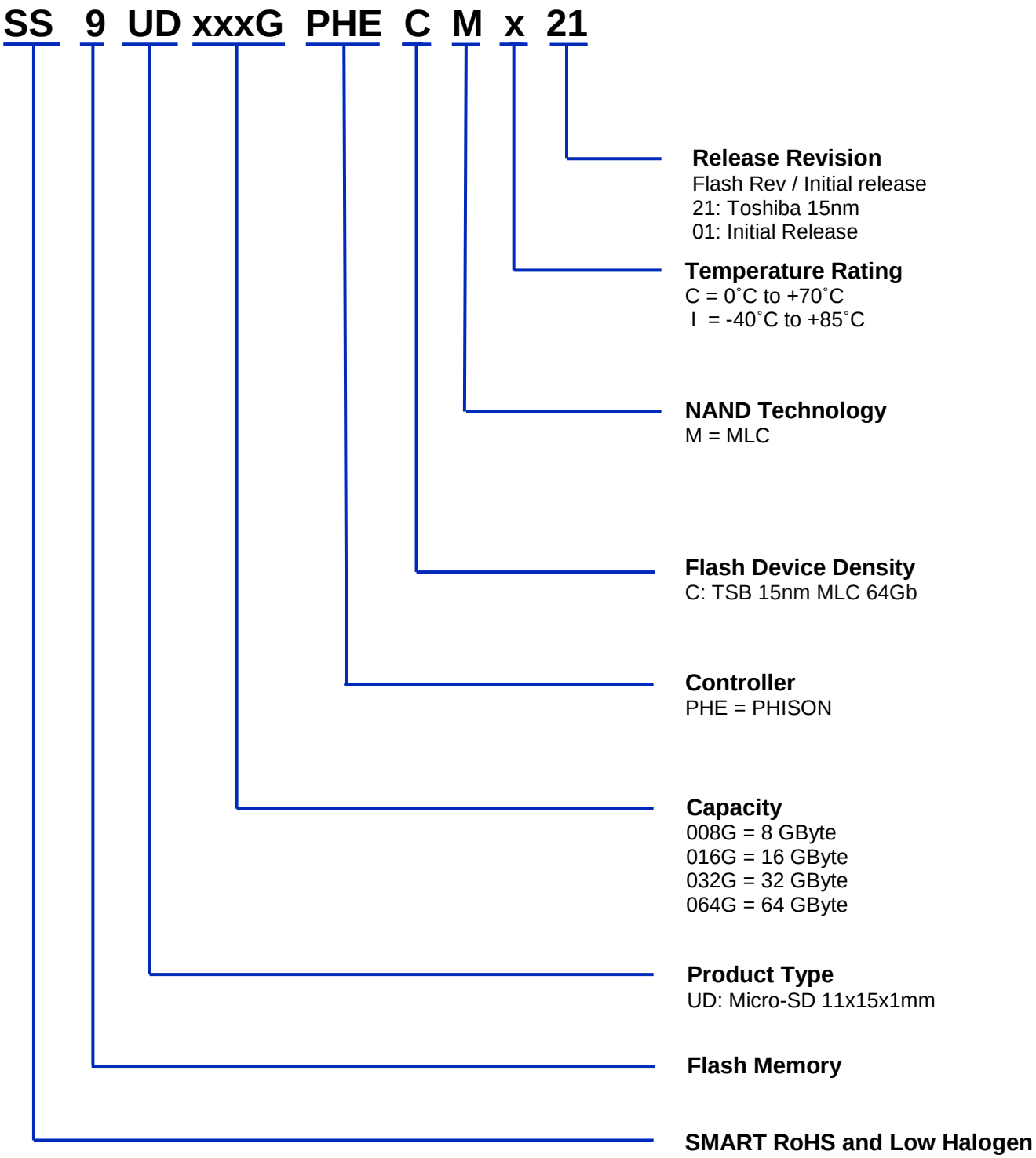
8.2 Part Number Decoder



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