SLG59M1658V

An Ultra-small 1.6 mm^2, 17 mΩ, 2.5 A, 125°C-Rated Internally-protected Integrated Power Switch with Discharge

General Description

The SLG59M1658V is a high performance 17 mΩ, 2.5 A single-channel nFET integrated power switch which can operate with a 2.5 V to 5.5 V V_{DD} supply to switch power rails from as low as 0.9 V up to the supply voltage. The SLG59M1658V incorporates two-level overload current protection, thermal shutdown protection, fast output voltage discharge, and in-rush current control which can easily be adjusted by a small external capacitor.

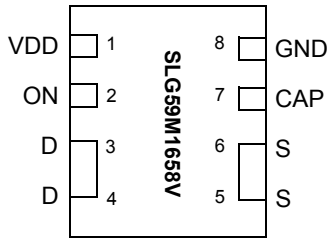
Using a proprietary MOSFET design, the SLG59M1658V achieves a stable 17 mΩ RDS_{ON} across a wide input voltage range. In addition, the SLG59M1658V's package also exhibits low thermal resistance for high-current operation using Silego's proprietary CuFET technology.

Fully specified over the -40 °C to 125 °C temperature range, the SLG59M1658V is packaged in a space-efficient, low thermal resistance, RoHS-compliant 1.0 mm x 1.6 mm STDFN package.

Features

- 1.0 x 1.6 x 0.55 mm STDFN 8L package (2 fused pins for drain and 2 fused pins for source)
- Logic level ON pin capable of supporting 0.85 V CMOS Logic
- User selectable ramp rate with external capacitor
- 17 mΩ RDS_{ON} while supporting 2.5 A
- Discharges load when off
- Two Over Current Protection Modes
  - Short Circuit Current Limit
  - Active Current Limit
- Over Temperature Protection
- Pb-Free / Halogen-Free / RoHS compliant
- Operating Temperature: -40 °C to 125°C
- Operating Voltage: 2.5 V to 5.5 V

Pin Configuration

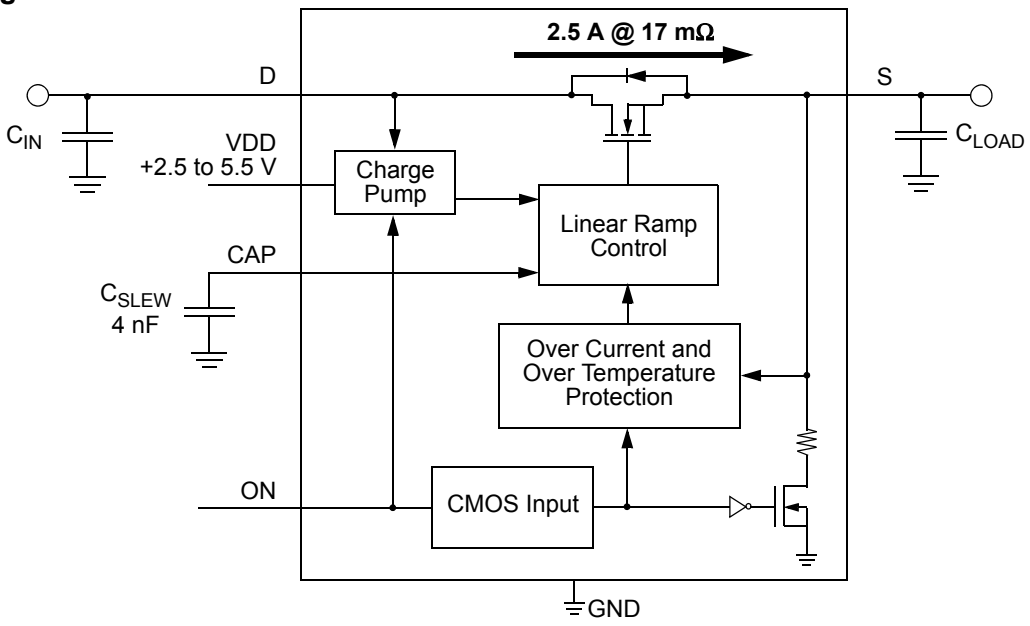


8-pin STDFN
(Top View)

Applications

- Notebook Power Rail Switching
- Tablet Power Rail Switching
- Smartphone Power Rail Switching

Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	With an internal 1.8 V UVLO threshold, VDD supplies the power for the operation of the power switch and internal control circuitry. Bypass the VDD pin to GND with a 0.1 µF (or larger) capacitor.
2	ON	Input	A low-to-high transition on this pin initiates the operation of the SLG59M1658V's state machine. ON is a CMOS input with V_{IL} < 0.25 V and V_{IH} > 0.85 V thresholds. While there is an internal pull-down circuit to GND (~4 MΩ), connect this pin directly to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller. Do not allow this pin to be open-circuited.
3, 4	D	MOSFET	Drain terminal connection of the n-channel MOSFET (2 pins fused for V_D). Connect at least a low-ESR 0.1 µF capacitor from this pin to ground. Capacitors used at V_D should be rated at 10 V or higher.
5, 6	S	MOSFET	Source terminal connection of the n-channel MOSFET (2 pins fused for V_S). Connect a low-ESR capacitor from this pin to ground and consult the Electrical Characteristics table for recommended C_{LOAD} range. Capacitors used at V_S should be rated at 10 V or higher.
7	CAP	Input	A low-ESR, stable dielectric, ceramic surface-mount capacitor connected from CAP pin to GND sets the V_S slew rate and overall turn-on time of the SLG59M1658V. For best performance C_{SLEW} value should be ≥ 1.5 nF and voltage level should be rated at 10 V or higher.
8	GND	GND	Ground connection. Connect this pin to system analog or power ground plane.

Ordering Information

Part Number	Type	Production Flow
SLG59M1658V	STDFN 8L	Extended Industrial, -40 °C to 125 °C
SLG59M1658VTR	STDFN 8L (Tape and Reel)	Extended Industrial, -40 °C to 125 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply		--	--	7	V
V_D to GND	Power Switch Input Voltage to GND		-0.3	--	7	V
V_S to GND	Power Switch Output Voltage to GND		-0.3	--	V_D	V
ON and CAP to GND	ON and CAP Pin Voltages to GND		-0.3	--	7	V
T_S	Storage Temperature		-65	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
ESD_{CDM}	ESD Protection	Charged Device Model	1000	--	--	V
MSL	Moisture Sensitivity Level		1			
θ_{JA}	Thermal Resistance	1.0 x 1.6 mm, 8L STDFN; Determined using 1 in^2, 1 oz. copper pads under each VD and VS terminals and FR4 pcb material	--	74	--	°C/W
W_{DIS}	Package Power Dissipation		--	--	0.4	W
MOSFET IDS	Max Continuous Switch Current		--	--	2.5	A
MOSFET IDS_{PK}	Peak Current from Drain to Source	For no more than 1 ms with 1% duty cycle	--	--	3.5	A

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

T_A = -40 to 125 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage	-40 to 125°C	2.5	--	5.5	V
V_{DD_UVLO}	V_{DD} Undervoltage Lockout Threshold	V_{DD} ↑	--	1.8	--	V
I_{DD}	Power Supply Current (PIN 1)	when OFF; T_A = 70 °C; V_S = 0 V; V_D = V_{DD} = 5.5 V	--	--	1	µA
		when OFF; T_A = 85 °C; V_S = 0 V; V_D = V_{DD} = 5.5 V	--	--	1	µA
		when OFF; T_A = 125 °C; V_S = 0 V; V_D = V_{DD} = 5.5 V	--	--	1	µA
		when ON, no Load	--	75	100	µA
RDS_{ON}	Static Drain to Source ON Resistance	T_A 25°C @ 100 mA	--	17	20.4	mΩ
		T_A 85°C @ 100 mA	--	20.5	24	mΩ
		T_A 125°C @ 100 mA	--	24	28.8	mΩ
V_D	Drain Voltage		0.9	--	V_{DD}	V
I_{FET_OFF}	MOSFET OFF Leakage Current	V_D = V_{DD} = 5.5 V; V_S = 0 V; ON = 0 V; T_A = 70°C	--	--	1	µA
		V_D = V_{DD} = 5.5 V; V_S = 0 V; ON = 0 V; T_A = 85°C	--	--	1	µA
		V_D = V_{DD} = 5.5 V; V_S = 0 V; ON = 0 V; T_A = 125°C	--	--	5	µA

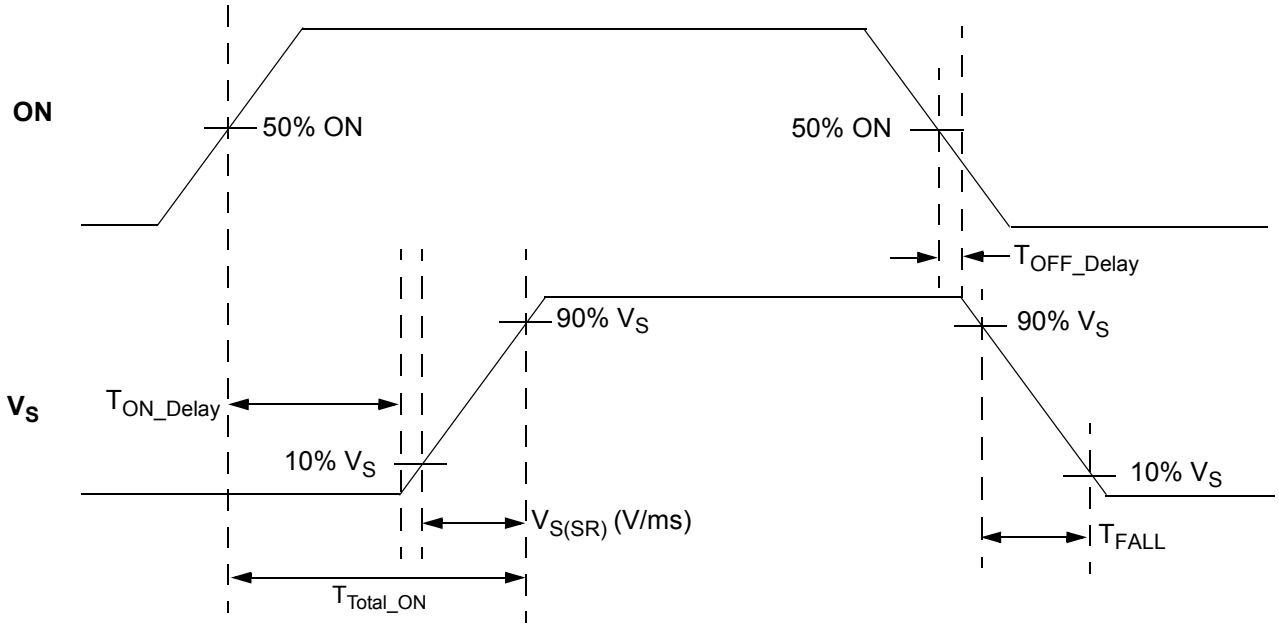
Electrical Characteristics (continued)

T_A = -40 to 125 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
T_{ON_Delay}	ON pin Delay Time	50% ON to Ramp Begin	--	200	--	µs
$V_{S(SR)}$	Slew Rate	10% V_S to 90% V_S	Configurable [1]			V/ms
		Example: C_{SLEW} (PIN 7) = 4 nF, V_{DD} = V_D = 5 V, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω	--	3.3	--	V/ms
T_{Total_ON}	Total Turn On Time	50% ON to 90% V_S	Configurable [1]			ms
		Example: C_{SLEW} (PIN 7) = 4 nF, V_{DD} = V_D = 5 V, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω	--	1.50	--	ms
T_{OFF_Delay}	OFF Delay Time	50% ON to V_S Fall Start, V_{DD} = V_D = 5 V, no C_{LOAD}, R_{LOAD} = 20 Ω	--	8	--	µs
T_{FALL}	V_S Fall Time	90% V_S to 10% V_S, V_{DD} = V_D = 5 V, no C_{LOAD}, R_{LOAD} = 20 Ω	--	3.3	--	µs
C_{LOAD}	Output Load Capacitance	C_{LOAD} connected from V_S to GND	--	--	500	µF
R_{DIS}	Discharge Resistance		100	200	300	Ω
ON_V_{IH}	High Input Voltage on ON pin		0.85	--	V_{DD}	V
ON_V_{IL}	Low Input Voltage on ON pin		-0.3	0	0.25	V
I_{LIMIT}	Active Current Limit (I_{ACL})	MOSFET will automatically limit current when V_S > 250 mV	--	4.5	--	A
	Short Circuit Current Limit (I_{SCL})	MOSFET will automatically limit current when V_S < 250 mV	--	0.5	--	A
$THERM_{ON}$	Thermal shutoff turn-on temperature		--	150	--	°C
$THERM_{OFF}$	Thermal shutoff turn-off temperature		--	130	--	°C
$THERM_{TIME}$	Thermal shutoff time		--	--	1	ms

Notes:
1. Refer to table for configuration details.

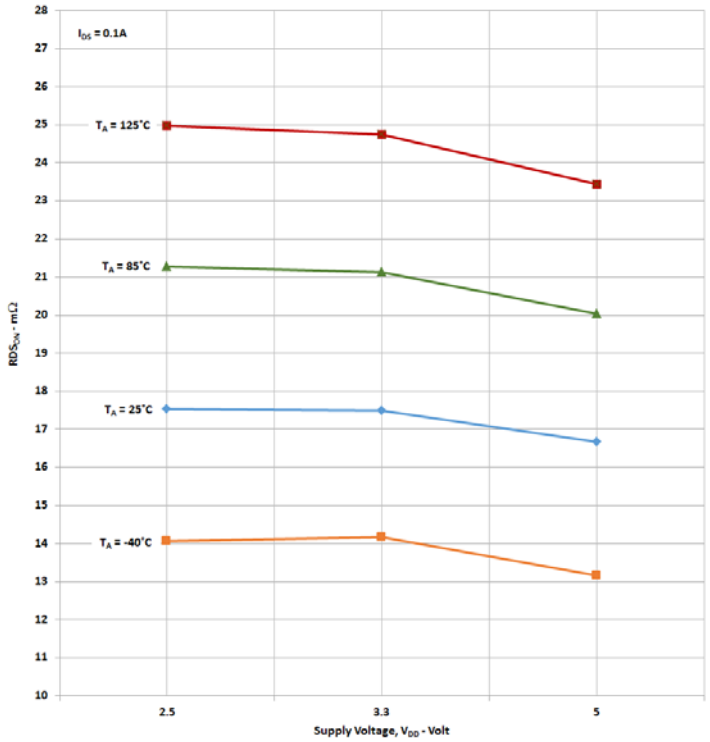
T_{Total_ON}, T_{ON_Delay} and Slew Rate Measurement



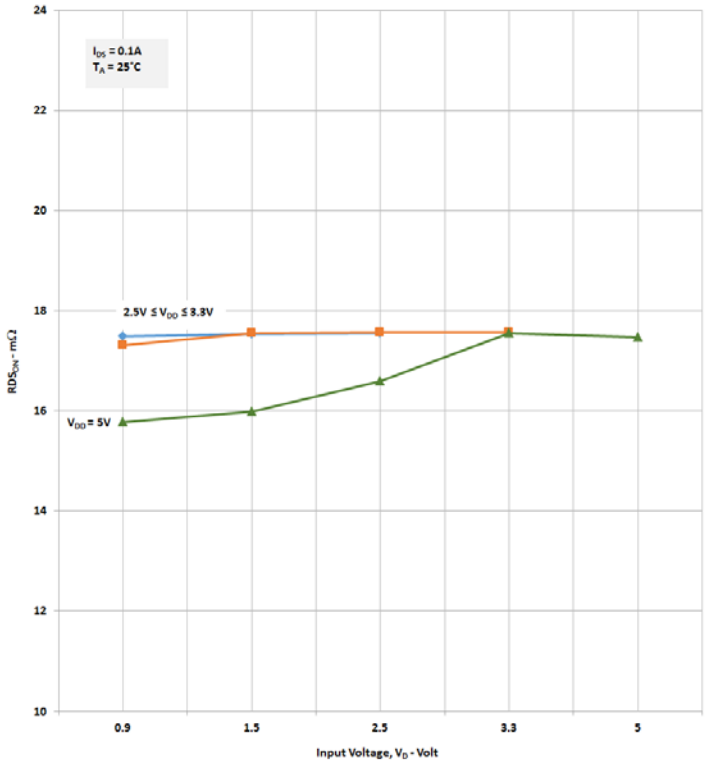
Note: Rise and Fall times of the ON signal are 100 ns

Typical Performance Characteristics

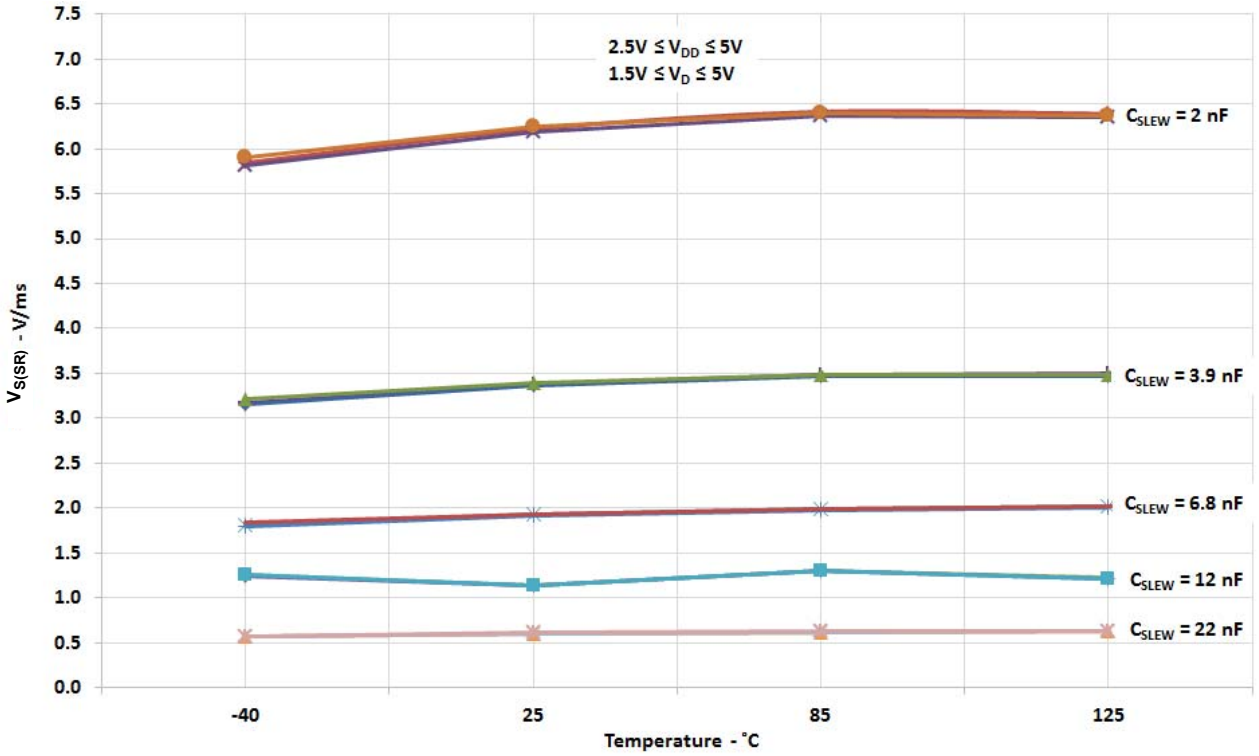
RDS_{ON} vs. V_{DD}, and Temperature



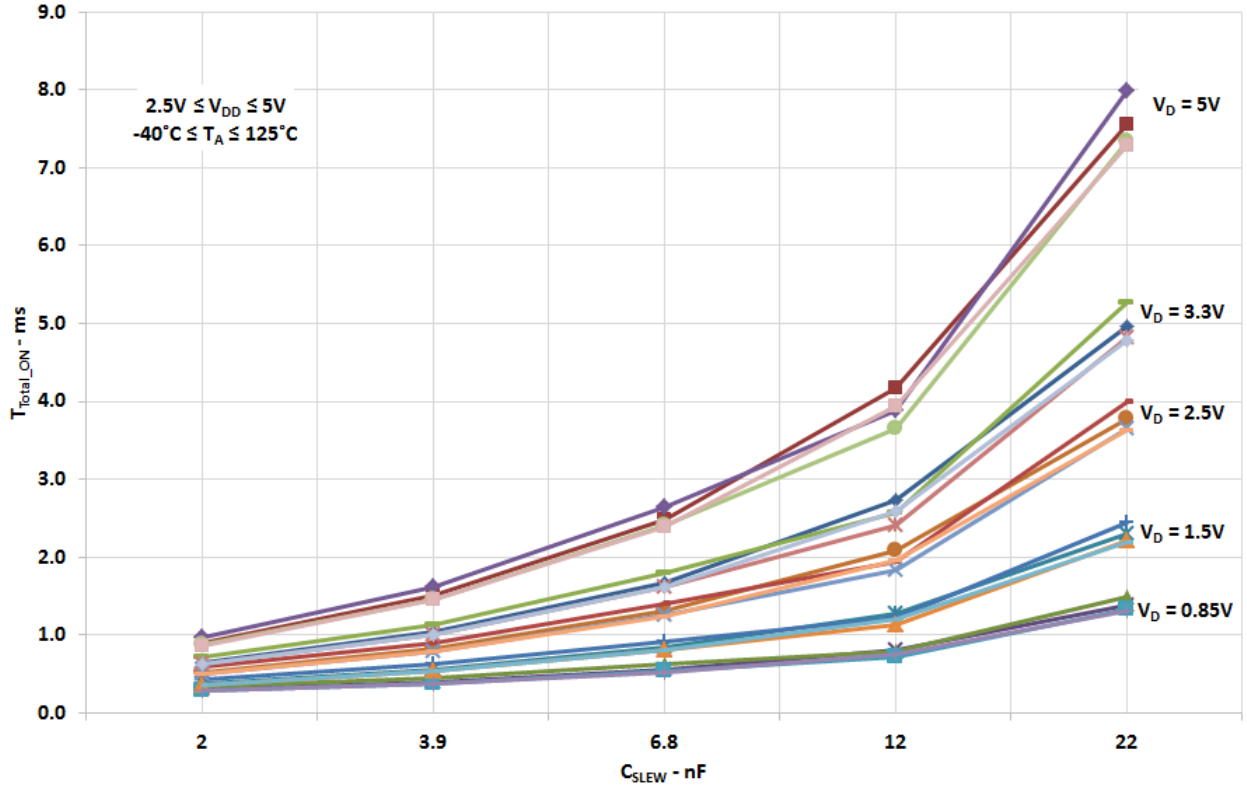
RDS_{ON} vs. V_D and V_{DD}



$V_{S(SR)}$ vs. Temperature, V_D, V_{DD}, and C_{SLEW}



$T_{Total\ ON}$ vs. C_{SLEW}, V_D, V_{DD}, and Temperature



Typical Operation Waveforms

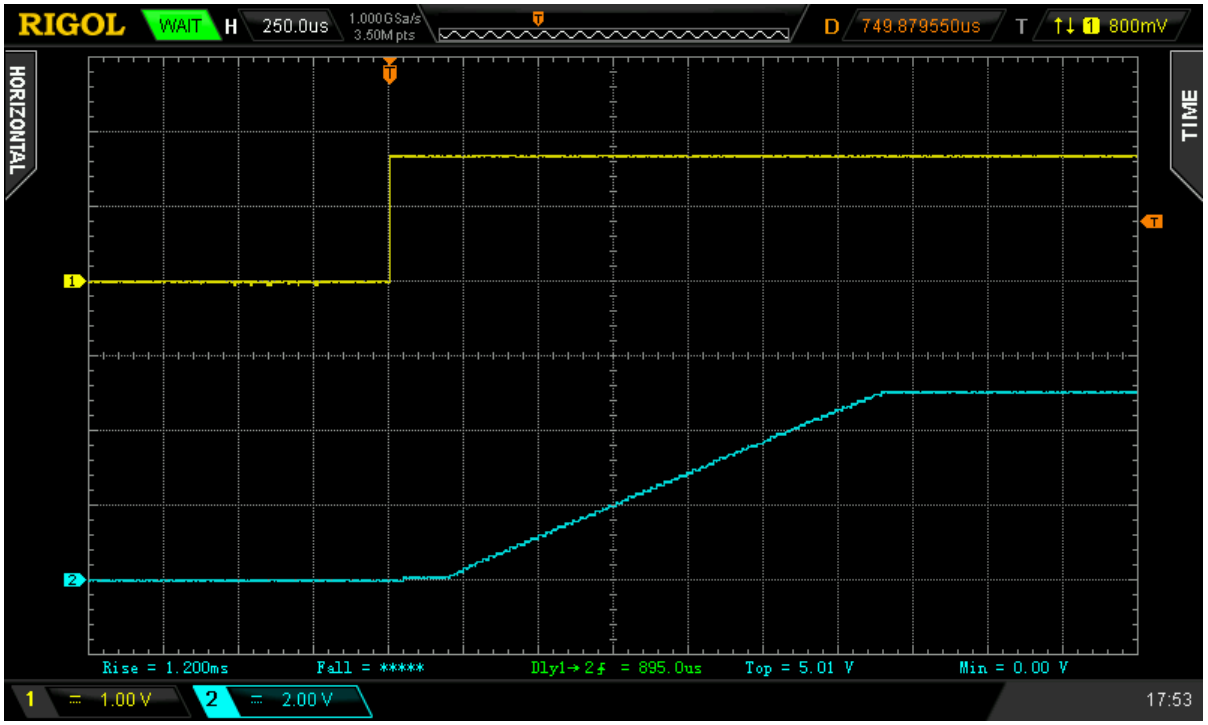


Figure 1. Typical Turn ON operation waveform for V_{DD} = V_D = 5 V, C_{SLEW} = 4 nF, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω

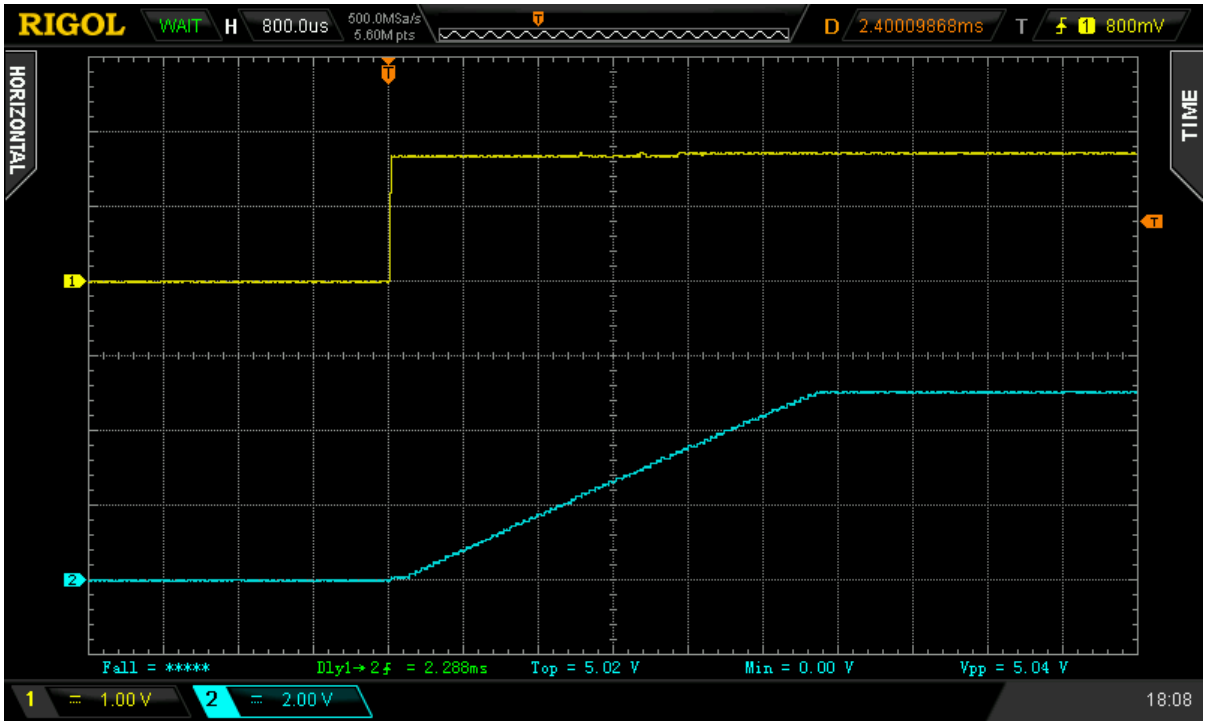


Figure 2. Typical Turn ON operation waveform for V_{DD} = V_D = 5 V, C_{SLEW} = 12 nF, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω

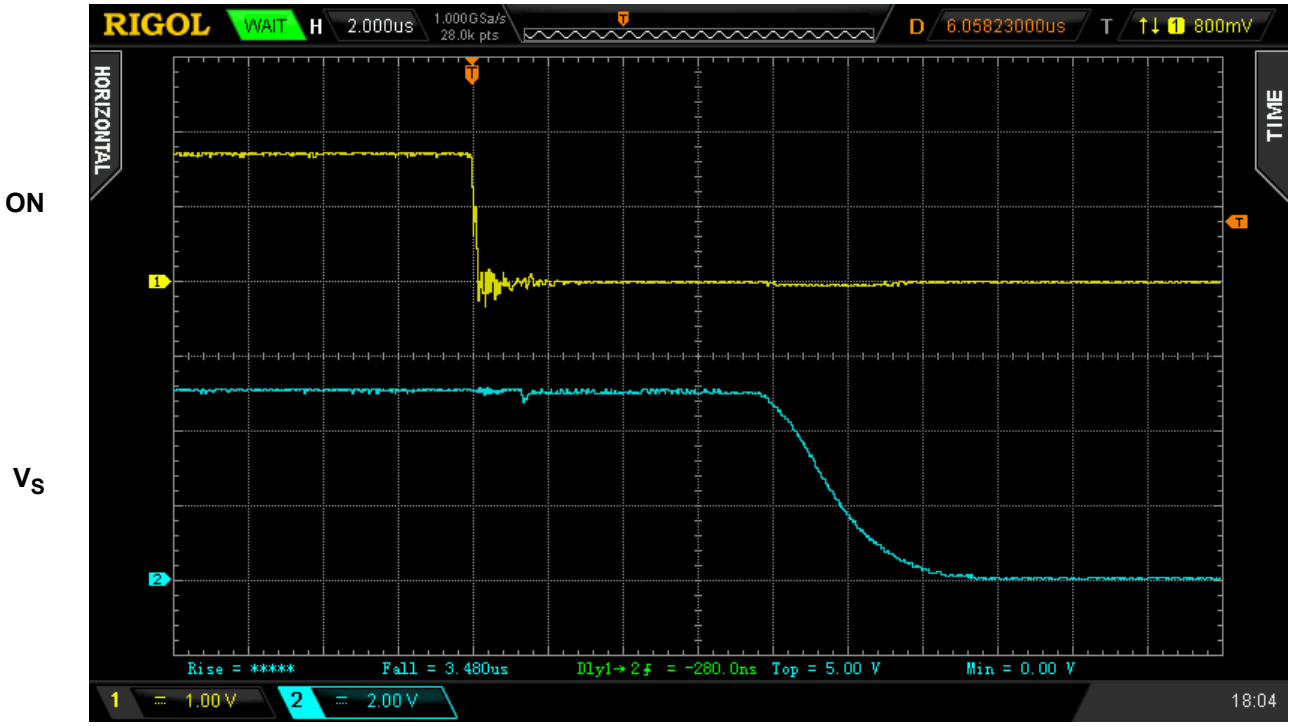


Figure 3. Typical Turn OFF operation waveform for V_{DD} = V_D = 5 V, C_{SLEW} = 4 nF, no C_{LOAD}, R_{LOAD} = 20 Ω

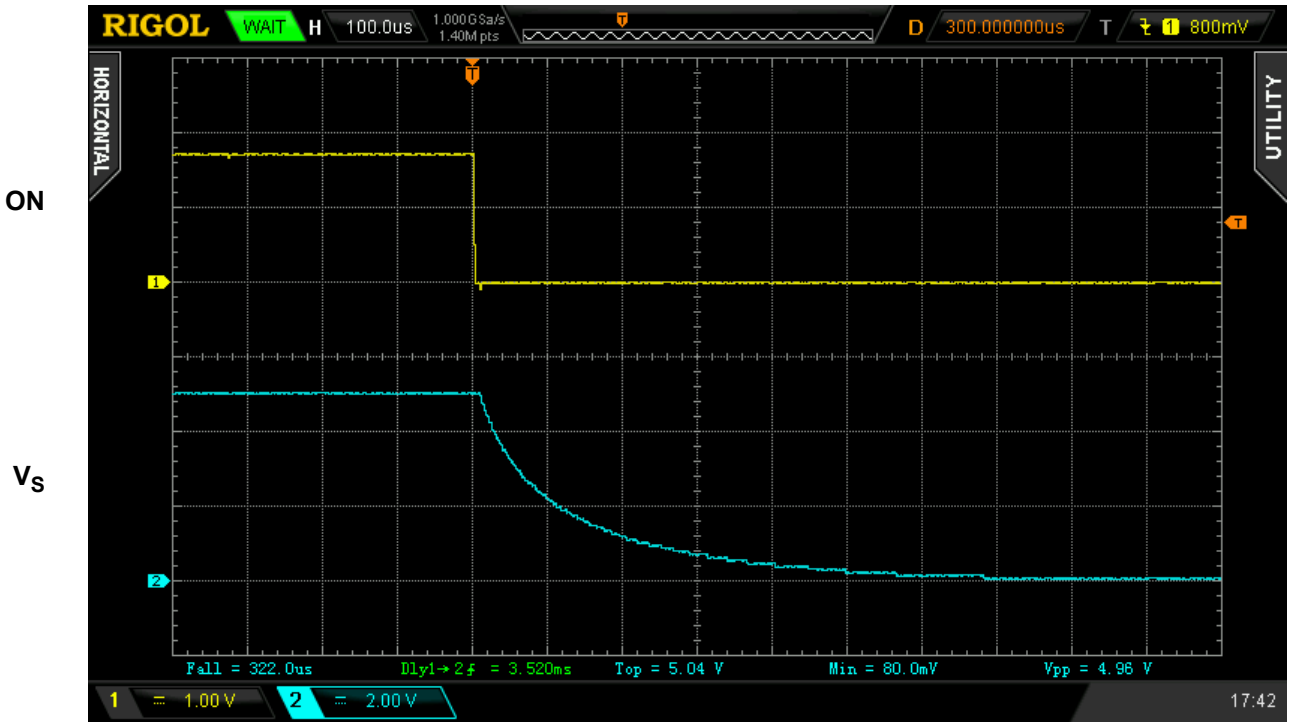


Figure 4. Typical Turn OFF operation waveform for V_{DD} = V_D = 5 V, C_{SLEW} = 4 nF, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω

SLG59M1658V Power-Up/Power-Down Sequence Considerations

To ensure glitch-free power-up under all conditions, apply V_{DD} first, followed by V_D after V_{DD} exceeds 1 V. Then allow V_D to reach 90% of its max value before toggling the ON pin from Low-to-High. Likewise, power-down in reverse order.

If V_{DD} and V_D need to be powered up simultaneously, glitching can be minimized by having a suitable load capacitor. A 10 µF C_{LOAD} will prevent glitches for rise times of V_{DD} and V_D less than 2 ms.

If the ON pin is toggled HIGH before V_{DD} and V_D have reached their steady-state values, the IPS timing parameters may differ from datasheet specifications.

The slew rate of output V_S follows a linear ramp set by a capacitor connected to the CAP pin. A larger capacitor value at the CAP pin produces a slower ramp, reducing inrush current from capacitive loads.

SLG59M1658V Current Limiting

The SLG59M1658V has two modes of current limiting, differentiated by the output (Source pin) voltage.

1. Standard Current Limiting Mode (with Thermal Protection)

When V(S) > 250 mV, the output current is initially limited to the Active Current Limit specification given in the Electrical Characteristics table. The current limiting circuit is very fast and responds within a few micro-seconds to sudden loads. When overload is sensed, the current limiting circuit increases the FET resistance to keep the current from exceedng the Active Current Limit.

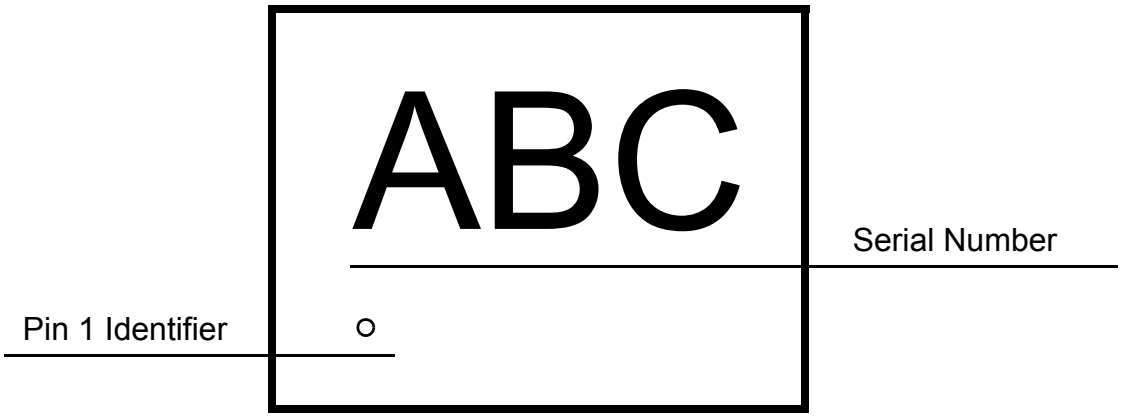
However, if an overload condition persists, the die temperature rise due to the increased FET resistance while at maximum current can activate Thermal Protection. If the die temperature exceeds the $THERM_{ON}$ specification, the FET is shut completely OFF, allowing the die to cool. When the die cools to the $THERM_{OFF}$ temperature, the FET is allowed to turn back on. This process may repeat as long as the overload condition is present.

2. Short Circuit Current Limiting Mode (with Thermal Protection)

When V(S) < 250 mV (which is the case with a hard short, such as a solder bridge on the power rail), the current is limited to approximately 500 mA. Thermal Protection is also present, but since the Short Circuit Current Limit is much lower than Standard Current Limit, activation may only occur at higher ambient temperatures.

For more information on Silego GreenFET3 integrated power switch features, please visit our Application Notes page at our website and see App Note “AN-1068 GreenFET3 Integrated Power Switch Basics”.

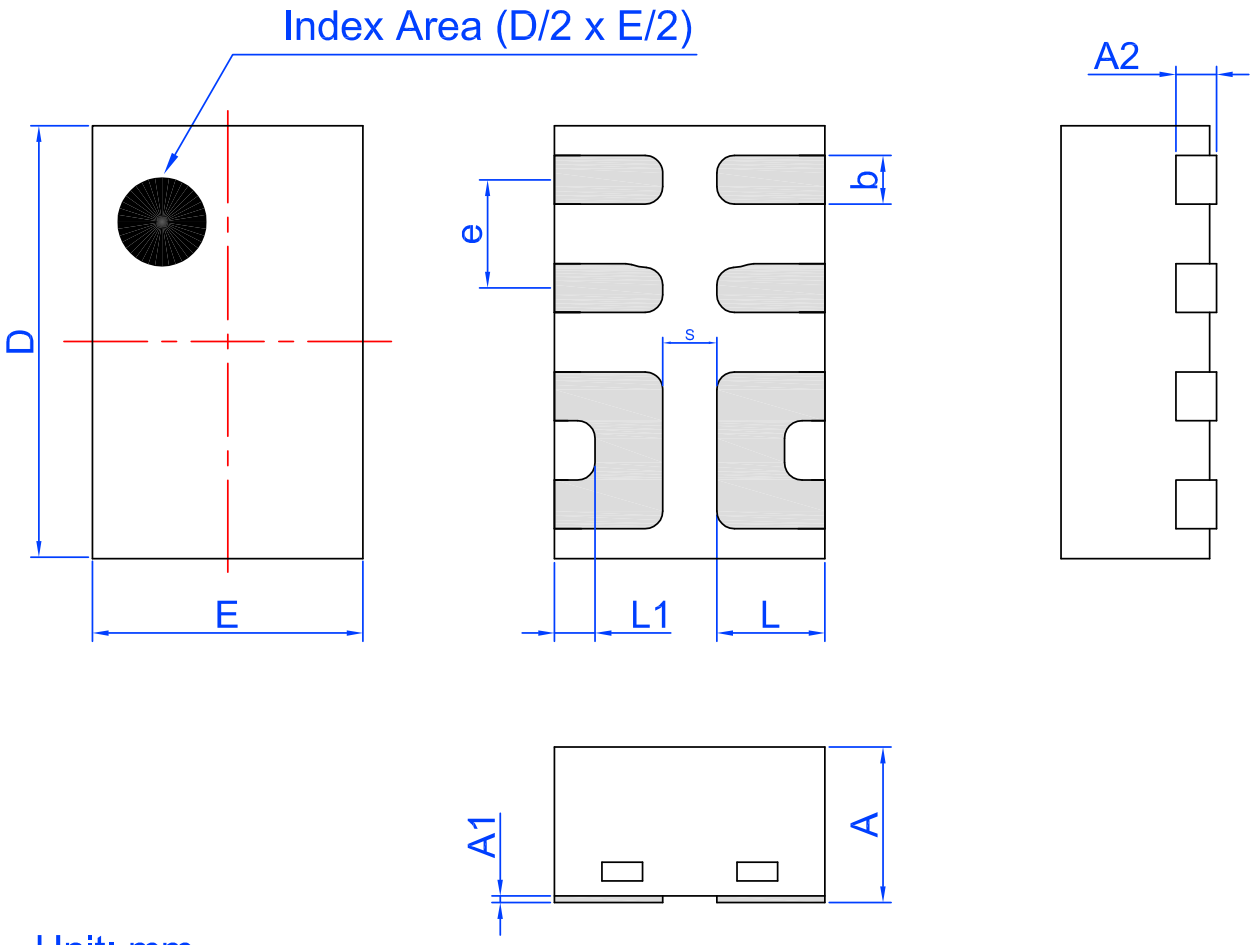
Package Top Marking System Definition



ABC - Part Serial Number Field
each A, B, and C character can be A-Z and 0-9

Package Drawing and Dimensions

8 Lead STDFN Package 1.0 x 1.6 mm (Fused Lead)



Unit: mm

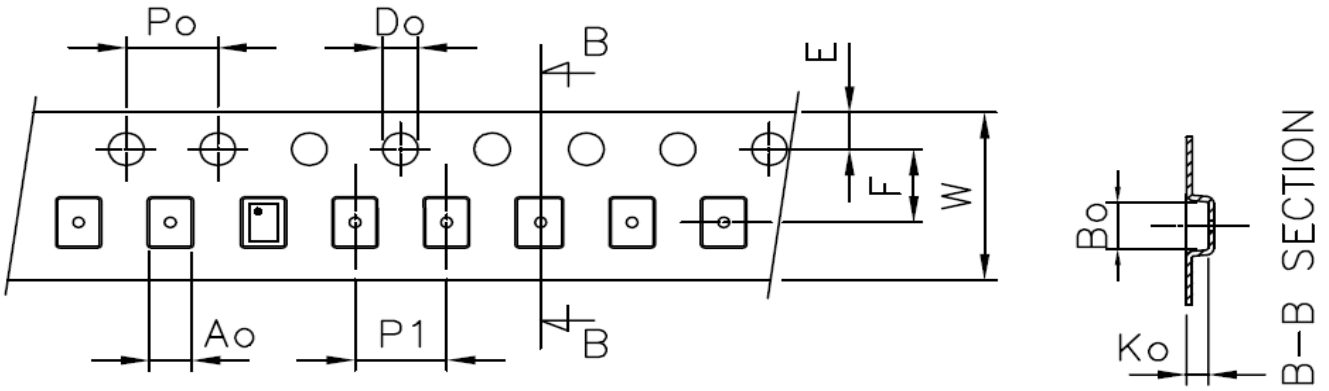
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.55	1.60	1.65
A1	0.005	-	0.060	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L	0.35	0.40	0.45
b	0.13	0.18	0.23	L1	0.10	0.15	0.20
e	0.40 BSC			S	0.2 REF		

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STDFN 8L 1x1.6mm 0.4P FC Green	8	1.0 x 1.6 x 0.55	3,000	3,000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STDFN 8L 1x1.6mm 0.4P FC Green	1.12	1.72	0.7	4	4	1.55	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.88 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
2/23/2017	1.00	Production Release

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Dialog Semiconductor:

SLG59M1658V