# RL78/G1G

RENESAS MCU

R01DS0241EJ0140
Rev. 1.40
Apr 26, 2024

# 1. OUTLINE

## 1.1 Features

**Ultra-low power consumption technology**
- $V_{DD}$ = single power supply voltage of 2.7 to 5.5 V
- HALT mode
- STOP mode
- SNOOZE mode

**RL78 CPU core**
- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high-speed (0.04167 μs: @ 24 MHz operation with high-speed on-chip oscillator) to low-speed (1.0 μs: @1 MHz operation with high-speed on-chip oscillator)
- Multiply/divide/multiply & accumulate instructions are supported.
- Address space: 1 MB
- General-purpose registers: (8-bit register × 8) × 4 banks
- On-chip RAM: 1.5 KB

**Code flash memory**
- Code flash memory: 8 to 16 KB
- Block size: 1 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debug function
- Self-programming (flash shield window function)

**High-speed on-chip oscillator**
- Select from 48 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 4 MHz, and 1 MHz
- High accuracy: ±2.0%

**Operating ambient temperature**
- $T_A$ = -40 to +85°C

**Power management and reset function**
- On-chip power-on-reset (POR) circuit
- On-chip voltage detector (LVD) (Select interrupt and reset from 6 levels)

**Event link controller (ELC)**
- Event signals of 18 to 19 types can be linked to the specified peripheral function.

**Serial interfaces**
- Simplified SPI (CSI$^{\text{Note 1}}$): 1 channel
- UART: 2 channels
- Simplified I$^2$C: 1 channel

**Timer**
- 16-bit timer: 7 channels
  (Timer Array Unit (TAU): 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels)
- 12-bit interval timer: 1 channel
- Watchdog timer: 1 channel (operable with the dedicated low-speed on-chip oscillator)

**A/D converter**
- 8/10-bit resolution A/D converter ($V_{DD}$ = 2.7 to 5.5 V)
- Analog input: 8 to 12 channels
- Internal reference voltage (1.45 V) and temperature sensor$^{\text{Note 2}}$

**Comparator**
- 2 channels
- The voltage from a dedicated 8-bit DAC (resolution of 256 with $V_{DD}$/$AV_{REFP}$ or $V_{SS}$/$AV_{REFM}$ as the internally generated reference voltage) can be selected as the reference voltage.

**Programmable gain amplifier**

**I/O port**
- I/O port: 26 to 40
- Can be set to N-ch open drain, TTL input buffer, and on-chip pull-up resistor
- Different potential interface: Can connect to a 2.5/3 V device
- On-chip key interrupt function
- On-chip clock output/buzzer output controller

Others
- On-chip BCD (binary-coded decimal) correction circuit

**Note 1.** Although the CSI function is generally called SPI, it is also called CSI in this product, so it is referred to as such in this manual.

**Note 2.** Selectable only in HS (high-speed main) mode.

**Remark** The functions mounted depend on the product. See **1.6 Outline of Functions**.

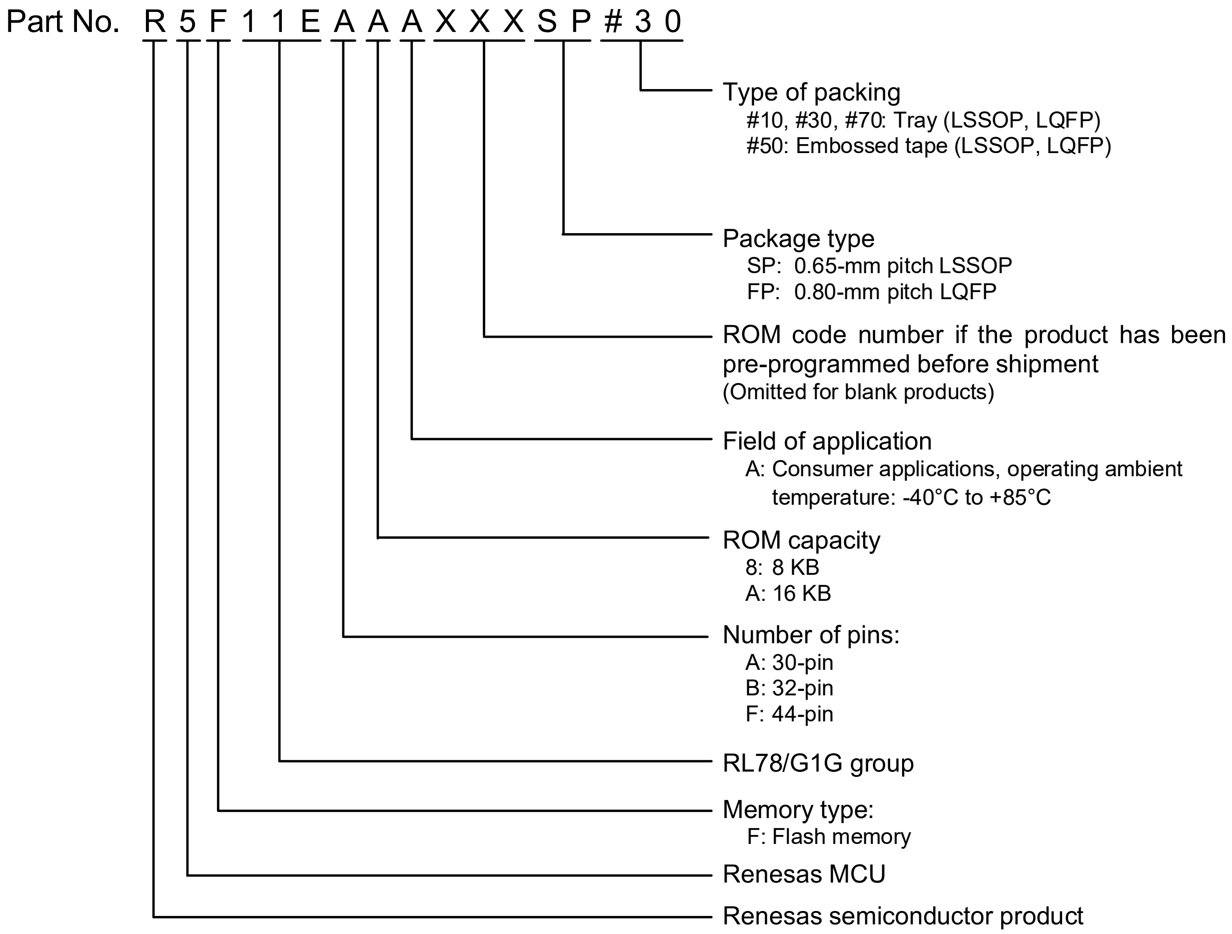
○ ROM, RAM capacities

| Flash ROM | RAM | 30 pins | 32 pins | 44 pins |
|---|---|---|---|---|
| 16 KB | 1.5 KB Note | R5F11EAAASP | R5F11EBAAFP | R5F11EFAAFP |
| 8 KB | | R5F11EA8ASP | R5F11EB8AFP | R5F11EF8AFP |

**Note** This is 630 bytes when the self-programming function is used. (For details, see **CHAPTER 3 CPU ARCHITECTURE** in the RL78/G1G User's Manual).

## 1.2 List of Part Numbers

<R> **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G1G**



Type of packing
#10, #30, #70: Tray (LSSOP, LQFP)
#50: Embossed tape (LSSOP, LQFP)

Package type
SP: 0.65-mm pitch LSSOP
FP: 0.80-mm pitch LQFP

ROM code number if the product has been pre-programmed before shipment
(Omitted for blank products)

Field of application
A: Consumer applications, operating ambient temperature: -40°C to +85°C

ROM capacity
8: 8 KB
A: 16 KB

Number of pins:
A: 30-pin
B: 32-pin
F: 44-pin

RL78/G1G group

Memory type:
F: Flash memory

Renesas MCU

Renesas semiconductor product

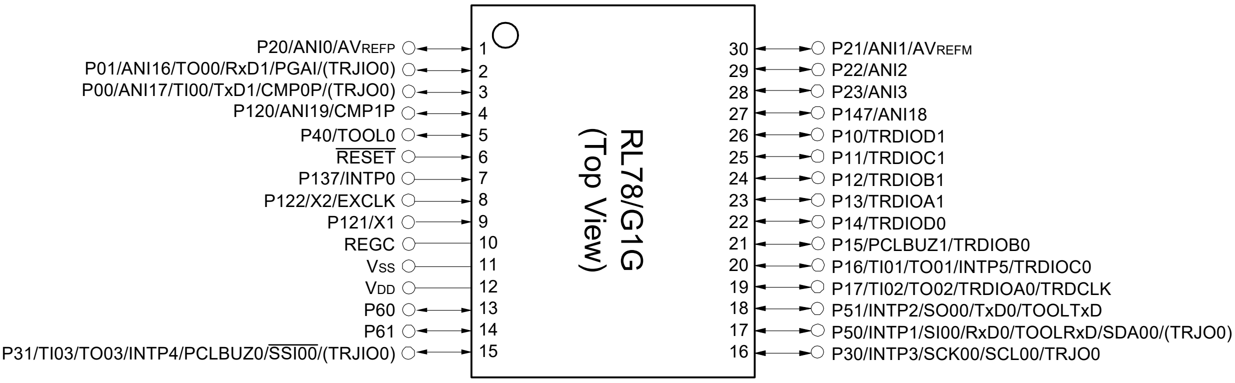
**Table 1 - 1 Orderable Part Numbers**

| Pin Count | Package | Part Number |
|---|---|---|
| 44 pins | 44-pin plastic LQFP (10 × 10 mm) | <R> R5F11EFAAFP#10, R5F11EFAAFP#30, R5F11EFAAFP#50, R5F11EFAAFP#70 |
| | | <R> R5F11EF8AFP#10, R5F11EF8AFP#30, R5F11EF8AFP#50, R5F11EF8AFP#70 |
| 32 pins | 32-pin plastic LQFP (7 × 7 mm) | <R> R5F11EBAAFP#10, R5F11EBAAFP#30, R5F11EBAAFP#50, R5F11EBAAFP#70 |
| | | <R> R5F11EB8AFP#10, R5F11EB8AFP#30, R5F11EB8AFP#50, R5F11EB8AFP#70 |
| 30 pins | 30-pin plastic LSSOP (7.62 mm (300)) | <R> R5F11EAAASP#10, R5F11EAAASP#30, R5F11EAAASP#50, R5F11EAAASP#70 |
| | | <R> R5F11EA8ASP#10, R5F11EA8ASP#30, R5F11EA8ASP#50, R5F11EA8ASP#70 |

## 1.3 Pin Configuration (Top View)

### 1.3.1 30-pin products

- 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)



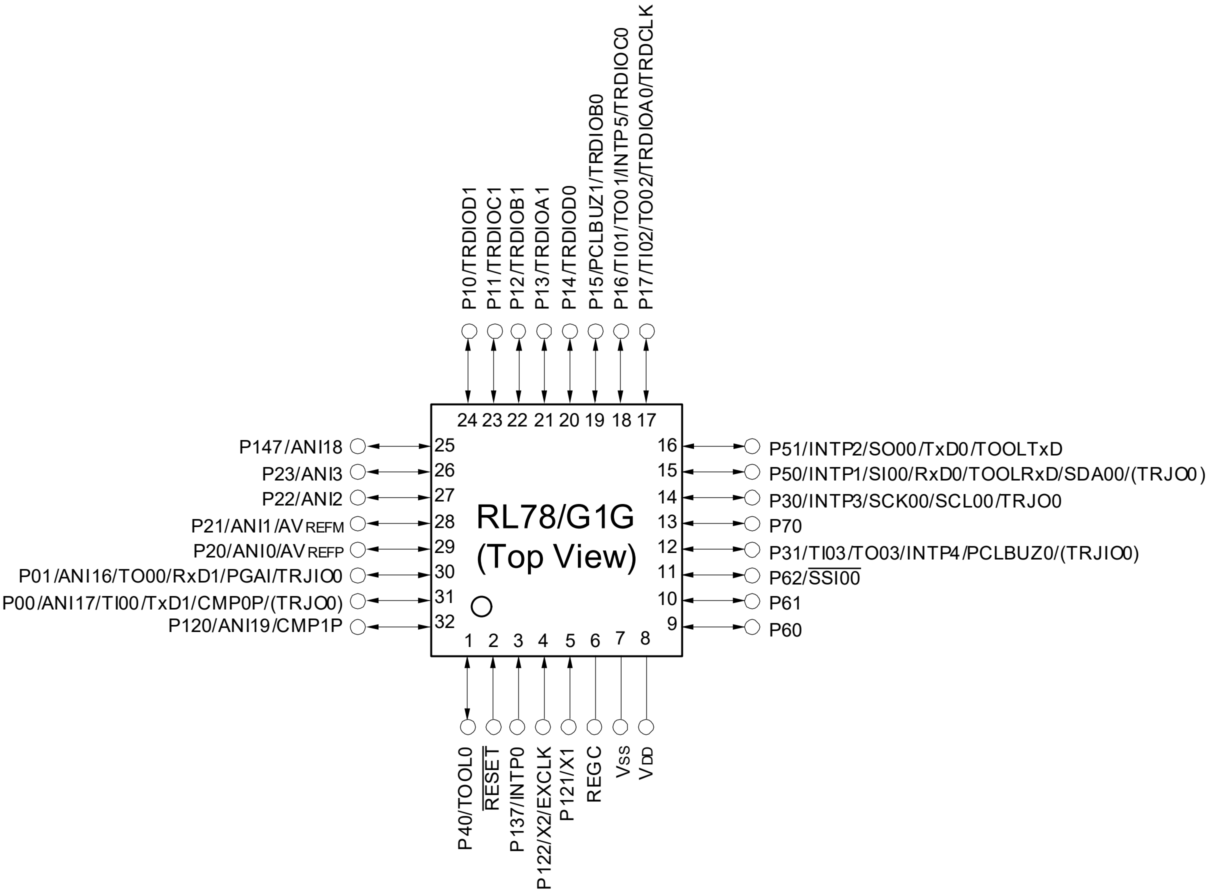
**Caution** **Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

**Remark 1.** For pin identification, see **1.4 Pin Identification**.

**Remark 2.** The functions in parentheses shown in the above figure can be assigned by setting peripheral I/O redirection register 1 (PIOR1).

## 1.3.2 32-pin products

- 32-pin plastic LQFP (7 x 7 mm, 0.8 mm pitch)



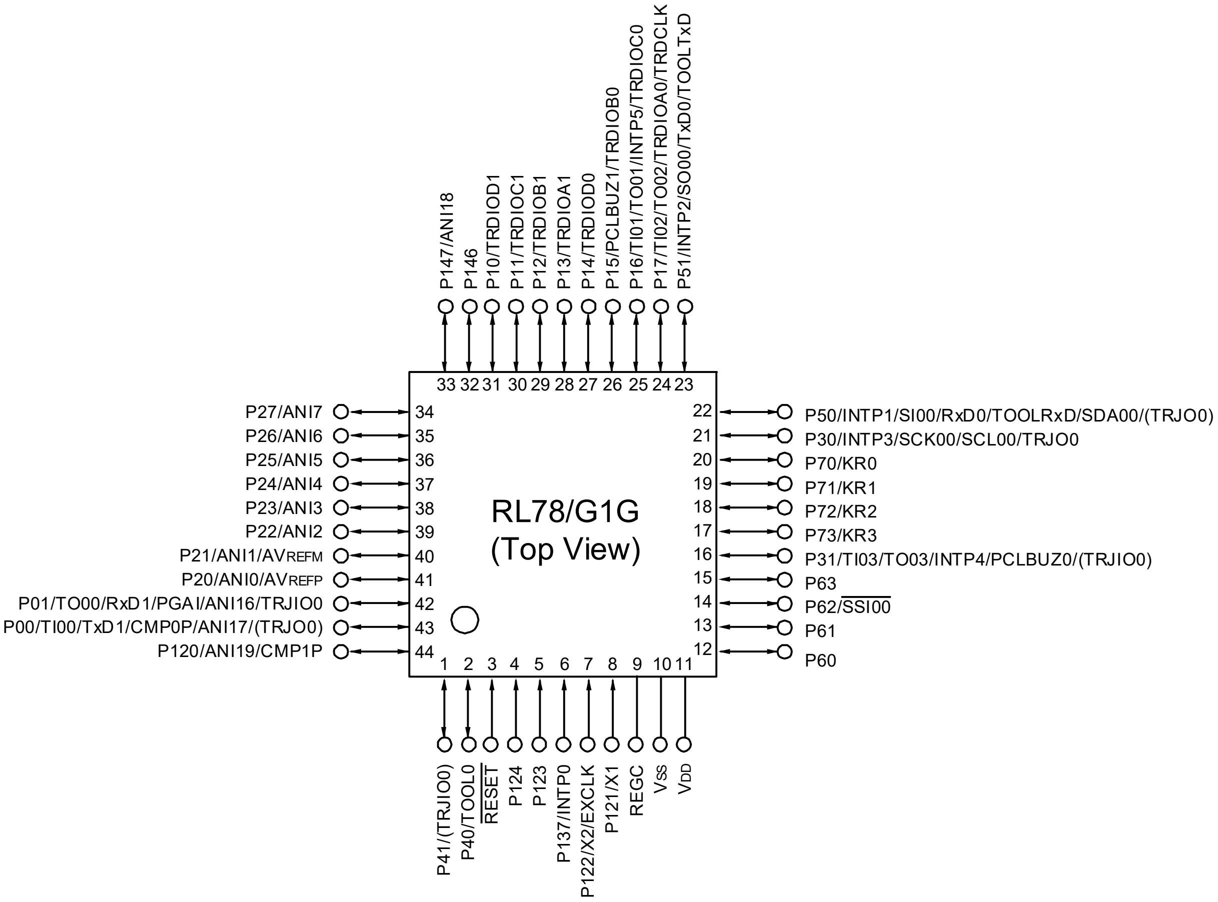
**Caution** **Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

**Remark 1.** For pin identification, see **1.4 Pin Identification**.

**Remark 2.** The functions in parentheses shown in the above figure can be assigned by setting peripheral I/O redirection register 1 (PIOR1).

### 1.3.3 44-pin products

- 44-pin plastic LQFP (10 x 10 mm, 0.8 mm pitch)



**Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

**Remark 1.** For pin identification, see **1.4 Pin Identification**.

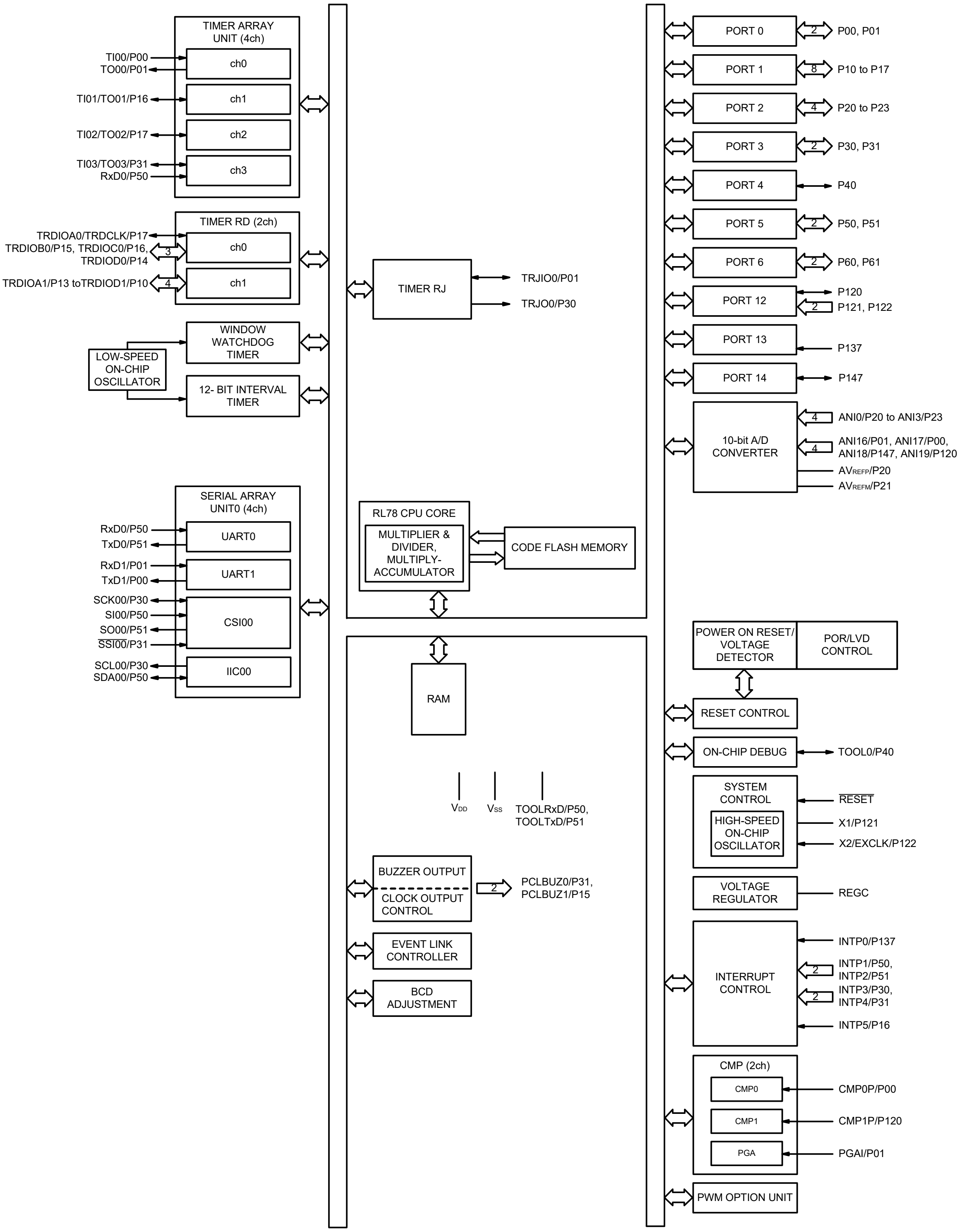
**Remark 2.** The functions in parentheses shown in the above figure can be assigned by setting peripheral I/O redirection register 1 (PIOR1).

## 1.4 Pin Identification

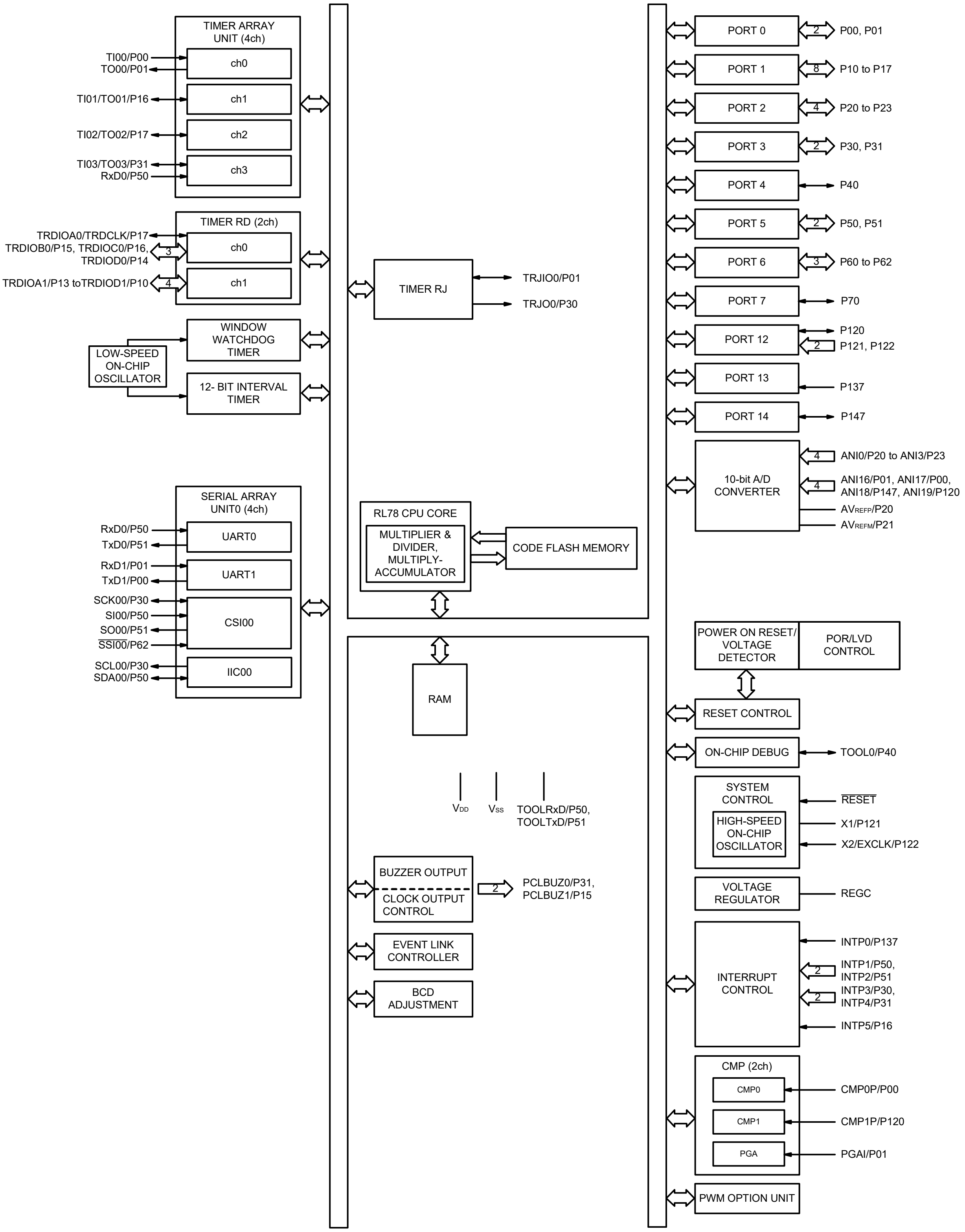
| | |
|---|---|
| ANI0 to ANI7, ANI16 to ANI19: | Analog input |
| AVREFM: | A/D converter reference potential (- side) input |
| AVREFP: | A/D converter reference potential (+ side) input |
| EXCLK: | External clock input (main system clock) |
| INTP0 to INTP5: | External interrupt input |
| KR0 to KR3: | Key Return |
| P00, P01: | Port 0 |
| P10 to P17: | Port 1 |
| P20 to P27: | Port 2 |
| P30, P31: | Port 3 |
| P40, P41: | Port 4 |
| P50, P51: | Port 5 |
| P60 to P63: | Port 6 |
| P70 to P73: | Port 7 |
| P120 to P124: | Port 12 |
| P137: | Port 13 |
| P146, P147: | Port 14 |
| PCLBUZ0, PCLBUZ1: | Programmable clock output/buzzer output |
| REGC: | Regulator capacitance |
| $\overline{\text{RESET}}$: | Reset |
| RxD0, RxD1: | Receive data |
| SCK00: | Serial clock input/output |
| SCL00: | Serial clock output |
| SDA00: | Serial data input/output |
| SI00: | Serial data input |
| SO00: | Serial data output |
| $\overline{\text{SSI00}}$: | Serial interface chip select input |
| TI00 to TI03: | Timer input |
| TO00 to TO03, TRJO0: | Timer output |
| TOOL0: | Data input/output for tool |
| TOOLRxD, TOOLTxD: | Data input/output for external device |
| TRDCLK: | Timer external input clock |
| TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0,:<br>TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1,<br>TRJIO0 | Timer input/output |
| TxD0, TxD1: | Transmit data |
| CMP0P, CMP1P: | Comparator input |
| PGAI: | PGA input |
| VDD: | Power supply |
| VSS: | Ground |
| X1, X2: | Crystal oscillator (main system clock) |

## 1.5 Block Diagram

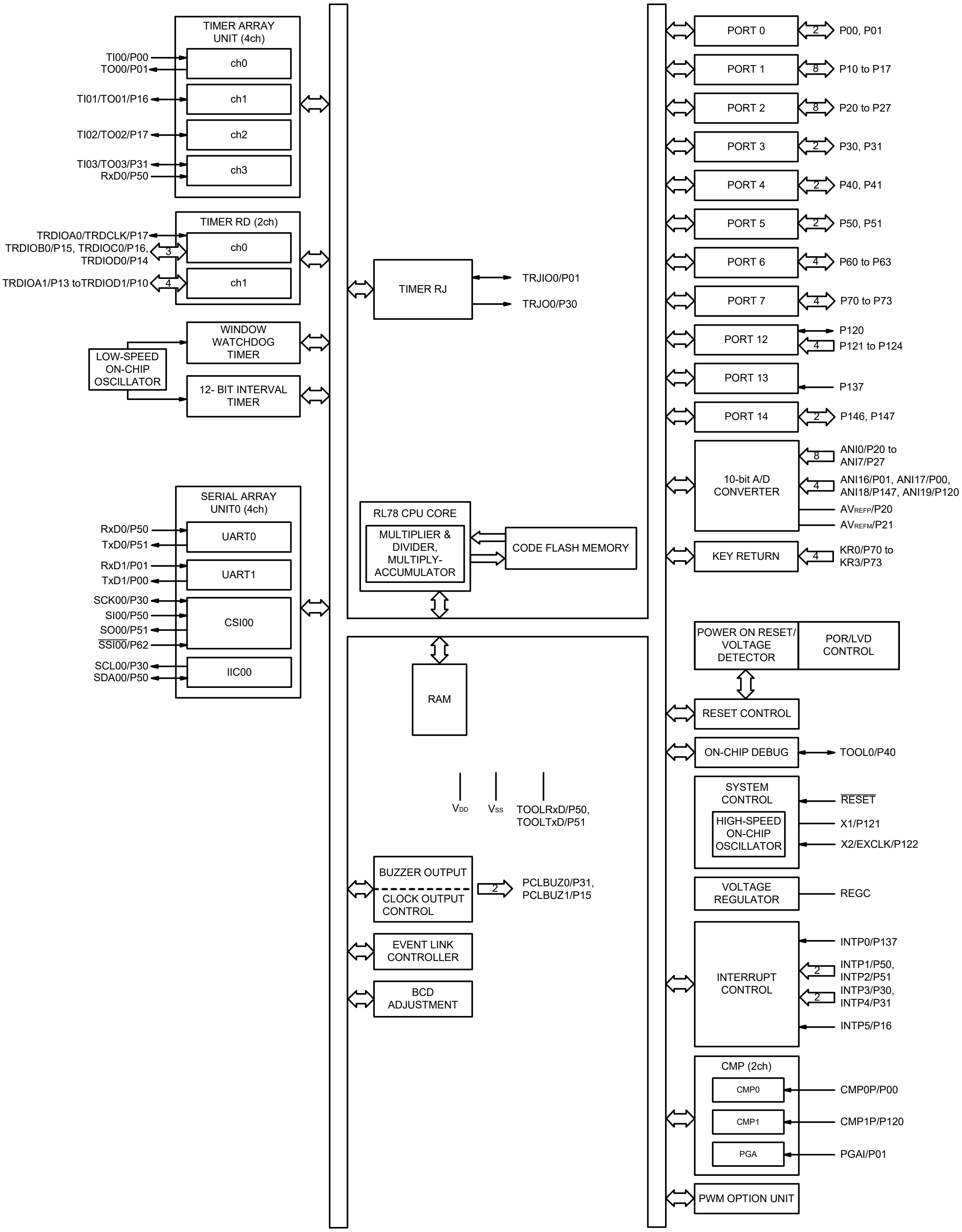
### 1.5.1 30-pin products



### 1.5.2 32-pin products



### 1.5.3 44-pin products



## 1.6 Outline of Functions

[30-pin, 32-pin, 44-pin products (code flash memory 8 KB to 16 KB)]

**Caution The above outline of the functions applies when peripheral I/O redirection register 1 (PIOR1) is set to 00H.**

(1/2)

| Item | | 30-pin | 32-pin | 44-pin |
|---|---|---|---|---|
| | | R5F11EA8ASP,<br>R5F11EAAASP | R5F11EB8AFP,<br>R5F11EBAAFP | R5F11EF8AFP,<br>R5F11EFAAFP |
| Code flash memory (KB) | | 8 to 16 | | |
| RAM (KB) | | 1.5 | | |
| Address space | | 1 MB | | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>LS (low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (high-speed main) mode: 1 to 20 MHz ($V_{DD}$ = 2.7 to 5.5 V) | | |
| | High-speed on-chip oscillator clock ($f_{IH}$) | LS (low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 2.7 to 5.5 V)<br>HS (high-speed main) mode: 1 to 24 MHz ($V_{DD}$ = 2.7 to 5.5 V) | | |
| Low-speed on-chip oscillator clock | | 15 kHz (TYP.): $V_{DD}$ = 2.7 to 5.5 V | | |
| General-purpose register | | 8 bits × 32 registers (8 bits × 8 registers × 4 banks) | | |
| Minimum instruction execution time | | 0.04167 μs (High-speed on-chip oscillator clock: $f_{IH}$ = 24 MHz operation) | | |
| | | 0.05 μs (High-speed system clock: $f_{MX}$ = 20 MHz operation) | | |
| Instruction set | | • Data transfer (8/16 bits)<br>• Adder and subtractor/logical operation (8/16 bits)<br>• Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits)<br>• Multiplication and Accumulation (16 bits × 16 bits + 32 bits)<br>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | | |
| I/O port | Total | 26 | 28 | 40 |
| | CMOS I/O | 23 | 25 | 35 |
| | CMOS input | 3 | 3 | 5 |
| | CMOS output | — | | |
| | N-ch open-drain I/O (6 V tolerance) | — | | |
| Timer | 16-bit timer | 7 channels<br>(TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels) | | |
| | Watchdog timer | 1 channel | | |
| | 12-bit interval timer | 1 channel | | |
| | Timer output | Timer outputs: 14 channels<br>PWM outputs: 9 channels | | |

**Caution Since a library is used when rewriting the flash memory using the user program, flash ROM and RAM areas are used. Refer to the RL78 Family Flash Self-Programming Library Type01 User's Manual before using these products.**

(2/2)

| Item | | 30-pin | 32-pin | 44-pin |
|---|---|---|---|---|
| | | R5F11EA8ASP,<br>R5F11EAAASP | R5F11EB8AFP,<br>R5F11EBAAFP | R5F11EF8AFP,<br>R5F11EFAAFP |
| Clock output/buzzer output | | 2 | | |
| | | • 2.44 kHz, 4.88 kHz, 9.77 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz<br>(Main system clock: $f_{MAIN}$ = 20 MHz operation) | | |
| 8/10-bit resolution A/D converter | | 8 channels | | 12 channels |
| Comparator | | 2 channels | | |
| PGA | | 1 channel | | |
| Serial interface | | • Simplified SPI (CSI): 1 channel/UART0: 1 channel/simplified $I^2C$: 1 channel<br>• UART1: 1 channel | | |
| Event link controller (ELC) | | Event input: 18<br>Event trigger output: 6 | | Event input: 19<br>Event trigger output: 6 |
| Vectored interrupt sources | Internal | 20 | | |
| | External | 6 | | 7 |
| Key interrupt | | — | | 4 |
| Reset | | • Reset by $\overline{\text{RESET}}$ pin<br>• Internal reset by watchdog timer<br>• Internal reset by power-on-reset<br>• Internal reset by voltage detector<br>• Internal reset by illegal instruction execution [Note]<br>• Internal reset by RAM parity error<br>• Internal reset by illegal-memory access | | |
| Power-on-reset circuit | | • Power-on-reset: 1.51 ±0.03 V<br>• Power-down-reset: 1.50 ±0.03 V | | |
| Voltage detector | | 2.75 V to 4.06 V (6 stages) | | |
| On-chip debug function | | Provided | | |
| Power supply voltage | | $V_{DD}$ = 2.7 to 5.5 V | | |
| Operating ambient temperature | | $T_A$ = -40 to +85°C | | |

**Note** The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

# 2. ELECTRICAL SPECIFICATIONS

**Caution 1. The RL78 microcontroller has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**

**Caution 2. The pins mounted are as follows according to product.**

## 2.1 Pins Mounted According to Product

### 2.1.1 Port functions

Refer to **2.1.1 30-pin products**, **2.1.2 32-pin products**, and **2.1.3 44-pin products** in the RL78/G1G User's Manual.

### 2.1.2 Non-port functions

Refer to **2.2.1 With functions for each product** in the RL78/G1G User's Manual.

## 2.2 Absolute Maximum Ratings

**Absolute Maximum Ratings** **(1/2)**

| Parameter | Symbols | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | -0.5 to +6.5 | V |
| REGC pin input voltage | $V_{IREGC}$ | REGC | -0.3 to +2.8<br>and -0.3 to $V_{DD}$ +0.3 Note 1 | V |
| Input voltage | $V_{I1}$ | P00, P01, P10 to P17, P20 to P27, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P121 to P124, P137, P146, P147, EXCLK, $\overline{\text{RESET}}$ | -0.3 to $V_{DD}$ +0.3 Note 2 | V |
| Output voltage | $V_{O1}$ | P00, P01, P10 to P17, P20 to P27, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P146, P147 | -0.3 to $V_{DD}$ +0.3 Note 2 | V |
| Analog input voltage | $V_{AI1}$ | ANI0 to ANI7, ANI16 to ANI19 | -0.3 to $V_{DD}$ +0.3 Notes 2, 3<br>and -0.3 to $AV_{REF}$ (+) +0.3 | V |

**Note 1.** Connect the REGC pin to $V_{SS}$ via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**Note 2.** Must be 6.5 V or lower.

**Note 3.** Do not exceed $AV_{REF}$ (+) + 0.3 V in case of A/D conversion target pin.

**Caution** **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**Remark 2.** $AV_{REF}$ (+): + side reference voltage of the A/D converter.

**Remark 3.** $V_{SS}$: Reference voltage

**Absolute Maximum Ratings** **(2/2)**

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Output current, high | $I_{OH1}$ | Per pin | P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P146, P147 | -40 | mA |
| | | Total of all pins<br>-170 mA | P00, P01, P40, P41, P120 | -70 | mA |
| | | | P10 to P17, P30, P31, P50, P51, P60 to P63, P70 to P73, P146, P147 | -100 | mA |
| | $I_{OH2}$ | Per pin | P20 to P27 | -0.5 | mA |
| | | Total of all pins | | -2 | mA |
| Output current, low | $I_{OL1}$ | Per pin | P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P146, P147 | 40 | mA |
| | | Total of all pins<br>170 mA | P00, P01, P40, P41, P120 | 70 | mA |
| | | | P10 to P17, P30, P31, P50, P51, P60 to P63, P70 to P73, P146, P147 | 100 | mA |
| | $I_{OL2}$ | Per pin | P20 to P27 | 1 | mA |
| | | Total of all pins | | 5 | mA |
| Operating ambient temperature | $T_A$ | In normal operation mode | | -40 to +85 | °C |
| | | In flash memory programming mode | | | |
| Storage temperature | $T_{stg}$ | | | -65 to +150 | °C |

**Caution** **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 2.3 Oscillator Characteristics

### 2.3.1 X1 oscillator characteristics

**($T_A$ = -40 to +85°C, 2.7 V $\leq$ $V_{DD}$ $\leq$ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Resonator | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| X1 clock oscillation frequency ($f_X$) Note | Ceramic resonator/ crystal resonator | 2.7 V $\leq$ $V_{DD}$ $\leq$ 5.5 V | 1.0 |  | 20.0 | MHz |

**Note** Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution** **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

**Remark** When using the X1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/G1G User's Manual.

### 2.3.2 On-chip oscillator characteristics

**($T_A$ = -40 to +85°C, 2.7 V $\leq$ $V_{DD}$ $\leq$ 5.5 V, $V_{SS}$ = 0 V)**

| Oscillators | Parameters | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| High-speed on-chip oscillator clock frequency Notes 1, 2 | $f_{IH}$ |  | 1 |  | 24 | MHz |
|  | $f_{HOCO}$ |  | 1 |  | 48 |  |
| High-speed on-chip oscillator clock frequency accuracy |  |  | -2 |  | +2 | % |
| Low-speed on-chip oscillator clock frequency | $f_{IL}$ |  |  | 15 |  | kHz |
| Low-speed on-chip oscillator clock frequency accuracy |  |  | -15 |  | +15 | % |

**Note 1.** High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

**Note 2.** This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

## 2.4 DC Characteristics

### 2.4.1 Pin characteristics

**($T_A$ = -40 to +85°C, $2.7\ V \le V_{DD} \le 5.5\ V$, $V_{SS} = 0\ V$)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, high Note 1 | $I_{OH1}$ | Per pin for P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P146, P147 | $2.7\ V \le V_{DD} \le 5.5\ V$ | | | -10.0<br>Note 2 | mA |
| | | Total of P00, P01, P40, P41, P120<br>(When duty ≤ 70% Note 3) | $4.0\ V \le V_{DD} \le 5.5\ V$ | | | -55.0 | mA |
| | | | $2.7\ V \le V_{DD} < 4.0\ V$ | | | -10.0 | mA |
| | | Total of P10 to P17, P30, P31, P50, P51, P60 to P63, P70 to P73, P146, P147<br>(When duty ≤ 70% Note 3) | $4.0\ V \le V_{DD} \le 5.5\ V$ | | | -80.0 | mA |
| | | | $2.7\ V \le V_{DD} < 4.0\ V$ | | | -19.0 | mA |
| | | Total of all pins<br>(When duty ≤ 70% Note 3) | $2.7\ V \le V_{DD} \le 5.5\ V$ | | | -135.0 | mA |
| | $I_{OH2}$ | Per pin for P20 to P27 | $2.7\ V \le V_{DD} \le 5.5\ V$ | | | -0.1<br>Note 2 | mA |
| | | Total of all pins<br>(When duty ≤ 70% Note 3) | $2.7\ V \le V_{DD} \le 5.5\ V$ | | | -1.5 | mA |

**Note 1.** Value of current at which the device operation is guaranteed even if the current flows from the $V_{DD}$ pin to an output pin.

**Note 2.** Do not exceed the total current value.

**Note 3.** Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OH}$ × 0.7)/(n × 0.01)
  <Example> Where n = 80% and $I_{OH}$ = -10.0 mA
  Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

**Caution** **P00, P10, P15, P17, P30, P50, P51 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, low [Note 1] | $I_{OL1}$ | Per pin for P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P146, P147 | | | | 20.0<br>Note 2 | mA |
| | | Total of P00, P01, P40, P41, P120 (When duty ≤ 70% [Note 3]) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 70.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | 15.0 | mA |
| | | Total of P10 to P17, P30, P31, P50, P51, P60 to P63, P70 to P73, P146, P147 (When duty ≤ 70% [Note 3]) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 80.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | 35.0 | mA |
| | | Total of all pins (When duty ≤ 70% [Note 3]) | | | | 150.0 | mA |
| | $I_{OL2}$ | Per pin for P20 to P27 | | | | 0.4<br>Note 2 | mA |
| | | Total of all pins (When duty ≤ 70% [Note 3]) | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 5.0 | mA |

**Note 1.** Value of current at which the device operation is guaranteed even if the current flows from an output pin to the $V_{SS}$ pin.

**Note 2.** However, do not exceed the total current value.

**Note 3.** Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OL}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OL}$ = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +85°C, 2.7 V $\leq V_{DD} \leq$ 5.5 V, $V_{SS}$ = 0 V)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage, high | $V_{IH1}$ | P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120 to P124, P146, P147 | Normal input buffer | 0.8 $V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH2}$ | P01, P10, P15 to P17, P30, P31, P50 | TTL input buffer<br>4.0 V $\leq V_{DD} \leq$ 5.5 V | 2.2 | | $V_{DD}$ | V |
| | | | TTL input buffer<br>3.3 V $\leq V_{DD} <$ 4.0 V | 2.0 | | $V_{DD}$ | V |
| | | | TTL input buffer<br>2.7 V $\leq V_{DD} <$ 3.3 V | 1.50 | | $V_{DD}$ | V |
| | $V_{IH3}$ | P20 to P27 | | 0.7 $V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH4}$ | EXCLK, $\overline{\text{RESET}}$ | | 0.8 $V_{DD}$ | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL1}$ | P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120 to P124, P146, P147 | Normal input buffer | 0 | | 0.2 $V_{DD}$ | V |
| | $V_{IL2}$ | P01, P10, P15 to P17, P30, P31, P50 | TTL input buffer<br>4.0 V $\leq V_{DD} \leq$ 5.5 V | 0 | | 0.8 | V |
| | | | TTL input buffer<br>3.3 V $\leq V_{DD} <$ 4.0 V | 0 | | 0.5 | V |
| | | | TTL input buffer<br>2.7 V $\leq V_{DD} <$ 3.3 V | 0 | | 0.32 | V |
| | $V_{IL3}$ | P20 to P27 | | 0 | | 0.3 $V_{DD}$ | V |
| | $V_{IL4}$ | EXCLK, $\overline{\text{RESET}}$ | | 0 | | 0.2 $V_{DD}$ | V |

**Caution** **The maximum value of $V_{IH}$ of pins P00, P10, P15, P17, P30, P50, and P51 is $V_{DD}$, even in the N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output voltage, high | $V_{OH1}$ | P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P146, P147 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH1}$ = -10.0 mA | $V_{DD}$ - 1.5 | | | V |
| | | | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH1}$ = -3.0 mA | $V_{DD}$ - 0.7 | | | V |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH1}$ = -2.0 mA | $V_{DD}$ - 0.6 | | | V |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH1}$ = -1.0 mA | $V_{DD}$ - 0.5 | | | V |
| | $V_{OH2}$ | P20 to P27 | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH2}$ = -100 μA | $V_{DD}$ - 0.5 | | | V |
| Output voltage, low | $V_{OL1}$ | P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P146, P147 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 20.0 mA | | | 1.3 | V |
| | | | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 8.5 mA | | | 0.7 | V |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 3.0 mA | | | 0.6 | V |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 1.5 mA | | | 0.4 | V |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 0.3 mA | | | 0.4 | V |
| | $V_{OL2}$ | P20 to P27 | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL2}$ = 400 μA | | | 0.4 | V |

**Caution P00, P10, P15, P17, P30, P50, and P51 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +85°C, 2.7 V $\leq V_{DD} \leq$ 5.5 V, $V_{SS}$ = 0 V)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Input leakage current, high | $I_{LIH1}$ | P00, P01, P10 to P17, P20 to P27, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P123, P124, P137, P146, P147, $\overline{\text{RESET}}$ | $V_I = V_{DD}$ | | | | 1 | μA |
| | $I_{LIH2}$ | P121, P122 (X1, X2, EXCLK) | $V_I = V_{DD}$ | In input port or external clock input | | | 1 | μA |
| | | | | In resonator connection | | | 10 | μA |
| Input leakage current, low | $I_{LIL1}$ | P00, P01, P10 to P17, P20 to P27, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P123, P124, P137, P146, P147, $\overline{\text{RESET}}$ | $V_I = V_{SS}$ | | | | -1 | μA |
| | $I_{LIL2}$ | P121, P122 (X1, X2, EXCLK) | $V_I = V_{SS}$ | In input port or external clock input | | | -1 | μA |
| | | | | In resonator connection | | | -10 | μA |
| On-chip pull-up resistance | $R_U$ | P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P146, P147 | $V_I = V_{SS}$, in input port | | 10 | 20 | 100 | kΩ |

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

### 2.4.2 Supply current characteristics

#### (1) Flash ROM: 16 KB of 30- pin to 44-pin products

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (high-speed main) mode Notes 3, 4 | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz | Basic operation | $V_{DD}$ = 5.0 V | | 1.8 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 1.8 | | |
| | | | HS (high-speed main) mode Notes 3, 4 | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz | Normal operation | $V_{DD}$ = 5.0 V | | 3.9 | 6.9 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.9 | 6.9 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz | Normal operation | $V_{DD}$ = 5.0 V | | 3.7 | 6.3 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.7 | 6.3 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz | Normal operation | $V_{DD}$ = 5.0 V | | 2.8 | 4.6 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.8 | 4.6 | |
| | | | LS (low-speed main) mode Notes 3, 4 | $f_{IH}$ = 8 MHz | Normal operation | $V_{DD}$ = 3.0 V | | 1.2 | 2.0 | mA |
| | | | HS (high-speed main) mode Notes 2, 4 | $f_{MX}$ = 20 MHz, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 3.1 | 5.3 | mA |
| | | | | | | Resonator connection | | 3.3 | 5.5 | |
| | | | | $f_{MX}$ = 20 MHz, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 3.1 | 5.3 | |
| | | | | | | Resonator connection | | 3.3 | 5.5 | |
| | | | | $f_{MX}$ = 10 MHz, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 2.0 | 3.1 | |
| | | | | | | Resonator connection | | 2.0 | 3.2 | |
| | | | | $f_{MX}$ = 10 MHz, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 2.0 | 3.1 | |
| | | | | | | Resonator connection | | 2.0 | 3.2 | |
| | | | LS (low-speed main) mode Notes 2, 4 | $f_{MX}$ = 8 MHz, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 1.2 | 1.9 | mA |
| | | | | | | Resonator connection | | 1.2 | 2.0 | |

**Note 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, comparator, programmable gain amplifier, watchdog timer, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.

**Note 2.** When high-speed on-chip oscillator is stopped.

**Note 3.** When high-speed system clock is stopped.

**Note 4.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high speed main) mode: $V_{DD}$ = 2.7 V to 5.5 V@1 MHz to 24 MHz
LS (low speed main) mode: $V_{DD}$ = 2.7 V to 5.5 V@1 MHz to 8 MHz

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (48 MHz max.)

**Remark 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (24 MHz max.)

**Remark 4.** Temperature condition of the TYP. value is $T_A$ = 25°C

### (1) Flash ROM: 16 KB of 30-pin to 44-pin products

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Notes 4, 6 | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz | $V_{DD}$ = 5.0 V | | 0.60 | 2.40 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.60 | 2.40 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz | $V_{DD}$ = 5.0 V | | 0.40 | 1.83 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.40 | 1.83 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz | $V_{DD}$ = 5.0 V | | 0.38 | 1.38 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.38 | 1.38 | |
| | | | LS (low-speed main) mode Notes 4, 6 | $f_{IH}$ = 8 MHz | $V_{DD}$ = 3.0 V | | 260 | 710 | μA |
| | | | HS (high-speed main) mode Notes 3, 6 | $f_{MX}$ = 20 MHz, $V_{DD}$ = 5.0 V | Square wave input | | 0.28 | 1.55 | mA |
| | | | | | Resonator connection | | 0.42 | 1.74 | |
| | | | | $f_{MX}$ = 20 MHz, $V_{DD}$ = 3.0 V | Square wave input | | 0.28 | 1.55 | |
| | | | | | Resonator connection | | 0.42 | 1.74 | |
| | | | | $f_{MX}$ = 10 MHz, $V_{DD}$ = 5.0 V | Square wave input | | 0.19 | 0.86 | |
| | | | | | Resonator connection | | 0.27 | 0.93 | |
| | | | | $f_{MX}$ = 10 MHz, $V_{DD}$ = 3.0 V | Square wave input | | 0.19 | 0.86 | |
| | | | | | Resonator connection | | 0.27 | 0.93 | |
| | | | LS (low-speed main) mode Notes 3, 6 | $f_{MX}$ = 8 MHz, $V_{DD}$ = 3.0 V | Square wave input | | 95 | 550 | μA |
| | | | | | Resonator connection | | 145 | 590 | |
| | $I_{DD3}$ | STOP mode Note 5 | $T_A$ = -40°C | | | | 0.18 | 0.51 | μA |
| | | | $T_A$ = +25°C | | | | 0.24 | 0.51 | |
| | | | $T_A$ = +50°C | | | | 0.29 | 1.10 | |
| | | | $T_A$ = +70°C | | | | 0.41 | 1.90 | |
| | | | $T_A$ = +85°C | | | | 0.90 | 3.30 | |

**Note 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, comparator, programmable gain amplifier, watchdog timer, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.

**Note 2.** During HALT instruction execution by flash memory.

**Note 3.** When high-speed on-chip oscillator is stopped.

**Note 4.** When high-speed system clock is stopped.

**Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When watchdog timer is stopped. The values below the MAX. column include the leakage current.

**Note 6.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high speed main) mode: $V_{DD}$ = 2.7 V to 5.5 V@1 MHz to 24 MHz
LS (low speed main) mode: $V_{DD}$ = 2.7 V to 5.5 V@1 MHz to 8 MHz

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (48 MHz max.)

**Remark 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (24 MHz max.)

**Remark 4.** Temperature condition of the TYP. value is $T_A$ = 25°C

### (2) Peripheral Functions (Common to all products)

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| 12-bit interval timer operating current | $I_{IT}$ Notes 1, 8 | | | | | 0.20 | | μA |
| Watchdog timer operating current | $I_{WDT}$ Notes 1, 2 | $f_{IL}$ = 15 kHz | | | | 0.22 | | μA |
| A/D converter operating current | $I_{ADC}$ Note 3 | When conversion at maximum speed | Normal mode, $AV_{REFP}$ = $V_{DD}$ = 5.0 V | | | 1.3 | 1.7 | mA |
| | | | Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | | 0.5 | 0.7 | mA |
| A/D converter reference voltage current | $I_{ADREF}$ | | | | | 75 | | μA |
| Temperature sensor operating current | $I_{TMPS}$ | | | | | 75 | | μA |
| Comparator operating current | $I_{CMP}$ Note 4 | Per channel of comparator 1 | When the comparator is operating | | | 45.0 | 65.0 | μA |
| | | | When the comparator is stopped | | | 0.0 | 0.1 | |
| Programmable gain amplifier operating current | $I_{PGA}$ Note 5 | When the programmable gain amplifier is operating | | | | 240.0 | 340.0 | μA |
| | | When the programmable gain amplifier is stopped | | | | 0.0 | 0.1 | |
| LVD operating current | $I_{LVI}$ Note 6 | | | | | 0.08 | | μA |
| SNOOZE operating current | $I_{SNOZ}$ | ADC operation | The mode is performed Note 7 | | | 0.50 | 0.60 | mA |
| | | | The A/D conversion operations are performed | Low voltage mode $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 1.20 | 1.44 | mA |
| | | Simplified SPI (CSI)/UART operation | | | | 0.70 | 0.84 | mA |

**Note 1.** When high speed on-chip oscillator and high-speed system clock are stopped.

**Note 2.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontroller is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{WDT}$ when the watchdog timer operates in STOP mode.

**Note 3.** Current flowing only to the A/D converter. The current value of the RL78 microcontroller is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{ADC}$ when the A/D converter operates in an operation mode or the HALT mode.

**Note 4.** Current flowing only to the comparator. The current value of the RL78 microcontroller is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{CMP}$ when the comparator operates in operating mode or HALT mode.

**Note 5.** Current flowing only to the programmable gain amplifier. The current value of the RL78 microcontroller is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{PGA}$ when the programmable gain amplifier operates in operating mode or HALT mode.

**Note 6.** Current flowing only to the LVD circuit. The current value of the RL78 microcontroller is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{LVI}$ when the LVD circuit operates in the Operating, HALT or STOP mode.

**Note 7.** For details on the transition time to SNOOZE mode, refer to **18.3.3 SNOOZE mode** in the RL78/G1G User's Manual.

**Note 8.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontroller is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{IT}$, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, $I_{FIL}$ should be added.

**Remark 1.** $f_{IL}$: Low-speed on-chip oscillator clock frequency

**Remark 2.** $f_{CLK}$: CPU/peripheral hardware clock frequency

**Remark 3.** Temperature condition of the TYP. value is $T_A$ = 25°C

## 2.5 AC Characteristics

### 2.5.1 Basic operation

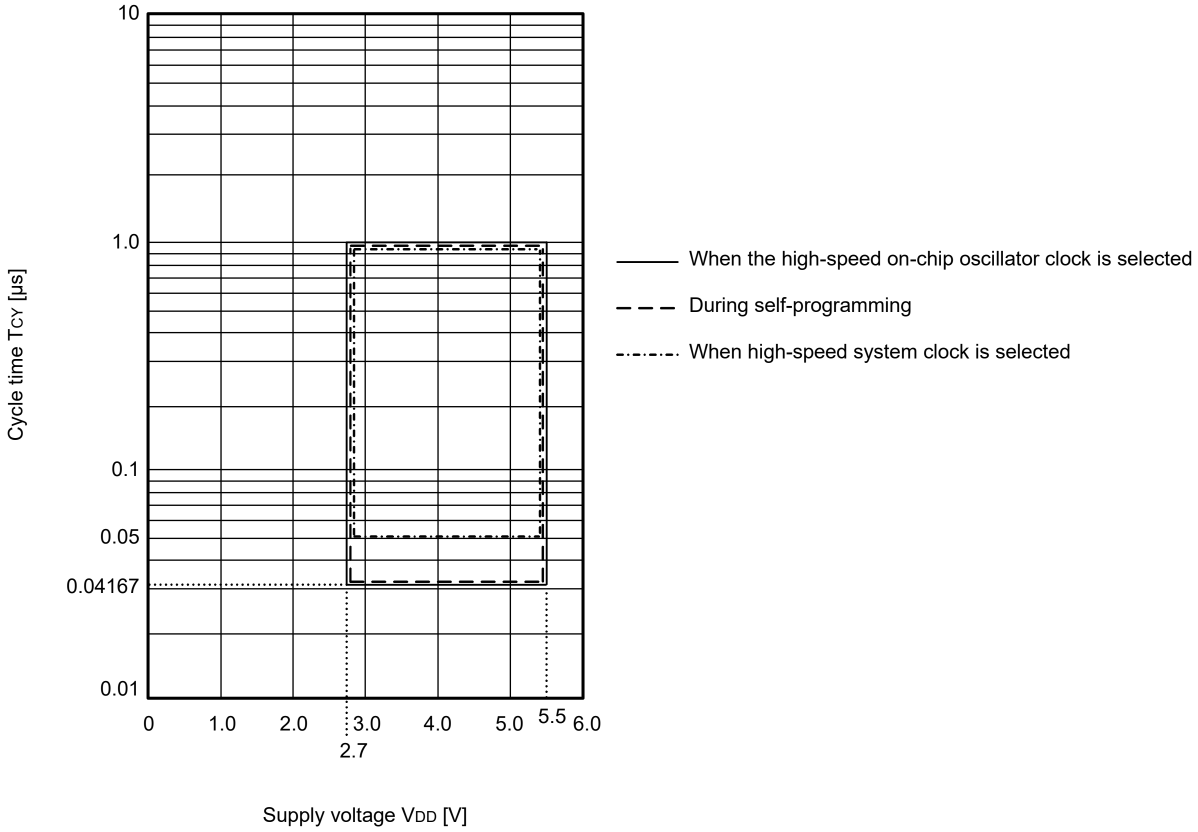
**($T_A$ = -40 to +85°C, $2.7\ \text{V} \le V_{DD} \le 5.5\ \text{V}$, $V_{SS}$ = 0 V)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Instruction cycle (minimum instruction execution time) | $T_{CY}$ | Main system clock ($f_{MAIN}$) operation | HS (high-speed main) mode | $2.7\ \text{V} \le V_{DD} \le 5.5\ \text{V}$ | 0.04167 | | 1 | μs |
| | | | LS (low-speed main) mode | $2.7\ \text{V} \le V_{DD} \le 5.5\ \text{V}$ | 0.125 | | 1 | μs |
| | | In the self programming mode | HS (high-speed main) mode | $2.7\ \text{V} \le V_{DD} \le 5.5\ \text{V}$ | 0.04167 | | 1 | μs |
| | | | LS (low-speed main) mode | $2.7\ \text{V} \le V_{DD} \le 5.5\ \text{V}$ | 0.125 | | 1 | μs |
| External main system clock frequency | $f_{EX}$ | $2.7\ \text{V} \le V_{DD} \le 5.5\ \text{V}$ | | | 1.0 | | 20.0 | MHz |
| External main system clock input high-level width, low-level width | $t_{EXH}$,<br>$t_{EXL}$ | $2.7\ \text{V} \le V_{DD} \le 5.5\ \text{V}$ | | | 24 | | | ns |
| TI00 to TI03 input high-level width, low-level width | $t_{TIH}$, $t_{TIL}$ | | | | $1/f_{MCK}$ + 10 | | | ns |
| Timer RJ input cycle | $f_C$ | TRJIO | | $2.7\ \text{V} \le V_{DD} \le 5.5\ \text{V}$ | 100 | | | ns |
| Timer RJ input high-level width, low-level width | $f_{WH}$, $f_{WL}$ | TRJIO | | $2.7\ \text{V} \le V_{DD} \le 5.5\ \text{V}$ | 40 | | | ns |
| TO00 to TO03, TRJIO0,TRJO, TRDIOA0/1, TRDIOB0/1, TRDIOC0/1,TRDIOD0/1 output frequency | $f_{TO}$ | HS (high-speed main) mode | | $4.0\ \text{V} \le V_{DD} \le 5.5\ \text{V}$ | | | 12 | MHz |
| | | | | $2.7\ \text{V} \le V_{DD} < 4.0\ \text{V}$ | | | 8 | MHz |
| | | LS (low-speed main) mode | | $2.7\ \text{V} \le V_{DD} \le 5.5\ \text{V}$ | | | 4 | MHz |
| PCLBUZ0, PCLBUZ1 output frequency | $f_{PCL}$ | HS (high-speed main) mode | | $4.0\ \text{V} \le V_{DD} \le 5.5\ \text{V}$ | | | 16 | MHz |
| | | | | $2.7\ \text{V} \le V_{DD} < 4.0\ \text{V}$ | | | 8 | MHz |
| | | LS (low-speed main) mode | | $2.7\ \text{V} \le V_{DD} \le 5.5\ \text{V}$ | | | 4 | MHz |
| Interrupt input high-level width, low-level width | $t_{INTH}$,<br>$t_{INTL}$ | INTP0 to INTP5 | | $2.7\ \text{V} \le V_{DD} \le 5.5\ \text{V}$ | 1 | | | μs |
| Key interrupt input low-level width | $t_{KR}$ | KR0-KR3 | | $2.7\ \text{V} \le V_{DD} \le 5.5\ \text{V}$ | 250 | | | ns |
| $\overline{\text{RESET}}$ low-level width | $t_{RSL}$ | | | | 10 | | | μs |

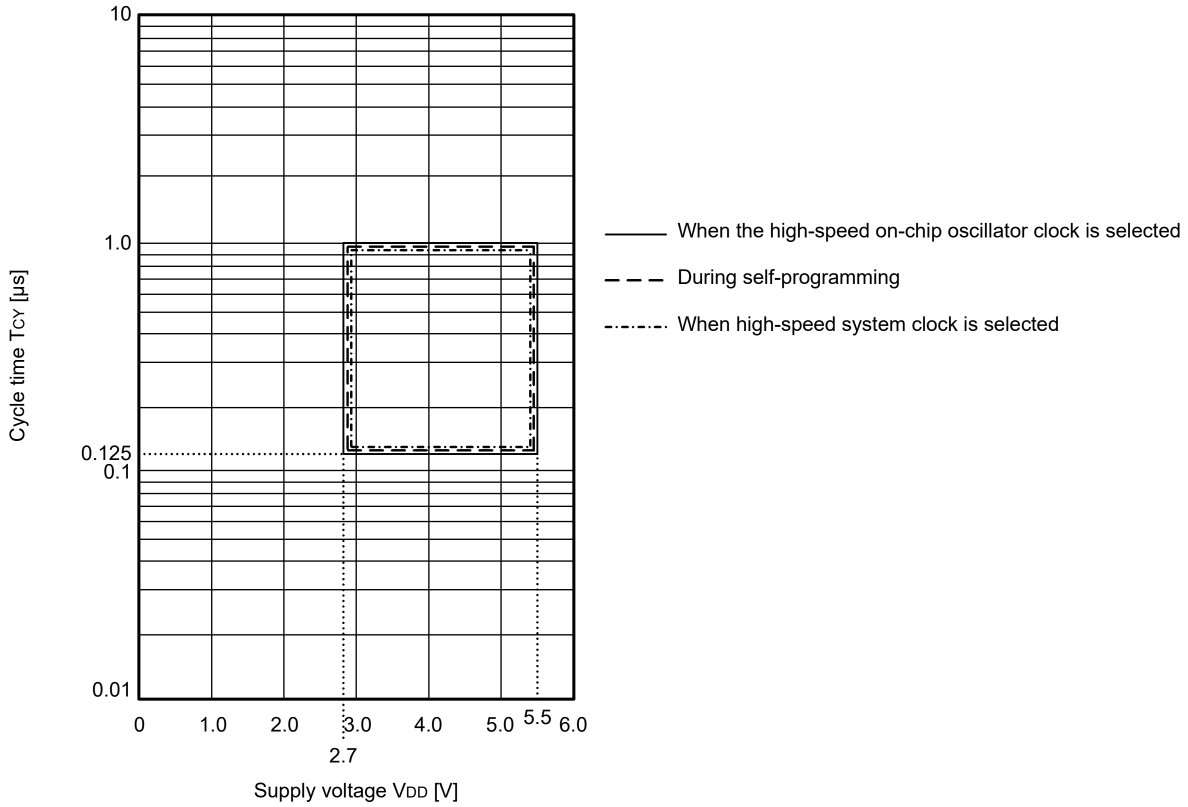
**Remark** $f_{MCK}$: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0), n: Channel number (n = 0 to 3))

Minimum Instruction Execution Time during Main System Clock Operation

TCY vs VDD (HS (high-speed main) mode)

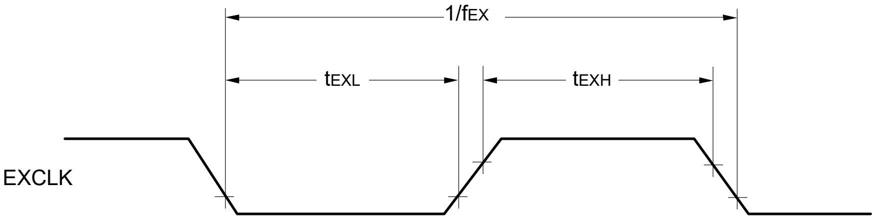


TCY vs VDD (LS (low-speed main) mode)

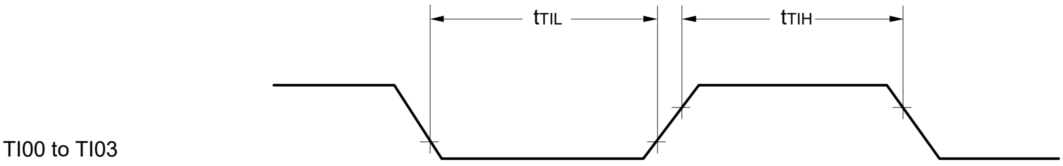


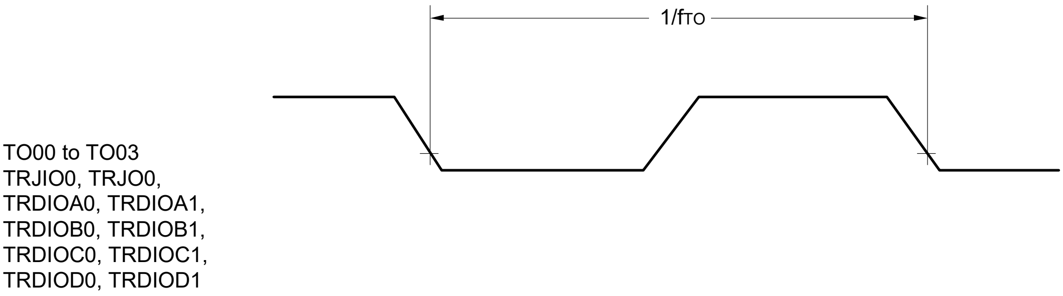
AC Timing Test Points

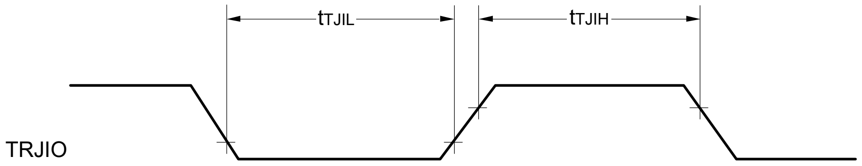
External System Clock Timing

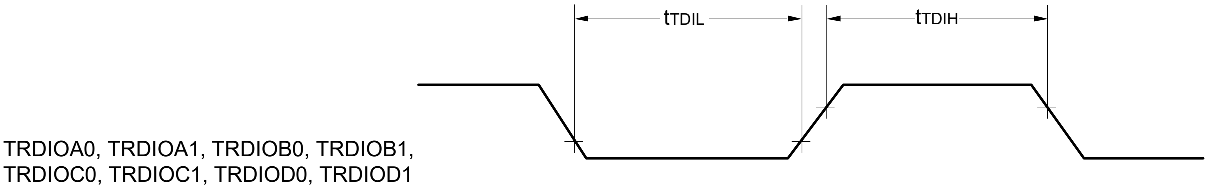


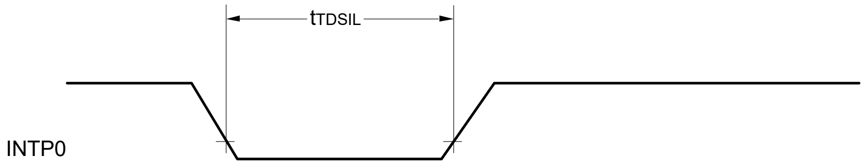
TI/TO Timing



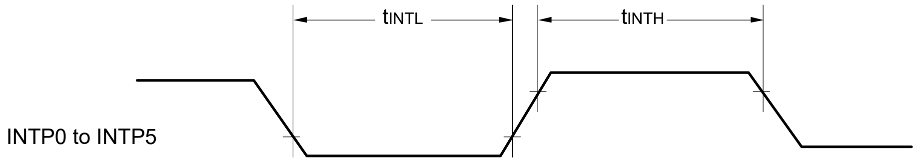



$t_{TJIL}$
$t_{TJIH}$
TRJIO

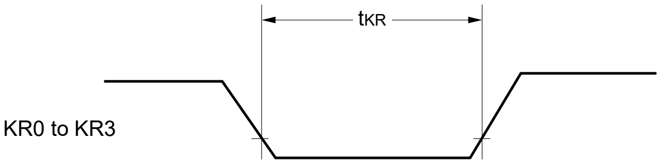

$t_{TDIL}$
$t_{TDIH}$
TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1,
TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1


$t_{TDSIL}$
INTP0

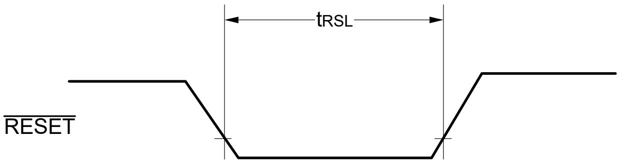
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



## 2.6 Peripheral Functions Characteristics

AC Timing Test Points

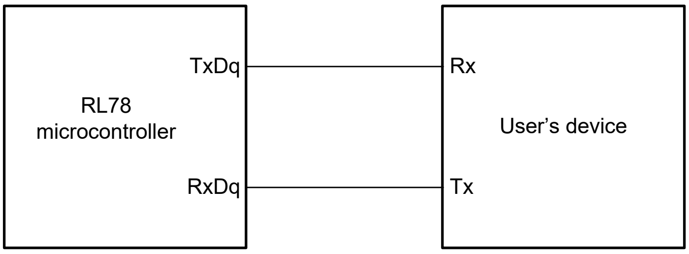
### 2.6.1 Serial array unit

**(1) During communication at same potential (UART mode)**

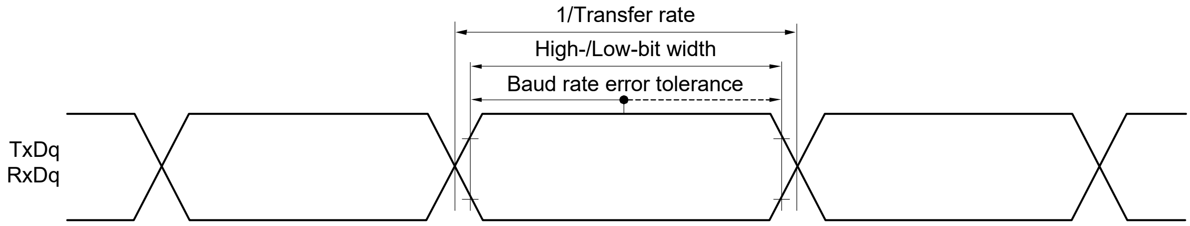
**($T_A$ = -40 to +85°C, 2.7 V ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate Note 1 | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | $f_{MCK}/6$ | | $f_{MCK}/6$ | bps |
| | | Theoretical value of the maximum transfer rate<br>$f_{MCK} = f_{CLK}$ Note 2 | | 4.0 | | 1.3 | Mbps |

**UART mode connection diagram (during communication at same potential)**



**UART mode bit width (during communication at same potential) (reference)**



**Note 1.** Transfer rate in the SNOOZE mode is 4800 bps only.
However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

**Note 2.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)
LS (low-speed main) mode: 8 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)

**Caution** **Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark 1.** q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 5)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

### (2) During communication at same potential (simplified SPI (CSI) mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 2/f_{CLK}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 83.3 | | 250 | | ns |
| SCKp high-/low-level width | $t_{KH1}$, $t_{KL1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY1}/2$ - 7 | | $t_{KCY1}/2$ - 50 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY1}/2$ - 10 | | $t_{KCY1}/2$ - 50 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | 23 | | 110 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 33 | | 110 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI1}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 10 | | 10 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO1}$ | C = 20 pF Note 4 | | | 10 | | 10 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SCKp and SOp output lines.

**Caution** **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark 1.** This value is valid only when CSI00's peripheral I/O redirect function is not used.

**Remark 2.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM numbers (g = 1)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00))

### (3) During communication at same potential (simplified SPI (CSI) mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1}$ ≥ 4/$f_{CLK}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 167 | | 500 | | ns |
| SCKp high-/low-level width | $t_{KH1}$, $t_{KL1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 12 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 18 | | $t_{KCY1}$/2 - 50 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | 44 | | 110 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 44 | | 110 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI1}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 19 | | 19 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO1}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V<br>C = 30 pF Note 4 | | | 25 | | 25 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SCKp and SOp output lines.

**Caution** **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark 1.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 5)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

### (4) During communication at same potential (simplified SPI (CSI) mode) (slave mode, SCKp... external clock input)

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time Note 5 | $t_{KCY2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 20 MHz < $f_{MCK}$ | 8/$f_{MCK}$ | | — | | ns |
| | | | $f_{MCK}$ ≤ 20 MHz | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 16 MHz < $f_{MCK}$ | 8/$f_{MCK}$ | | — | | ns |
| | | | $f_{MCK}$ ≤ 16 MHz | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$,<br>$t_{KL2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2 - 7 | | $t_{KCY2}$/2 - 7 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2 - 8 | | $t_{KCY2}$/2 - 8 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK2}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI2}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO2}$ | C = 30 pF Note 4 | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 44 | | 2/$f_{MCK}$ + 110 | ns |
| $\overline{\text{SSI00}}$ setup time | $t_{SSIK}$ | DAPmn = 0 | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 120 | | 120 | | ns |
| | | DAPmn = 1 | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1/$f_{MCK}$ + 120 | | 1/$f_{MCK}$ + 120 | | ns |
| $\overline{\text{SSI00}}$ hold time | $t_{KSSI}$ | DAPmn = 0 | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1/$f_{MCK}$ + 120 | | 1/$f_{MCK}$ + 120 | | ns |
| | | DAPmn = 1 | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 120 | | 120 | | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SOp output lines.

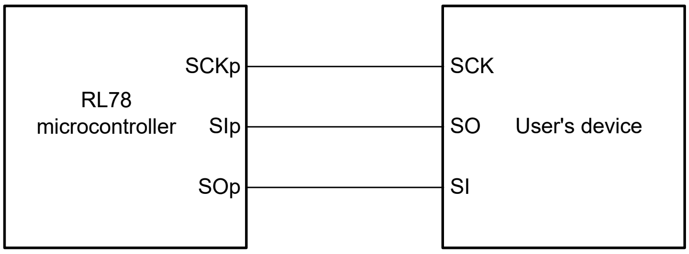
**Note 5.** The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

**Caution** **Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

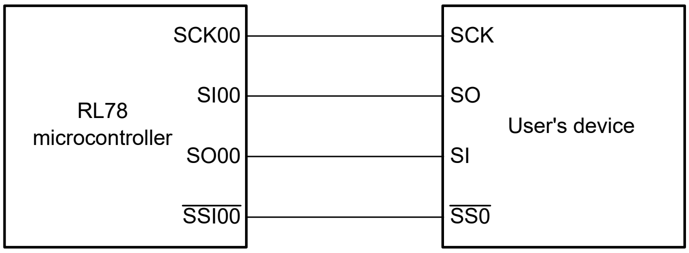
**Remark 1.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 5)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00))

**Simplified SPI (CSI) mode connection diagram (during communication at same potential)**



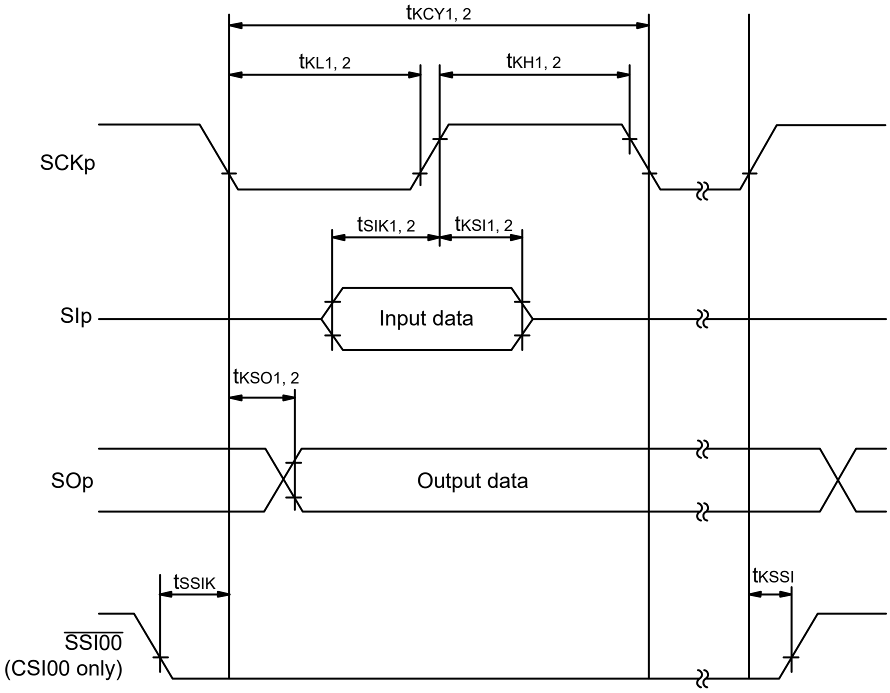
**Simplified SPI (CSI) mode connection diagram (during communication at same potential)**
**(Slave Transmission of slave select input function (CSI00))**



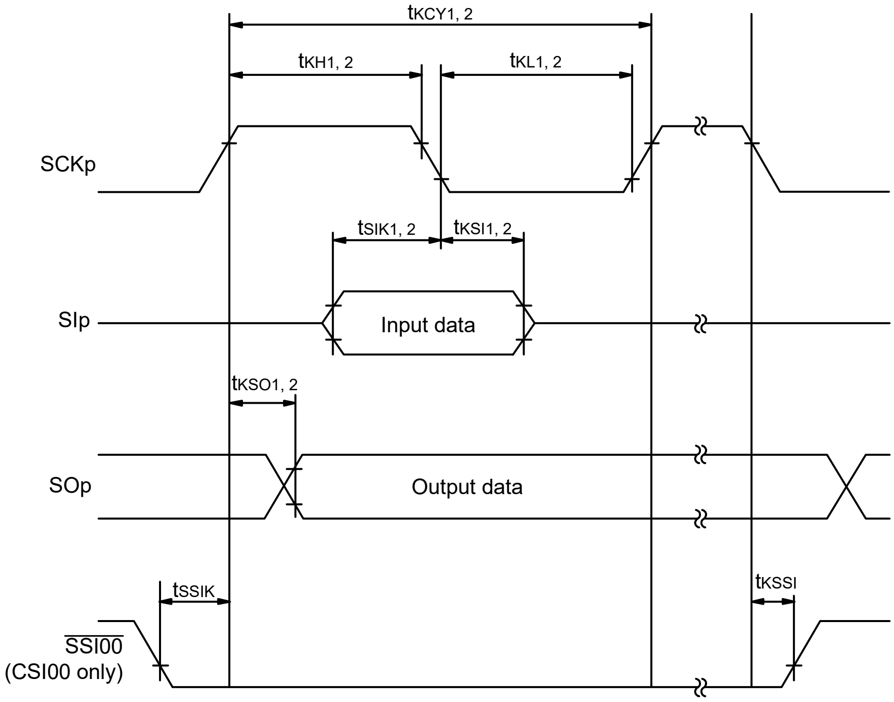
**Remark 1.** p: CSI number (p = 00)

**Remark 2.** m: Unit number, n: Channel number (mn = 00)

**Simplified SPI (CSI) mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**Simplified SPI (CSI) mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



**Remark 1.** p: CSI number (p = 00)

**Remark 2.** m: Unit number, n: Channel number (mn = 00)

### (5) During communication at same potential (simplified I$^2$C mode)

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

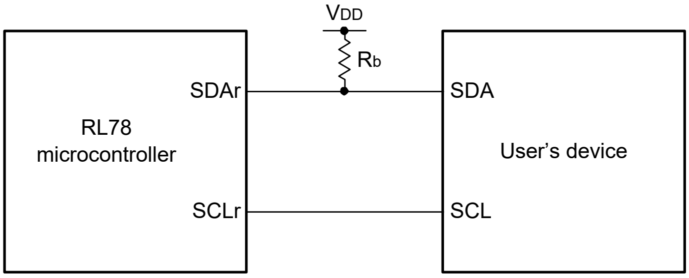
| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V,<br>$C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 1000 Note 1 | | 400 Note 1 | kHz |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V,<br>$C_b$ = 100 pF, $R_b$ = 3 kΩ | | 400 Note 1 | | 400 Note 1 | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V,<br>$C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 475 | | 1150 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V,<br>$C_b$ = 100 pF, $R_b$ = 3 kΩ | 1150 | | 1150 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V,<br>$C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 475 | | 1150 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V,<br>$C_b$ = 100 pF, $R_b$ = 3 kΩ | 1150 | | 1150 | | ns |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V,<br>$C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 85 Note 2 | | 1/$f_{MCK}$ + 145 Note 2 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V,<br>$C_b$ = 100 pF, $R_b$ = 3 kΩ | 1/$f_{MCK}$ + 145 Note 2 | | 1/$f_{MCK}$ + 145 Note 2 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V,<br>$C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 305 | 0 | 305 | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V,<br>$C_b$ = 100 pF, $R_b$ = 3 kΩ | 0 | 355 | 0 | 355 | ns |

**Note 1.** The value must also be equal to or less than $f_{MCK}$/4.

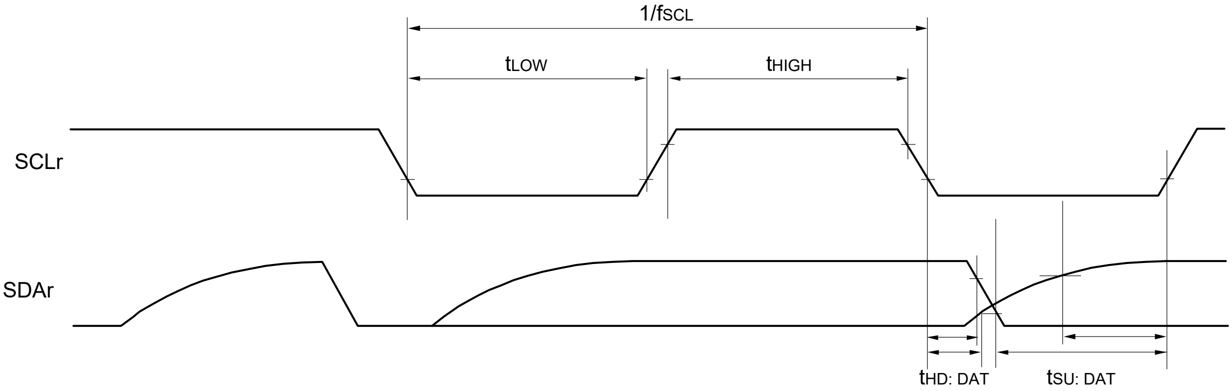
**Note 2.** Set the $f_{MCK}$ value to keep the hold time of SCLr = “L” and SCLr = “H”.

(Remarks are listed on the next page.)

**Simplified I²C mode connection diagram (during communication at same potential)**



**Simplified I²C mode serial transfer timing (during communication at same potential)**



**Caution** **Select the normal input buffer and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).**

**Remark 1.** $R_b$[Ω]: Communication line (SDAr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance

**Remark 2.** r: IIC number (r = 00), g: PIM number (g = 3, 5), h: POM number (h = 3, 5)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0),
n: Channel number (n = 0), mn = 00)

### (6) Communication at different potential (2.5 V, 3 V) (UART mode)

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(1/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate | | Reception | $4.0\ V \le V_{DD} \le 5.5\ V$,<br>$2.7\ V \le V_b \le 4.0\ V$ | | $f_{MCK}/6$ Note 1 | | $f_{MCK}/6$ Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate<br>$f_{MCK} = f_{CLK}$ Note 3 | | 4.0 | | 1.3 | Mbps |
| | | | $2.7\ V \le V_{DD} < 4.0\ V$,<br>$2.3\ V \le V_b \le 2.7\ V$ | | $f_{MCK}/6$ Note 1 | | $f_{MCK}/6$ Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate<br>$f_{MCK} = f_{CLK}$ Note 3 | | 4.0 | | 1.3 | Mbps |
| | | | $2.7\ V \le V_{DD} < 3.3\ V$,<br>$1.6\ V \le V_b \le 2.0\ V$ | | $f_{MCK}/6$<br>Notes 1, 2 | | $f_{MCK}/6$<br>Notes 1, 2 | bps |
| | | | Theoretical value of the maximum transfer rate<br>$f_{MCK} = f_{CLK}$ Note 3 | | 4.0 | | 1.3 | Mbps |

**Note 1.** Transfer rate in the SNOOZE mode is 4800 bps only.
However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

**Note 2.** Use it with $V_{DD} \ge V_b$.

**Note 3.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:

| | |
|---|---|
| HS (high-speed main) mode: | 24 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V) |
| LS (low-speed main) mode: | 8 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V) |

**Caution** **Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remark 1.** $V_b$[V]: Communication line voltage

**Remark 2.** q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 5)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03)

**Remark 4.** $V_{IH}$ and $V_{IL}$ below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in UART mode.
$4.0\ V \le V_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$: $V_{IH}$ = 2.2 V, $V_{IL}$ = 0.8 V
$2.7\ V \le V_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$: $V_{IH}$ = 2.0 V, $V_{IL}$ = 0.5 V
$2.7\ V \le V_{DD} < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V$: $V_{IH}$ = 1.50 V, $V_{IL}$ = 0.32 V

### (6) Communication at different potential (2.5 V, 3 V) (UART mode)

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate | | transmission | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V,<br>2.7 V ≤ $V_b$ ≤ 4.0 V | | Note 1 | | Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate<br>$C_b$ = 50 pF, $R_b$ = 1.4 kΩ,<br>$V_b$ = 2.7 V | | 2.8 Note 2 | | 2.8 Note 2 | Mbps |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V,<br>2.3 V ≤ $V_b$ ≤ 2.7 V | | Note 3 | | Note 3 | bps |
| | | | Theoretical value of the maximum transfer rate<br>$C_b$ = 50 pF, $R_b$ = 2.7 kΩ,<br>$V_b$ = 2.3 V | | 1.2 Note 4 | | 1.2 Note 4 | Mbps |
| | | | 2.7 V ≤ $V_{DD}$ < 3.3 V,<br>1.6 V ≤ $V_b$ ≤ 2.0 V | | Note 5, 6 | | Note 5, 6 | bps |
| | | | Theoretical value of the maximum transfer rate<br>$C_b$ = 50 pF, $R_b$ = 5.5 kΩ,<br>$V_b$ = 1.6 V | | 0.43 Note 7 | | 0.43 Note 7 | Mbps |

**Note 1.** The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ $V_{DD}$ ≤ 5.5 V and 2.7 V ≤ $V_b$ ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**Note 2.** This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

**Note 3.** The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ $V_{DD}$ < 4.0 V and 2.3 V ≤ $V_b$ ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**Note 4.** This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

**Note 5.** Use it with $V_{DD}$ ≥ $V_b$.

**Note 6.** The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when $2.7\ V \leq V_{DD} < 3.3\ V$ and $1.6\ V \leq V_b \leq 2.0\ V$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \ [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100\ [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**Note 7.** This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

**Caution** **Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

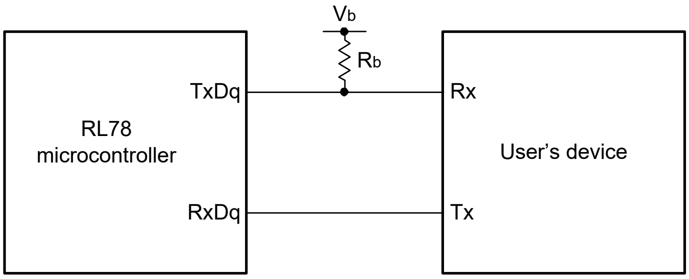
**Remark 1.** $R_b$[Ω]: Communication line (TxDq) pull-up resistance,
$C_b$[F]: Communication line (TxDq) load capacitance, $V_b$[V]: Communication line voltage

**Remark 2.** q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 5)

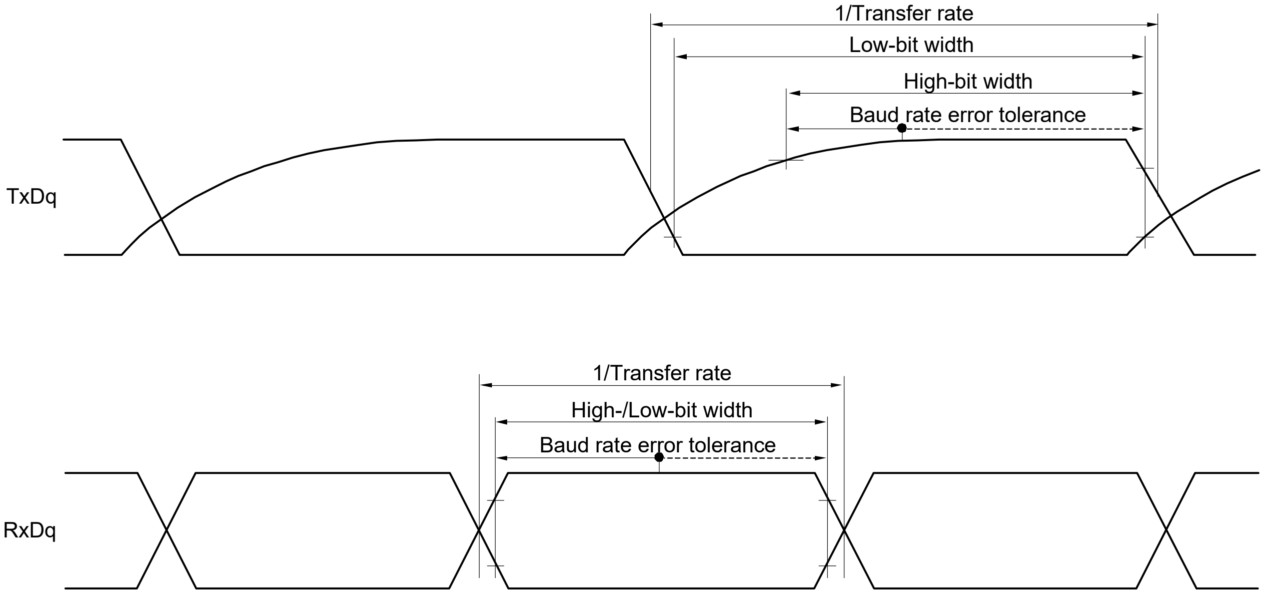
**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03))

**Remark 4.** $V_{IH}$ and $V_{IL}$ below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in UART mode.
$4.0\ V \leq V_{DD} \leq 5.5\ V$, $2.7\ V \leq V_b \leq 4.0\ V$: $V_{IH} = 2.2\ V$, $V_{IL} = 0.8\ V$
$2.7\ V \leq V_{DD} < 4.0\ V$, $2.3\ V \leq V_b \leq 2.7\ V$: $V_{IH} = 2.0\ V$, $V_{IL} = 0.5\ V$
$2.7\ V \leq V_{DD} < 3.3\ V$, $1.6\ V \leq V_b \leq 2.0\ V$: $V_{IH} = 1.50\ V$, $V_{IL} = 0.32\ V$

### UART mode connection diagram (during communication at different potential)



**UART mode bit width (during communication at different potential) (reference)**



**Remark 1.** $R_b$[Ω]: Communication line (TxDq) pull-up resistance, $V_b$[V]: Communication line voltage

**Remark 2.** q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 5)

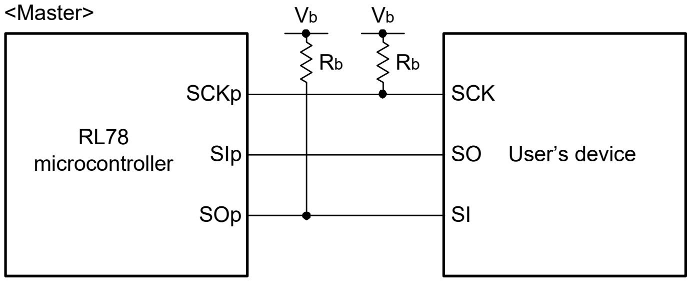
### (7) Communication at different potential (2.5 V, 3 V) (simplified SPI (CSI) mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \ge 2/f_{CLK}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V,<br>2.7 V ≤ $V_b$ ≤ 4.0 V,<br>$C_b$ = 20 pF, $R_b$ = 1.4 kΩ | 200 | | 1150 | | ns |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V,<br>2.3 V ≤ $V_b$ ≤ 2.7 V,<br>$C_b$ = 20 pF, $R_b$ = 2.7 kΩ | 300 | | 1150 | | ns |
| SCKp high-level width | $t_{KH1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}/2 - 50$ | | $t_{KCY1}/2 - 50$ | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}/2 - 120$ | | $t_{KCY1}/2 - 120$ | | ns |
| SCKp low-level width | $t_{KL1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}/2 - 7$ | | $t_{KCY1}/2 - 50$ | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}/2 - 10$ | | $t_{KCY1}/2 - 50$ | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 58 | | 479 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 121 | | 479 | | ns |
| SIp hold time (from SCKp↑) Note 1 | $t_{KSI1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 10 | | 10 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 10 | | 10 | | ns |
| Delay time from SCKp↓ to SOp output Note 1 | $t_{KSO1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | | 60 | | 60 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | | 130 | | 130 | ns |
| SIp setup time (to SCKp↓) Note 2 | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 23 | | 110 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 33 | | 110 | | ns |
| SIp hold time (from SCKp↓) Note 2 | $t_{KSI1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 10 | | 10 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 10 | | 10 | | ns |
| Delay time from SCKp↑ to SOp output Note 2 | $t_{KSO1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | | 10 | | 10 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | | 10 | | 10 | ns |

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

**Simplified SPI (CSI) mode connection diagram (during communication at different potential)**



**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

**Note 2.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution** **Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remark 1.** $R_b$[Ω]: Communication line (SCKp, SOp) pull-up resistance, $C_b$[F]: Communication line (SCKp, SOp) load capacitance, $V_b$[V]: Communication line voltage

**Remark 2.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 3, 5)

**Remark 3.** $V_{IH}$ and $V_{IL}$ below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in simplified SPI (CSI) mode.
$4.0 V \leq V_{DD} \leq 5.5 V$, $2.7 V \leq V_b \leq 4.0 V$: $V_{IH} = 2.2 V$, $V_{IL} = 0.8 V$
$2.7 V \leq V_{DD} < 4.0 V$, $2.3 V \leq V_b \leq 2.7 V$: $V_{IH} = 2.0 V$, $V_{IL} = 0.5 V$

**Remark 4.** This value is valid only when CSI00's peripheral I/O redirect function is not used.

### (8) Communication at different potential (2.5 V, 3 V) ($f_{MCK}$/4) (simplified SPI (CSI) mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(1/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1}$ ≥ 4/$f_{CLK}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 300 | | 1150 | | ns |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 500 | | 1150 | | ns |
| | | | 2.7 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 1150 | | 1150 | | ns |
| SCKp high-level width | $t_{KH1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 - 75 | | $t_{KCY1}$/2 - 75 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 170 | | $t_{KCY1}$/2 - 170 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 - 458 | | $t_{KCY1}$/2 - 458 | | ns |
| SCKp low-level width | $t_{KL1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 - 12 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 18 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |

**Caution 1. Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Caution 2. Use it with $V_{DD}$ ≥ $V_b$.**

**Remark 1.** $R_b$[Ω]: Communication line (SCKp, SOp) pull-up resistance, $C_b$[F]: Communication line (SCKp, SOp) load capacitance, $V_b$[V]: Communication line voltage

**Remark 2.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 3, 5)

**Remark 3.** $V_{IH}$ and $V_{IL}$ below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in simplified SPI (CSI) mode.

4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V: $V_{IH}$ = 2.2 V, $V_{IL}$ = 0.8 V
2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V: $V_{IH}$ = 2.0 V, $V_{IL}$ = 0.5 V

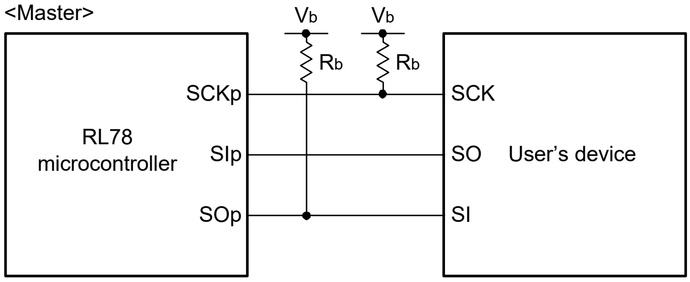
### (8) Communication at different potential (2.5 V, 3 V) ($f_{MCK}$/4) (simplified SPI (CSI) mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| SIp setup time (to SCKp↑) [Note 1] | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 81 | | 479 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 177 | | 479 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 479 | | 479 | | ns |
| SIp hold time (from SCKp↑) [Note 1] | $t_{KSI1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 19 | | 19 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 19 | | 19 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 19 | | 19 | | ns |
| Delay time from SCKp↓ to SOp output [Note 1] | $t_{KSO1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 100 | | 100 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 195 | | 195 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 483 | | 483 | ns |
| SIp setup time (to SCKp↓) [Note 2] | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 44 | | 110 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 44 | | 110 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 110 | | 110 | | ns |
| SIp hold time (from SCKp↓) [Note 2] | $t_{KSI1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 19 | | 19 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 19 | | 19 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 19 | | 19 | | ns |
| Delay time from SCKp↑ to SOp output [Note 2] | $t_{KSO1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 25 | | 25 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 25 | | 25 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 25 | | 25 | ns |

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

### Simplified SPI (CSI) mode connection diagram (during communication at different potential)



**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

**Note 2.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution 1. Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Caution 2. Use it with $V_{DD} \geq V_b$.**

**Remark 1.** $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[F]$: Communication line (SCKp, SOp) load capacitance, $V_b[V]$: Communication line voltage

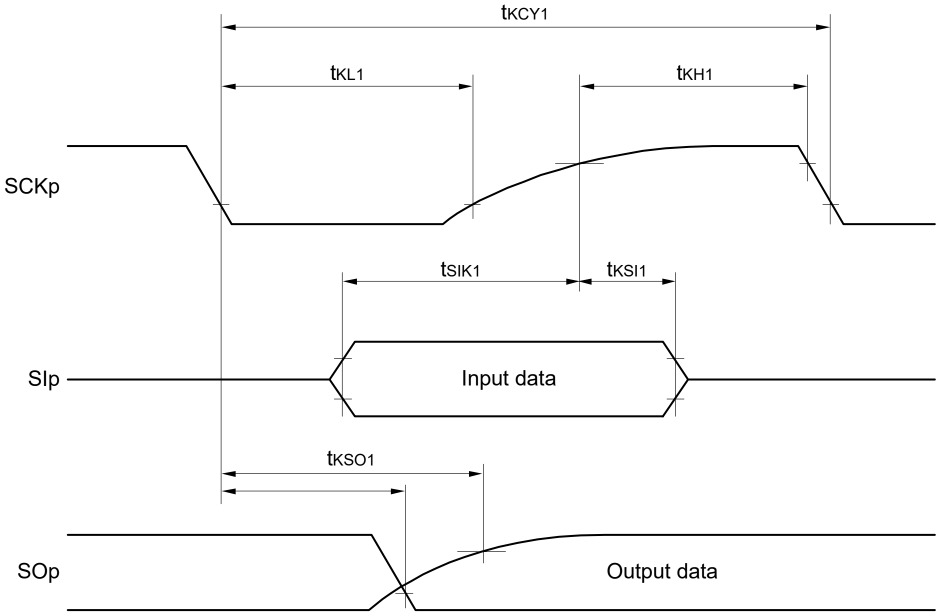
**Remark 2.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 3, 5)

**Remark 3.** $V_{IH}$ and $V_{IL}$ below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in simplified SPI (CSI) mode.

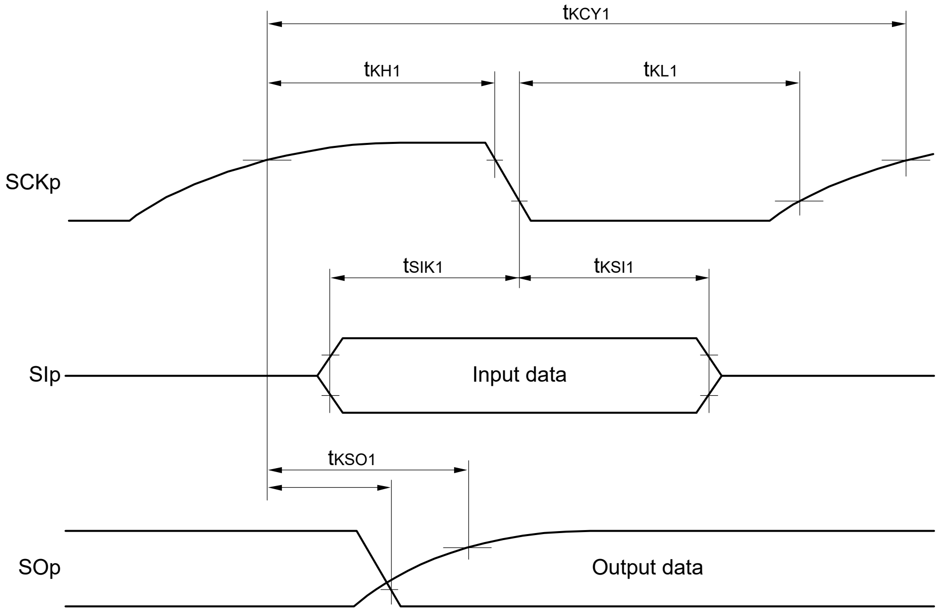
$4.0 V \leq V_{DD} \leq 5.5 V, 2.7 V \leq V_b \leq 4.0 V$: $V_{IH} = 2.2 V, V_{IL} = 0.8 V$

$2.7 V \leq V_{DD} < 4.0 V, 2.3 V \leq V_b \leq 2.7 V$: $V_{IH} = 2.0 V, V_{IL} = 0.5 V$

### Simplified SPI (CSI) mode serial transfer timing (master mode) (during communication at different potential) (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



### Simplified SPI (CSI) mode serial transfer timing (master mode) (during communication at different potential) (When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



**Remark** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 3, 5)

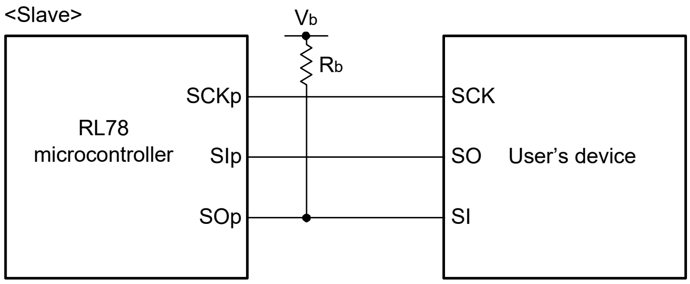
### (9) Communication at different potential (2.5 V, 3 V) (simplified SPI (CSI) mode) (slave mode, SCKp... external clock input)

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time Note 1 | $t_{KCY2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V,<br>2.7 V ≤ $V_b$ ≤ 4.0 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 12/$f_{MCK}$ | | — | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 20 MHz | 10/$f_{MCK}$ | | — | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 8/$f_{MCK}$ | | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 6/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V,<br>2.3 V ≤ $V_b$ ≤ 2.7 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 16/$f_{MCK}$ | | — | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 14/$f_{MCK}$ | | — | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 12/$f_{MCK}$ | | — | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 8/$f_{MCK}$ | | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 6/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 3.3 V,<br>1.6 V ≤ $V_b$ ≤ 2.0 V<br>Note 2 | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 36/$f_{MCK}$ | | — | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 32/$f_{MCK}$ | | — | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 26/$f_{MCK}$ | | — | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$,<br>$t_{KL2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $t_{KCY2}$/2 - 12 | | $t_{KCY2}$/2 - 50 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $t_{KCY2}$/2 - 18 | | $t_{KCY2}$/2 - 50 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | | $t_{KCY2}$/2 - 50 | | $t_{KCY2}$/2 - 50 | | ns |
| SIp setup time (to SCKp↑) Note 3 | $t_{SIK2}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | ns |
| SIp hold time (from SCKp↑) Note 4 | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| Delay time from SCKp↓ to SOp output Note 5 | $t_{KSO2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V,<br>$C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | | 2/$f_{MCK}$ + 120 | | 2/$f_{MCK}$ + 573 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V,<br>$C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | | 2/$f_{MCK}$ + 214 | | 2/$f_{MCK}$ + 573 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2,<br>$C_b$ = 30 pF, $R_v$ = 5.5 kΩ | | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

### Simplified SPI (CSI) mode connection diagram (during communication at different potential)



**Note 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps

**Note 2.** Use it with $V_{DD} \geq V_b$.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 5.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution** **Select the TTL input buffer for the SIp pin and SCKp pin, and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remark 1.** $R_b$[Ω]: Communication line (SOp) pull-up resistance, $C_b$[F]: Communication line (SOp) load capacitance,
$V_b$[V]: Communication line voltage

**Remark 2.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 3, 5)

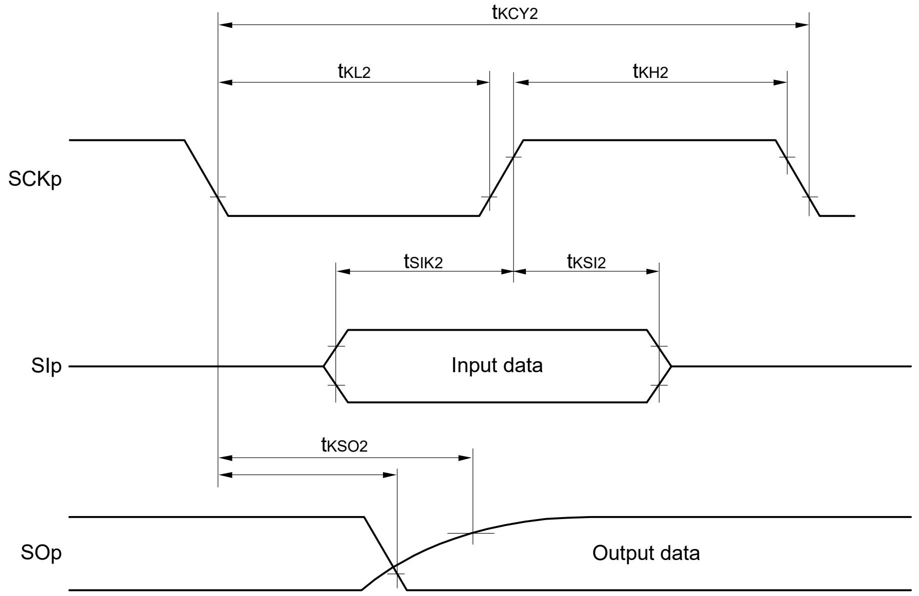
**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

**Remark 4.** $V_{IH}$ and $V_{IL}$ below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in simplified SPI (CSI) mode.

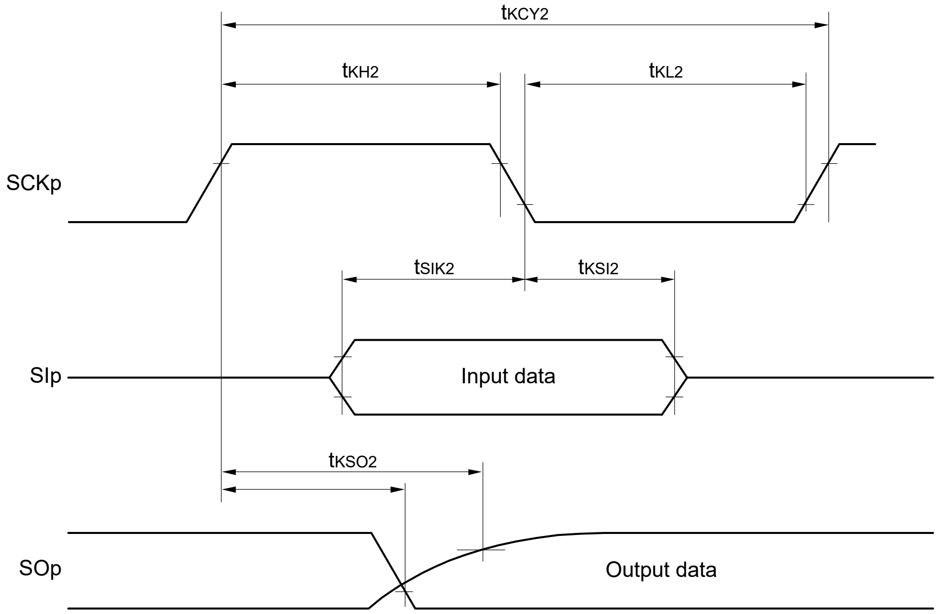
$4.0 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}, 2.7 \text{ V} \leq V_b \leq 4.0 \text{ V}: V_{IH} = 2.2 \text{ V}, V_{IL} = 0.8 \text{ V}$
$2.7 \text{ V} \leq V_{DD} < 4.0 \text{ V}, 2.3 \text{ V} \leq V_b \leq 2.7 \text{ V}: V_{IH} = 2.0 \text{ V}, V_{IL} = 0.5 \text{ V}$

**Remark 5.** Communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

**Simplified SPI (CSI) mode serial transfer timing (slave mode) (during communication at different potential) (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**Simplified SPI (CSI) mode serial transfer timing (slave mode) (during communication at different potential) (When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



**Remark 1.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 3, 5)

**Remark 2.** Communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

### (10) Communication at different potential (2.5 V, 3 V) (simplified I$^2$C mode)

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(1/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 1000 Note 1 | | 300 Note 1 | kHz |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ < 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 1000 Note 1 | | 300 Note 1 | kHz |
| | | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | | 400 Note 1 | | 300 Note 1 | kHz |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | | 400 Note 1 | | 300 Note 1 | kHz |
| | | 2.7 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ < 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | | 300 Note 1 | | 300 Note 1 | kHz |
| Hold time when SCLr = "L" | $t_{LOW}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 475 | | 1550 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ < 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 475 | | 1550 | | ns |
| | | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 1150 | | 1550 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 1150 | | 1550 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ < 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1550 | | 1550 | | ns |
| Hold time when SCLr = "H" | $t_{HIGH}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 245 | | 610 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ < 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 200 | | 610 | | ns |
| | | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 675 | | 610 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 600 | | 610 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ < 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 610 | | 610 | | ns |

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

### (10) Communication at different potential (2.5 V, 3 V) (simplified $I^2C$ mode)

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| Data setup time (reception) | $t_{SU:DAT}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V,<br>2.7 V ≤ $V_b$ ≤ 4.0 V,<br>$C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 135 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V,<br>2.3 V ≤ $V_b$ < 2.7 V,<br>$C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 135 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | ns |
| | | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V,<br>2.7 V ≤ $V_b$ ≤ 4.0 V,<br>$C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 1/$f_{MCK}$ + 190 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V,<br>2.3 V ≤ $V_b$ < 2.7 V,<br>$C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 190 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 3.3 V,<br>1.6 V ≤ $V_b$ < 2.0 V Note 2,<br>$C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1/$f_{MCK}$ + 190 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V,<br>2.7 V ≤ $V_b$ ≤ 4.0 V,<br>$C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 305 | 0 | 305 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V,<br>2.3 V ≤ $V_b$ < 2.7 V,<br>$C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 305 | 0 | 305 | ns |
| | | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V,<br>2.7 V ≤ $V_b$ ≤ 4.0 V,<br>$C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 0 | 355 | 0 | 355 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V,<br>2.3 V ≤ $V_b$ < 2.7 V,<br>$C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 0 | 355 | 0 | 355 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 3.3 V,<br>1.6 V ≤ $V_b$ < 2.0 V Note 2,<br>$C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 0 | 405 | 0 | 405 | ns |

**Note 1.** The value must also be equal to or less than $f_{MCK}/4$.

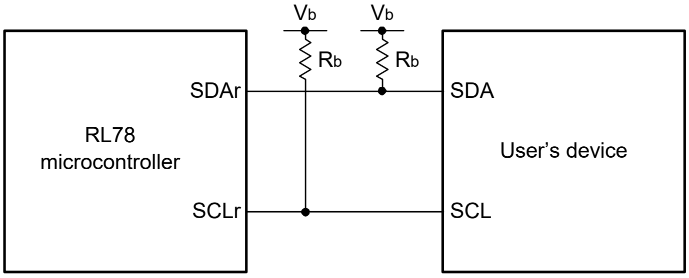
**Note 2.** Use it with $V_{DD} \geq V_b$.

**Note 3.** Set the $f_{MCK}$ value to keep the hold time of SCLr = “L” and SCLr = “H”.

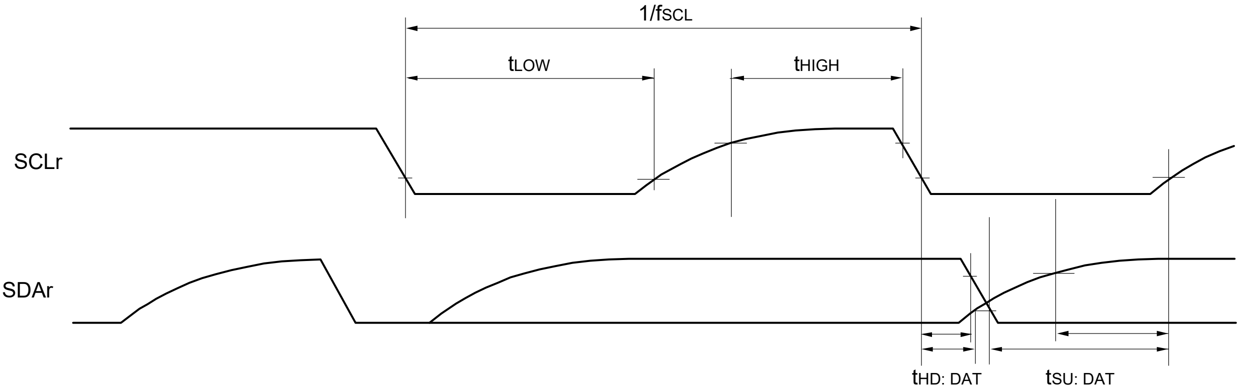
**Caution** **Select the TTL input buffer and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SDAr pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

### Simplified I²C mode connection diagram (during communication at different potential)



### Simplified I²C mode serial transfer timing (during communication at different potential)



**Remark 1.** $R_b$[Ω]: Communication line (SDAr, SCLr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance, $V_b$[V]: Communication line voltage

**Remark 2.** r: IIC number (r = 00), g: PIM, POM number (g = 3, 5)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0), mn = 00)

**Remark 4.** $V_{IH}$ and $V_{IL}$ below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in simplified I²C mode.

$4.0 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}, 2.7 \text{ V} \leq V_b \leq 4.0 \text{ V}: V_{IH} = 2.2 \text{ V}, V_{IL} = 0.8 \text{ V}$
$2.7 \text{ V} \leq V_{DD} < 4.0 \text{ V}, 2.3 \text{ V} \leq V_b \leq 2.7 \text{ V}: V_{IH} = 2.0 \text{ V}, V_{IL} = 0.5 \text{ V}$

## 2.7 Analog Characteristics

### 2.7.1 A/D converter characteristics

**Classification of A/D converter characteristics**

| Reference Voltage / Input channel | Reference voltage (+) = AVREFP<br>Reference voltage (-) = AVREFM | Reference voltage (+) = VDD<br>Reference voltage (-) = VSS | Reference voltage (+) = VBGR<br>Reference voltage (-) = AVREFM |
|---|---|---|---|
| ANI0 to ANI7 | Refer to **2.7.1 (1)**. | Refer to **2.7.1 (3)**. | Refer to **2.7.1 (4)**. |
| ANI16 to ANI19 | Refer to **2.7.1 (2)**. | | |
| Internal reference voltage<br>Temperature sensor output voltage | Refer to **2.7.1 (1)**. | | — |

**(1) When AVREF (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), AVREF (-) = AVREFM/ANI1 (ADREFM = 1), target ANI pin: ANI2 to ANI7**

**(TA = -40 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V, Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution<br>AVREFP = VDD | 2.7 V ≤ VDD ≤ 5.5 V | | 1.2 | ±3.5 | LSB |
| Conversion time | tCONV | 10-bit resolution<br>AVREFP = VDD | 3.6 V ≤ VDD ≤ 5.5 V | 2.125 | | 39 | μs |
| | | | 2.7 V ≤ VDD ≤ 5.5 V | 3.1875 | | 39 | μs |
| Zero-scale error Notes 1, 2 | EZS | 10-bit resolution<br>AVREFP = VDD | 2.7 V ≤ VDD ≤ 5.5 V | | | ±0.25 | % FSR |
| Full-scale error Notes 1, 2 | EFS | 10-bit resolution<br>AVREFP = VDD | 2.7 V ≤ VDD ≤ 5.5 V | | | ±0.25 | % FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution<br>AVREFP = VDD | 2.7 V ≤ VDD ≤ 5.5 V | | | ±2.5 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution<br>AVREFP = VDD | 2.7 V ≤ VDD ≤ 5.5 V | | | ±1.5 | LSB |
| Reference voltage (+) | AVREFP | | | 2.7 | | VDD | V |
| Analog input voltage | VAIN | | | 0 | | AVREFP | V |
| | VBGR | Select internal reference voltage output,<br>2.7 V ≤ VDD ≤ 5.5 V,<br>HS (high-speed main) mode | | 1.38 | 1.45 | 1.5 | V |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (% FSR) to the full-scale value.

**(2) When $AV_{REF}$ (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), $AV_{REF}$ (-) = $AV_{REFM}$/ANI1 (ADREFM = 1), target ANI pin: ANI16 to ANI19**

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (-) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 1.2 | ±5.0 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | μs |
| Zero-scale error Notes 1, 2 | EZS | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.35 | % FSR |
| Full-scale error Notes 1, 2 | EFS | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.35 | % FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±3.5 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.0 | LSB |
| Reference voltage (+) | $AV_{REFP}$ | | | 2.7 | | $V_{DD}$ | V |
| Analog input voltage | $V_{AIN}$ | | | 0 | | $AV_{REFP}$ | V |
| | $V_{BGR}$ | Select internal reference voltage output,<br>2.7 V ≤ $V_{DD}$ ≤ 5.5 V,<br>HS (high-speed main) mode | | 1.38 | 1.45 | 1.5 | V |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (% FSR) to the full-scale value.

### (3) When $AV_{REF}$ (+) = $V_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), $AV_{REF}$ (-) = $V_{SS}$ (ADREFM = 0), target ANI pin: ANI0 to ANI7, ANI16 to ANI19

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $V_{DD}$, Reference voltage (-) = $V_{SS}$)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | $R_{ES}$ | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 1.2 | ±7.0 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | µs |
| Zero-scale error Notes 1, 2 | EZS | 10-bit resolution | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | % FSR |
| Full-scale error Notes 1, 2 | EFS | 10-bit resolution | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | % FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±4.0 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI0 to ANI7 | | 0 | | $V_{DD}$ | V |
| | | ANI16 to ANI19 | | 0 | | $V_{DD}$ | V |
| | $V_{BGR}$ | Select internal reference voltage output,<br>2.7 V ≤ $V_{DD}$ ≤ 5.5 V,<br>HS (high-speed main) mode | | 1.38 | 1.45 | 1.5 | V |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (% FSR) to the full-scale value.

### (4) When AVREF (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), AVREF (-) = AVREFM/ANI1 (ADREFM = 1), target ANI pin: ANI0 to ANI7, ANI16 to ANI19

**(TA = -40 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V, Reference voltage (+) = VBGR, Reference voltage (-) = AVREFM = 0 V, HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | | bit |
| Conversion time | tCONV | 8-bit resolution | 2.7 V ≤ VDD ≤ 5.5 V | 17 | | 39 | μs |
| Zero-scale error Notes 1, 2 | EZS | 8-bit resolution | 2.7 V ≤ VDD ≤ 5.5 V | | | ±0.60 | % FSR |
| Integral linearity error Note 1 | ILE | 8-bit resolution | 2.7 V ≤ VDD ≤ 5.5 V | | | ±2.0 | LSB |
| Differential linearity error Note 1 | DLE | 8-bit resolution | 2.7 V ≤ VDD ≤ 5.5 V | | | ±1.0 | LSB |
| Reference voltage (+) | VBGR | | | 1.38 | 1.45 | 1.5 | V |
| Analog input voltage | VAIN | | | 0 | | VBGR | V |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (% FSR) to the full-scale value.

### 2.7.2 Temperature sensor characteristics

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Temperature sensor output voltage | $V_{TMPS25}$ | Setting ADS register = 80H, $T_A$ = +25°C | | 1.05 | | V |
| Reference output voltage | $V_{CONST}$ | Setting ADS register = 81H | 1.38 | 1.45 | 1.5 | V |
| Temperature coefficient | $F_{VTMPS}$ | Temperature sensor that depends on the temperature | | -3.6 | | mV/°C |
| Operation stabilization wait time | $t_{AMP}$ | | 5 | | | μs |

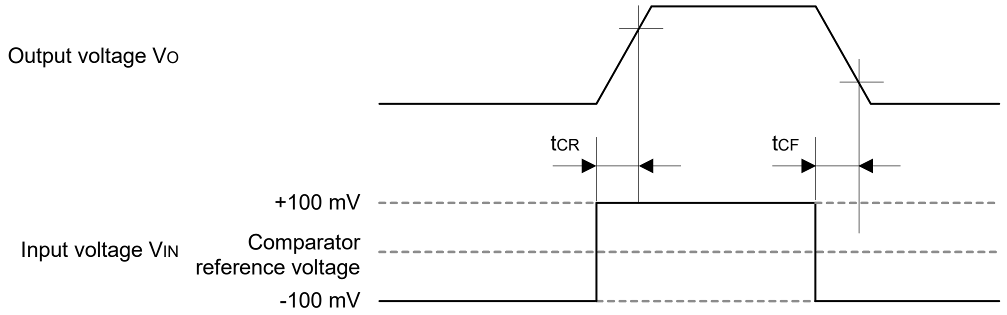
### 2.7.3 Comparator

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input offset voltage | $V_{IOCMP}$ | | | | ±5 | ±40 | mV |
| Input voltage range | $V_{ICMP}$ | | | 0 | | $V_{DD}$ | V |
| Internal reference voltage deviation | $\Delta V_{IREF}$ | CmRVM register value: 7FH to 80H (m = 0, 1) | | | | ±2 | LSB |
| | | Other than above | | | | ±1 | LSB |
| Response time | $t_{CR}$, $t_{CF}$ | Input amplitude = ±100 mV | | | 70 | 150 | ns |
| Operation stabilization time [Note 1] | $t_{CMP}$ | CMPnEN = 0→1 | $V_{DD}$ = 3.3 to 5.5 V | | | 1 | μs |
| | | | $V_{DD}$ = 2.7 to 3.3 V | | | 3 | |
| Reference voltage stabilization wait time | $t_{VR}$ | CVRE: 0→1 [Note 2] | | | | 20 | μs |

**Note 1.** Time required after the operation enable signal of the comparator has been changed (CMPnEN = 0 → 1) until a state satisfying the DC and AC characteristics of the comparator is entered.

**Note 2.** Enable operation of internal reference voltage generation (CVREm bit = 1; m = 0, 1) and wait for the operation stabilization wait time before enabling the comparator output (CnOE bit = 1; n = 0, 1).



### 2.7.4 Programmable gain amplifier

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input offset voltage | $V_{IOPGA}$ | | | | ±5 | ±10 | mV |
| Input voltage range | $V_{IPGA}$ | | | 0 | | 0.9 × $V_{DD}$/gain | V |
| Response time | $V_{OHPGA}$ | | | 0.9 × $V_{DD}$ | | | V |
| | $V_{OLPGA}$ | | | | | 0.1 × $V_{DD}$ | |
| Gain error | — | 4, 8 times | | | | ±1 | % |
| | | 16 times | | | | ±1.5 | |
| | | 32 times | | | | ±2 | |
| Slew rate | $SR_{RPGA}$ | Rising edge | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 1.4 | | | V/μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 4.0 V | 0.5 | | | |
| | $SR_{FPGA}$ | Falling edge | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 1.4 | | | |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 4.0 V | 0.5 | | | |
| Operation stabilization wait time Note | $t_{PGA}$ | 4, 8 times | | | | 5 | μs |
| | | 16, 32 times | | | | 10 | |

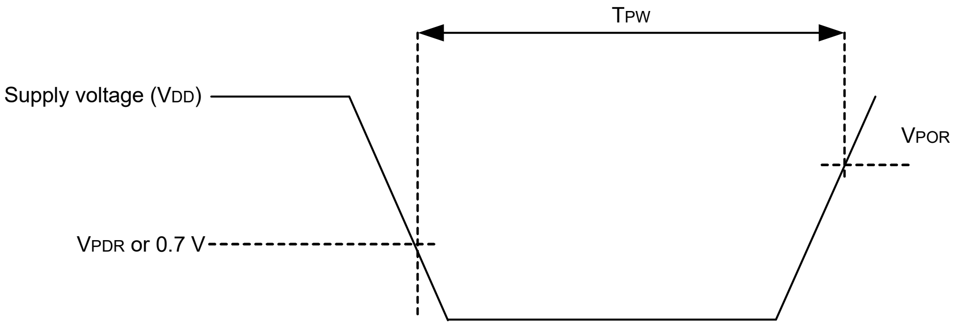
**Note** Time required after the PGA operation has been enabled (PGAEN = 1) until a state satisfying the DC and AC specifications of the PGA is entered.

### 2.7.5 POR circuit characteristics

**($T_A$ = -40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Detection voltage | $V_{POR}$ | Power supply rise time | 1.47 | 1.51 | 1.55 | V |
| | $V_{PDR}$ | Power supply fall time | 1.46 | 1.50 | 1.54 | V |
| Minimum pulse width Note | $t_{PW}$ | | 300 | | | μs |

**Note** Minimum time required for a POR reset when $V_{DD}$ exceeds below $V_{PDR}$. This is also the minimum time required for a POR reset from when $V_{DD}$ exceeds below 0.7 V to when $V_{DD}$ exceeds $V_{POR}$ while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



### 2.7.6 LVD circuit characteristics

**($T_A$ = -40 to +85°C, $V_{PDR} \leq V_{DD} \leq 5.5$ V, $V_{SS}$ = 0 V)**

| Parameter | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Detection voltage | Supply voltage level | $V_{LVD0}$ | Power supply rise time | 3.98 | 4.06 | 4.14 | V |
| | | | Power supply fall time | 3.90 | 3.98 | 4.06 | V |
| | | $V_{LVD1}$ | Power supply rise time | 3.68 | 3.75 | 3.82 | V |
| | | | Power supply fall time | 3.60 | 3.67 | 3.74 | V |
| | | $V_{LVD2}$ | Power supply rise time | 3.07 | 3.13 | 3.19 | V |
| | | | Power supply fall time | 3.00 | 3.06 | 3.12 | V |
| | | $V_{LVD3}$ | Power supply rise time | 2.96 | 3.02 | 3.08 | V |
| | | | Power supply fall time | 2.90 | 2.96 | 3.02 | V |
| | | $V_{LVD4}$ | Power supply rise time | 2.86 | 2.92 | 2.97 | V |
| | | | Power supply fall time | 2.80 | 2.86 | 2.91 | V |
| | | $V_{LVD5}$ | Power supply rise time | 2.76 | 2.81 | 2.87 | V |
| | | | Power supply fall time | 2.70 | 2.75 | 2.81 | V |
| Minimum pulse width | | $t_{LW}$ | | 300 | | | μs |
| Detection delay time | | $t_{LD}$ | | | | 300 | μs |

**Remark** $V_{LVD\,(n-1)} > V_{LVDn}$: n = 1 to 5

**LVD Detection Voltage of Interrupt & Reset Mode**

**($T_A$ = -40 to +85°C, $V_{PDR} \leq V_{DD} \leq 5.5$ V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Interrupt and reset mode | $V_{LVD5}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 1, 1, falling reset voltage: 2.7 V | | | 2.70 | 2.75 | 2.81 | V |
| | $V_{LVD4}$ | | LVIS1, LVIS0 = 1, 0 (+0.1 V) | Rising release reset voltage | 2.86 | 2.92 | 2.97 | V |
| | | | | Falling interrupt voltage | 2.80 | 2.86 | 2.91 | V |
| | $V_{LVD3}$ | | LVIS1, LVIS0 = 0, 1 (+0.2 V) | Rising release reset voltage | 2.96 | 3.02 | 3.08 | V |
| | | | | Falling interrupt voltage | 2.90 | 2.96 | 3.02 | V |
| | $V_{LVD0}$ | | LVIS1, LVIS0 = 0, 0 (+1.2 V) | Rising release reset voltage | 3.98 | 4.06 | 4.14 | V |
| | | | | Falling interrupt voltage | 3.90 | 3.98 | 4.06 | V |

## 2.7.7 Power supply voltage rising slope characteristics

**($T_A$ = -40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power supply voltage rising slope | $S_{VDD}$ | | | | 54 | V/ms |

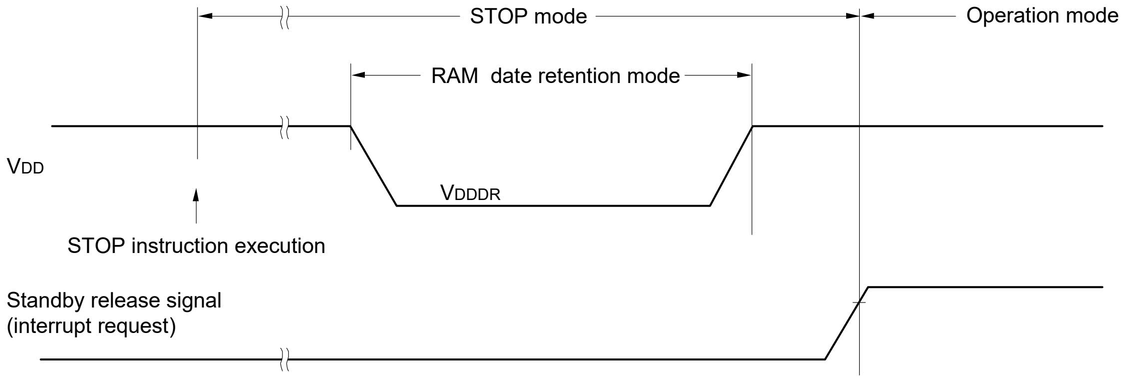
**Caution** **Make sure to keep the internal reset state by the LVD circuit or an external reset until $V_{DD}$ reaches the operating voltage range shown in 2.5 AC Characteristics.**

## 2.8 RAM Data Retention Characteristics

**($T_A$ = -40 to +85°C)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 1.46 Note | | 5.5 | V |

**Note** The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



## 2.9 Flash Memory Programming Characteristics

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| CPU/peripheral hardware clock frequency | $f_{CLK}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 1 | | 24 | MHz |
| Number of code flash rewrites Notes 1, 2, 3 | $C_{erwr}$ | Retained for 20 years | $T_A$ = 85°C Note 3 | 1,000 | | | Times |

**Note 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite.
The retaining years are until next rewrite after the rewrite.

**Note 2.** When using flash memory programmer and Renesas Electronics self programming library.

**Note 3.** These specifications show the characteristics of the flash memory and the results obtained from Renesas Electronics reliability testing.

**Remark** When updating data multiple times, use the flash memory as one for updating data.

## 2.10 Dedicated Flash Memory Programmer Communication (UART)

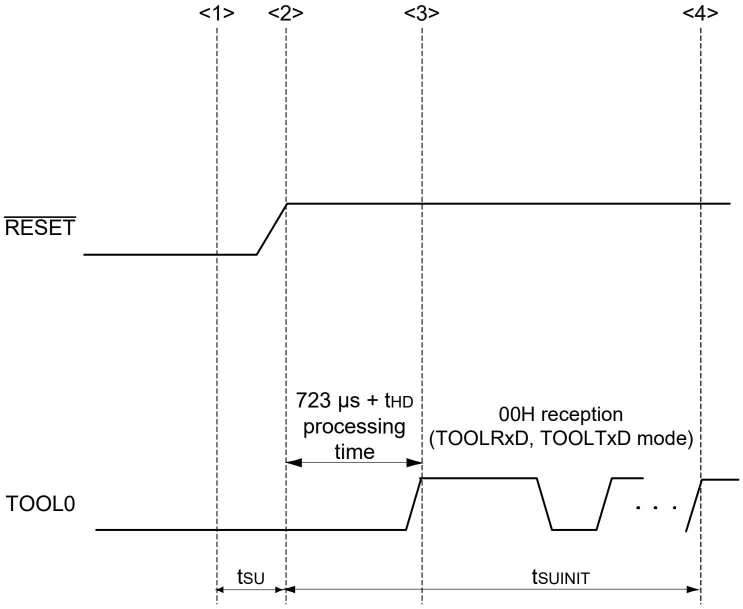
**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | During serial programming | 115.2 k | | 1 M | bps |

## 2.11 Timing for Switching Flash Memory Programming Modes

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| How long from when an external reset ends until the initial communication settings are specified | $t_{SUINIT}$ | POR and LVD reset must end before the external reset ends. | | | 100 | ms |
| How long from when the TOOL0 pin is placed at the low level until an external reset ends | $t_{SU}$ | POR and LVD reset must end before the external reset ends. | 10 | | | μs |
| How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory) | $t_{HD}$ | POR and LVD reset must end before the external reset ends. | 1 | | | ms |



<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the external reset ends.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

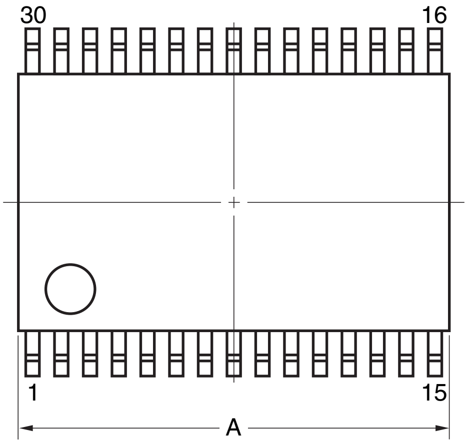
**Remark** $t_{SUINIT}$: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.
$t_{SU}$: How long from when the TOOL0 pin is placed at the low level until a pin reset ends
$t_{HD}$: How long to keep the TOOL0 pin at the low level from when the external resets end (the flash firmware processing time is excluded)

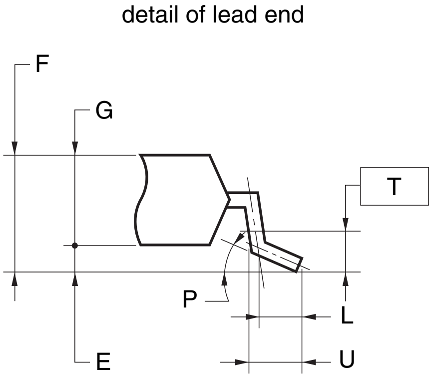
# 3. PACKAGE DRAWINGS

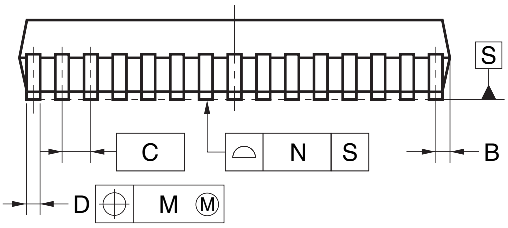
## 3.1 30-pin Products

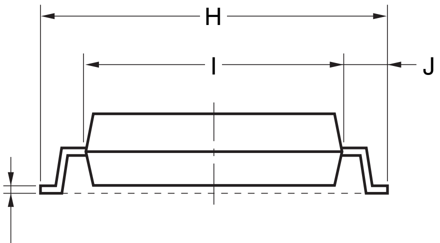
R5F11EA8ASP, R5F11EAAASP

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LSSOP30-0300-0.65 | PLSP0030JB-B | S30MC-65-5A4-3 | 0.18 |









**NOTE**

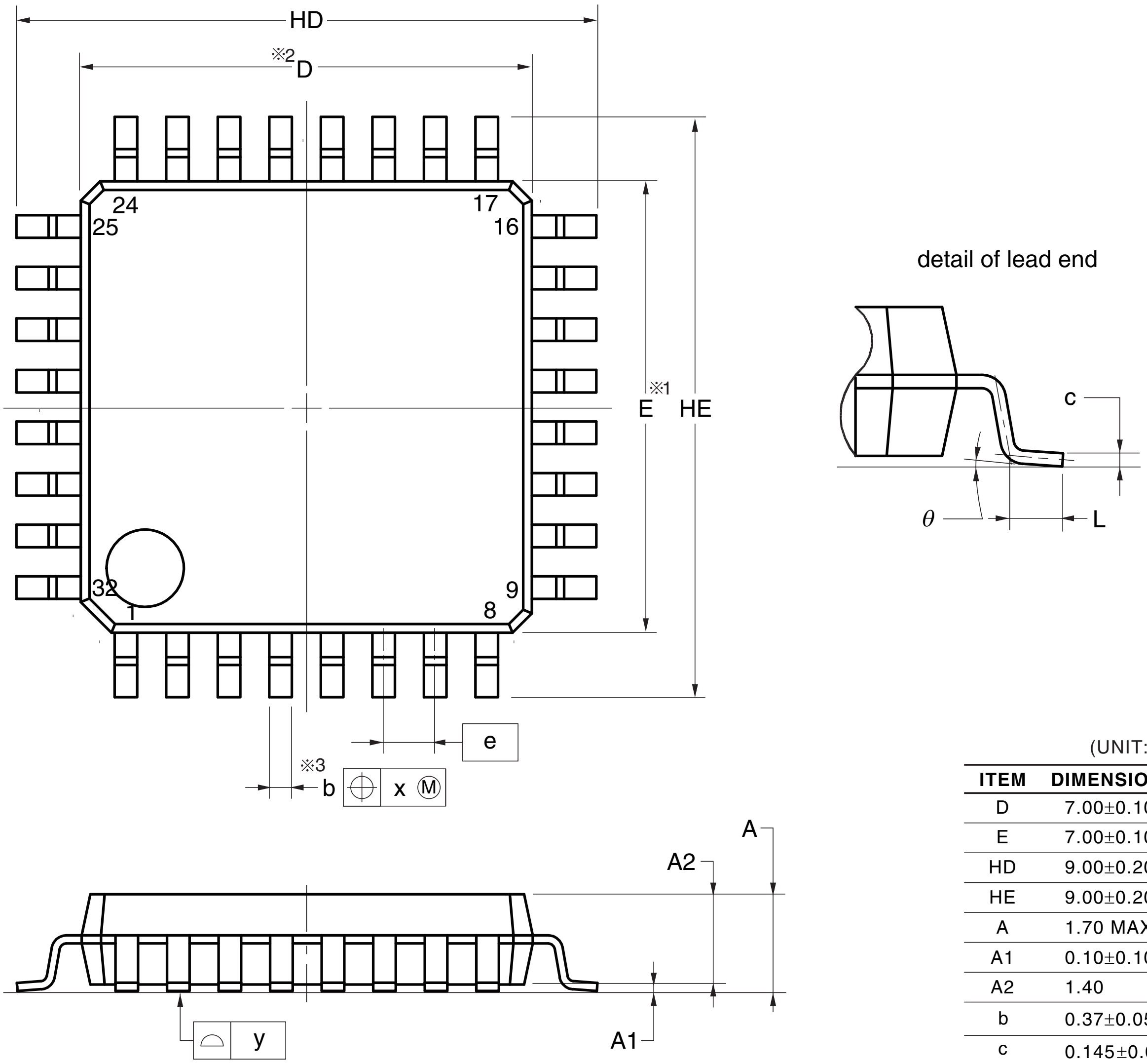
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|---|---|
| A | 9.85±0.15 |
| B | 0.45 MAX. |
| C | 0.65 (T.P.) |
| D | $0.24^{+0.08}_{-0.07}$ |
| E | 0.1±0.05 |
| F | 1.3±0.1 |
| G | 1.2 |
| H | 8.1±0.2 |
| I | 6.1±0.2 |
| J | 1.0±0.2 |
| K | 0.17±0.03 |
| L | 0.5 |
| M | 0.13 |
| N | 0.10 |
| P | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| T | 0.25 |
| U | 0.6±0.15 |

## 3.2 32-pin Products

R5F11EB8AFP, R5F11EBAAFP

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LQFP32-7x7-0.80 | PLQP0032GB-A | P32GA-80-GBT-1 | 0.2 |



(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 7.00±0.10 |
| E | 7.00±0.10 |
| HD | 9.00±0.20 |
| HE | 9.00±0.20 |
| A | 1.70 MAX. |
| A1 | 0.10±0.10 |
| A2 | 1.40 |
| b | 0.37±0.05 |
| c | 0.145±0.055 |
| L | 0.50±0.20 |
| θ | 0° to 8° |
| e | 0.80 |
| x | 0.20 |
| y | 0.10 |

**NOTE**

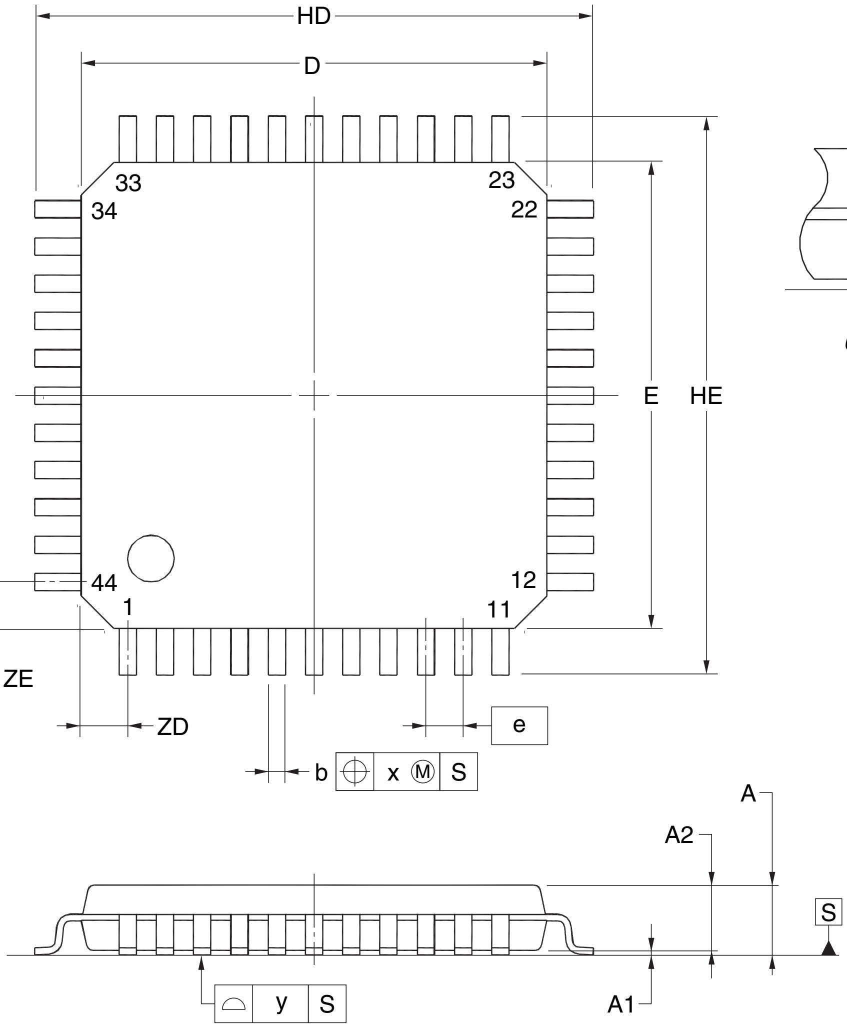
1.Dimensions “※1” and “※2” do not include mold flash.

2.Dimension “※3” does not include trim offset.

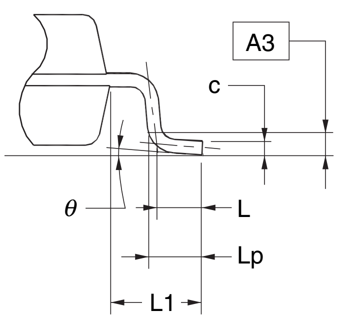
## 3.3 44-pin Products

R5F11EF8AFP, R5F11EFAAFP

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LQFP44-10x10-0.80 | PLQP0044GC-A | P44GB-80-UES-2 | 0.36 |



detail of lead end



(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 10.00±0.20 |
| E | 10.00±0.20 |
| HD | 12.00±0.20 |
| HE | 12.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | $0.37^{+0.08}_{-0.07}$ |
| c | $0.145^{+0.055}_{-0.045}$ |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| θ | $3°^{+5°}_{-3°}$ |
| e | 0.80 |
| x | 0.20 |
| y | 0.10 |
| ZD | 1.00 |
| ZE | 1.00 |

**NOTE**
Each lead centerline is located within 0.20 mm of its true position at maximum material condition.

| REVISION HISTORY | RL78/G1G Datasheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | Jul 31, 2014 | — | First Edition issued |
| 1.20 | Mar 25, 2015 | 1 | Change of description in 1.1 Features |
| | | 3 | Change of Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G1G |
| | | 3 | Change of Table 1 - 1 Orderable Part Numbers |
| | | 11 | Change of 1.6 Outline of Functions |
| 1.30 | Sep 30, 2016 | 1 | Addition of Note to 1.1 Features |
| | | 4 | Modification of Pin configuration in 1.3.1 30-pin products |
| | | 5 | Modification of Pin configuration in 1.3.2 32-pin products |
| | | 6 | Modification of Pin configuration in 1.3.3 44-pin products |
| | | 63 | Change of Note in 2.8 RAM Data Retention Characteristics |
| 1.31 | Mar 20, 2023 | All | “CSI” was modified to “simplified SPI (CSI)”. |
| | | 1 | 1.1 Features: Note 1 was added. |
| | | 3 | 1.2 List of Part Numbers: Ordering part numbers were added. |
| 1.40 | Apr 26, 2024 | 3 | Modification of Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G1G |
| | | 3 | Modification of Table 1 - 1 Orderable Part Numbers |

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# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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