ISL28233, ISL28433

Dual and Quad Micropower Chopper Stabilized, RRIO Operational Amplifiers

FN7692
Rev 3.00
July 26, 2011

The ISL28233 and ISL28433 are dual and quad micropower, chopper stabilized operational amplifiers that are optimized for single and dual supply operation from 1.8V to 6.0V and ±0.825V to ±3.0V. Their low supply current of 18µA and wide input range enable the ISL28233, ISL28433 to be excellent general purpose op amps for a wide range of applications. The ISL28233 and ISL28433 are ideal for handheld devices that operate off 2 AA or single Li-ion batteries.

The ISL28233 is available in 8 Ld MSOP, 8 Ld SOIC and 8 Ld DFN packages. The ISL28433 is available in 14 Ld TSSOP, 14 Ld SOIC and 14 Ld 3mmx4mm TDFN packages. All devices operate over the temperature range of -40°C to +125°C.

Related Literature

- See AN1596, "ISL28233SOICEVAL1Z Evaluation Board User's Guide"
- See AN1575, "ISL28433SOICEVAL1Z, ISL28433TSSOPEVAL1Z Evaluation Board User's Guide"

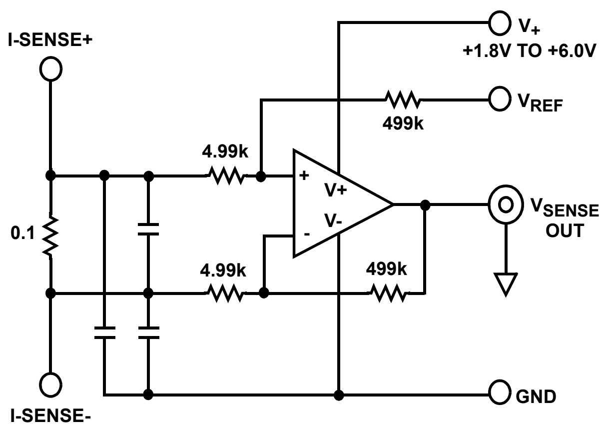
Features

- Low Input Offset Voltage . . . . 6µV, Max.
- Low Offset Drift . . . . 0.05µV/°C, Max.
- Quiescent Current (Per Amplifier) . . . . .18µA, Typ.
- Single Supply Range . . . .+1.8V to +6.0V
- Dual Supply Range . . . . ±0.825V to ±3.0V
- Low Noise (0.01Hz to 10Hz) . . . . 1.0µV_{P-P}, Typ.
- Rail-to-Rail Inputs and Output
- Input Bias Current . . . . .180pA, Max.
- Operating Temperature Range . . . .-40°C to +125°C

Applications

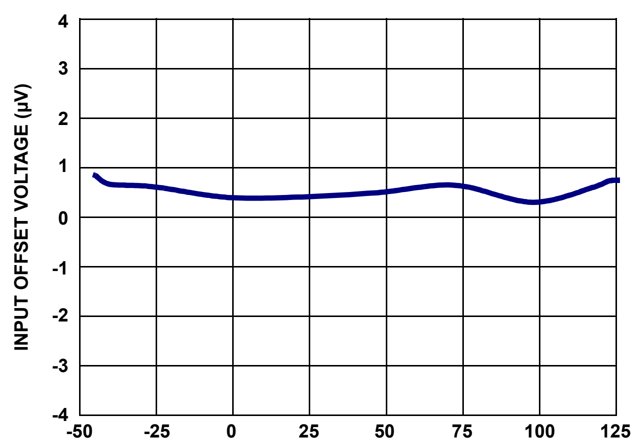
- Bi-Directional Current Sense
- Temperature Measurement
- Medical Equipment
- Electronic Weigh Scales
- Precision/Strain Gauge Sensor
- Precision Regulation
- Low Ohmic Current Sense
- High Gain Analog Front Ends

Typical Application



BI-DIRECTIONAL CURRENT SENSE AMPLIFIER

V_{OS} vs Temperature



Ordering Information

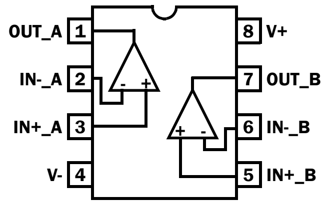
PART NUMBER (Notes 1, 2, 3)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
ISL28233FUZ	233FZ	8 Ld MSOP	M8.118A
ISL28233FRZ	233Z	8 Ld 3mmx3mm DFN	L8.3x3J
ISL28233FBZ	28233 FBZ	8 Ld SOIC	M8.15E
ISL28433FBZ	28433 FBZ	14 Ld SOIC	MDP0027
ISL28433FVZ	28433 FVZ	14 Ld TSSOP	MDP0044
Coming Soon ISL28433FRTZ	TBD	14 Ld 3x4 mm TDFN	TBD
ISL28233SOICEVAL1Z	Evaluation Board		
ISL28433TSSOPEVAL1Z	Evaluation Board		
ISL28433SOICEVAL1Z	Evaluation Board		

NOTES:

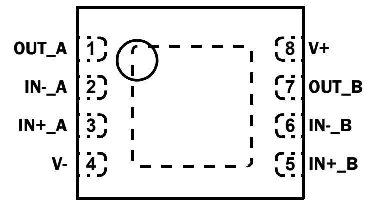
1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL28233, ISL28433. For more information on MSL please see techbrief TB363.

Pin Configurations

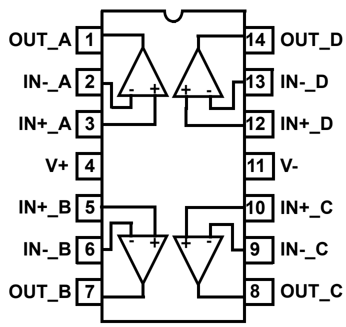
ISL28233
(8 LD MSOP, SOIC)
TOP VIEW



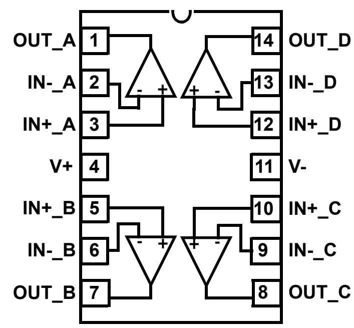
ISL28233
(8 LD DFN)
TOP VIEW



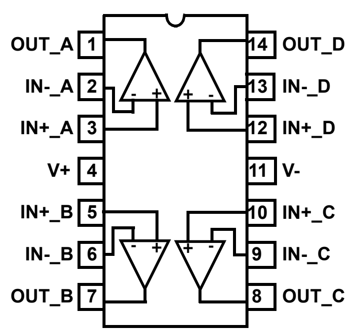
ISL28433
(14 LD SOIC)
TOP VIEW



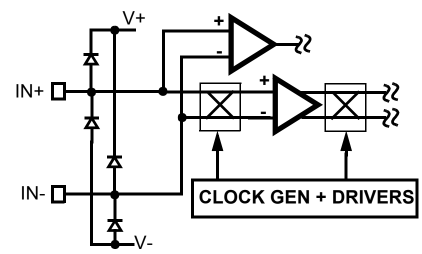
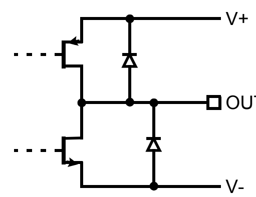
ISL28433
(14 LD TDFN)
TOP VIEW



ISL28433
(14 LD TSSOP)
TOP VIEW



Pin Descriptions

ISL28233 (8 LD MSOP, SOIC, DFN)	ISL28433 (14 LD TSSOP, SOIC, TDFN)	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
3	3	IN+_A	Non-inverting input	 Circuit 1
5	5	IN+_B		
-	10	IN+_C		
-	12	IN+_D		
4	11	V-	Negative supply	
2	2	IN-_A	Inverting input	(See Circuit 1)
6	6	IN-_B		
-	9	IN-_C		
-	13	IN-_D		
1	1	OUT_A	Output	 Circuit 2
7	7	OUT_B		
-	8	OUT_C		
-	14	OUT_D		
8	4	V+	Positive supply	
-	-	PAD	Thermal Pad	Thermal Pad. Connect to most negative supply. TDFN and DFN packages only.

Absolute Maximum Ratings

Max Supply Voltage V+ to V- 6.5V
Max Voltage VIN to GND . . . . (V- - 0.3V) to (V+ + 0.3V)V
Max Input Differential Voltage 6.5V
Max Input Current 20mA
Max Voltage VOUT to GND (10s) . . . . ±3.0V
ESD Tolerance
Human Body Model (Tested per JESD22-A114F) 4000V
Machine Model (Tested per JESD22-A115B) 400V
Charged Device Model (Tested per JESD22-C110D) 2000V
Latch-Up (Tested per JESD78B) . . . . +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
14 Ld TSSOP (Notes 4, 7)	110	40
14 Ld SOIC (Notes 4, 7)	75	47
14 Ld TDFN (Notes 5, 6)	TBD	TBD
8 Ld MSOP (Notes 4, 7)	180	65
8 Ld SOIC (Notes 4, 7)	125	90
8 Ld DFN (Notes 5, 6)	53	12

Maximum Storage Temperature Range . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
6. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
7. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

V+ = 5V, V- = 0V, V_{CM} = 2.5V, T_A = +25°C, R_L = 10kΩ, unless otherwise specified. **Boldface limits apply over the operating temperature range,-40°C to +125°C.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
DC SPECIFICATIONS						
V_{OS}	Input Offset Voltage		-6	±2	6	µV
		T = -40°C to +125°C	**-11**	-	**11**	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient	T = -40°C to +125°C	**-0.05**	0.01	**0.05**	µV/°C
I_{OS}	Input Offset Current		-	10	-	pA
TCI_{OS}	Input Offset Current Temperature Coefficient	T = -40°C to +85°C	-	0.11	-	pA/°C
I_B	Input Bias Current	T = -40°C to +85°C	-180	-	180	pA
		T = -40°C to +125°C	**-600**	-	**600**	pA
TCI_B	Input Bias Current Temperature Coefficient	T = -40°C to +85°C	-	0.49	-	pA/°C
CMIR		V+ = 5.0V, V- = 0V Guaranteed by CMRR	**-0.1**	-	**5.1**	V
CMRR	Common Mode Rejection Ratio	VCM = -0.1V to 5.1V	118	125	-	dB
			115	-	-	dB
PSRR	Power Supply Rejection Ratio	Vs = 1.8V to 6.0V	110	138	-	dB
			110	-	-	dB
V_{OH}	Output Voltage, High		**4.965**	4.981	-	V
V_{OL}	Output Voltage, Low		-	18	**35**	mV
A_{OL}	Open Loop Gain	R_L = 1MΩ	-	174	-	dB
V+	Supply Voltage	Guaranteed by PSRR	**1.8**	-	**6.0**	V
I_S	Supply Current, Per Amplifier	R_L = OPEN	-	18	25	µA
			-	-	**35**	µA

Electrical Specifications V+ = 5V, V- = 0V, V_{CM} = 2.5V, T_A = +25°C, R_L = 10kΩ, unless otherwise specified. **Boldface limits apply over the operating temperature range,-40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
I_{SC+}	Output Source Short Circuit Current	R_L = Short to V-	13	17	26	mA
I_{SC-}	Output Sink Short Circuit Current	R_L = Short to V+	-26	-19	-13	mA
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	A_V = 100, R_F = 100kΩ, R_G = 1kΩ, R_L = 10kΩ to V_{CM}	-	400	-	kHz
e_N V_{P-P}	Peak-to-Peak Input Noise Voltage	f = 0.01Hz to 10Hz	-	1.0	-	μV_{P-P}
e_N	Input Noise Voltage Density	f = 1kHz	-	65	-	nV/√(Hz)
i_N	Input Noise Current Density	f = 1kHz	-	72	-	fA/√(Hz)
		f = 10Hz	-	79	-	fA/√(Hz)
C_{in}	Differential Input Capacitance	f = 1MHz	-	1.6	-	pF
	Common Mode Input Capacitance		-	1.12	-	pF
TRANSIENT RESPONSE						
SR	Positive Slew Rate	V_{OUT} = 1V to 4V, R_L = 10kΩ	-	0.2	-	V/µs
	Negative Slew Rate		-	0.1	-	V/µs
t_r, t_f, Small Signal	Rise Time, t_r 10% to 90%	A_V = +1, V_{OUT} = 0.1V_{P-P}, R_F = 0Ω, R_L = 10kΩ, C_L = 1.2pF	-	1.1	-	µs
	Fall Time, t_f 10% to 90%		-	1.1	-	µs
t_r, t_f Large Signal	Rise Time, t_r 10% to 90%	A_V = +1, V_{OUT} = 2V_{P-P}, R_F = 0Ω, R_L = 10kΩ, C_L = 1.2pF	-	20	-	µs
	Fall Time, t_f 10% to 90%		-	30	-	µs
t_s	Settling Time to 0.1%, 2V_{P-P} Step	A_V = +1, R_F = 0Ω, R_L = 10kΩ, C_L = 1.2pF	-	35	-	µs
$t_{recover}$	Output Overload Recovery Time, Recovery to 90% of output saturation	A_V = +2, R_F = 10kΩ, R_L = Open, C_L = 3.7pF	-	10.5	-	µs

NOTE:

8. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves
$V+ = 5V$, $V- = 0V$, $V_{CM} = 2.5V$, R_L = Open, T = +25°C, unless otherwise specified.

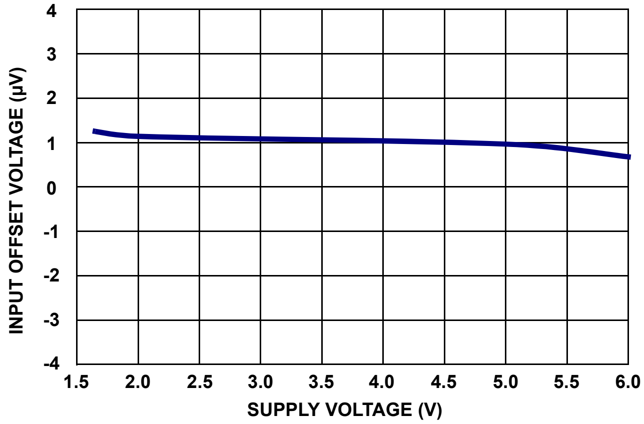


FIGURE 1. V_{OS} vs SUPPLY VOLTAGE

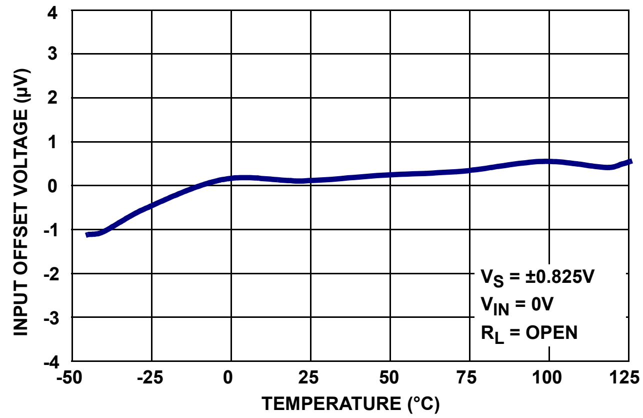


FIGURE 2. V_{OS} vs TEMPERATURE

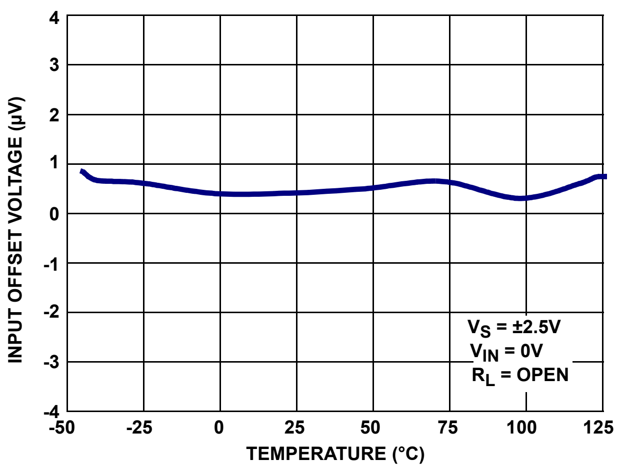


FIGURE 3. V_{OS} vs TEMPERATURE

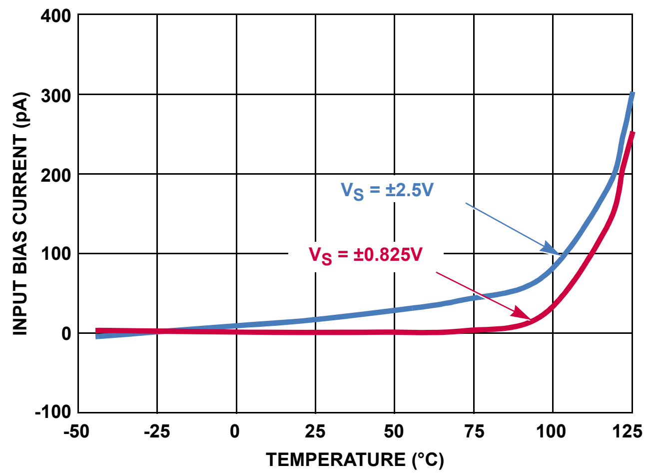


FIGURE 4. I_{B+} vs TEMPERATURE

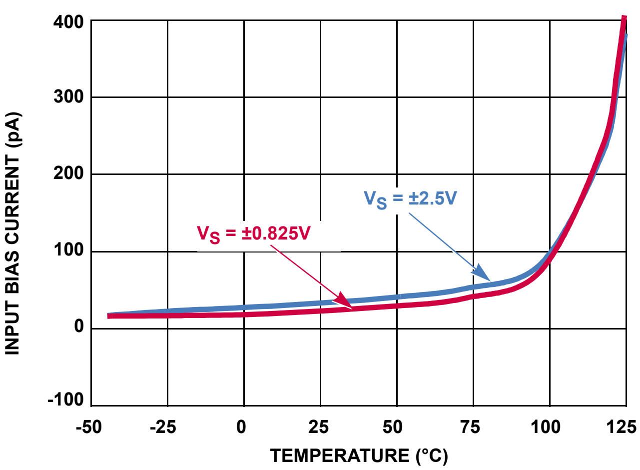


FIGURE 5. I_{B-} vs TEMPERATURE

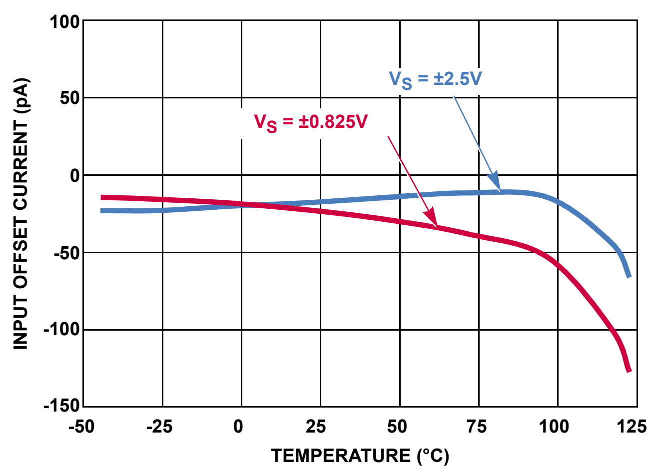


FIGURE 6. I_{OS} vs TEMPERATURE

Typical Performance Curves
$V+ = 5V$, $V- = 0V$, $V_{CM} = 2.5V$, R_L = Open, T = +25°C, unless otherwise specified. **(Continued)**

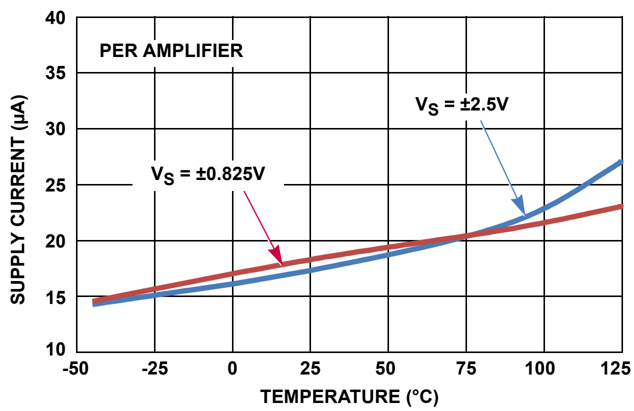


FIGURE 7. SUPPLY CURRENT vs TEMPERATURE

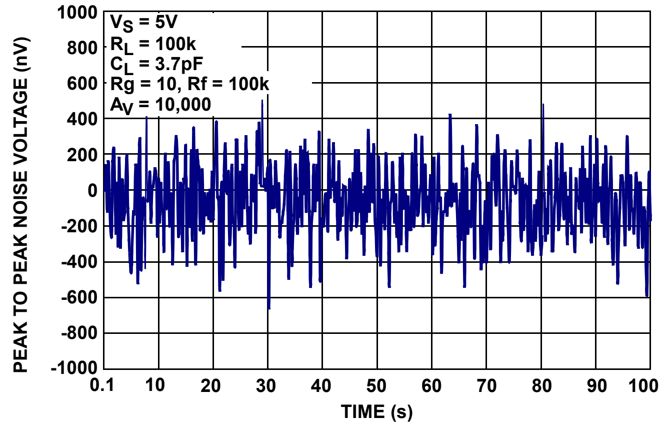


FIGURE 8. INPUT NOISE VOLTAGE 0.01Hz TO 10Hz

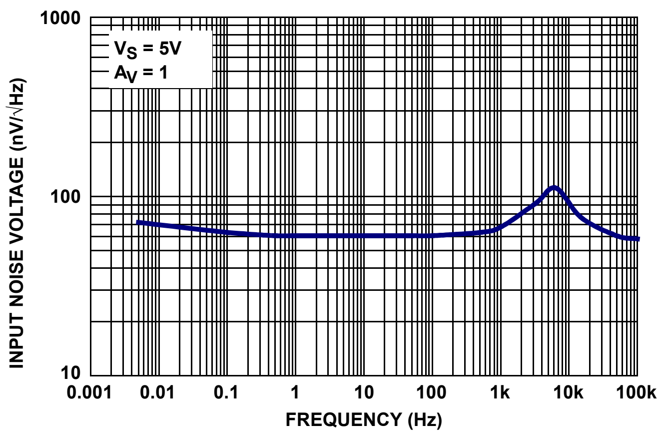


FIGURE 9. INPUT NOISE VOLTAGE DENSITY vs FREQUENCY

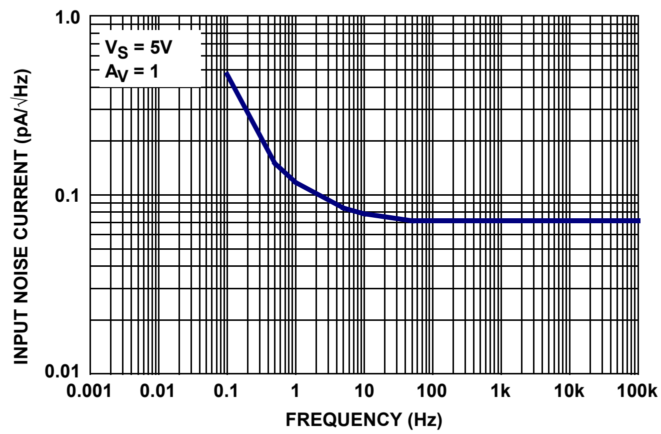


FIGURE 10. INPUT NOISE CURRENT DENSITY vs FREQUENCY

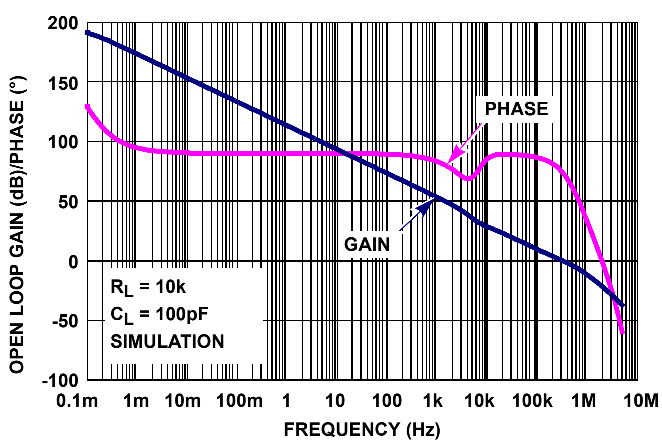


FIGURE 11. FREQUENCY RESPONSE vs OPEN LOOP GAIN, R_L = 10kΩ

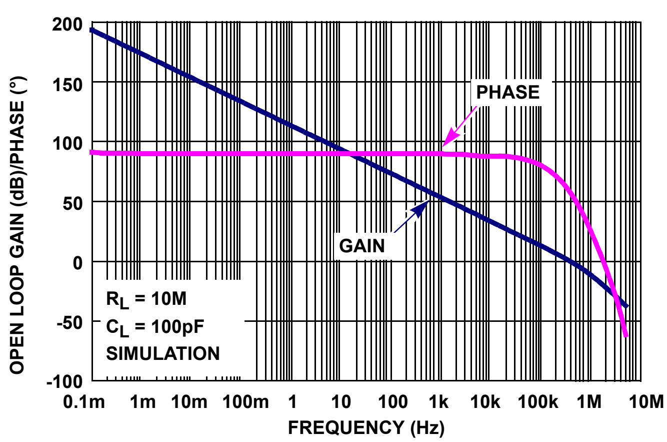


FIGURE 12. FREQUENCY RESPONSE vs OPEN LOOP GAIN, R_L = 10MΩ

Typical Performance Curves V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open, T = +25°C, unless otherwise specified. (Continued)

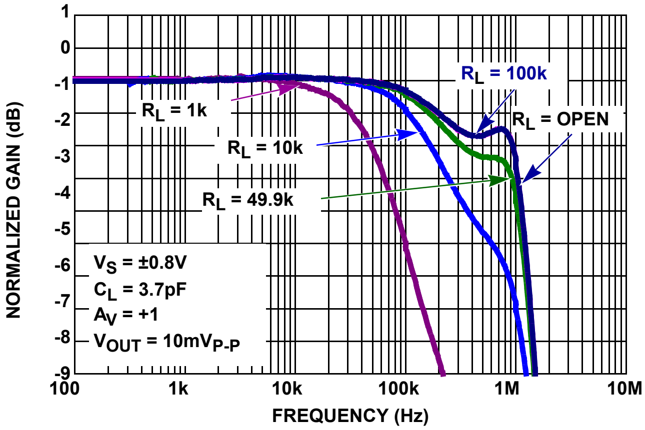


FIGURE 13. GAIN vs FREQUENCY vs R_L, V_S = ±0.8V

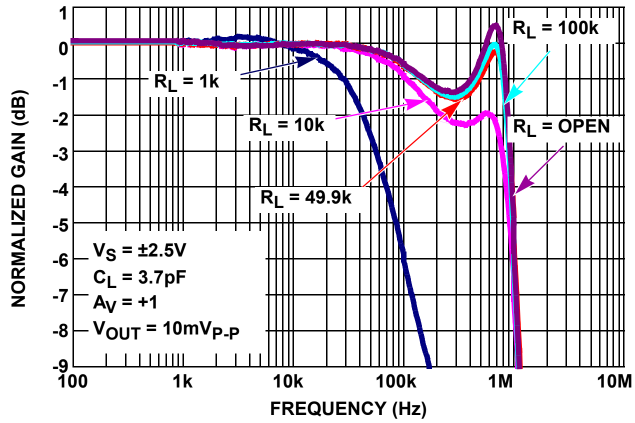


FIGURE 14. GAIN vs FREQUENCY vs R_L, V_S = ±2.5V

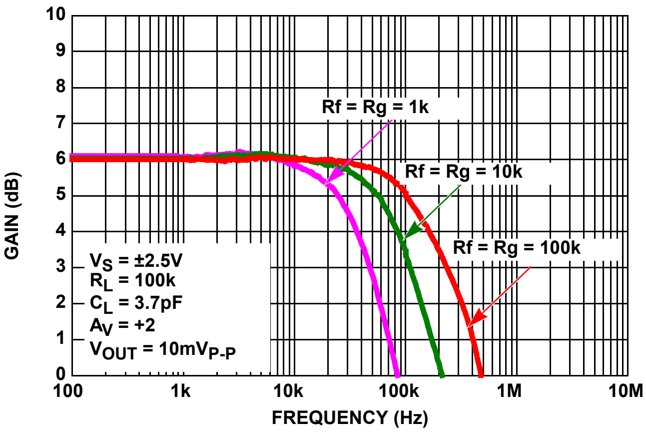


FIGURE 15. GAIN vs FREQUENCY vs FEEDBACK RESISTOR VALUES R_f/R_g

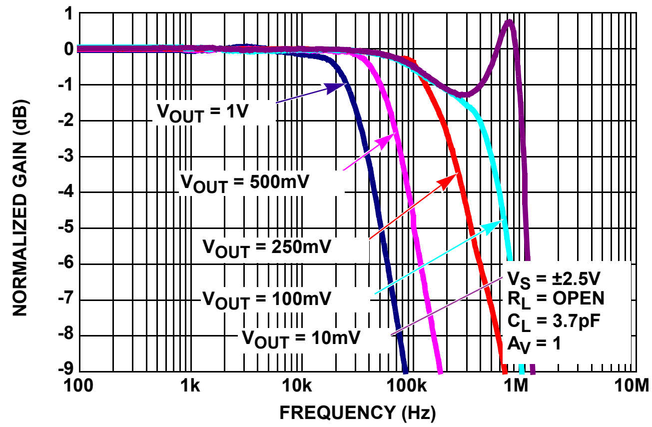


FIGURE 16. GAIN vs FREQUENCY vs V_{OUT}, R_L = OPEN

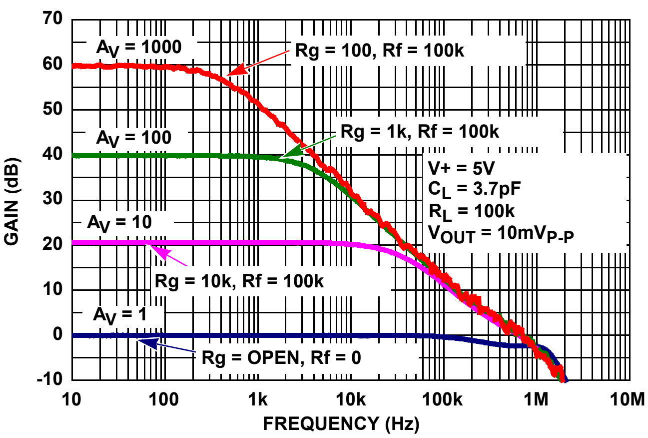


FIGURE 17. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

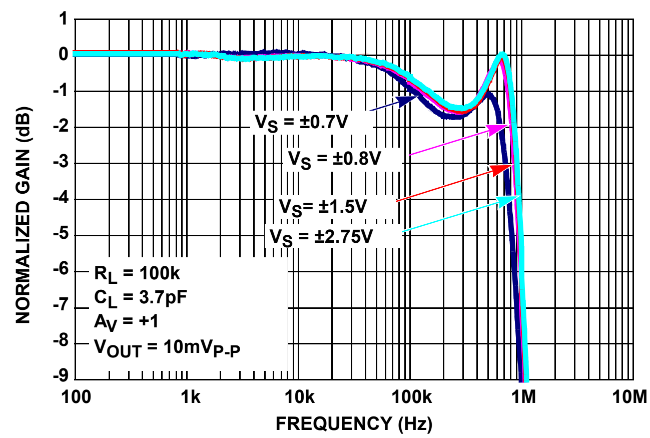


FIGURE 18. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

Typical Performance Curves V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open, T = +25°C, unless otherwise specified. (Continued)

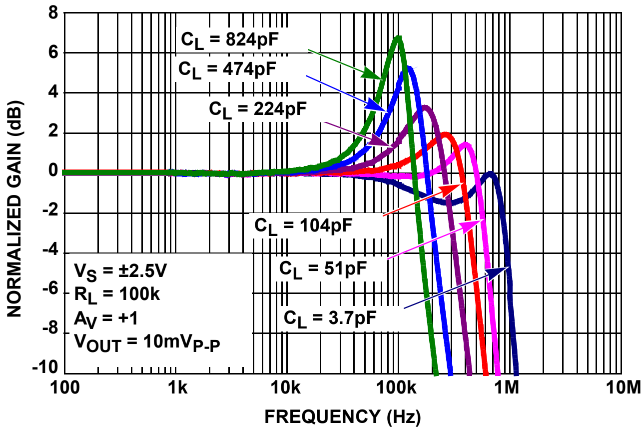


FIGURE 19. GAIN vs FREQUENCY vs C_L

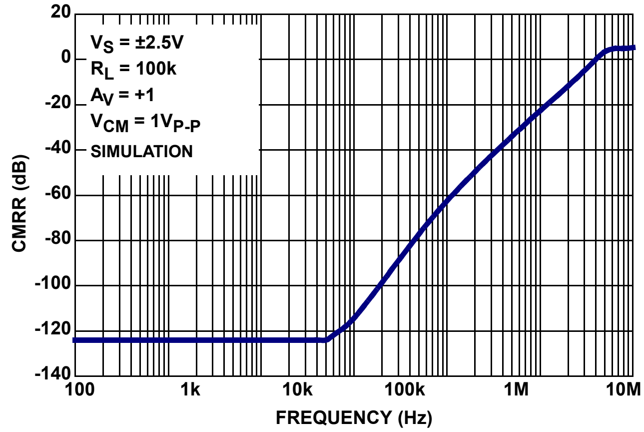


FIGURE 20. CMRR vs FREQUENCY, V_S = ±2.5V

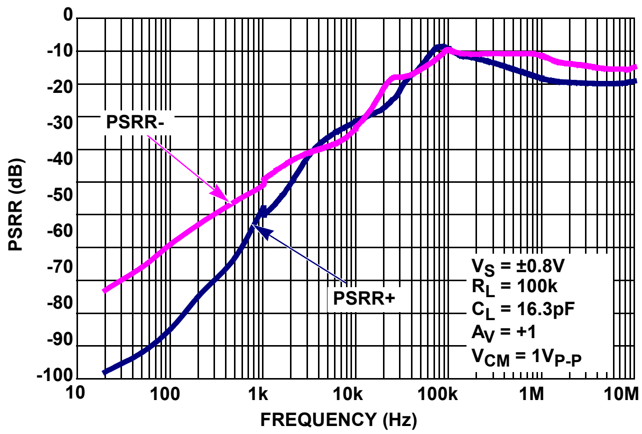


FIGURE 21. PSRR vs FREQUENCY, V_S = ±0.8V

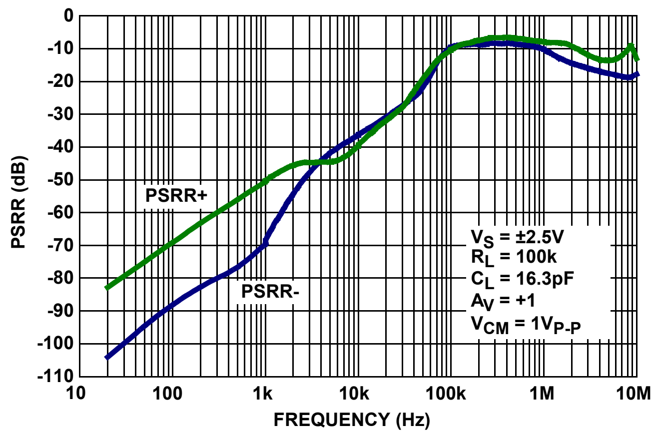


FIGURE 22. PSRR vs FREQUENCY, V_S = ±2.5V

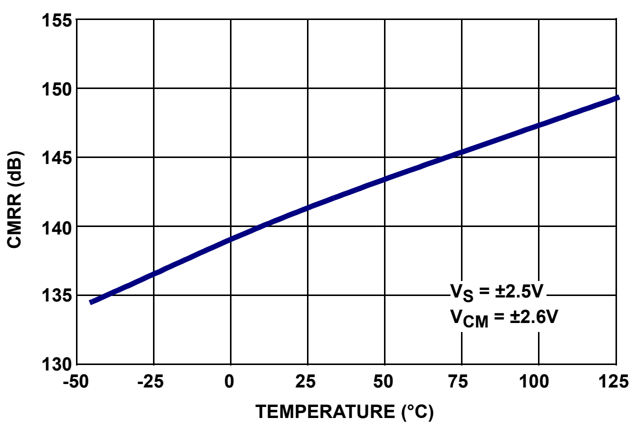


FIGURE 23. CMRR vs TEMPERATURE

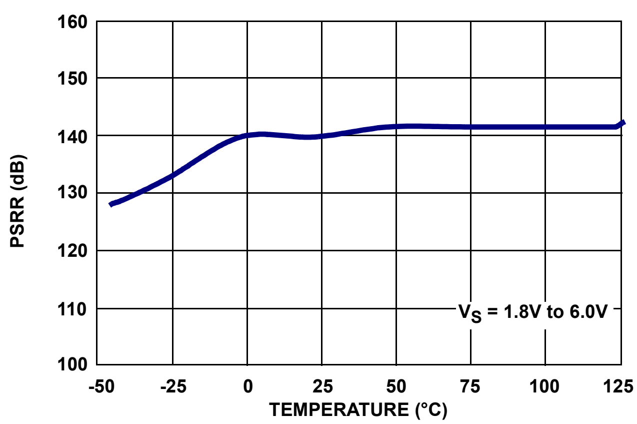


FIGURE 24. PSRR vs TEMPERATURE

Typical Performance Curves
V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open, T = +25°C, unless otherwise specified. **(Continued)**

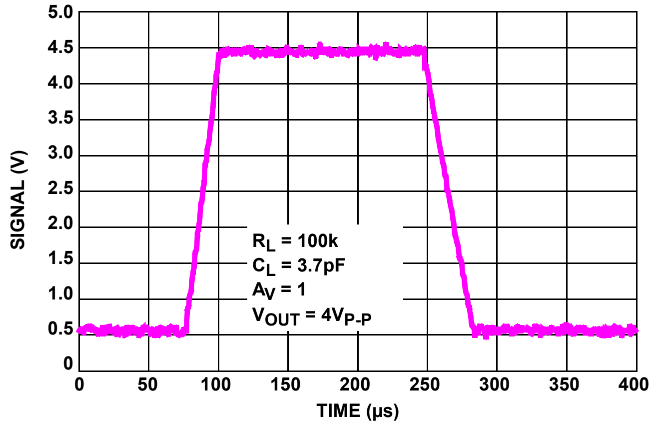


FIGURE 25. LARGE SIGNAL STEP RESPONSE (4V)

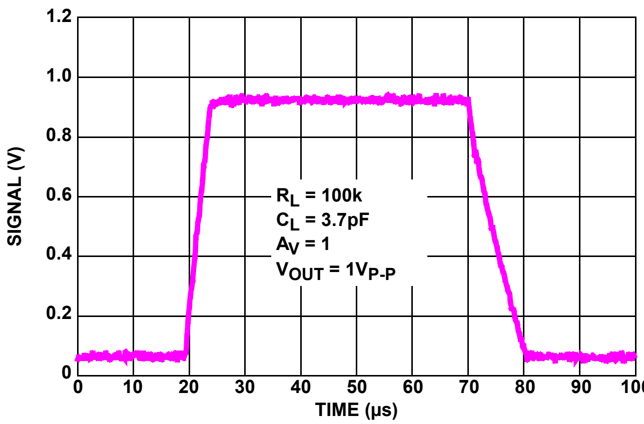


FIGURE 26. LARGE SIGNAL STEP RESPONSE (1V)

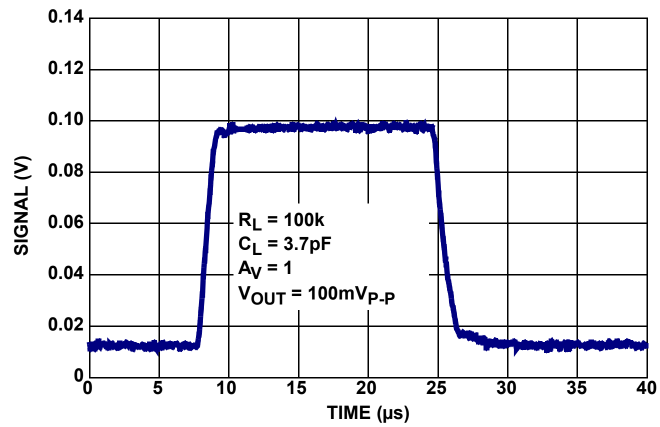


FIGURE 27. SMALL SIGNAL STEP RESPONSE (100mV)

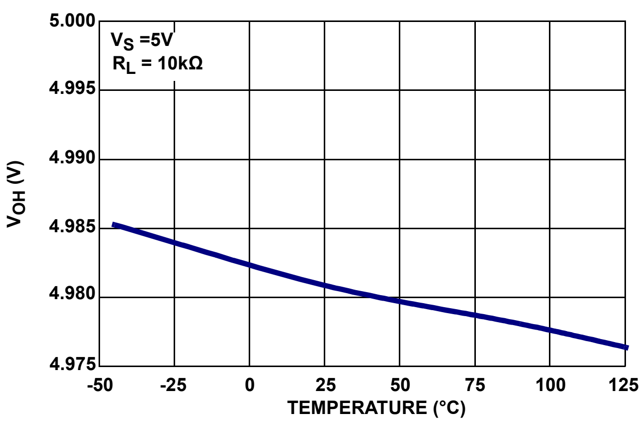


FIGURE 28. V_{OH} vs TEMPERATURE

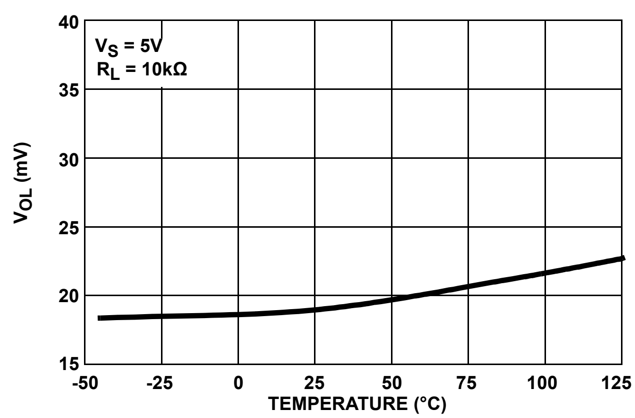


FIGURE 29. V_{OL} vs TEMPERATURE

Typical Performance Curves
$V+ = 5V$, $V- = 0V$, $V_{CM} = 2.5V$, R_L = Open, T = +25°C, unless otherwise specified. **(Continued)**

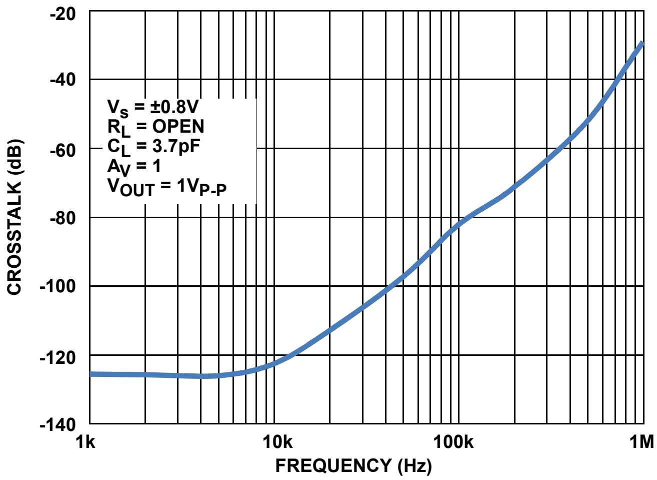


FIGURE 30. CROSSTALK vs FREQUENCY, $V_S = \pm0.8V$

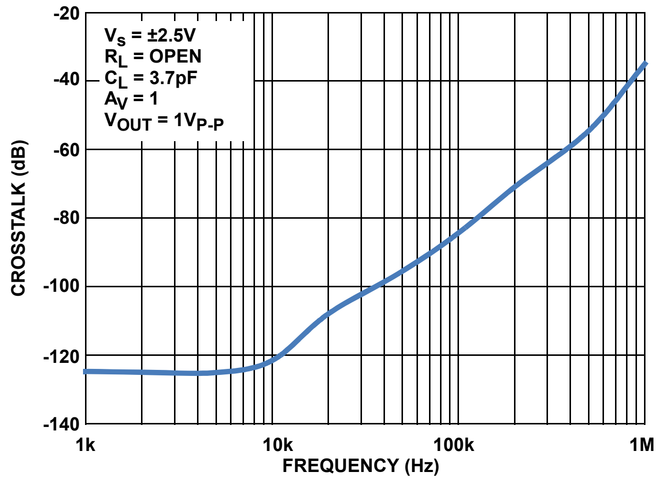


FIGURE 31. CROSSTALK vs FREQUENCY, $V_S = \pm2.5V$

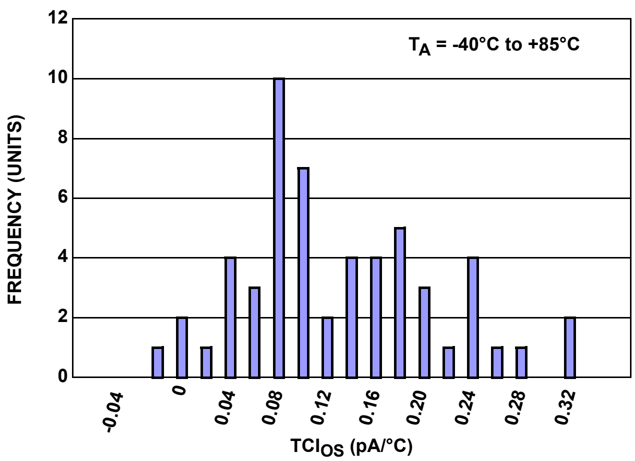


FIGURE 32. TCI_{OS} HISTOGRAM

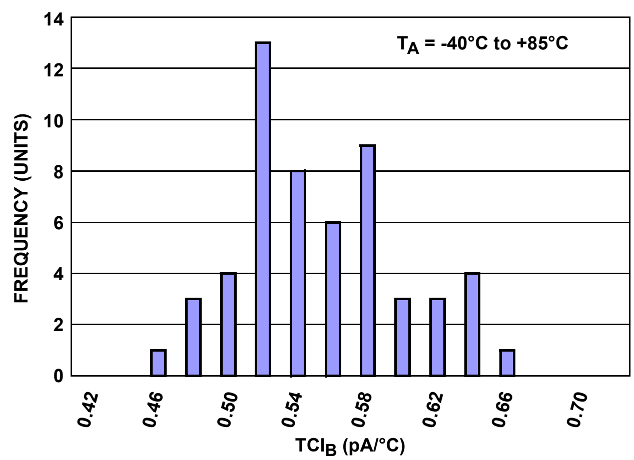


FIGURE 33. TCI_B HISTOGRAM

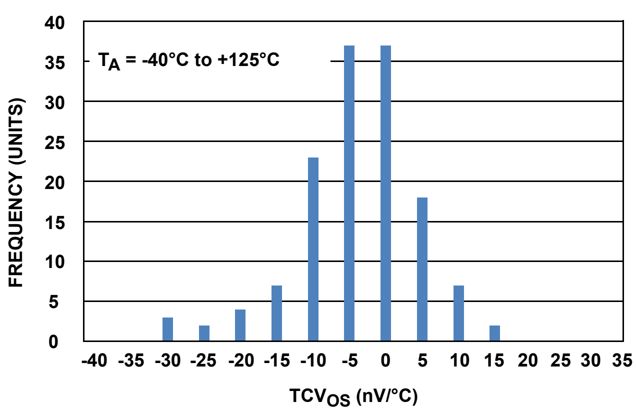


FIGURE 34. TCV_{OS} HISTOGRAM

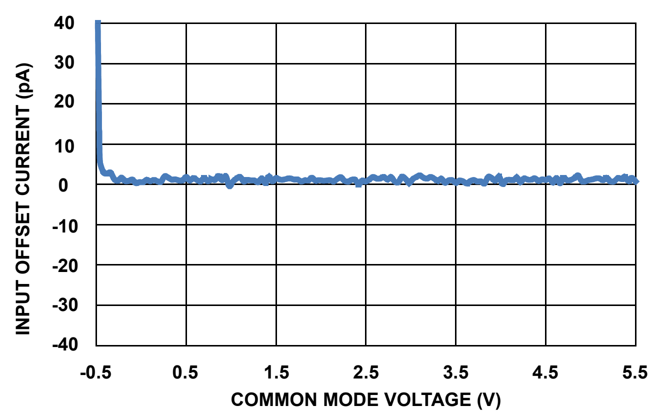


FIGURE 35. I_{OS} vs V_{CM}

Typical Performance Curves $V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open, T = +25°C$, unless otherwise specified. (Continued)

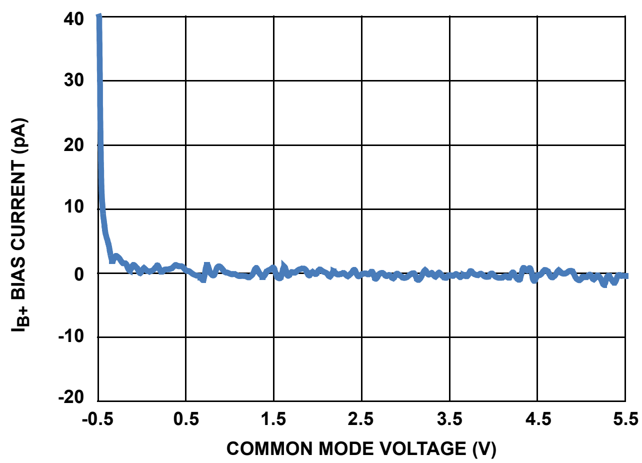


FIGURE 36. I_{B+} vs V_{CM}

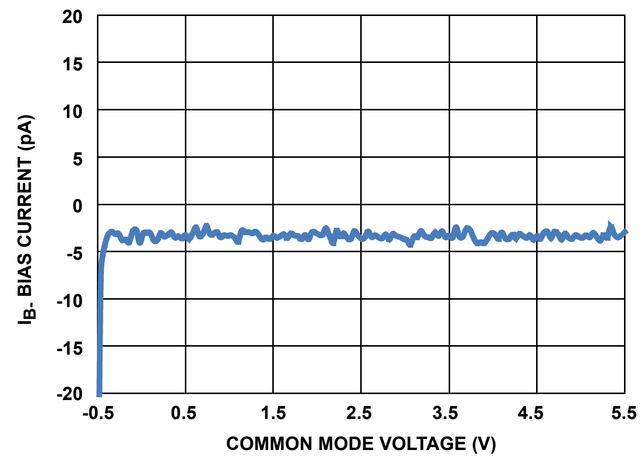


FIGURE 37. I_{B-} vs V_{CM}

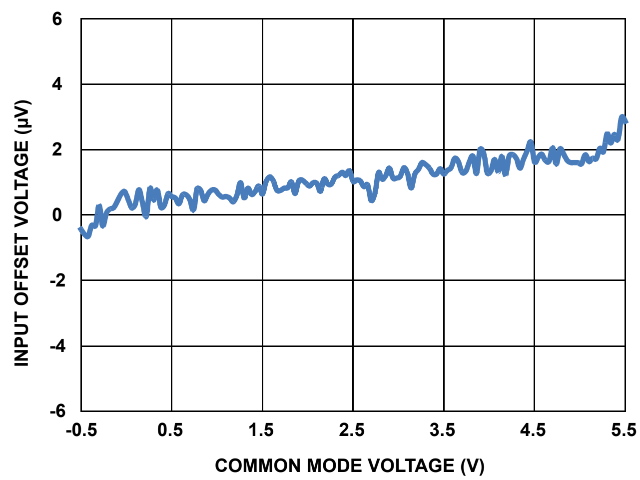


FIGURE 38. V_{OS} vs V_{CM}

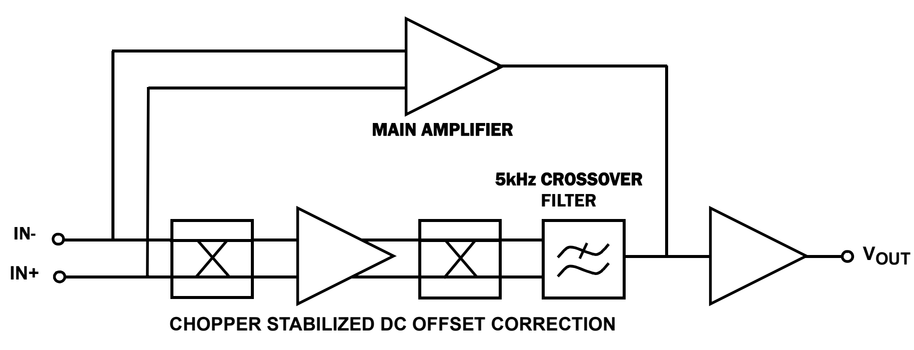


FIGURE 39. ISL28233, ISL28433 FUNCTIONAL BLOCK DIAGRAM

Applications Information

Functional Description

The ISL28233 and ISL28433 use a proprietary chopper-stabilized technique (see Figure 39) that combines a 400kHz main amplifier with a very high open loop gain (174dB) chopper amplifier to achieve very low offset voltage and drift (2µV, 0.01µV/°C typical) while consuming only 18µA of supply current per channel.

This multi-path amplifier architecture contains a time continuous main amplifier whose input DC offset is corrected by a parallel-connected, high gain chopper stabilized DC correction amplifier operating at 100kHz. From DC to ~5kHz, both amplifiers are active with DC offset correction and most of the low frequency gain is provided by the chopper amplifier. A 5kHz crossover filter cuts off the low frequency amplifier path leaving the main amplifier active out to the 400kHz gain-bandwidth product of the device.

The key benefits of this architecture for precision applications are very high open loop gain, very low DC offset, and low 1/f noise. The noise is virtually flat across the frequency range from a few millihertz out to 100kHz, except for the narrow noise peak at the amplifier crossover frequency (5kHz).

Rail-to-rail Input and Output (RRIO)

The RRIO CMOS amplifier uses parallel input PMOS and NMOS that enable the inputs to swing 100mV beyond either supply rail. The inverting and non-inverting inputs do not have back-to-back input clamp diodes and are capable of maintaining high input impedance at high differential input voltages. This is effective in eliminating output distortion caused by high slew-rate input signals.

The output stage uses common source connected PMOS and NMOS devices to achieve rail-to-rail output drive capability with 17mA current limit and the capability to swing to within 20mV of either rail while driving a 10kΩ load.

IN+ and IN- Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. For applications where either input is expected to exceed the rails by 0.5V, an external series resistor must be used to ensure the input currents never exceed 20mA (see Figure 40).

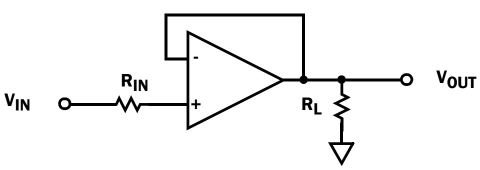


FIGURE 40. INPUT CURRENT LIMITING

Layout Guidelines for High Impedance Inputs

To achieve the maximum performance of the high input impedance and low offset voltage of the ISL28233 and ISL28433 amplifiers, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board.

High Gain, Precision DC-Coupled Amplifier

The circuit in Figure 41 implements a single-stage DC-coupled amplifier with an input DC sensitivity of under 100nV that is only possible using a low VOS amplifier with high open loop gain. High gain DC amplifiers operating from low voltage supplies are not practical using typical low offset precision op amps. For example, a typical precision amplifier in a gain of 10kV/V with a ±100µV V_{OS} and offset drift 0.5µV/°C of a low offset op amp would produce a DC error of >1V with an additional 5mV/°C of temperature dependent error making it difficult to resolve DC input voltage changes in the mV range.

The ±6µV max V_{OS} and 0.05µV/°C max temperature drift of the ISL28233, ISL28433 produces a temperature stable maximum DC output error of only ±60mV with a maximum output temperature drift of 0.5mV/°C. The additional benefit of a very low 1/f noise corner frequency and some feedback filtering enables DC voltages and voltage fluctuations well below 100nV to be easily detected with a simple single stage amplifier.

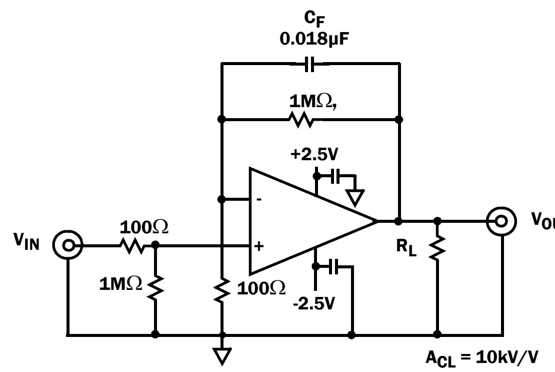


FIGURE 41. HIGH GAIN, PRECISION DC-COUPLED AMPLIFIER

ISL28233, ISL28433 SPICE Model

Figure 42 shows the SPICE model schematic and Figure 43 shows the net list for the ISL28233, ISL28433 SPICE model. The model is a simplified version of the actual device and simulates important parameters such as noise, Slew Rate, Gain and Phase. The model uses typical parameters from the “Electrical Specifications Table” on page 5. The poles and zeroes in the model were determined from the actual open and closed-loop gain and phase response. This enables the model to present an accurate AC representation of the actual device. The model is configured for ambient temperature of +25°C.

Figures 44 through 51 show the characterization vs simulation results for the Noise Density, Frequency Response vs Close Loop Gain, Gain vs Frequency vs C_L and Large Signal Step Response (4V).

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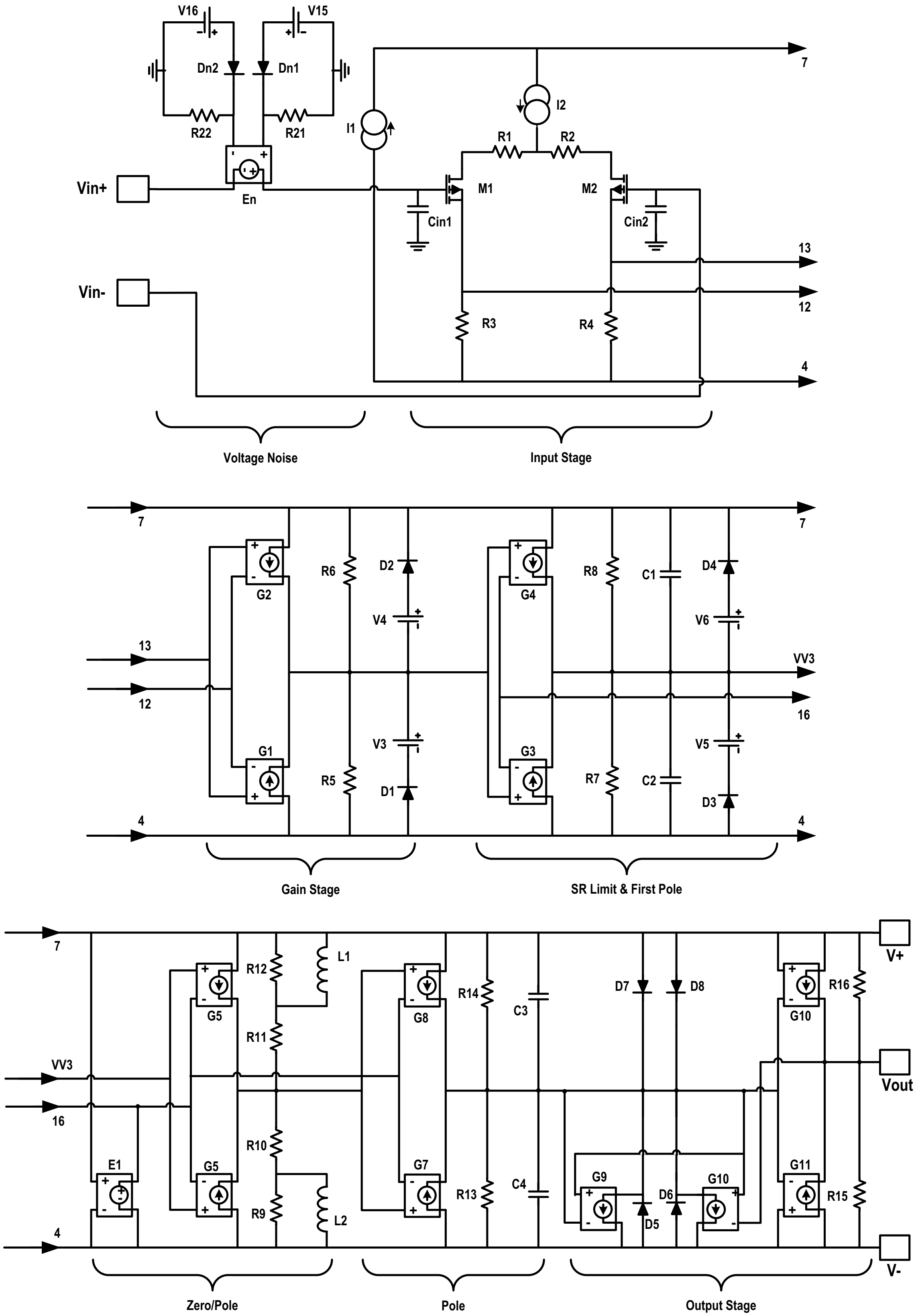

FIGURE 42. SPICE CIRCUIT SCHEMATIC

```
* ISL28233, ISL28433 Macromodel
* Revision B, April 2009
* AC characteristics, Voltage Noise
*Copyright 2009 by Intersil Corporation
*Refer to data sheet "LICENSE STATEMENT" Use of
*this model indicates your acceptance with the
*terms and provisions in the License Statement.
* Connections:          +input
*                         |      -input
*                         |        |      +Vsupply
*                         |        |        |      -Vsupply
*                         |        |        |        |      output
*                         |        |        |        |        |
.subckt ISL28233          3        2        7        4        6
*
*Voltage Noise
D_DN1       102 101 DN
D_DN2       104 103 DN
R_R21       0 101  120k
R_R22       0 103  120k
E_EN        8 3 101 103 1
V_V15       102 0 0.1Vdc
V_V16       104 0 0.1Vdc
*
*Input Stage
C_Cin1      8 0  0.4p
C_Cin2      2 0  2.0p
R_R1        9  10  10
R_R2        10 11  10
R_R3        4  12  100
R_R4        4  13  100
M_M1        12 8 9 9   pmosisil
+ L=50u
+ W=50u
M_M2        13 2 11 11 pmosisil
+ L=50u
+ W=50u
I_I1        4 7 DC 92uA
I_I2        7 10 DC 100uA
*
*Gain stage
G_G1        4 VV2 13 12 0.0002
G_G2        7 VV2 13 12 0.0002
R_R5        4 VV2  1.3Meg
R_R6        VV2 7  1.3Meg
D_D1        4 14 DX
D_D2        15 7 DX
V_V3        VV2 14 0.7Vdc
V_V4        15 VV2 0.7Vdc
*
*SR limit first pole
G_G3        4  VV3 VV2 16 1
G_G4        7  VV3 VV2 16 1
R_R7        4 VV3  1meg
R_R8        VV3 7  1meg
C_C1        VV3 7  12u
C_C2        4 VV3  12u
D_D3        4 17 DX
D_D4        18 7 DX
V_V5        VV3 17 0.7Vdc
V_V6        18 VV3 0.7Vdc
*
*Zero/Pole
E_E1        16 4 7 4 0.5
G_G5        4  VV4 VV3 16 0.000001
G_G6        7  VV4 VV3 16 0.000001
L_L1        20 7   0.3H
R_R12       20 7  2.5meg
R_R11       VV4 20  1meg
L_L2        4  19  0.3H
R_R9        4  19  2.5meg
R_R10       19 VV4  1meg
*Pole
G_G7        4 VV5 VV4 16 0.000001
G_G8        7 VV5 VV4 16 0.000001
C_C3        VV5 7  0.12p
C_C4        4 VV5  0.12p
R_R13       4 VV5  1meg
R_R14       VV5 7  1meg
*
*Output Stage
G_G9        21 4 6 VV5 0.0000125
G_G10       22 4 VV5 6 0.0000125
D_D5        4 21 DY
D_D6        4 22 DY
D_D7        7  21 DX
D_D8        7  22 DX
R_R15       4 6  8k
R_R16       6 7  8k
G_G11       6 4 VV5 4 -0.000125
G_G12       7 6 7 VV5 -0.000125
*
.model pmosisil pmos (kp=16e-3 vto=10m)
.model DN D(KF=6.4E-16 AF=1)
.MODEL DX D(IS=1E-18 Rs=1)
.MODEL DY D(IS=1E-15 BV=50 Rs=1)
.ends ISL28233
```

FIGURE 43. SPICE NET LIST

Characterization vs Simulation Results

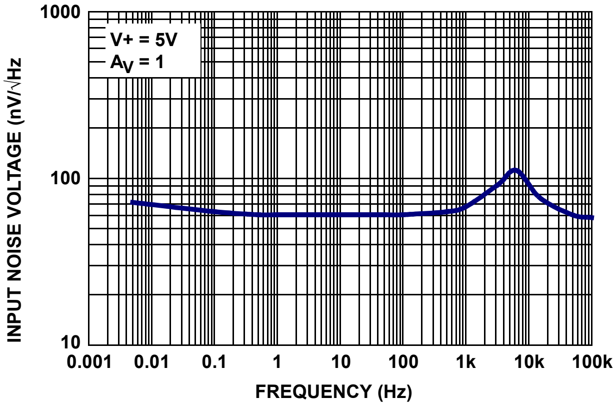

FIGURE 44. CHARACTERIZED INPUT NOISE VOLTAGE DENSITY vs FREQUENCY

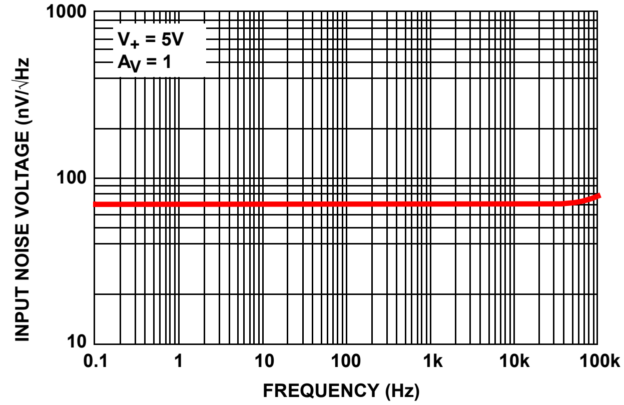

FIGURE 45. SIMULATED INPUT NOISE VOLTAGE DENSITY vs FREQUENCY

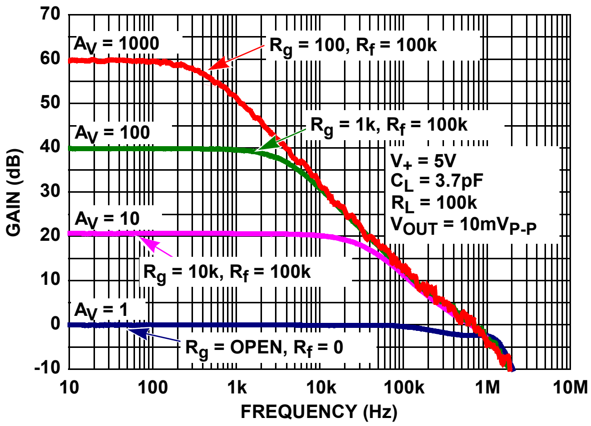

FIGURE 46. CHARACTERIZED FREQUENCY RESPONSE vs CLOSED LOOP GAIN

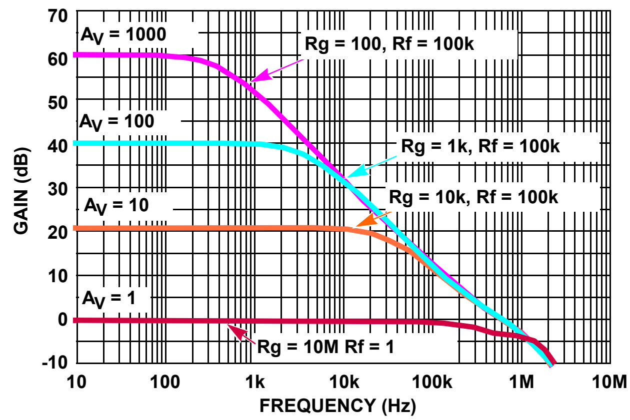

FIGURE 47. SIMULATED FREQUENCY RESPONSE vs CLOSED LOOP GAIN

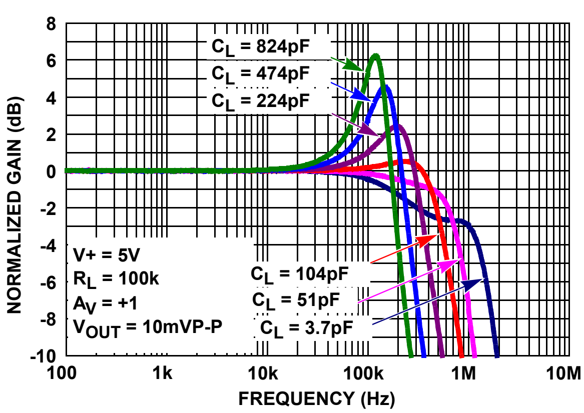

FIGURE 48. CHARACTERIZED GAIN vs FREQUENCY vs C_L

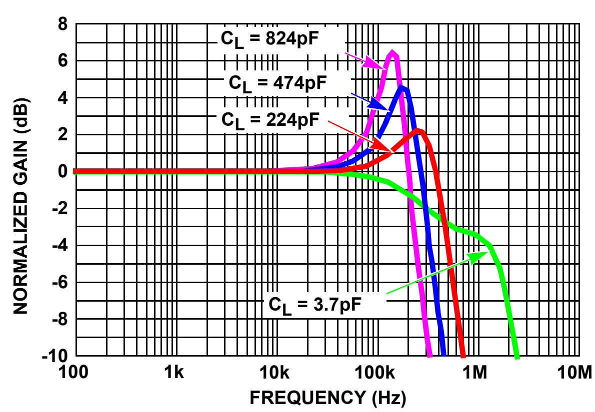

FIGURE 49. SIMULATED GAIN vs FREQUENCY vs C_L

Characterization vs Simulation Results (Continued)

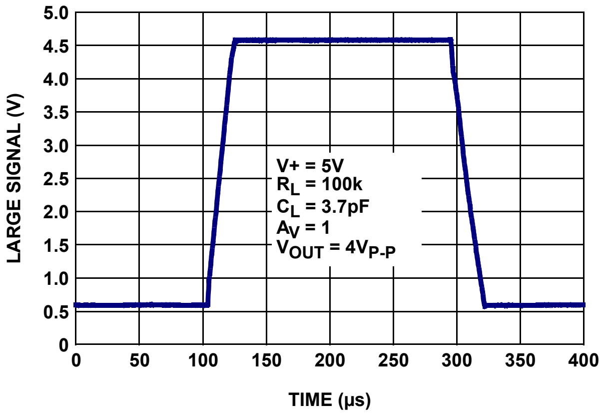

FIGURE 50. CHARACTERIZED LARGE SIGNAL STEP RESPONSE (4V)

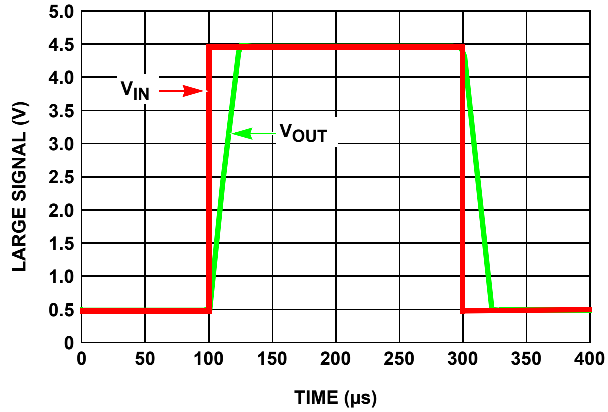

FIGURE 51. SIMULATED LARGE SIGNAL STEP RESPONSE (4V)

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
5/31/11	FN7692.3	Changed minimum operating supply voltage from +1.65V to +1.8V throughout entire datasheet.
3/24/11		Added to Ordering Information Table on page 2 - ISL28233SOICEVAL1Z, ISL28433TSSOPEVAL1Z, ISL28433SOICEVAL1Z
12/2/10	FN7692.2	Added "Related Literature" on page 1 Removed "Coming Soon" from ISL28233FRZ device (8 Ld DFN) in "Ordering Information" on page 2. Corrected Thermal Pad Pin Name in "Pin Descriptions" on page 4 from "NC" to "PAD" Corrected θ_{JA} note for TDFN package in "Thermal Information" on page 5 from "θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details." To "θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379." (since TDFN has thermal pad; TDFN package option not released yet)
10/27/10	FN7692.1	Changed Part Marking for ISL28233FUZ from 8233Z to 233FZ in "Ordering Information" table on page 2 Added ISL28233 in DFN package to Ordering Information" table on page 2. On page 6, removed Note 8. Changed note in MIN MAX columns of "Electrical Specifications" table from: "Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested." To: "Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design."
8/25/10	FN7692.0	Initial Release.

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*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL28233, ISL28433

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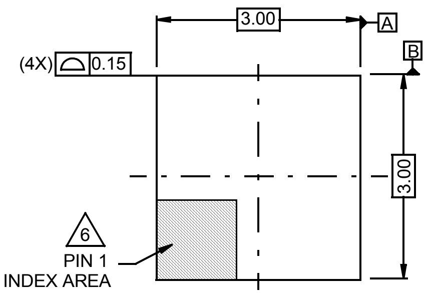
FITs are available from our website at http://rel.intersil.com/reports/search.php

Package Outline Drawing

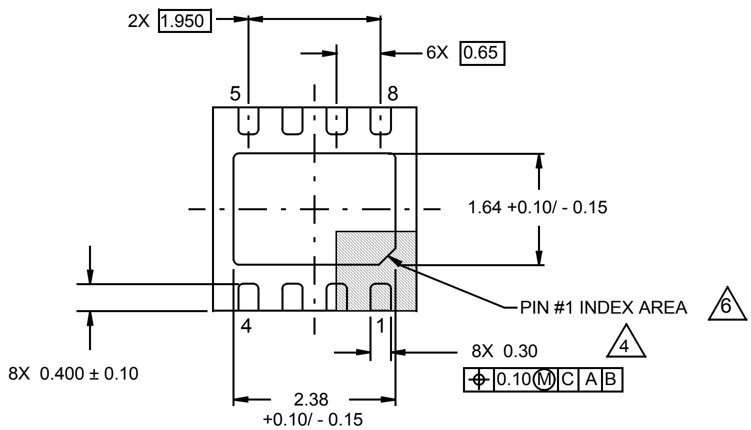
L8.3x3J

8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

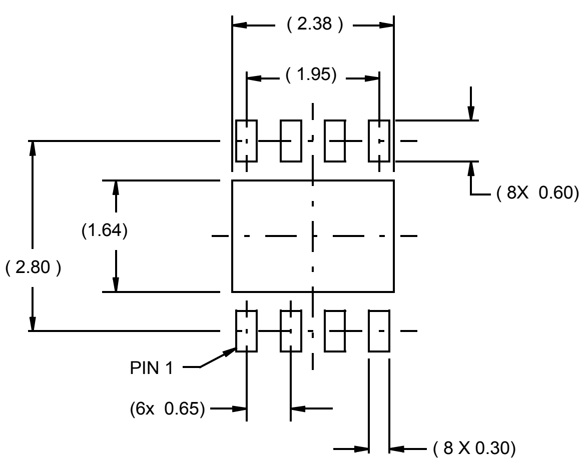
Rev 0 9/09



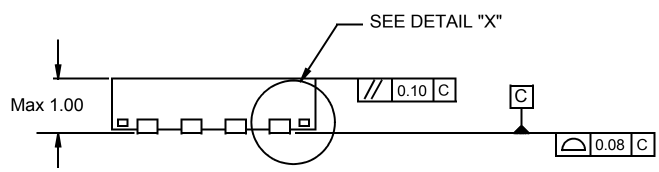
TOP VIEW



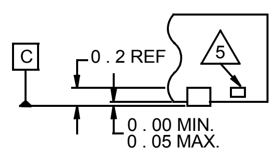
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

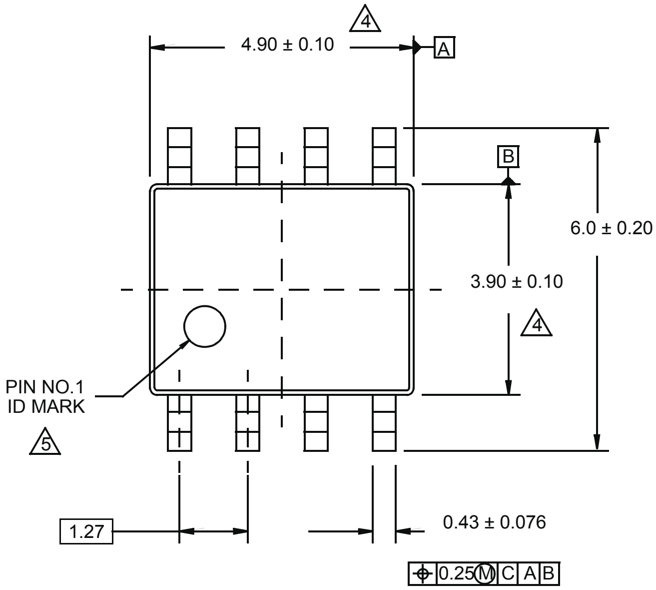
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

Package Outline Drawing

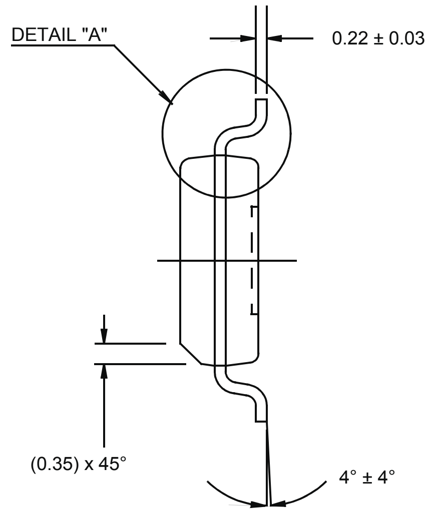
M8.15E

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

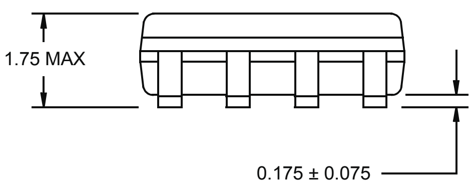
Rev 0, 08/09



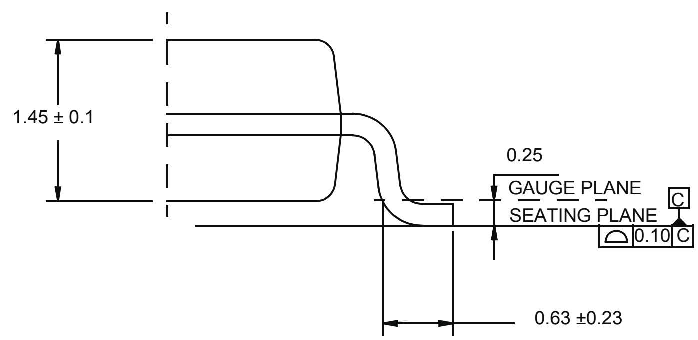
TOP VIEW



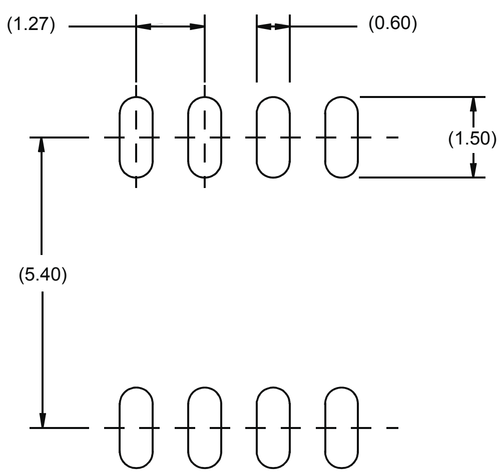
SIDE VIEW “B”



SIDE VIEW “A



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

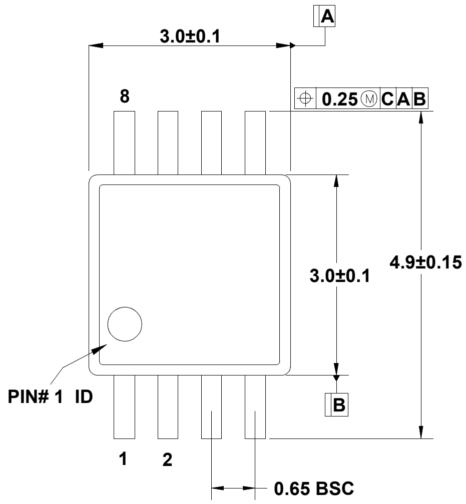
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

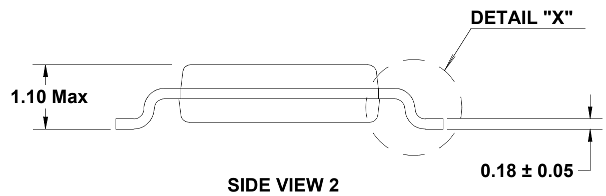
Package Outline Drawing

M8.118A

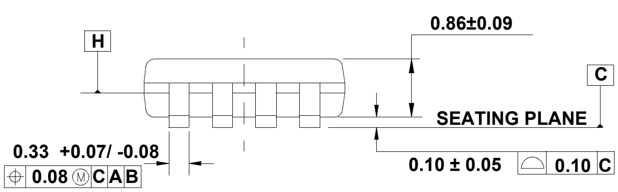
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE (MSOP)
Rev 0, 9/09



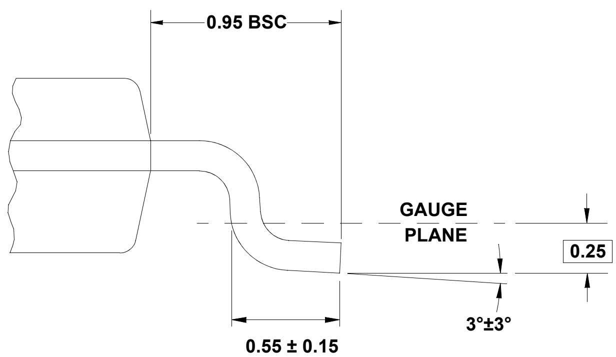
TOP VIEW



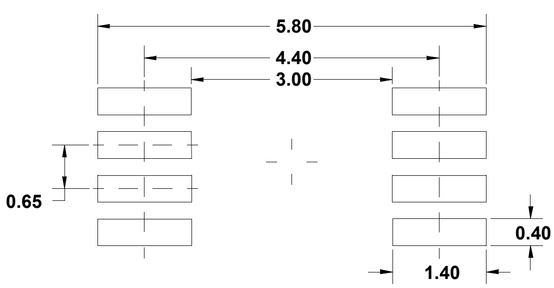
SIDE VIEW 2



SIDE VIEW 1



DETAIL "X"

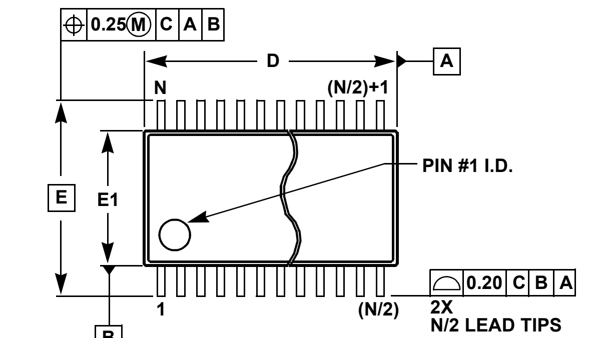


TYPICAL RECOMMENDED LAND PATTERN

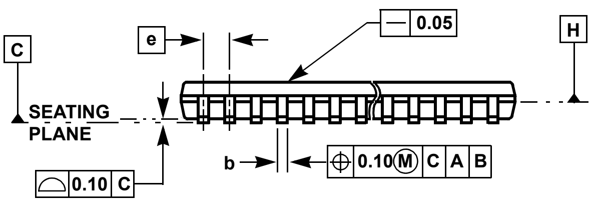
NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSE Y14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.25mm max per side are not included.
5. Dimensions “D” and “E1” are measured at Datum Plane “H”.
6. This replaces existing drawing # MDP0043 MSOP 8L.

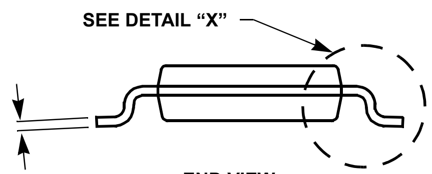
Thin Shrink Small Outline Package Family (TSSOP)



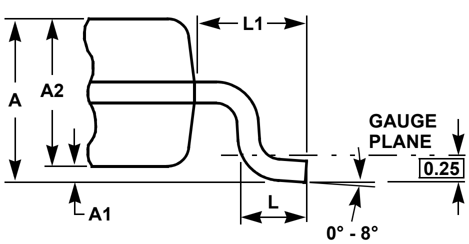
TOP VIEW



SIDE VIEW



END VIEW



DETAIL X

MDP0044

THIN SHRINK SMALL OUTLINE PACKAGE FAMILY

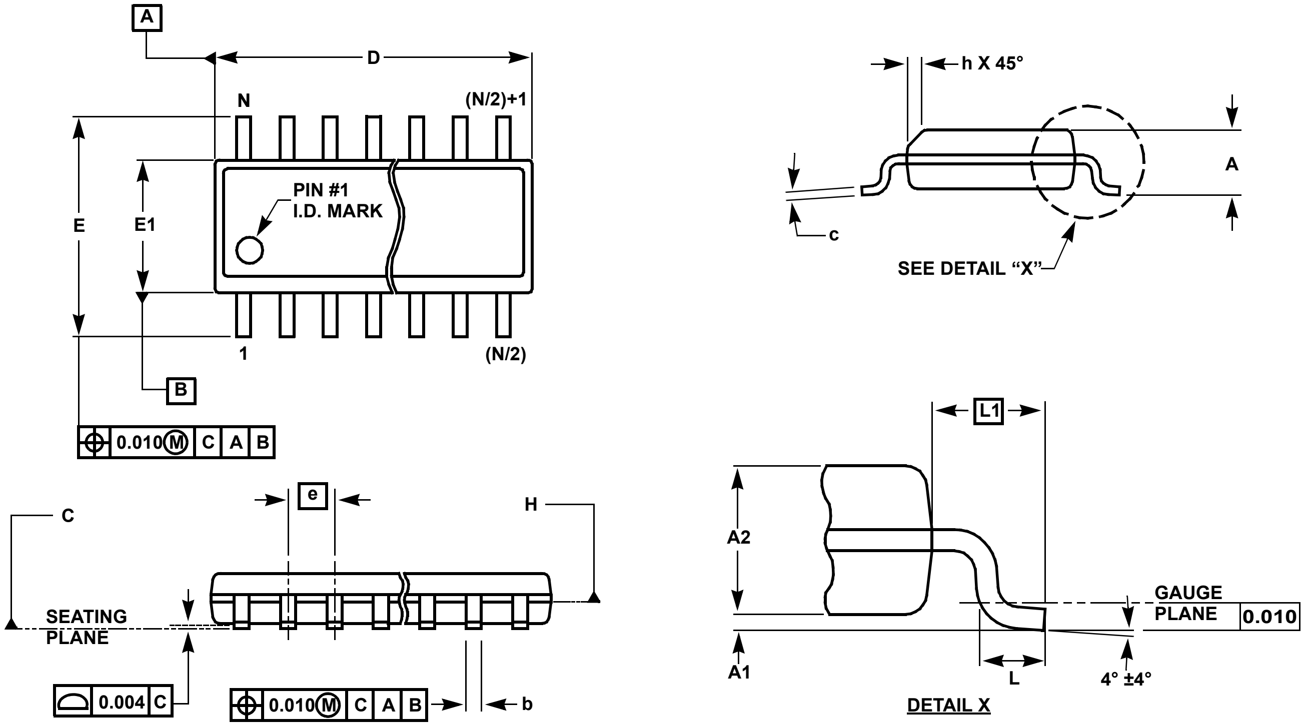
SYMBOL	MILLIMETERS					TOLERANCE
	14 LD	16 LD	20 LD	24 LD	28 LD	
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.10	0.10	0.10	0.10	0.10	±0.05
A2	0.90	0.90	0.90	0.90	0.90	±0.05
b	0.25	0.25	0.25	0.25	0.25	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	5.00	6.50	7.80	9.70	±0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
e	0.65	0.65	0.65	0.65	0.65	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference

Rev. F 2/07

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions "D" and "E1" are measured at dAtum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994