

μPA2738GR

P-channel MOSFET

-30 V, -10 A, 15 mΩ

R07DS1321EJ0100

Rev.1.00

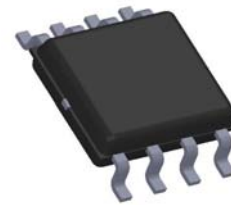
Jan 25, 2016

Description

The μPA2738GR is P-channel MOS Field Effect Transistor designed for DC/DC converter and power management applications of portable equipment.

Features

- $V_{DSS} = -30\text{ V}$ ($T_A = 25^\circ\text{C}$)
- Low on-state resistance
— $R_{DS(on)} = 15\text{ m}\Omega$ MAX. ($V_{GS} = -10\text{ V}$, $I_D = -10\text{ A}$)
- 4.5 V Gate-drive available
- Small and surface mount package (SOP-8)
- Pb-free and Halogen free



SOP-8

Ordering Information

Part No.	LEAD PLATING	PACKING	Package
μ PA2738GR-E1-AX	Ni / Pd / Au	Tape 2500 p/reel	SOP-8
μ PA2738GR-E2-AX			0.085 g TYP.

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to Source Voltage ($V_{GS} = 0\text{ V}$)	V_{DSS}	-30	V
Gate to Source Voltage ($V_{DS} = 0\text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 10	A
Drain Current (pulse) *1	$I_{D(pulse)}$	± 100	A
Total Power Dissipation *2	P_{T1}	1.1	W
Total Power Dissipation (PW = 10 sec) *2	P_{T2}	2.5	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
Single Avalanche Current *3	I_{AS}	10	A
Single Avalanche Energy *3	E_{AS}	10	mJ

Thermal Resistance

Channel to Ambient Thermal Resistance *2 $R_{th(ch-A)}$ 114 $^\circ\text{C/W}$

Notes: *1. $PW \leq 10\ \mu\text{s}$, Duty Cycle $\leq 1\%$

*2. Mounted on a glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mm

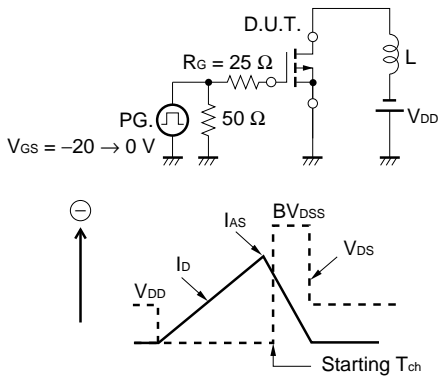
*3. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = -15\text{ V}$, $R_G = 25\ \Omega$, $V_{GS} = -20 \rightarrow 0\text{ V}$, $L = 100\ \mu\text{H}$

Electrical Characteristics (T_A = 25°C)

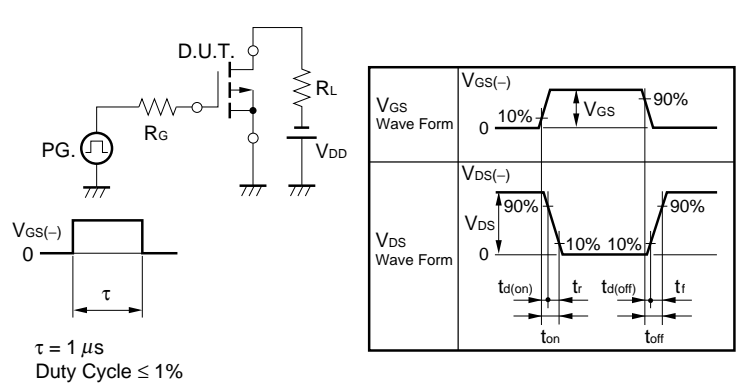
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DS}			-1	μA	V _{DS} = -30 V, V _{GS} = 0 V
Gate Leakage Current	I _{GSS}			±100	nA	V _{GS} = ±20 V, V _{DS} = 0 V
Gate Cut-off Voltage	V _{GS(off)}	-1.0		-2.5	V	V _{DS} = -10 V, I _D = -1 mA
Forward Transfer Admittance *1	y _{fs}	4			S	V _{DS} = -10 V, I _D = -5.0 A
Drain to Source On-state Resistance *1	R _{DS(on)1}		12	15	mΩ	V _{GS} = -10 V, I _D = -10 A
	R _{DS(on)2}		19	29	mΩ	V _{GS} = -4.5 V, I _D = -10 A
Input Capacitance	C _{iSS}		1450		pF	V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz
Output Capacitance	C _{oSS}		710		pF	
Reverse Transfer Capacitance	C _{rSS}		650		pF	
Turn-on Delay Time	t _{d(on)}		14		ns	V _{DD} = -15 V, I _D = -5.0 A, V _{GS} = -10 V, R _G = 10 Ω
Rise Time	t _r		30		ns	
Turn-off Delay Time	t _{d(off)}		60		ns	
Fall Time	t _f		50		ns	
Total Gate Charge	Q _G		37		nC	V _{DD} = -24 V, V _{GS} = -10 V, I _D = -10 A
Gate to Source Charge	Q _{GS}		2.5		nC	
Gate to Drain Charge	Q _{GD}		20		nC	
Body Diode Forward Voltage *1	V _{F(S-D)}		0.86		V	I _F = 10 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		47		ns	I _F = 10 A, V _{GS} = 0 V, di/dt = 100 A/μs
Reverse Recovery Charge	Q _{rr}		43		nC	

Note: *1. Pulsed

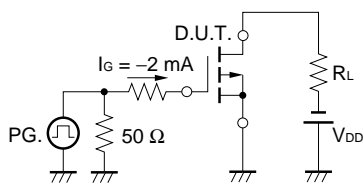
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

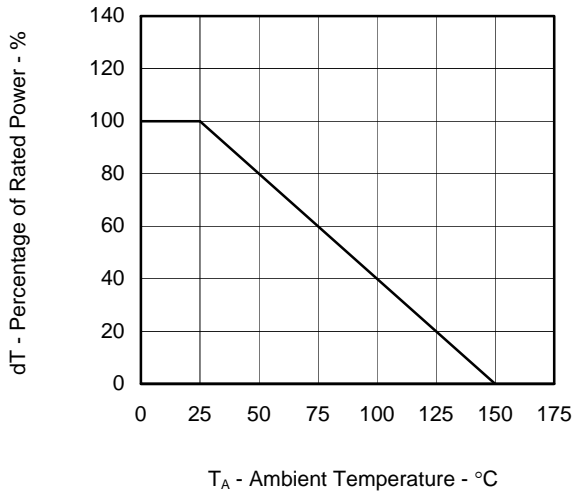


TEST CIRCUIT 3 GATE CHARGE

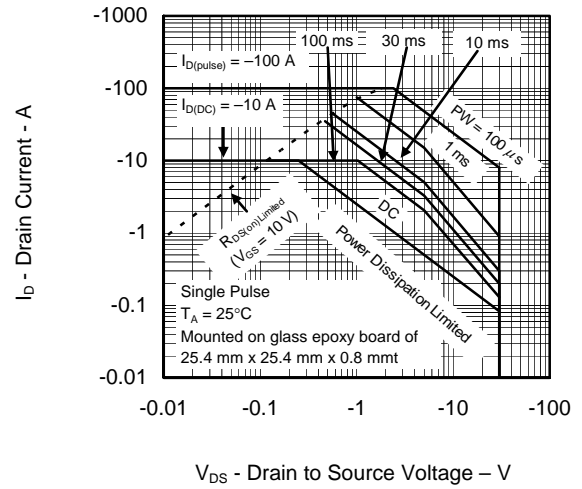


TYPICAL CHARACTERISTICS (T_A = 25°C)

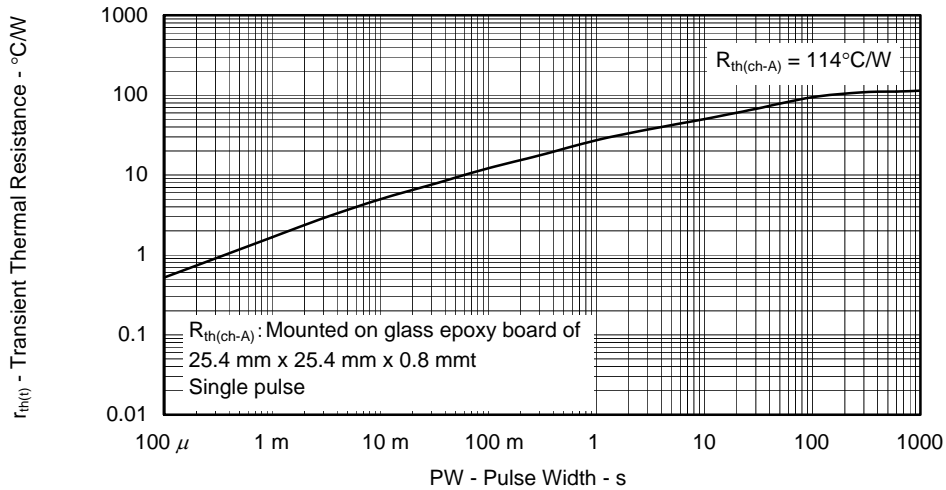
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



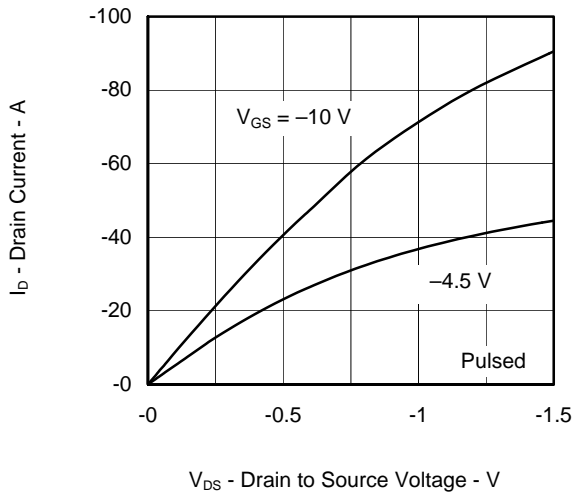
FORWARD BIAS SAFE OPERATING AREA



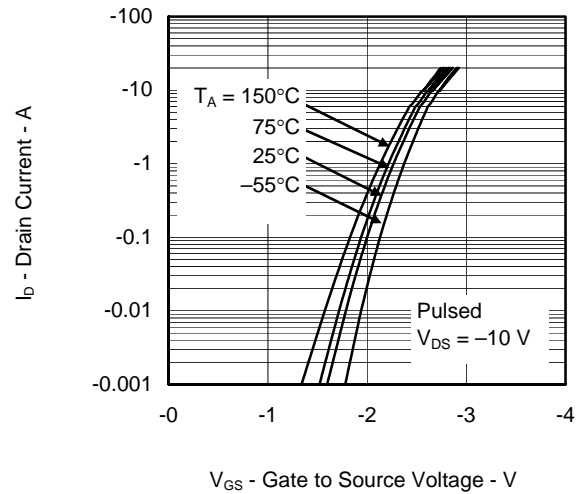
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



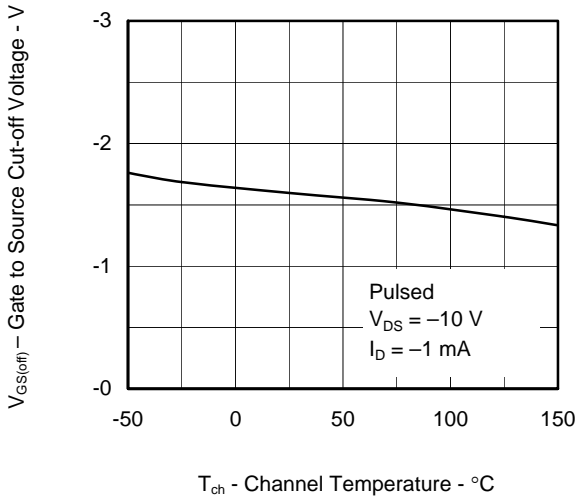
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



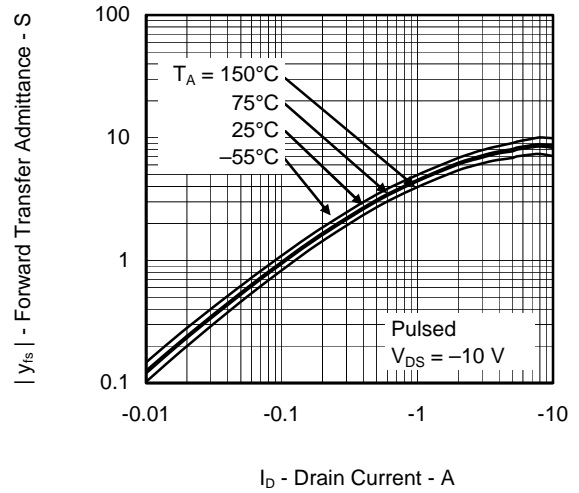
FORWARD TRANSFER CHARACTERISTICS



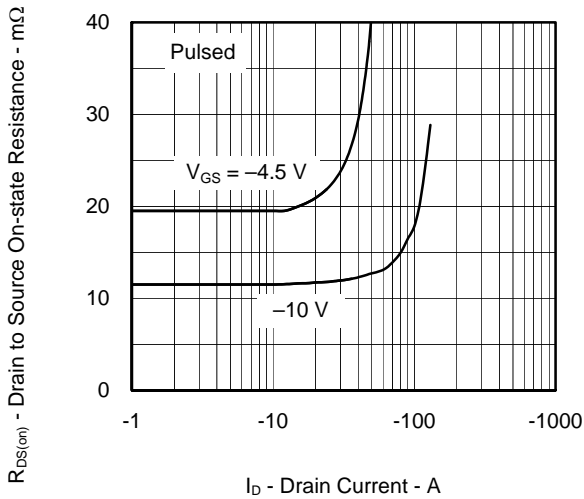
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



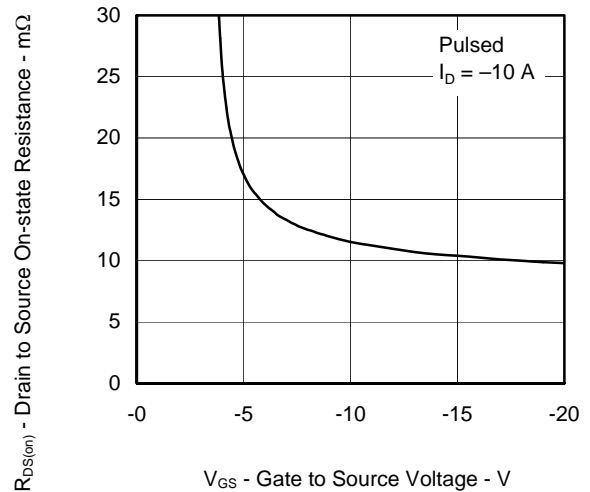
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



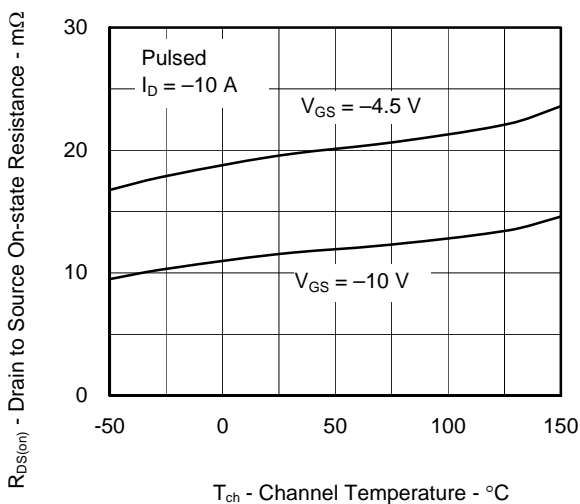
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



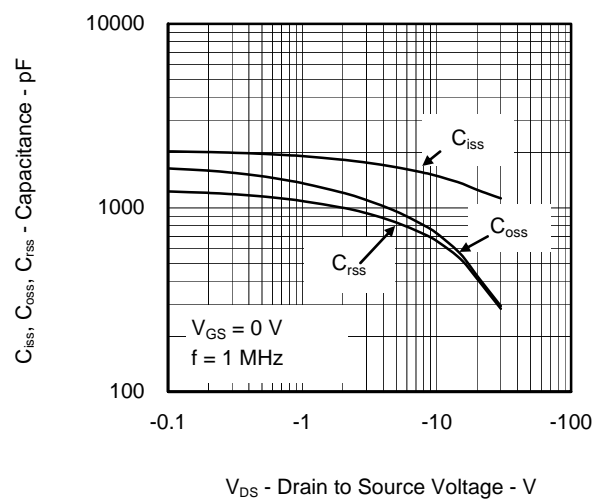
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



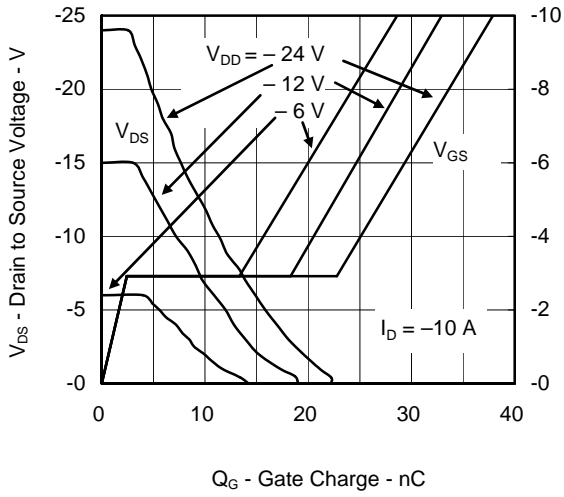
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



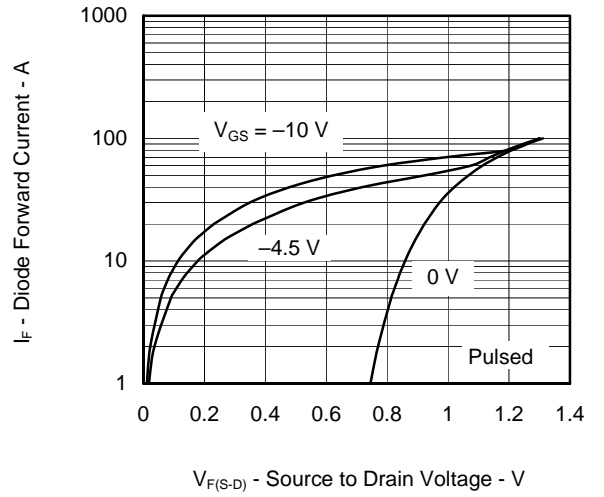
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



DYNAMIC INPUT/OUTPUT CHARACTERISTICS

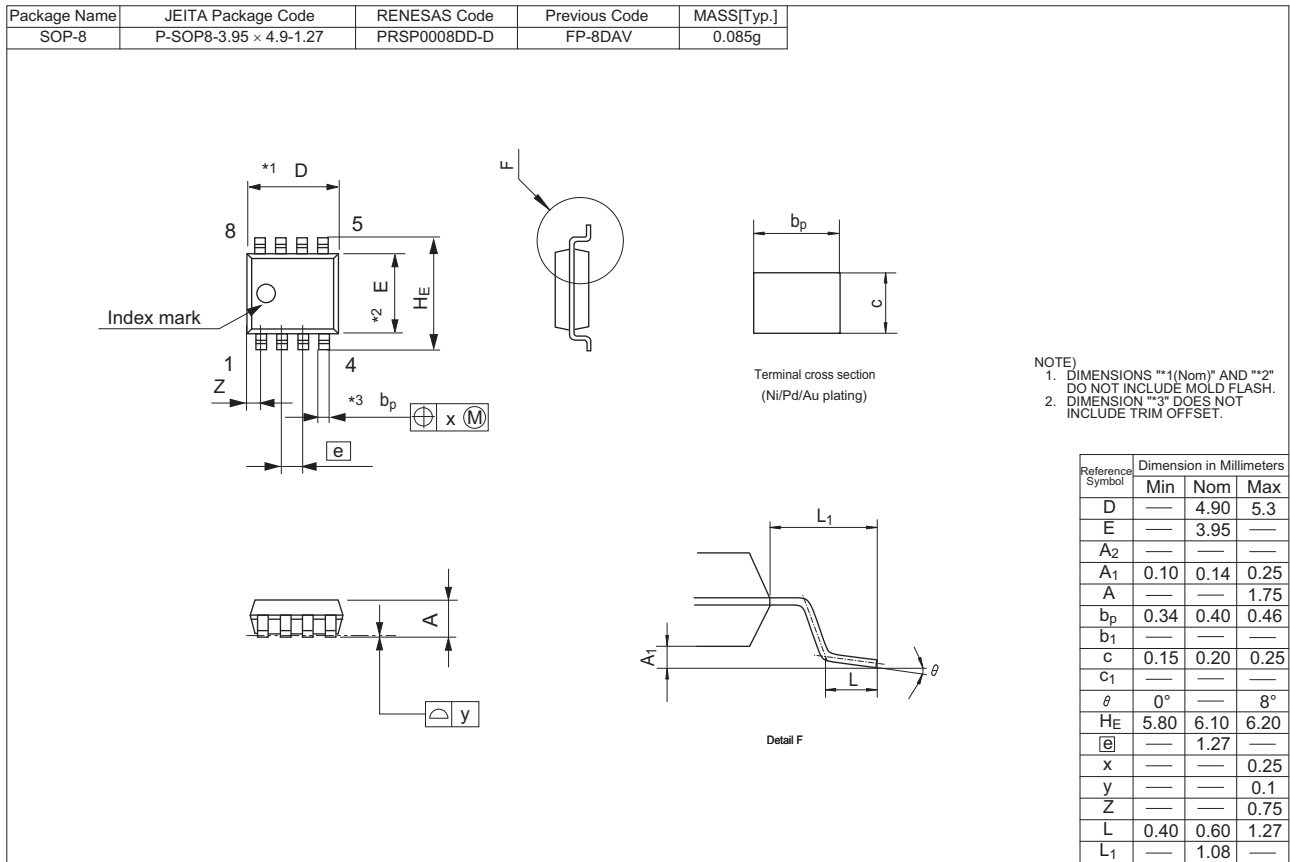


SOURCE TO DRAIN DIODE FORWARD VOLTAGE

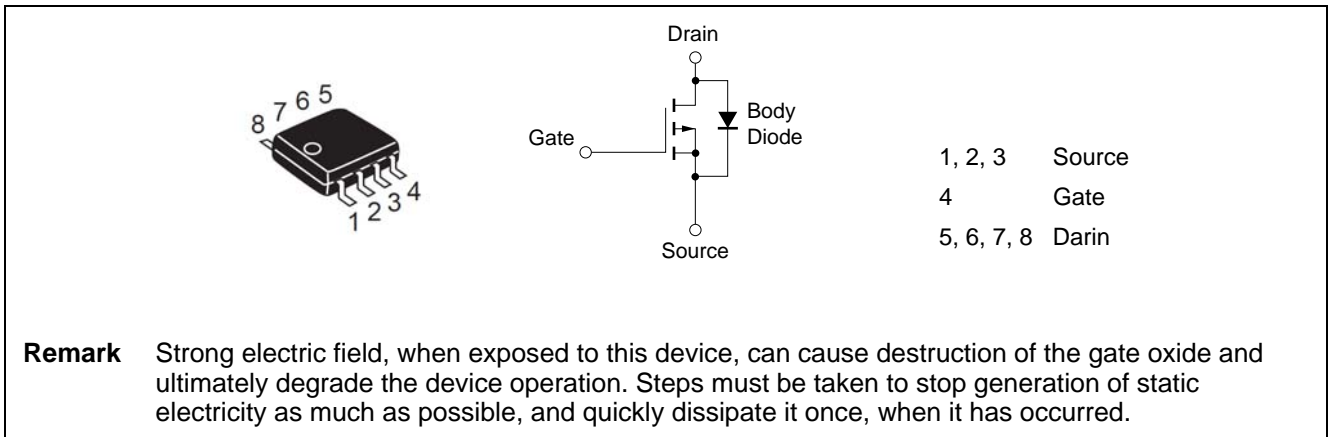


Package Drawings (Unit: mm)

SOP-8



Equivalent Circuit



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